BRAC UNIVERSITY
Department of Computer Science & Engineering
Practice Problem sheet (Week5)

Question 1

(a)	An analog signal in the range −1V to 16V is to be converted to a digital signal with a quantization error of less than or equal to 0.781% of the input voltage range for quantization. **e.g the overall quantization error for this input signal should be less than or equal to 0.781% of the ADC's maximum quantization error.** The quantization error is the maximum error occurring after quantizing the analog signal. **Find** the required number of bits for the above expression.
(b)	**Determine** the minimum sampling frequency of a signal.

a) ΔQ = Quantization error = $\frac{1}{2}\frac{V_{max} - V_{min}}{2^N}$

$\therefore$ Quantization error = $\frac{0.781}{100} \times (V_{max} - V_{min})$

$\Rightarrow \frac{\Delta Q}{V_{max} - V_{min}} = \frac{0.781}{100}$

$\Rightarrow \frac{1}{2} \times \frac{V_{max} - V_{min}}{2^N} \times \frac{1}{V_{max} - V_{min}} = \frac{0.781}{100}$

$\Rightarrow \frac{1}{2^{N+1}} = \frac{0.781}{100}$

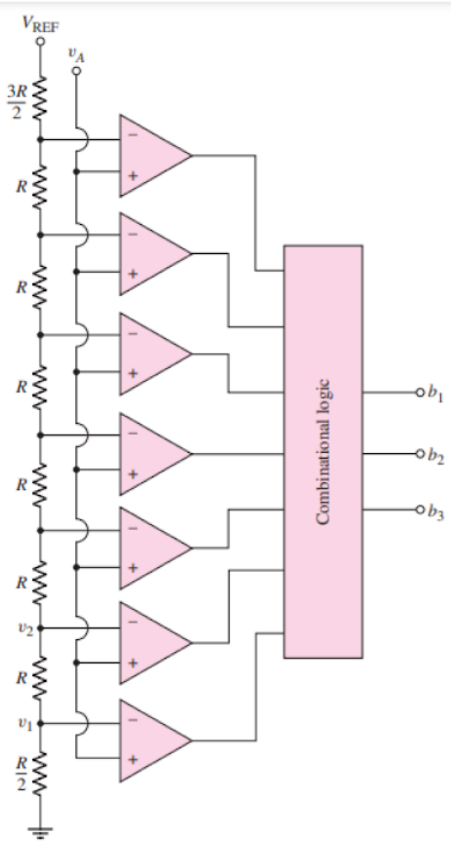
$\Rightarrow 2^{N+1} = 128 \Rightarrow \boxed{N = 6}$

b) $\boxed{f_{sampling} = 2 \times f_{input}}$

Question 2

Design a 3 bit flash ADC with a reference voltage of $V_{REF}=10V$. The quantized levels for this ADC should be **uniform (Equal step size).**

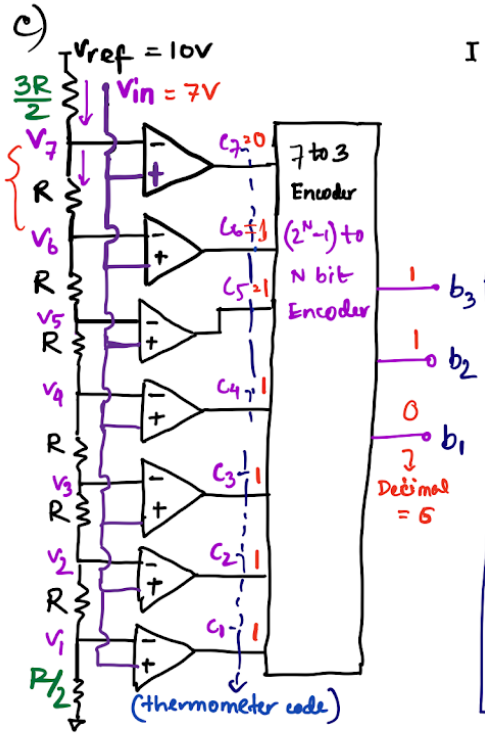
(a)	**Calculate** total number of resistors and comparators required to fabricate a 3-bit flash A/ D converter.
(b)	Calculate the 1LSB value or each step size (quantization range) for this 3 bit ADC. What would be the resolution for this ADC?
(c)	Calculate each **quantization level** and plot the **Vin vs Dout** graph.
(d)	If the input voltage **Vin= 7 V,** i) Comment on the **quantization range** in which the input lies. ii) Find the **digital output** for the given input.
(e)	If the 3-bit output is 110 What is the maximum and minimum value of v_A that produces this output?(Hint:find the quantization range).
(f)	If 1 bit was increased from this 3 bit Flash ADC, how many resistors and comparators are required? comment on the hardware changes for this 1 bit of increment.



a) N = 3; Resistor required = $2^N = 2^3 = 8$
Comparator required = $2^3 - 1 = 7$

b) 1 LSB = resolution or step size $= \frac{V_{max} - V_{min}}{2^N} = \frac{10-0}{2^3} = \boxed{1.25\,V}$

c)



$$I = \frac{10V}{\frac{3R}{2} + 6R + \frac{R}{2}} = \frac{10V}{R\left(\frac{3}{2} + \frac{12}{2} + \frac{1}{2}\right)} = \frac{10V}{R \cdot \frac{16}{2}}$$

$$\therefore I = \frac{10}{8R} = \frac{1.25}{R}$$ (same as previous example)

$V_0 = 0V$

$V_1 = \frac{1.25}{R} \cdot \frac{R}{2} = 0.625V\ (\frac{1}{2}\ LSB)$

$V_2 = \frac{1.25}{R} \cdot \left(R + \frac{R}{2}\right) = \frac{1.25}{R} \times \frac{3R}{2} = 1.875V\ (1\frac{1}{2}\ LSB)$

$V_3 = \frac{1.25}{R} \cdot \left(\frac{5R}{2}\right) = 3.125V$

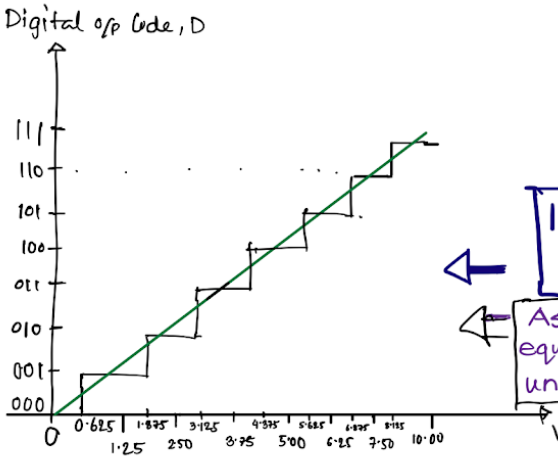
$V_4 = \frac{1.25}{R} \cdot \frac{7R}{2} = 4.375V$

$V_5 = \frac{1.25}{R} \cdot \frac{9R}{2} = 5.625V$

$V_6 = \frac{1.25}{R} \cdot \frac{11R}{2} = 6.875V$ } ← input 7

$V_7 = \frac{1.25}{R} \cdot \frac{13R}{2} = 8.125V$

$V_{ref} = \frac{1.25}{R} \cdot \left(\frac{13R}{2} + \frac{3R}{2}\right) = 10V$



Input Vin Vs Digital output code, D

As all the step size is uniform or equal to '1LSB; this distribution is a uniform distribution. from ($V_1 - V_7$)

d) if input = 7V ; it will be in between the quantization range of $V_6 - V_7$ or 6.875V - 8.125V.

Quantization Range	Quantized value	Digital O/P ($b_2 b_1 b_0$)
6.875V - 8.125V	6	110

e) If digital output = 110 = 6 (quantized value)

Maximum value of V_A = 8.125V

Minimum value of V_A = 6.875V

f) If 1 bit was increased → N = 3+1 = 4 bit

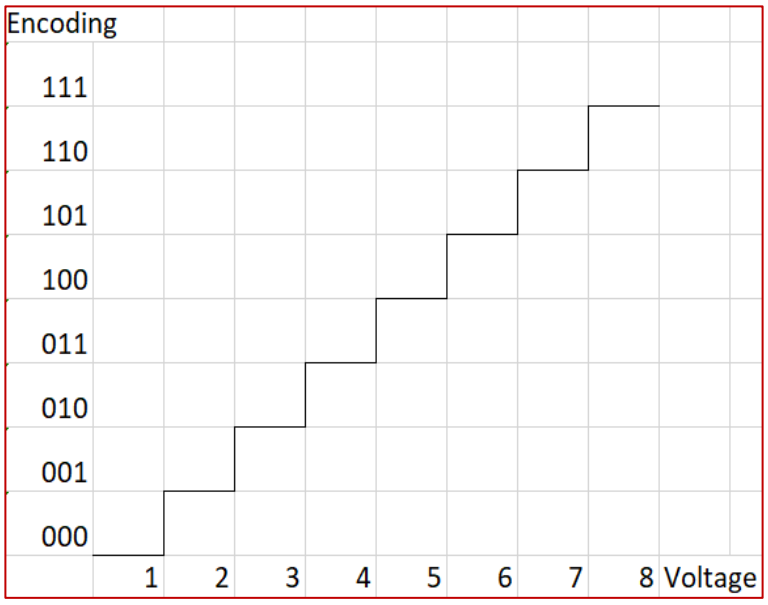
No. of R = $2^N = 2^4 = 16$

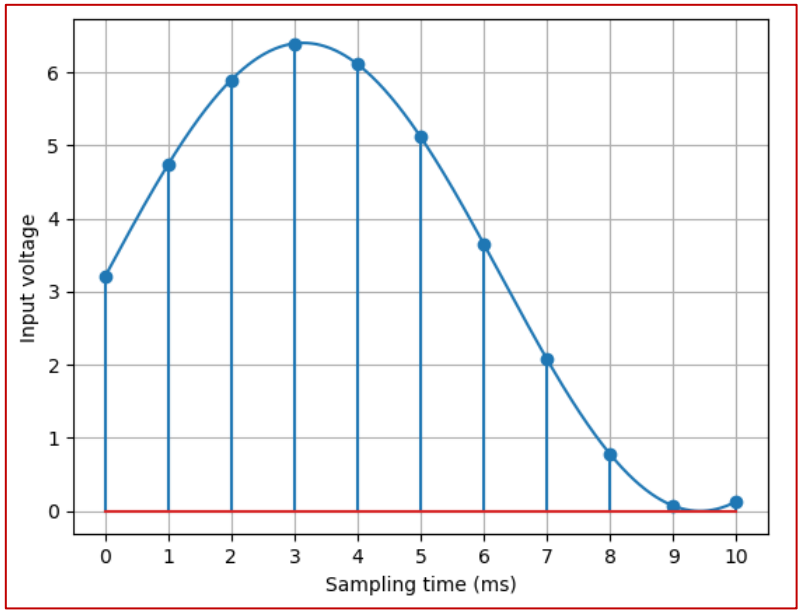
No. of Comparator = $2^4 - 1 = 15$

Encoder = 15 lines to 4 lines

1 bit of increament doubles the hardware needed.

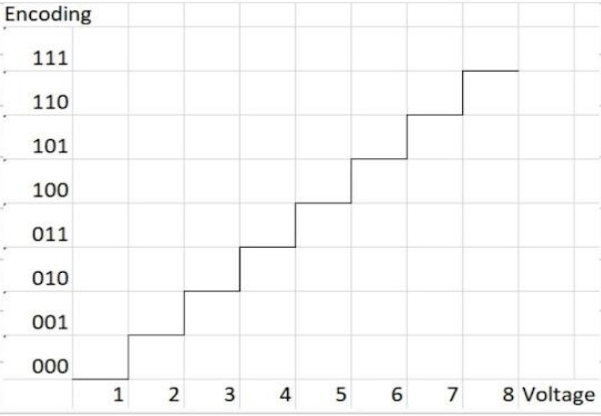
Question 3

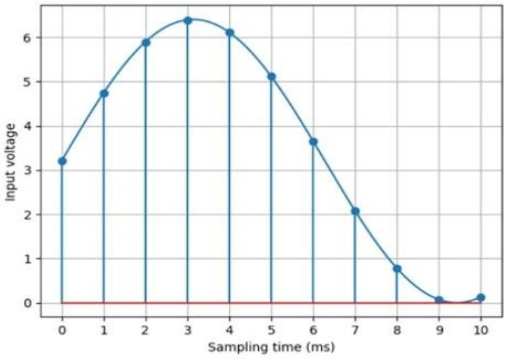




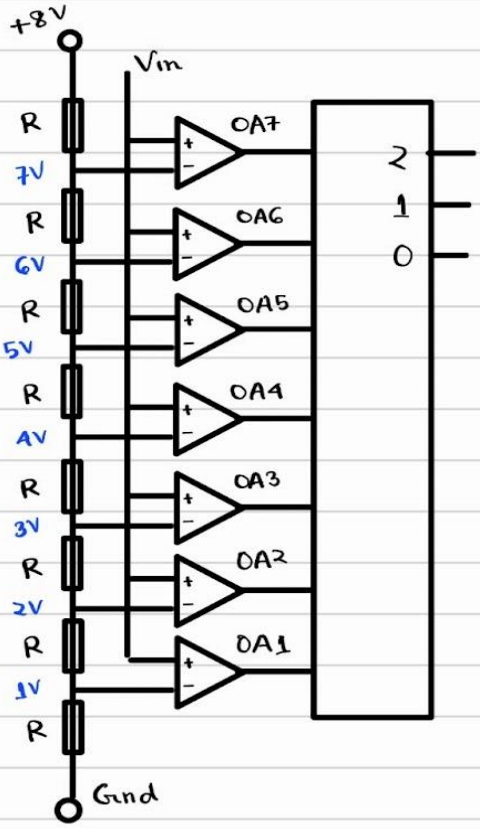
(a)	Design a 3-bit Flash ADC circuit for the given input-output characteristics.
(b)	An unknown signal is passed to the ADC as input. The ADC takes samples at a rate of 1kHz. In the graph, the input signal is shown where the x-axis represents time, and the y-axis represents the voltage at any specific time. The sampling instances are given in the figure. Find the encoded output that represents the analog signal inside the given time frame.

Solution:





(a) 3 bit ADC – $2^3 - 1 = 7$ op amps and 8 resistors required.



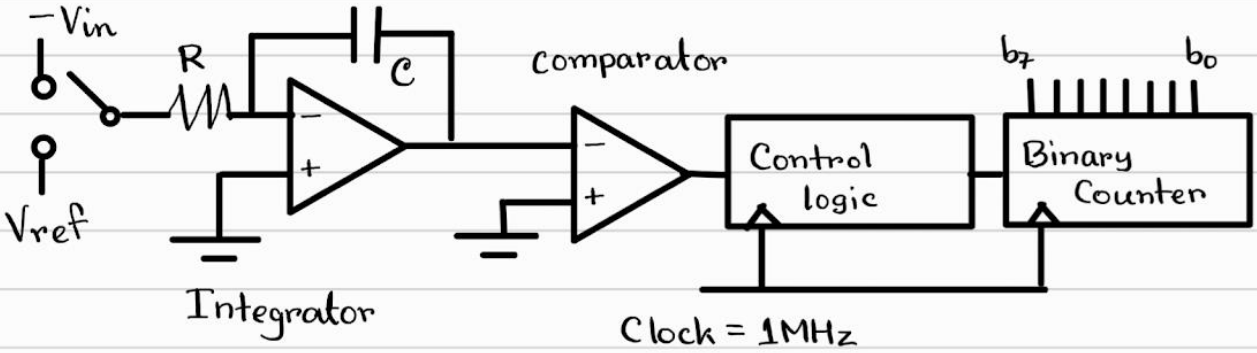
(b)

Sampling instance	Level	Encoding
0	3	011
1	4	100
2	5	101
3	6	110
4	6	110
5	5	101
6	3	011
7	2	010
8	0	000
9	0	000
10	0	000

Question 4

Dual – Slope A/D Converter

A dual slope A/D converter has $V_{ref} = 5V$, and a 8 bit counter that outputs an 8-bit representation of the input signal. A 1 MHz clock is used for the clock and counter circuits



(I) Determine the input voltage range, number of steps and step size (resolution) of the A/D converter.

(II) For a specific input voltage, the ADC outputs a count of m=100. Determine the input voltage.

(III) Determine the total time required to get the reading in (II)

(IV) Calculate the maximum sampling rate of the ADC.

(V) A person wishes to get a sampling rate 4 times that of the current circuit. Determine how many bits should be used for the counter without changing any other system parameters.

(I) Input voltage range : 5V (0 − Vref)

number of steps $= 2^n = 2^8 = 256$

step size $= \dfrac{\text{voltage range}}{\text{number of steps}} = 0.0195\ V$

(II) We know, $V_{in} = \dfrac{m}{2^n} V_{ref} = \dfrac{100}{256} \times 5V = 1.95V$

(III) For a single conversion, the integrator

(a) integrates $-V_{in}$ for t_1 duration as counter counts from $0 - 2^n$

$$t_1 = \frac{2^n}{\text{Clock rate}} = \frac{256}{1 \times 10^6} = 2.56 \times 10^{-4}\ s$$

(b) integrates V_{ref} for t_2 duration as counter counts from $0 - m$

$$t_2 = \frac{m}{\text{clock rate}} = \frac{100}{1 \times 10^6} = 1 \times 10^{-4}\ s$$

total conversion time $= t_1 + t_2 = 3.56 \times 10^{-4}\ s$

(IV) Maximum sampling rate is limited by the time required for worst case conversion of input = 5V

In that case, $t_1 = t_2 = 2.56 \times 10^{-4}\ s$

thus, worst case conversion duration $= t_1 + t_2 = 5.12 \times 10^{-4}\ s$

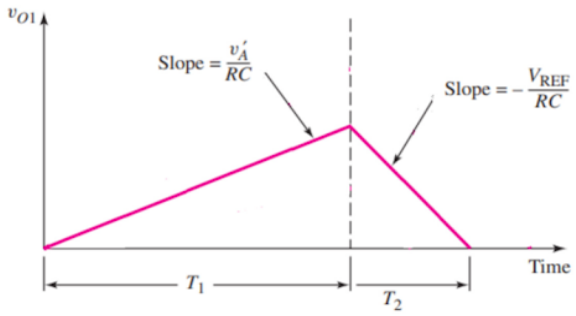
Max sampling rate $= 1 / 5.12 \times 10^{-4}\ s = 1953.125\ Hz$

(V) Sampling duration $\propto 2^n$ // Sampling rate $\propto \dfrac{1}{2^n}$

For 4 times sampling rate, counter bit $= (8 - 2) = 6$

f) $\frac{D}{2^N} = \frac{V_A'}{V_{REF}} \Rightarrow D = \frac{V_A' \times 2^N}{V_{REF}} = \frac{3}{5} \times 2^8 = 153.6 \approx 153$

Digital o/p (binary value of 153) = 10011001



Clock period of 6 µs
V_A' = 2V

(a)	Find the value of v_{O1} at $t=T_1$, suppose $R=25k\Omega$ and $C=2\mu F$.
(b)	If R= 50 $k\Omega$ and we $C=2\mu F$, calculate the new value of V_{01} at $t=T_1$, compare it with (a) and comment on the changes between two output voltages.

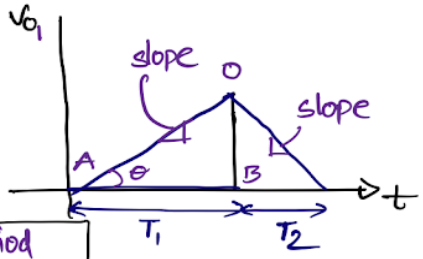
a) slope = $\frac{\Delta Y}{\Delta x} = \tan\theta = \frac{OB}{AB}$

As, $\tan\theta = \frac{V_A'}{RC}$; so $\frac{OB}{AB} = \frac{V_A'}{RC}$

$\Rightarrow V_{01} = OB = \frac{V_A'}{RC} \times AB$

$\Rightarrow V_{01} = \frac{V_A'}{RC} \times T_1$

$\Rightarrow V_{01} = \frac{2}{25K \times 2\mu F} \times 2^6 \times 6\mu S$



$T_1 = 2^N \cdot 1$ clock period
$= 2^N . T = 2^6 . 6\mu S$

$V_{01} = 0.01536V$

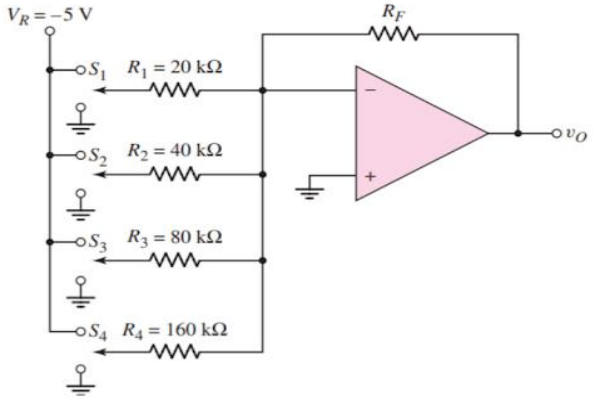
b) $V_{01} = \frac{2}{50K\Omega \times 2\mu F} \times 2^6 \times 6\mu S$

$V_{01} = 0.00768V$

Comment:
As, resistance increases by 2, it decreases the output by half.

Question 5

(a)	**Determine** the output voltage, ***vo*** in V of the 4-bit weighted-resistor D/A in the following figure for input =1010 and input=1100? Assume R_F= 5kΩ.
(b)	**Identify** the maximum allowed tolerance (± percent) in the value of R_1 so that the maximum error in the output is limited to $\pm\frac{1}{2}$ **LSB** quantized voltage value? (hint: Do two separate calculations for output error being $+\frac{1}{2}$**LSB** and $-\frac{1}{2}$**LSB** Then, calculate the percentage change in R1 in these two cases.)



a) Input = 1010 ; ~~RF = 5kΩ~~

$V_0 = 5 \times \frac{5}{20} + 5 \times \frac{5}{80} =$ **1.5625V**

Input = 1100 ; RF = 5kΩ

$v_0 = 5 \times \frac{5}{20} + 5 \times \frac{5}{40} =$ **1.875V**

b) $1\ LSB = 5 \times \frac{5}{160} = 0.15625\ V$

$\Rightarrow \frac{1}{2} LSB = 0.078125V$

1 MSB = 1.25V →

$V_0 = 1.25 \pm 0.078125V$

= 1.328125V or 1.171875V

$-5 \times \frac{5}{R_1} = 1.328125V$ or $-5 \times \frac{5}{R_1} = 1.171875V$

$\Rightarrow$

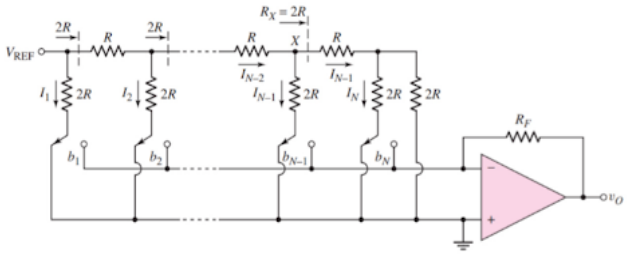
$R_1 = 18.823K\Omega \rightarrow$ % change in $R_1 = \frac{20-18.82}{20} \times 100 =$ **5.88%**

Or $21.33K\Omega \rightarrow$ % change in $R_1 = \frac{21.33-20}{20} \times 100 = 6.67\%$

Max tolerance → 5.88%

$V_0 = 1\ MSB + \frac{1}{2} LSB$ or $V_0 = 1\ MSB - \frac{1}{2} LSB$ } Output error

Question 6



The N-bit D/A converter with an R–$2R$ ladder network in the above figure is to be designed as a 6-bit D/A device. Suppose $V_{REF} = -5V$ and $R_F = R = 5k\Omega$.

(a)	Find currents $I_1 I_2 I_3 I_4 I_5 I_6$.
(b)	What is the output voltage if the input is 010011?
(c)	What is the change in output voltage if the input changes from 101010 to 010101?

a) $I_1 = \frac{V_{REF}}{2R} = \frac{-5}{10} \Rightarrow I_1 = -0.50mA$

$I_2 = \frac{I_1}{2} = -0.25mA$

$I_3 = \frac{I_2}{2} = -0.125mA$

$I_4 = \frac{I_3}{2} = -0.0625mA$

$I_5 = \frac{I_4}{2} = -0.03125mA$

$I_6 = \frac{I_5}{2} = -0.015625\ mA$

b) Input = 010011

$v_o = -[I_2 + I_5 + I_6] R_F = [0.25 + 0.03125 + 0.015625]mA \times 5K\Omega = 1.484375V$

c) Input = 101010

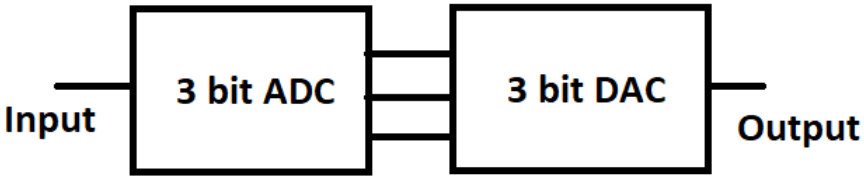
$v_o = -[I_1 + I_3 + I_5] R_F = [0.50 + 0.125 + 0.03125]\ mA \times 5K\Omega = 3.28125V$

Input = 010101

$v_o = -[I_2 + I_4 + I_6] R_F = [0.25 + 0.0625 + 0.015625]mA \times 5K\Omega = 1.640625V$

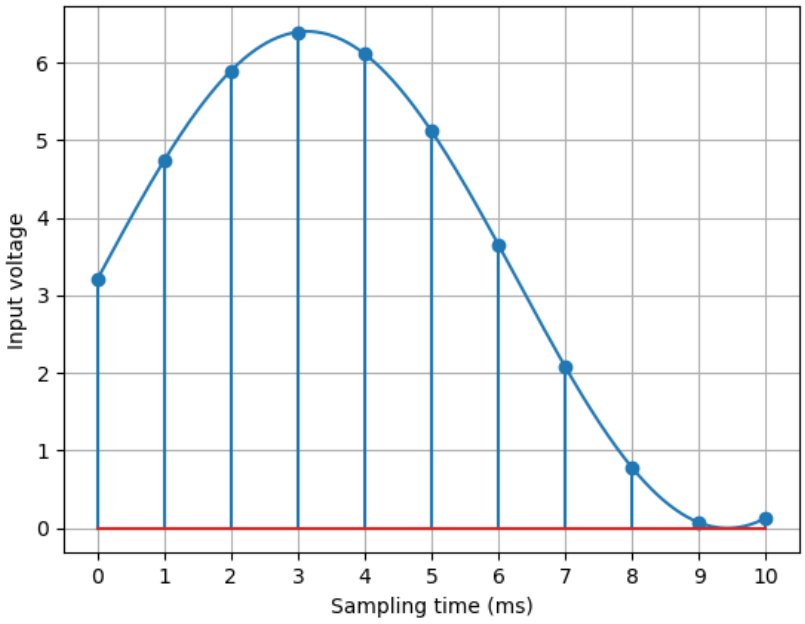
$\Delta V_o = 1.640625V$

Question 7



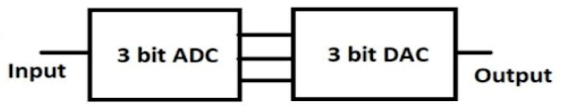
ADC Input Voltage	Encoding	DAC Output Voltage
0-1	000	0.5
1-2	001	1.5
2-3	010	2.5
3-4	011	3.5
4-5	100	4.5
5-6	101	5.5
6-7	110	6.5
7-8	111	7.5

(a)	For the following input waveshape, draw the reconstructed output by the DAC. The sampling instances are marked on the input waveshape.
(b)	Comment on the quality of the reconstructed signal and how the quality would be affected if additional bits were used for both the ADC and DAC.



Solution:

(a)



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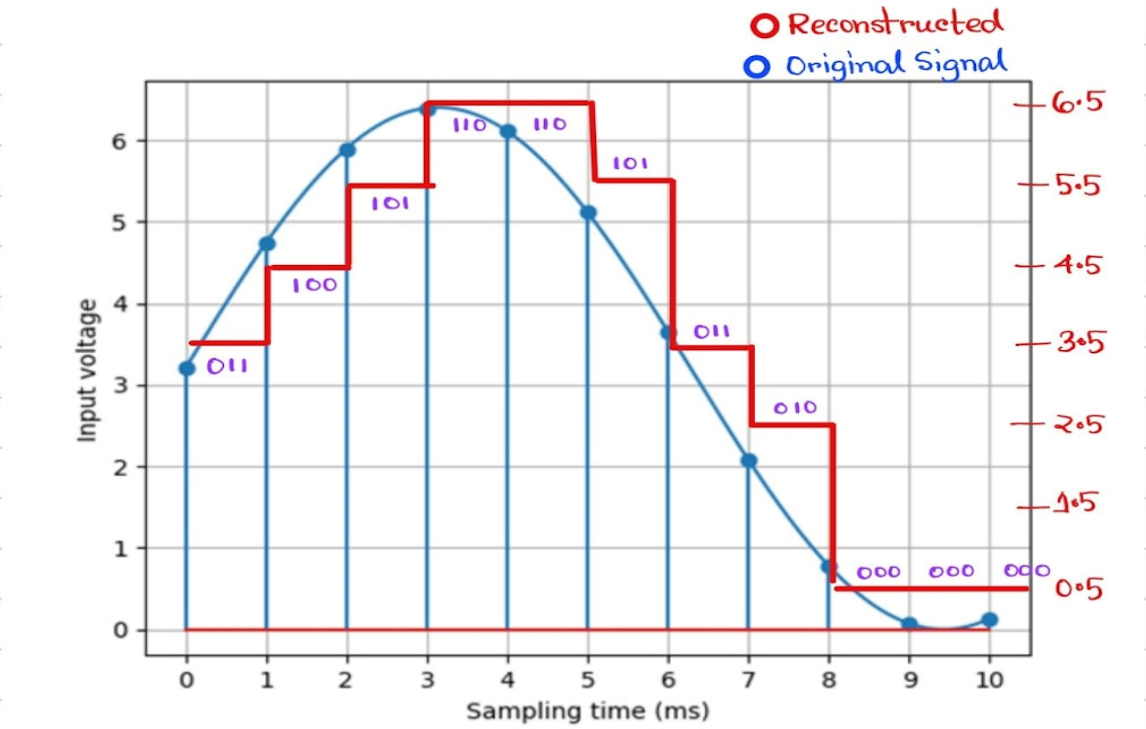
6-7	110	6.5
7-8	111	7.5



(b) Reconstructed signal roughly estimates the original input, and the quality is not very good.

Using higher number of bits for both the ADC and DAC will give a better voltage resolution. The reconstructed voltage levels would be closer to that of the originally sampled value.