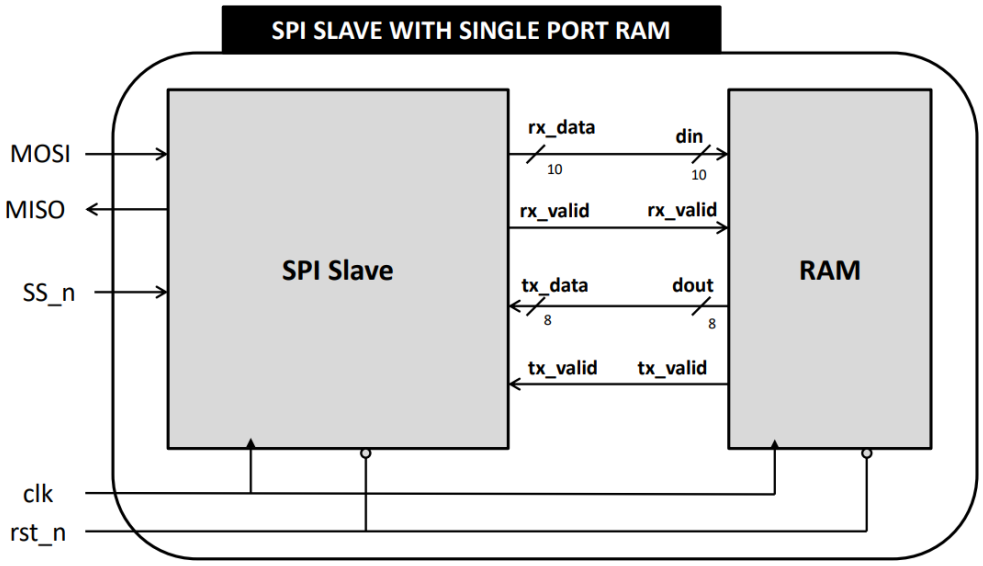
Digital IC Design

SPI Slave Interface with Single Port RAM



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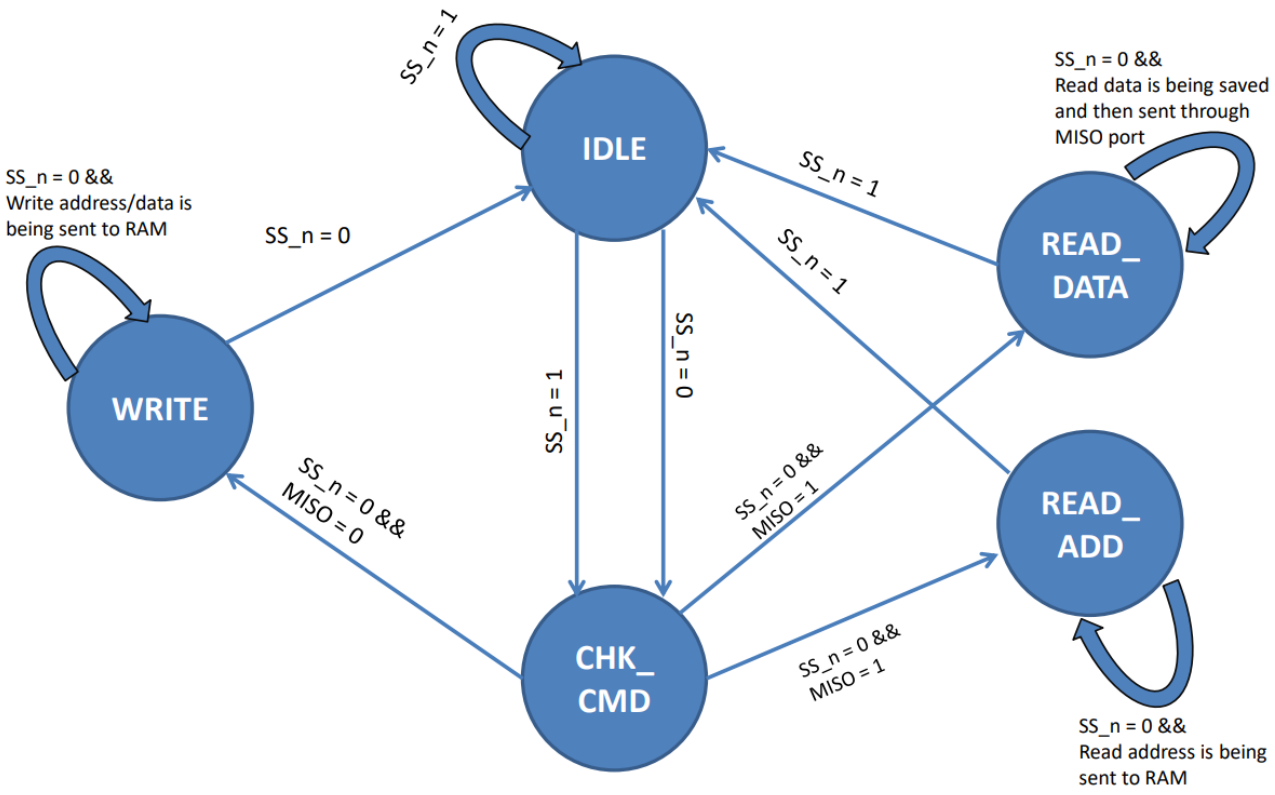
Overview

This project demonstrates a custom SPI slave module implemented in Verilog, designed to communicate with a master device using the SPI protocol. The SPI slave is capable of handling read and write commands via serial input (MOSI) and converting it to parallel data for internal RAM access.

A Finite State Machine (FSM) is used to manage the communication process:

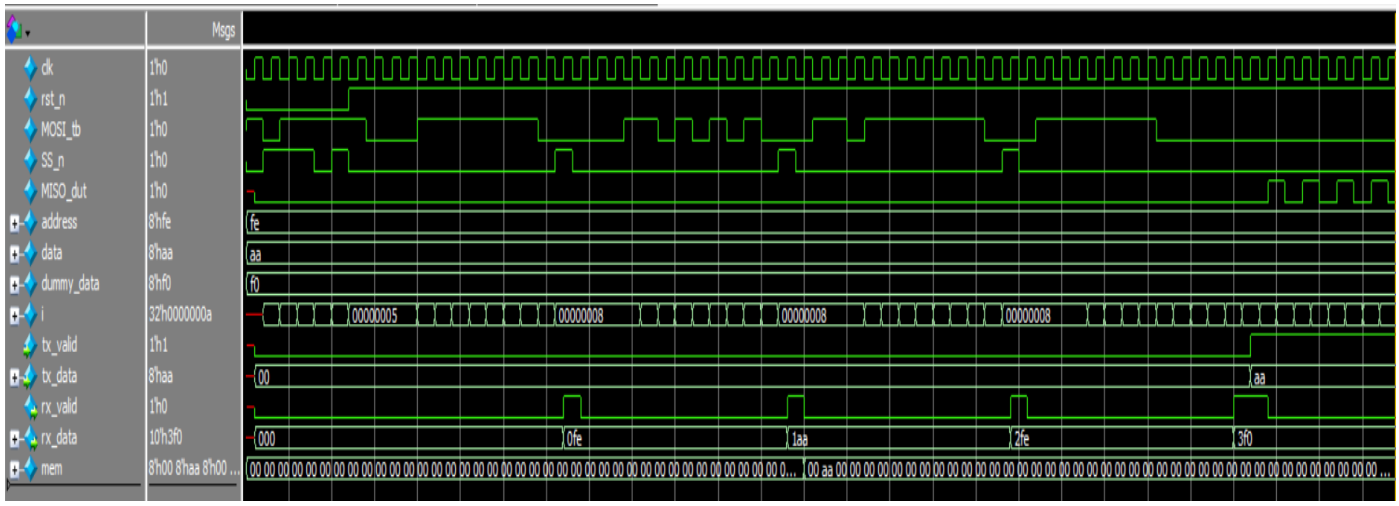


1. Simulation Snippet - Questa-Sim

- Automated Simulation - Do File

```
vlib work
vlog SPI_old.v ram.v top.v tb.v
vsim -voptargs=+acc tb
add wave *
add wave -position insertpoint  \
sim:/tb/top1/m1/tx_valid \
sim:/tb/top1/m1/tx_data \
sim:/tb/top1/m1/rx_valid \
sim:/tb/top1/m1/rx_data
add wave -position insertpoint /tb/top1/m2/mem
run -all
#quit -sim
```

- Waveform



2. Linting - Questa Lint

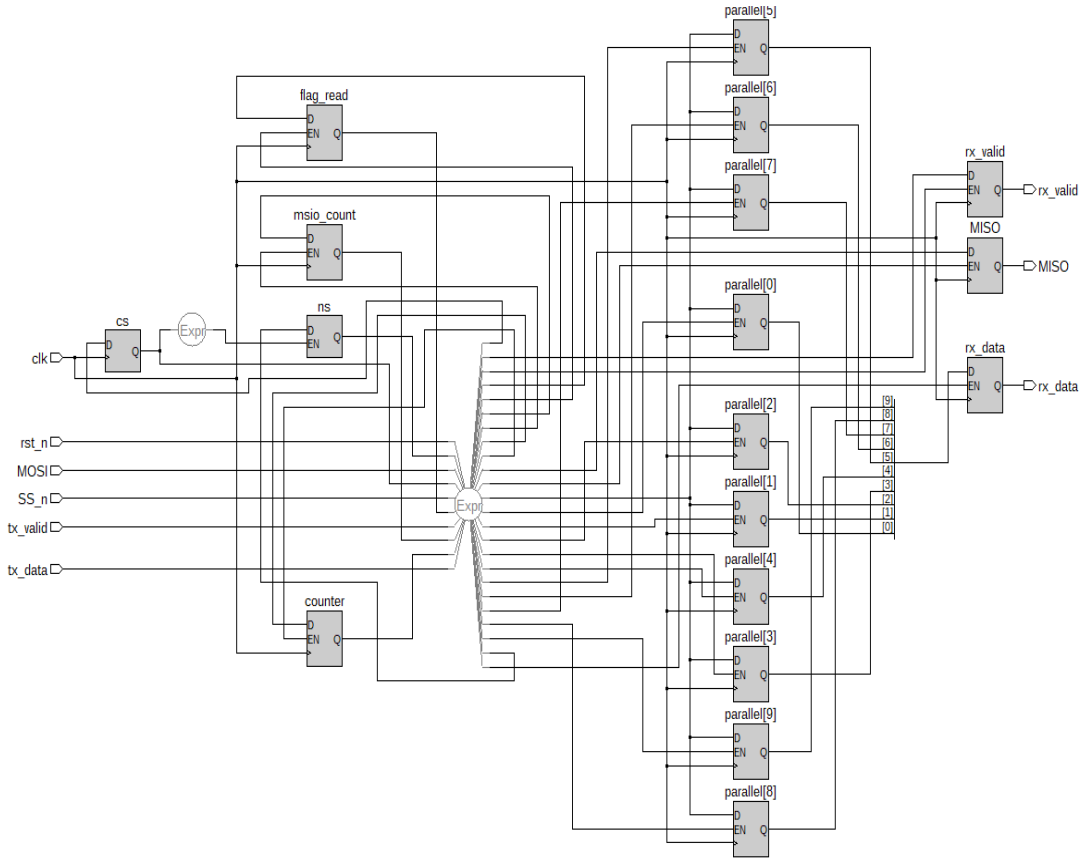
➢ Lint Checks Result

Lint Checks

Filter: Type here | Waived | Fixed | Pending | Uninspected | Bug | Verified | Total : 3 | Selected : 0

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
		always_signal_assign_large		Always block has more signal assignments than the s...	spi	Rtl Design Style	open	unassig...	2.6.1.3
		comment_not_in_english		Comments include non-English characters. File C:/Us...	none	Nomenclature...	open	unassig...	3.5.6.4, 3.5.6.6
		multi_ports_in_single_line		Multiple ports are declared in one line. Module spi, Fil...	spi	Rtl Design Style	open	unassig...	3.5.6.3

➢ Schematic



3. Encoding – Vivado

➢ One – Hot

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [C:/Users/DELL/Desktop/digital
```

➢ Gray

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [C:/Users/DELL/Desktop/digital
```

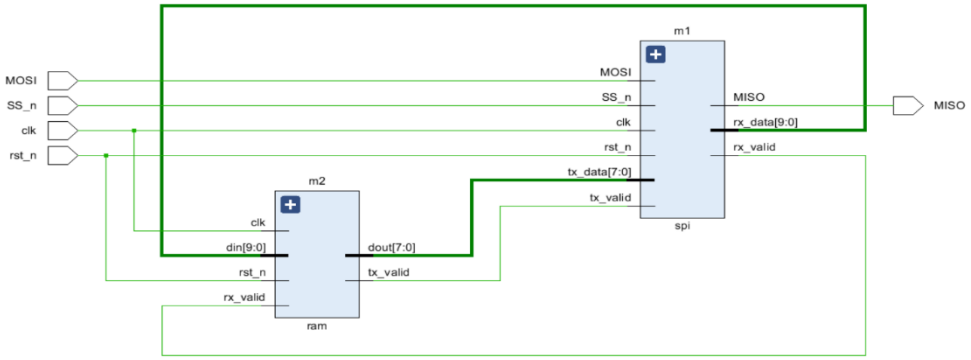
➢ Sequential

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

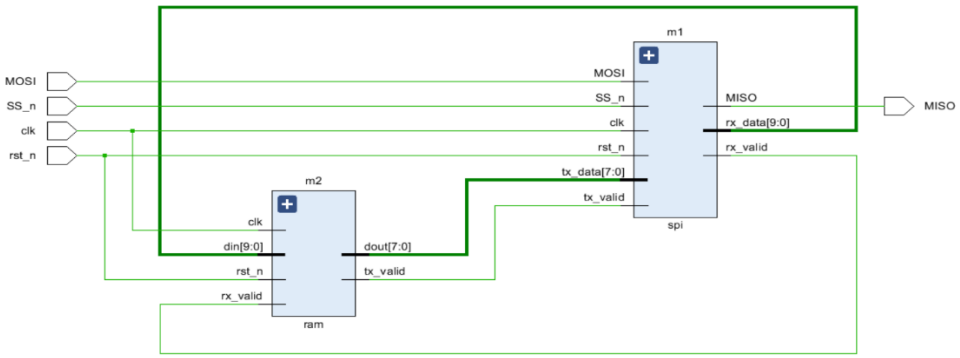
```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'spi'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [C:/Users/DELL/Desktop/digital
```

4. Elaboration – Vivado

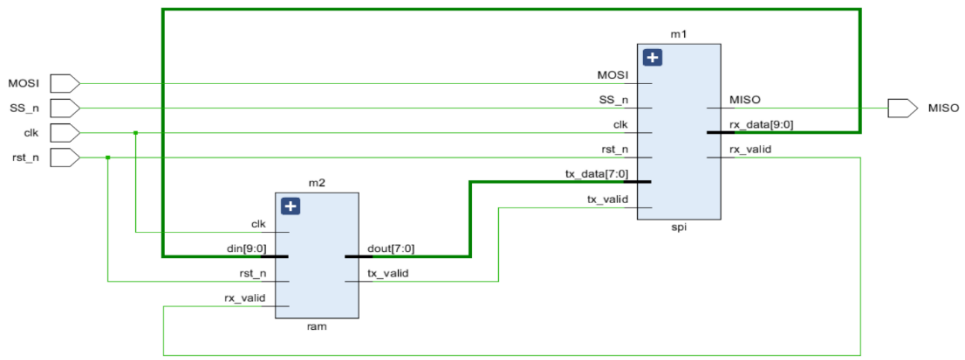
- Schematic
  1. One Hot



  2. Gray



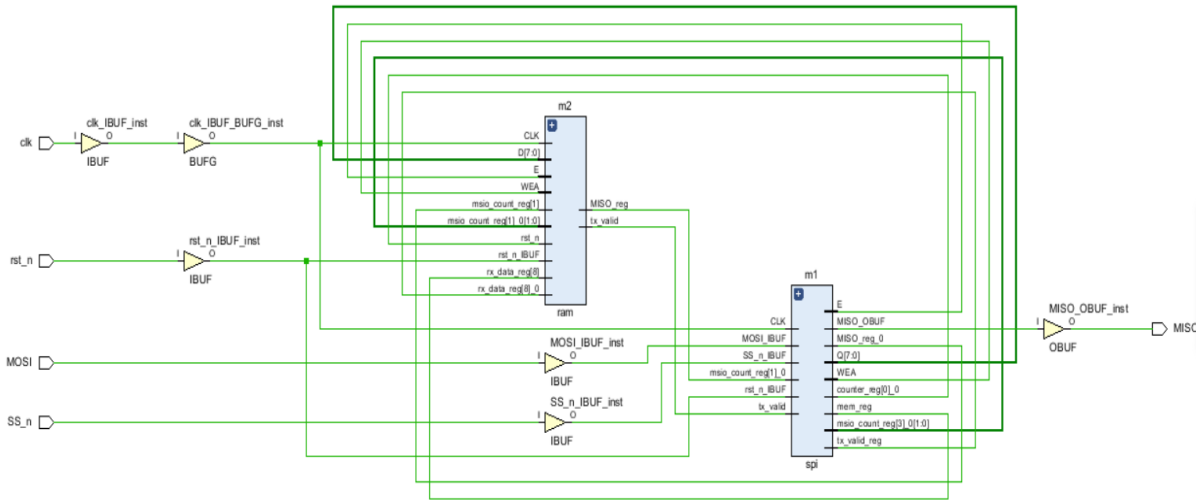
  3. Sequential



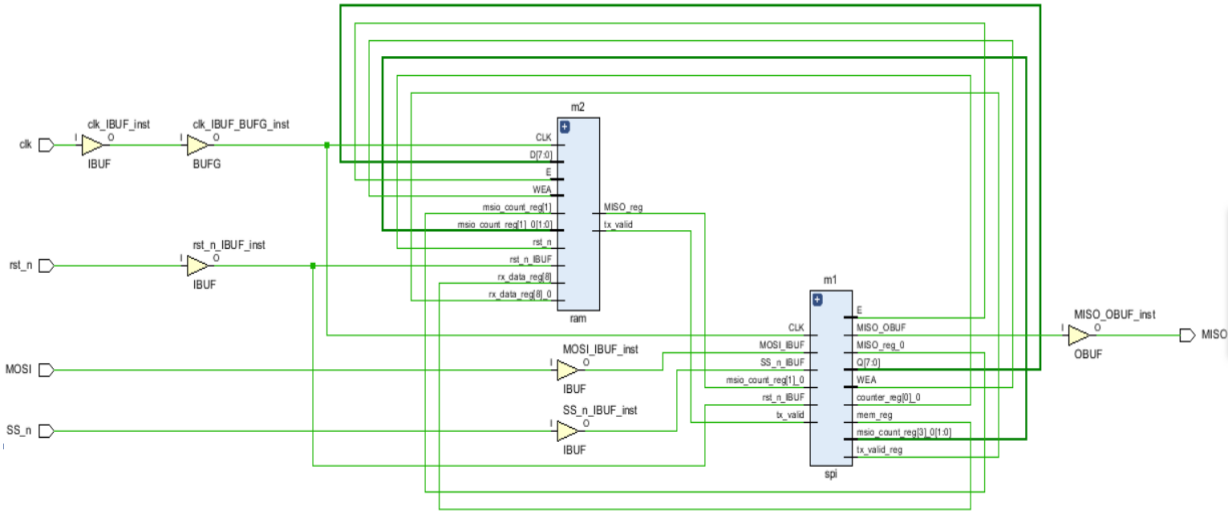
5. Synthesis - Vivado

➢ Schematic

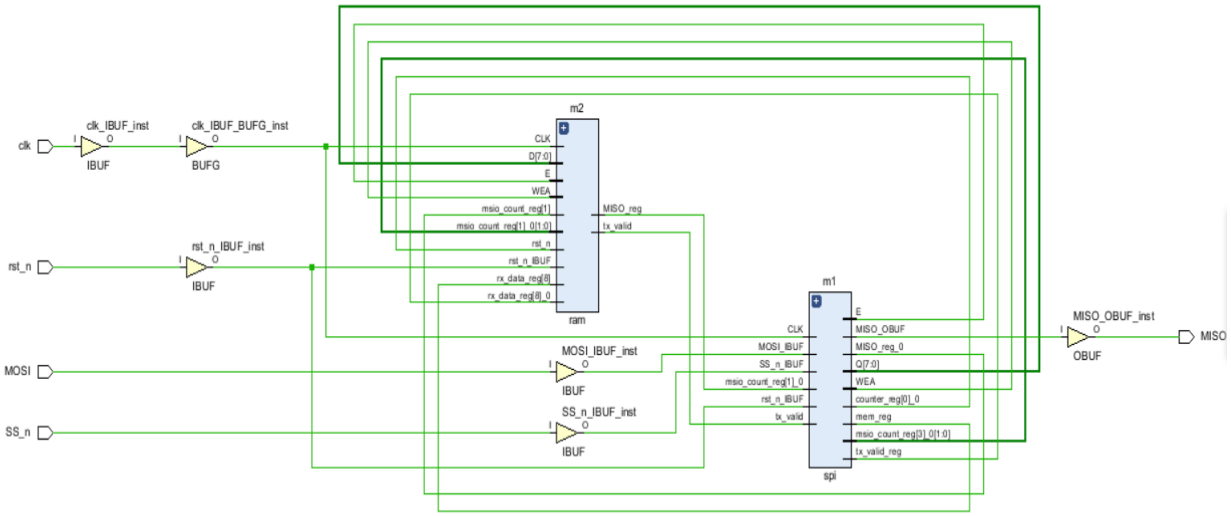
1. One Hot



2. Gray



3. Sequential



➢ Timing Report

1. One Hot

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.261 ns	Worst Hold Slack (WHS):	0.149 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94	Total Number of Endpoints:	94	Total Number of Endpoints:	48

All user specified timing constraints are met.

2. Gray

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.261 ns	Worst Hold Slack (WHS):	0.149 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94	Total Number of Endpoints:	94	Total Number of Endpoints:	48

All user specified timing constraints are met.

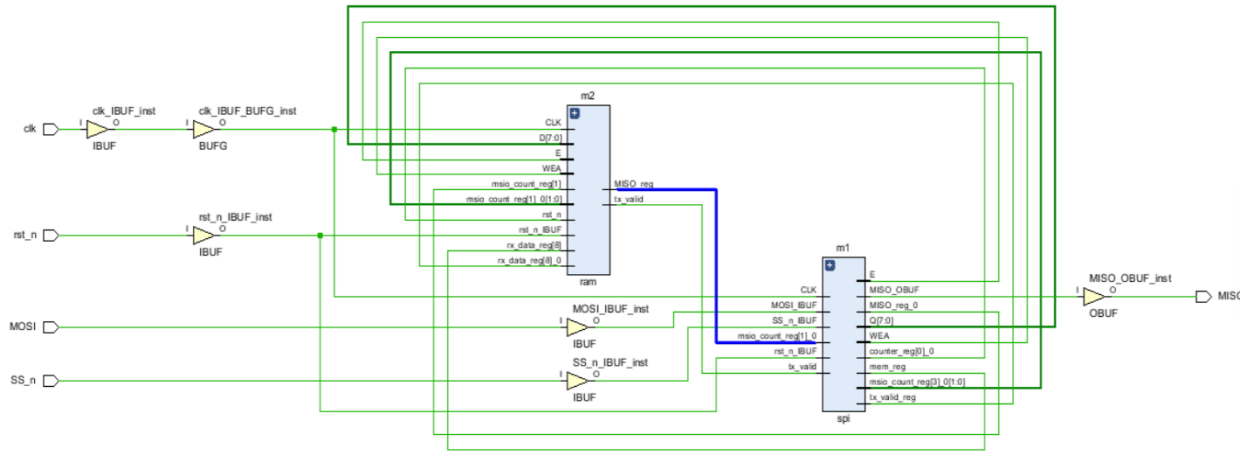
3. Sequential

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.261 ns	Worst Hold Slack (WHS):	0.149 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94	Total Number of Endpoints:	94	Total Number of Endpoints:	48

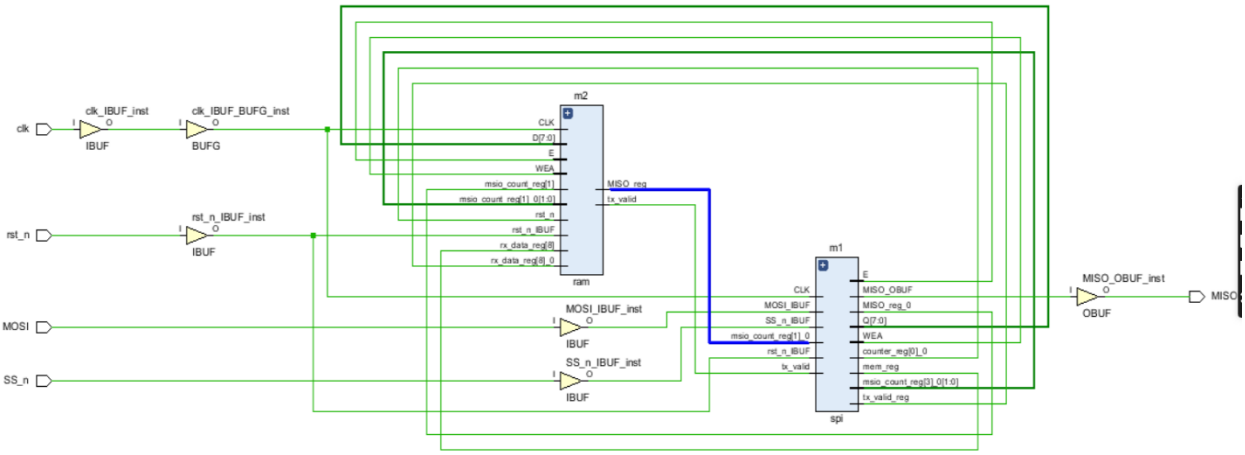
All user specified timing constraints are met.

➢ Critical Path

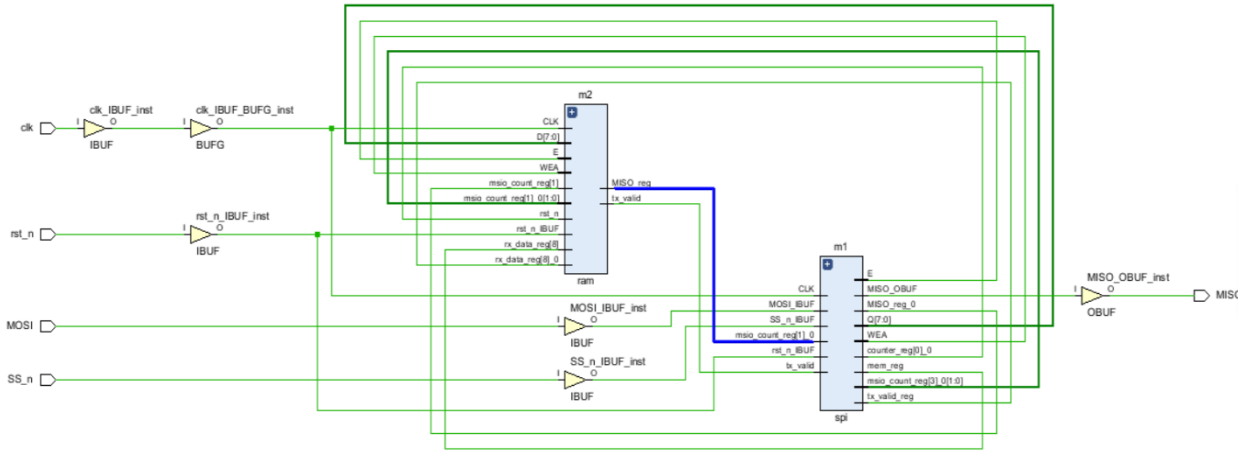
1. One Hot



2. Gray



3. Sequential



6. Implementation - Vivado

➢ Utilization Report

1. One Hot

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
top	37	50	1	23	37	14	0.5	5	1
m1 (spi)	34	41	0	22	34	12	0	0	0
m2 (ram)	3	9	1	3	3	0	0.5	0	0

2.Gray

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
top	34	46	1	20	34	10	0.5	5	1
m1 (spi)	31	37	0	19	31	9	0	0	0
m2 (ram)	3	9	1	3	3	0	0.5	0	0

3.Sequential

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
top	35	46	1	20	35	12	0.5	5	1
m1 (spi)	32	37	0	19	32	11	0	0	0
m2 (ram)	3	9	1	4	3	0	0.5	0	0

➢ Timing Report

1. One Hot

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.026 ns	Worst Hold Slack (WHS):	0.070 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	48

All user specified timing constraints are met.

2. Gray

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.724 ns	Worst Hold Slack (WHS):	0.071 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	46

All user specified timing constraints are met.

3. Sequential

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.052 ns	Worst Hold Slack (WHS):	0.046 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	46

All user specified timing constraints are met.

➢ Messages

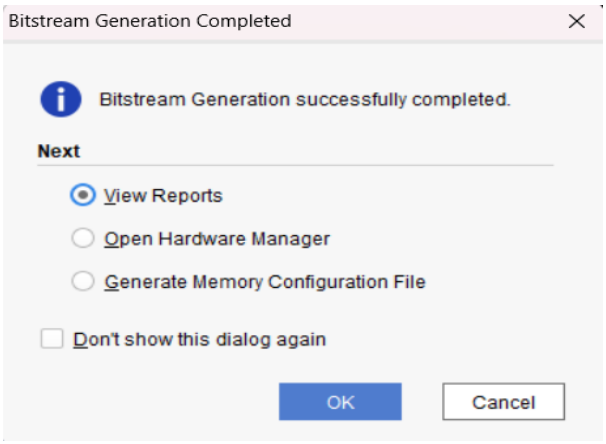
1. One Hot

2. Gray

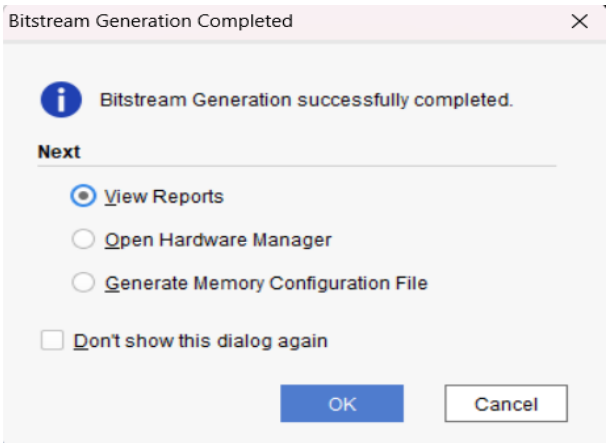
3. Sequential

➢ Bit Stream Generation

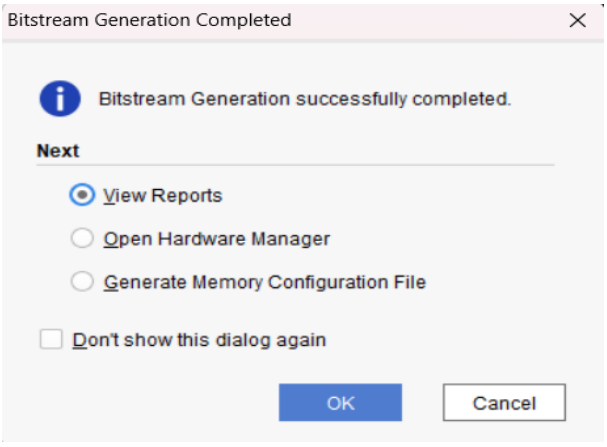
1. One Hot



2. Gray

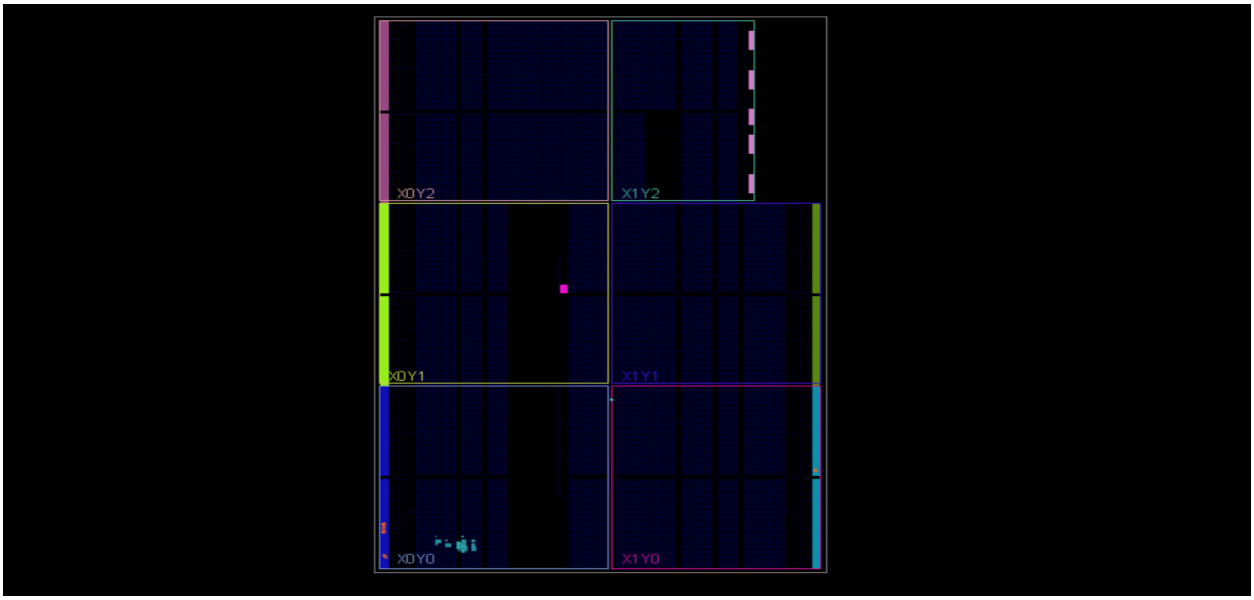


3. Sequential

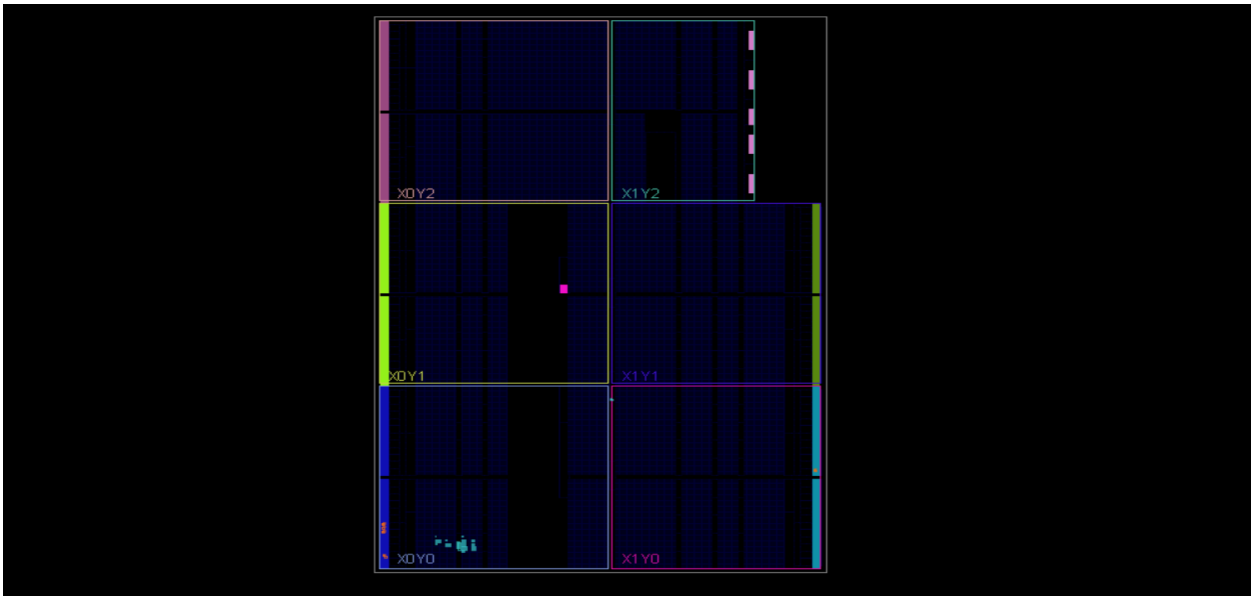


➢ FPGA Device Snippet (Before Adding Debug Core)

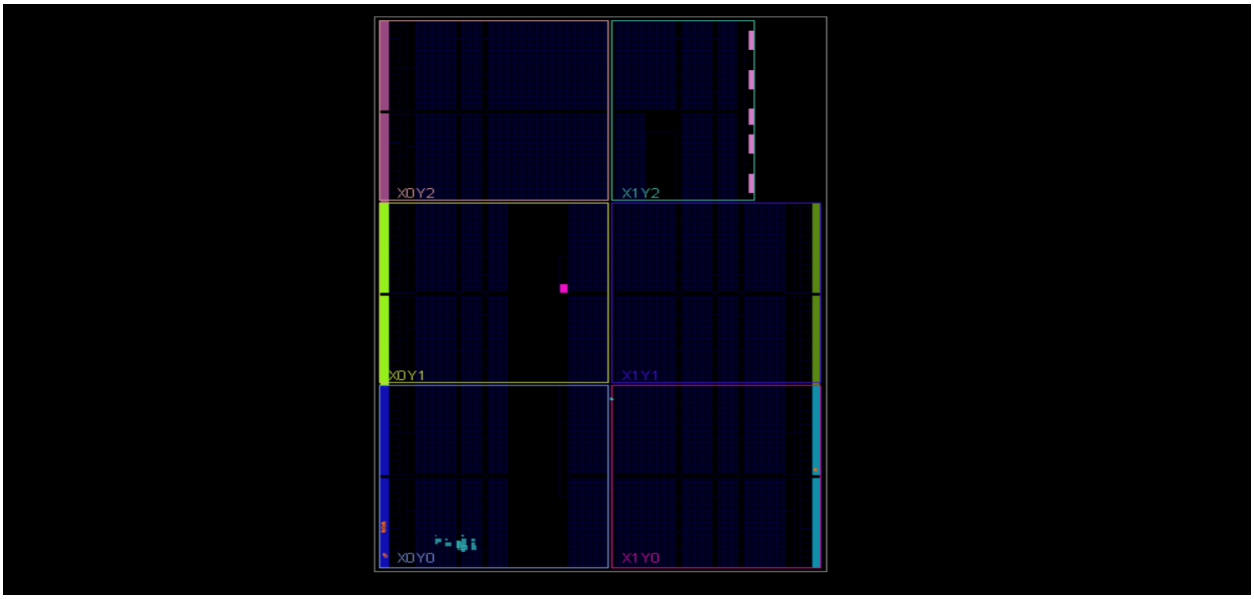
1. One Hot



2. Gray



3. Sequential



➢ FPGA Device Snippet (After Adding Debug Core)