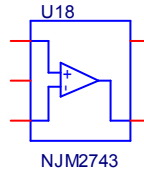# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER:NJM2743
MANUFACTURER: NEW JAPAN RADIO CO.,LTD

**Bee Technologies Inc.**

Spice Model

U18

NJM2743

```
*$
* PART NUMBER:NJM2743
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2006
.Subckt NJM2743 +IN V- -IN OUT V+
X_U1     +IN -IN V+ V- OUT NJM2743_ME
.ends  NJM2743
.subckt NJM2743_ME  1 2 3 4 5
 c1   11 12 8.6603E-12
 c2    6  7 30.000E-12
 dc    5 53 dy
 de   54  5 dy
 dlp  90 91 dx
 dln  92 90 dx
 dp    4  3 dx
 egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
 fb    7 99 poly(5) vb vc ve vlp vln 0 22.818E6 -1E3 1E3 23E6 -23E6
 ga    6  0 11 12 167.30E-6
 gcm   0  6 10 99 5.5435E-9
 iee   3 10 dc 25.700E-6
 hlim 90  0 vlim 1K
 q1   11  2 13 qx1
 q2   12  1 14 qx2
 r2    6  9 100.00E3
 rc1   4 11 5.7045E3
 rc2   4 12 5.7045E3
 re1  13 10 3.6474E3
 re2  14 10 3.6474E3
 ree  10 99 7.7821E6
 ro1   8  5 50
 ro2   7 99 25
 rp    3  4 125.08
 vb    9  0 dc 0
 vc    3 53 dc 1.4979
 ve   54  4 dc 1.4577
 vlim  7  8 dc 0
 vlp  91  0 dc 20
 vln   0 92 dc 20
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=121.25)
.model qx2 PNP(Is=864.3162E-18 Bf=134.3)
.ends
*$
```
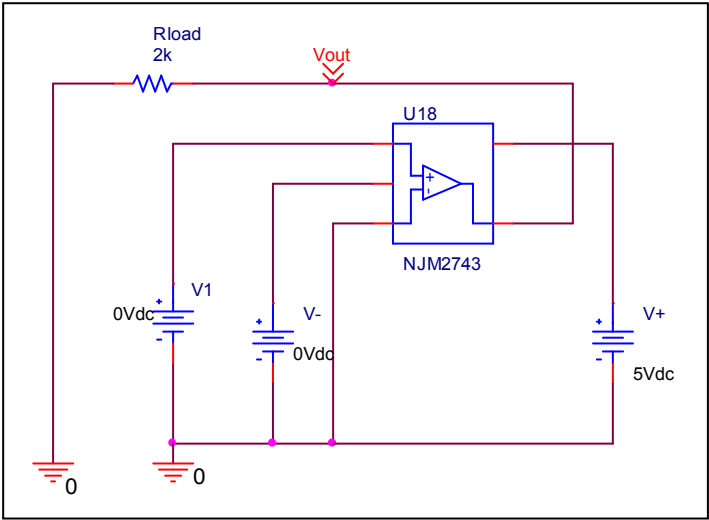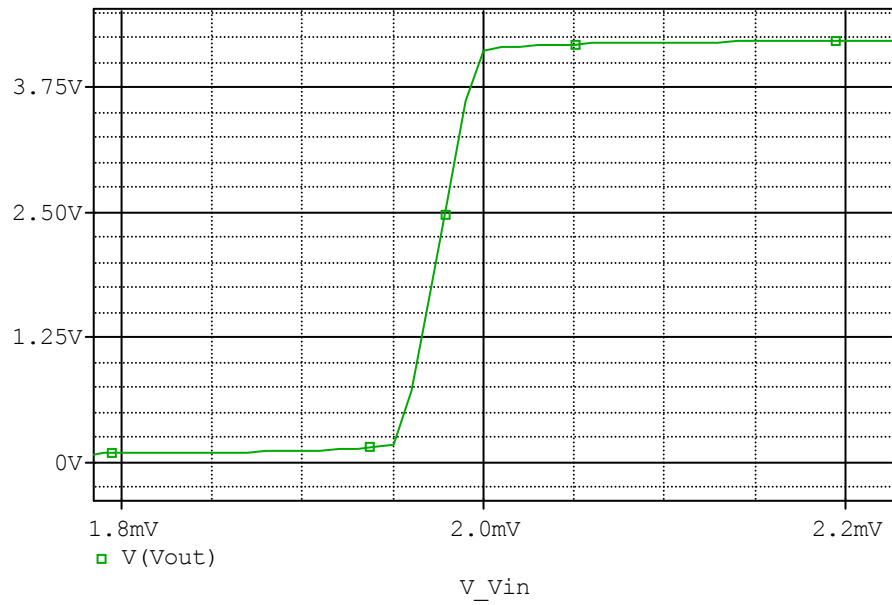
Output Voltage Swing

V(Vout)

V_V1
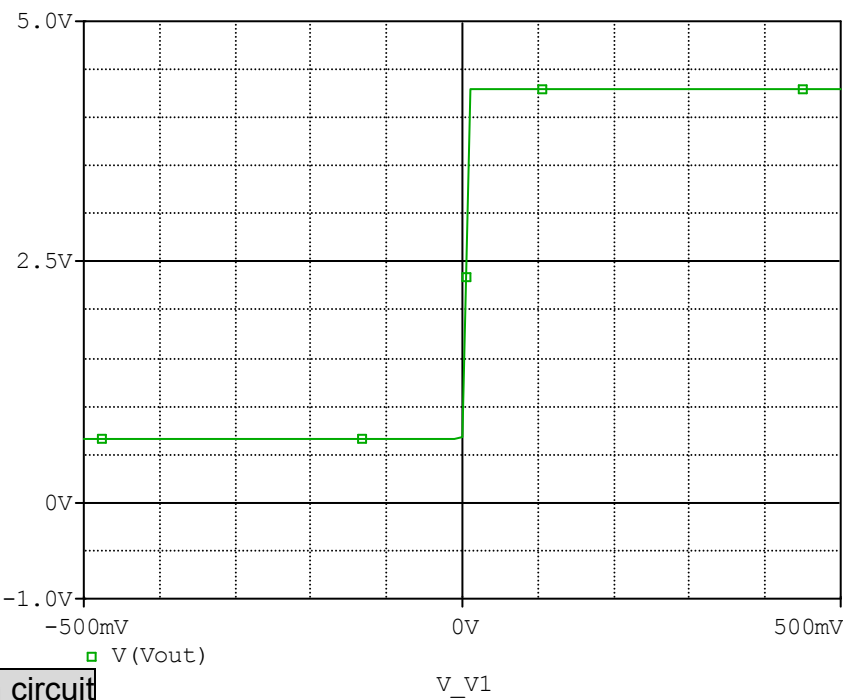
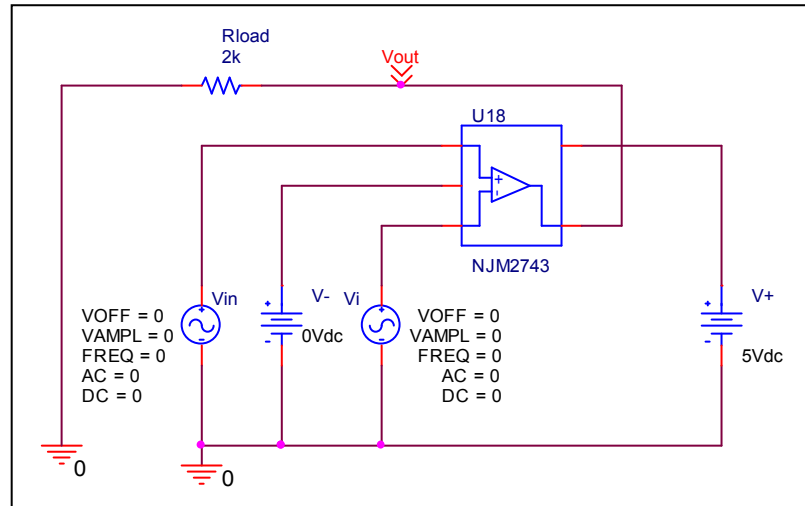| Output Voltage Swing	Data sheet	Simulation	%Error
Vout(V)	4.300	4.298	-0.047
VoL(V)	0.650	0.658	1.231

Input Offset Voltage

Simulation result

□ V(Vout)

V_Vin

Evaluation circuit

	Measurement		Simulation		Error	
Vos	2.000	mV	1.974	mV	-1.300	%

Slew Rate

V(Vout)

Time

Rload
2k

Vout

U18

NJM2743

V1 = 0
V2 = 10
TD = 0
TR = 10n
TF = 10n
PW = 5u
PER = 500u

Vi

V- Vin

VOFF = 0
VAMPL = 0
FREQ = 0
AC = 0
DC = 0

V+

-1.974m

V2

0Vdc

5Vdc

0

0
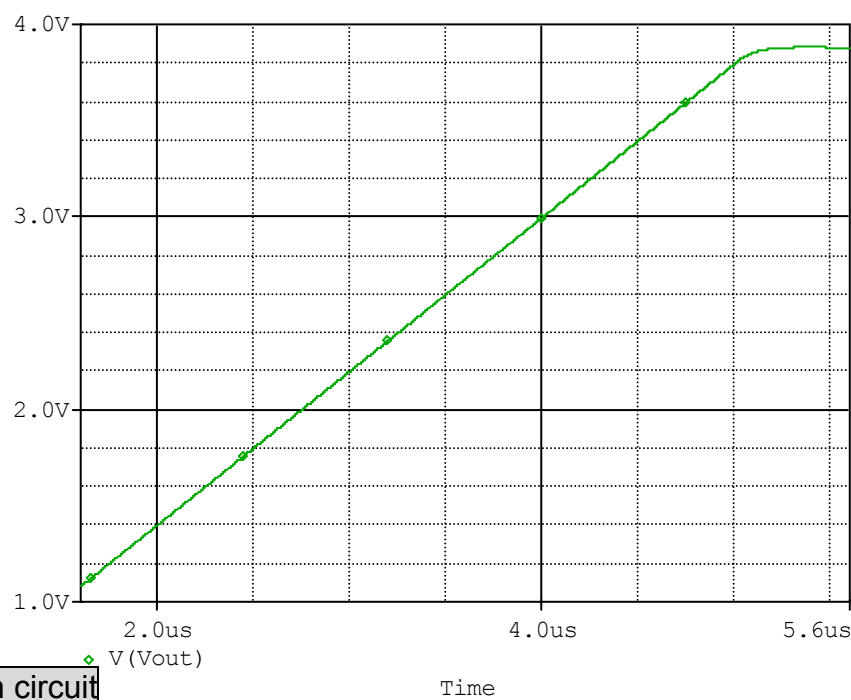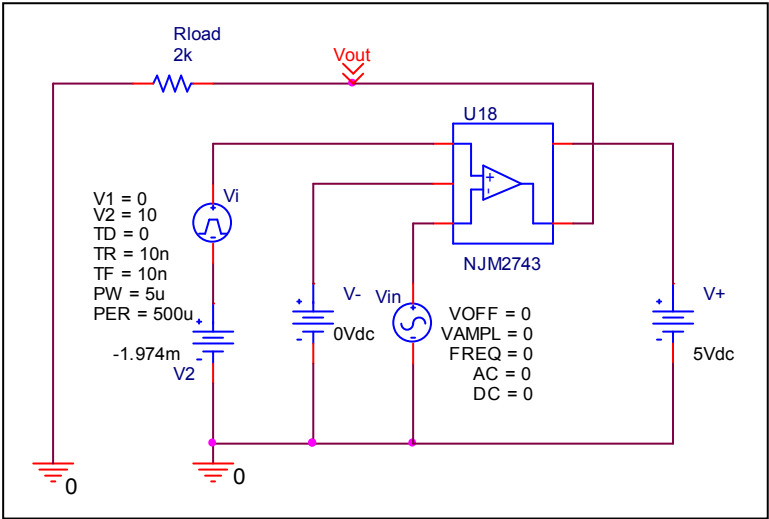
Slew Rate(v/us)	Data sheet	Simulation	%Error
	0.800	0.798	-0.250

Input current

104nA

102nA

100nA

98nA

0s   0.5ms   1.0ms

□ I(Vi)   ◇ I(Vin)

Time
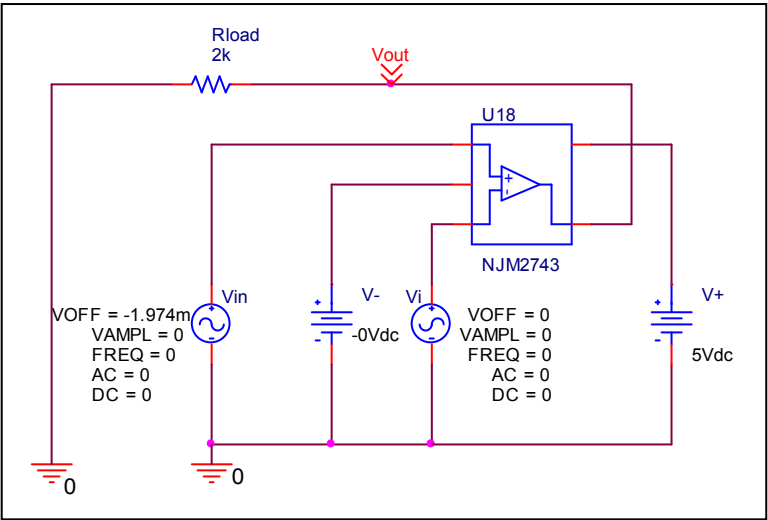
	Data sheet	Simulation	%Error
Ib(nA)	100.000	100.829	0.829
Ibos(nA)	5.000	4.776	-4.480

Open Loop Voltage Gain vs. Frequency

DB(V(Vout)/V(Vin:+))

Frequency
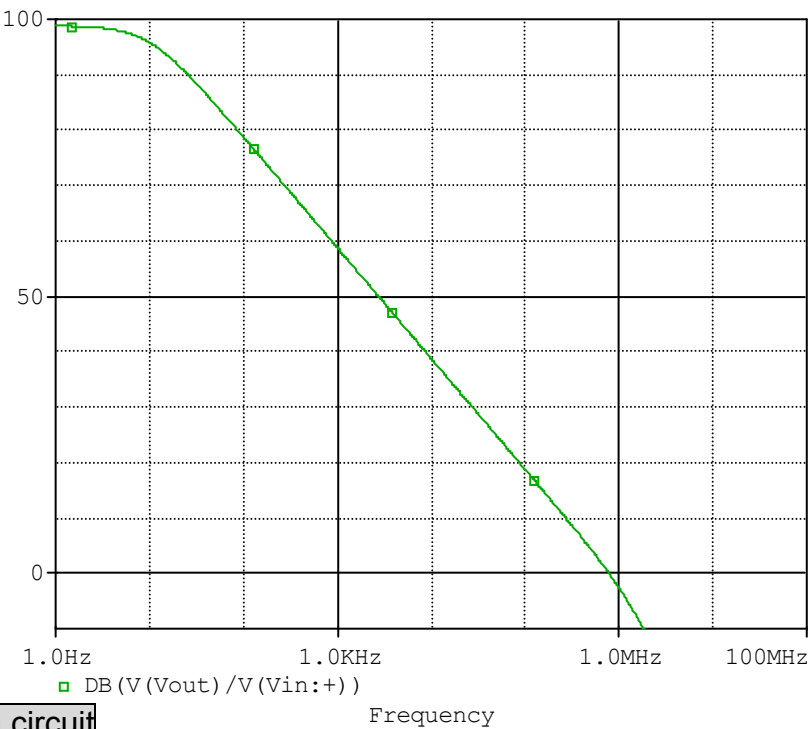
Evaluation circuit
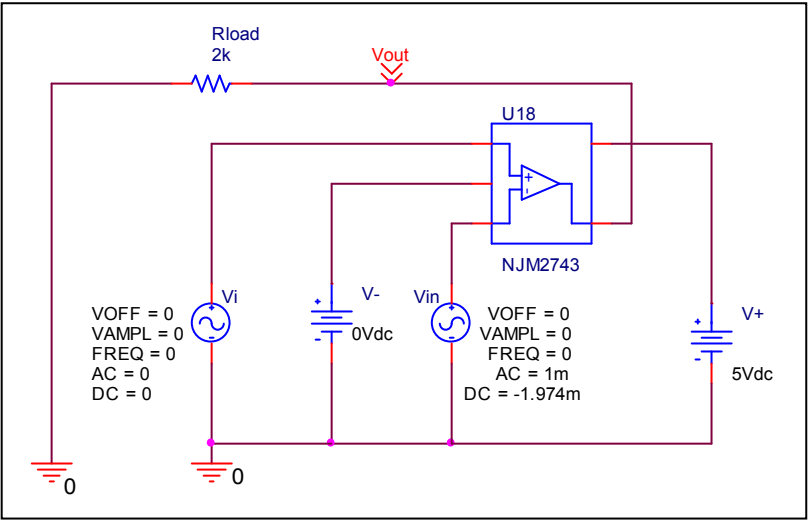
	Data sheet	Simulation	%Error
f-0dB(MHz)	0.850	0.810	-4.706
Av-dc(dB)	100.000	98.791	-1.209

Common-Mode Rejection Voltage gain

Simulation result

- □ V(Vout)

Time
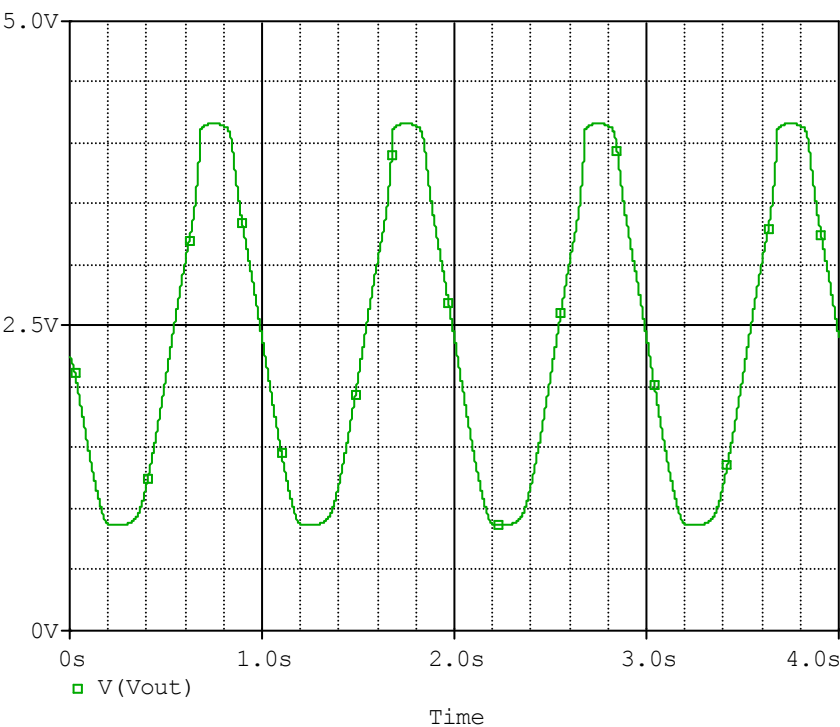
Evaluation circuit
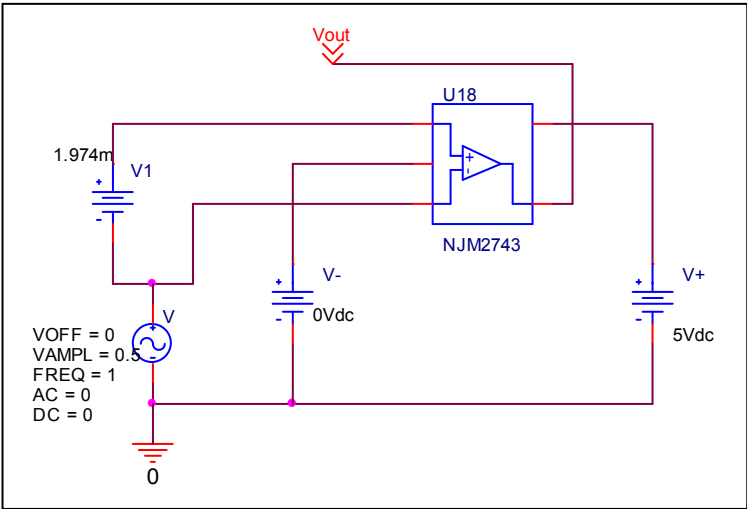
Common Mode Reject Ratio=87006.159/3.293=26405.511

CMRR	Data sheet	Simulation	%Error
	90.000	88.433	-1.741