Analog & Mixed Signal IC Design

Project Report

2-Stage OTA Design

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TASK: Design a 2-Stage OTA with the following specifications:

- UGBW = 160M Hz
- Gain = 65 dB
- Load Capacitance ($\mathbf{C_L}$) = 2.5p F
- Power Consumption < 1m Watt
- V_{DD} = 1.2 V
- Optimize ICMR
- Optimize Slew Rate
- Maximize Output swing

1. Designing

- We first design the 2-stage OTA schematic.

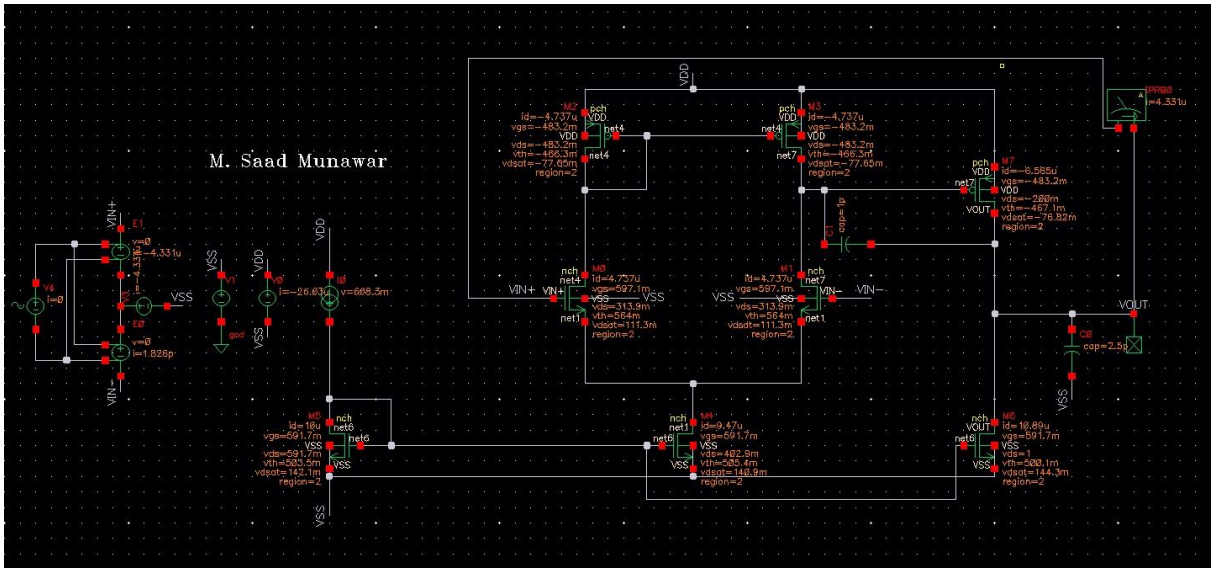

Figure 1.1: 2 Stage OTA schematic

- To make referring to the different transistors in the schematic easier, we refer to them with the following label:
    - Current Mirror transistor directly connected to the current source referred to as M5 in the schematic = **MN_CM1**
    - Current Mirror transistor directly connected to the OTA referred to as M4 in the schematic = **MN_CM2**
    - Current Mirror transistor directly connected to the common source amplifier referred to as M6 in the schematic = **MN_CM3**
    - OTA transistors receiving VIN+ and VIN- = **MN_DA**
    - OTA transistors acting as active load connected to MN_DA, they are referred to as M2 and M3 in the schematic = **MP_AL**
    - Transistor acting as the common source amplifier that is connected to MN_CM3, it is referred to as M7 in the schematic = **MP_CS**
- We connect the OTA to the CS amplifier through another path via a capacitor, the capacitor is referred to as **Cc.**
- Later, a resistor will also be attached in series to the capacitor, it will be referred to as **Rz.**

2. Biasing

- By biasing, we mean that we set all of our transistors to region 2 which is the saturation region.

2.1 MN_CM1

- MN_CM1 is a diode connected current mirror transistor.
- It provides the biasing voltages to MN_CM2 and MN_CM3.
- As long as Vgs is greater than Vth, this transistor will always be in region 2.

$$g_m = \sqrt{2 * I_D * {}^{W}/_{L} * u_{n,p} * C_{ox}} \quad \text{... (1)}$$

Resistance (r) ∝ 1/Transconductance (g_m) … (2)

- In order to increase Vgs greater than Vth, we can as per equation (1) and (2), decrease width of the transistor by **decreasing the multipliers** of the transistor to decrease g_m hence causing an increase in the resistance, which causes an increased voltage drop across the transistor. And as the Source terminal is grounded, so the only way that is possible is by increasing the voltage of the Gate/Drain terminal. Causing Vgs to increase.

For Diode Connected: Vgs = Vds … (3)

For Diode Connected: $V_{DS} = \sqrt{\frac{2*I_D}{K_n}} + V_{TH}$ **… (4)**

Where $K_n = u_n * C_{ox} * (W/L)$ … (5)

- As per equation (4), **increasing the current** through a diode connected transistor will also increase the value of Vds/Vgs as well.
- Vgs greater than Vth will allow the transistor to enter region 2 and hence be properly biased.
- Instead of the current source, we can also connect a diode connected PMOS as well, this will allow the two transistors to act as a voltage divider. By changing the aspect ratios of the two transistors we can set the value of Vgs as per our requirement.

2.2 MN_CM2

- If we properly bias MN_CM1, then MN_CM2 will have a Vgs greater than Vth. The problem that may occur here is that the transistor may be in region 1 (triode region) if its Vds is less than Vov (Vov = Vgs - Vth).
- In this case we can either **reduce Vgs through MN_CM1** to be as close to Vth as possible, while ensuring that MN_CM1 is biased and Vgs stays above Vth. This will cause Vds_sat to fall, hence requiring minimum Vds to operate in region 2.

For Saturation Region: Vds >= Vgs – Vth … (6)

- We can also **decrease the Vds voltage drops of MP_AL and MN_DA**. Doing this will give us enough voltage at the drain terminal of MN_CM2 to ensure proper biasing.

2.2.1 MP_AL

- Vsd can be decreased across MP_AL by decreasing its resistance, which is done by increasing its transconductance, which is done by increasing its width, which is then done by **increasing the multiples of the transistor**.
- As per eq (4), Vsd can also be decreased by **decreasing the I_D through MP_AL**.

2.2.2 MN_DA

- Vds across MN_DA can be decreased, by decreasing its resistance, which can be done by increasing the transconductance, which is done by increasing the width, which is done **by increasing the multipliers of the transistor**.
- Vds can also be decreased by **increasing the current through the transistor** as this causes the transconductance to increase as well causing the resistance to decrease and hence casing Vds to drop.

2.3 MP_AL

- MP_AL is a PMOS current mirror. Meaning that one transistor is diode connected. And the Vg of that transistor is provided to the other transistor in the current mirror.
- So both transistors will always be in region 2, provided effect of Channel length modulation is not too great and provided that Vsg is greater than |Vth|.
- We can ensure biasing for these transistors by making sure that the Vsd/Vsg drop across the transistor is greater than Vth. We can increase the voltage drop

across the transistor by decreasing its transconductance. Which as per equation (1), can be decreased by decreasing its width by **reducing the number of multipliers**.

- As per equation (4), we can increase Vgs across the transistor by **increasing its I_D** as well.
- We can also increase voltage drop across MP_AL by reducing the voltage drop across MN_CM2 and MN_DA as well.

2.4 MN_DA

- MN_DA consists of the main amplifier transistors in the OTA stage, they take a differential input and give out output on a single node.
- MN_DA can go either into region 1 (triode) and region 3 (sub-threshold) as well.
- To avoid region 3, we need to make sure Vgs is greater than Vth. This can be done by:
    - **Increasing V_CM** provided to the transistors.
    - **Increasing I_D** provided to the transistors, as doing this increases the current through MN_CM2, causing its transconductance to increase, causing its resistance to decrease and hence causing a lower Vds across it. As Vs is connected to VSS, so Vd of MN_CM2 decreases, this is also the VS of MN_DA, so decreasing this increases Vgs of MN_DA.
- To avoid region 1, we need to increase Vds to be greater than Vov. This can be done by:
    - Increasing I_D for the same reason mentioned above.
    - To **finetune V_CM** so that Vgs is as close as possible to Vth while being greater than it.
    - By **decreasing the multipliers** of the transistors -> decreases width -> decreases transconductance -> increases resistance -> increases Vds.
    - By decreasing the Vds drops across MP_AL and MN_CM2.

2.5 MP_CS And MN_CM3

- MP_CS acts as the main amplifier transistor for the CS stage.
- MN_CM3 acts as the drain resistance which is biased with help of MN_CM1.
- If proper biasing is done of all the previous transistors, then MP_CS and MN_CM3 will remain either in region 1 or in region 2.
- This is because biasing gate voltage of MN_CM3 is provided by MN_CM1, and biasing gate voltage of MP_CS is provided by the output of the OTA stage.
- MN_CM3 and MP_CS act as voltage divider, and by **changing their aspect ratios** -> changes transconductance -> changes resistance, we can ensure that voltage drop across each resistor is done so that they are both in region 2 (saturation region).

3. Gain

- The Gain formula is given as:

$$A_V = gm_{MN\_DA} (r_{DS\_MN\_DA} \,||\, r_{DS\_MP\_AL}) * gm_{MP\_CS} (r_{DS\_MP\_CS} \,||\, r_{DS\_MN\_CM3}) \ldots (7)$$

- Gain is not affected by the values of Cc and Rz.
- To increase our gain, we need to increase the transconductances of MN_DA and MP_CS. This can be done by **increasing the multiples of MN_DA and MP_CS** -> increases width -> increases transconductance.
- We can also **increase the current** flowing through the circuit to increase the transconductances of the transistors resulting in a higher value for gain.
- We also need to optimize the values of the resistances of MN_DA, MP_AL, MP_CS and MN_CM3 as well.
- As we have already decided on the aspect ratios and the current flowing through the transistors for optimizing transconductances of MP_CS and MN_DA, so we cannot change r_{DS} for MP_CS and MN_DA as it also depends on the same parameters.
- We now optimize the r_{DS} of MN_CM3 and MP_AL, by **decreasing their multiples of MP_AL and MN_CM3** -> decreases width -> decreases transconductance -> increases resistance.
- We increase the resistance as in the numerator the resistances are being multiplied while in the denominator they are being added. So the numerator has the more dominant value.

3.1 Results For Achieving Required Gain (65 dB)

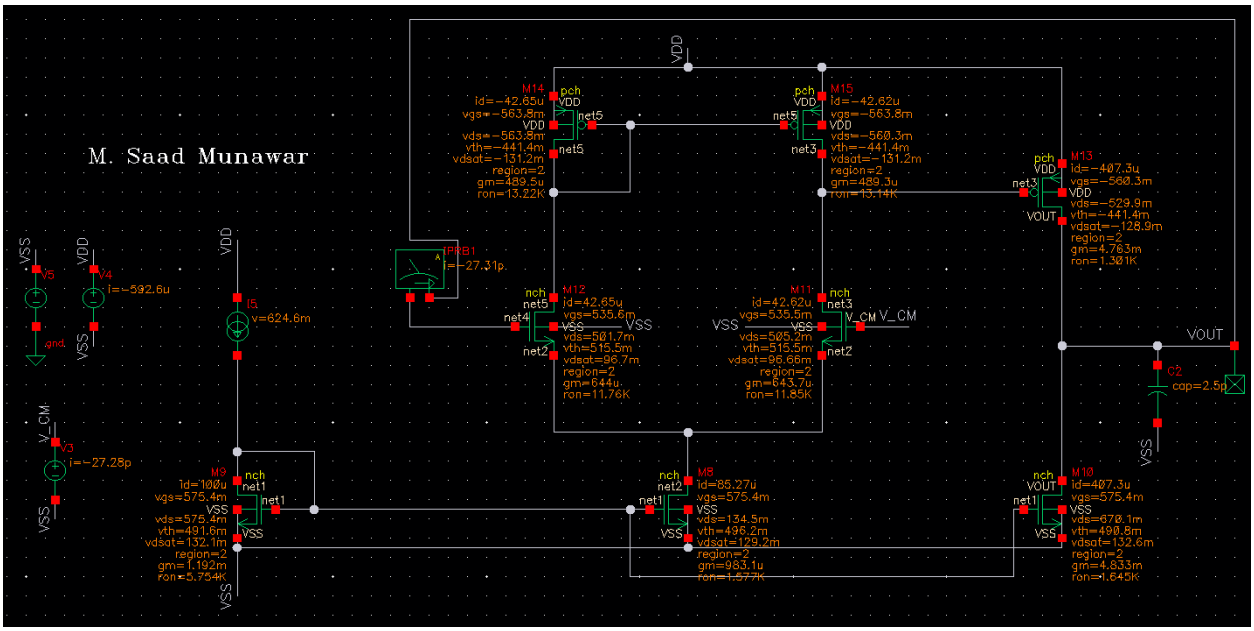

Figure 3.1: Circuit Diagram for Feedback

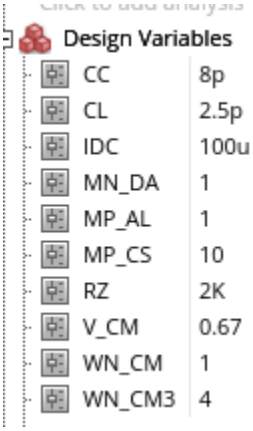

Figure 3.2: Final Parameter values for required Gain (exclude CC and RZ for now); Unit Transistor **Length = 500n m**; Unit Transistor **Width = 18u m**; MN_DA = Multipliers of MN_DA; MP_AL = Multipliers of MP_AL; MP_CS = Multipliers of MP_CS; WN_CM = Multipliers of MN_CM1 and Multipliers of MN_CM2; WN_CM3 = Multipliers of MN_CM3

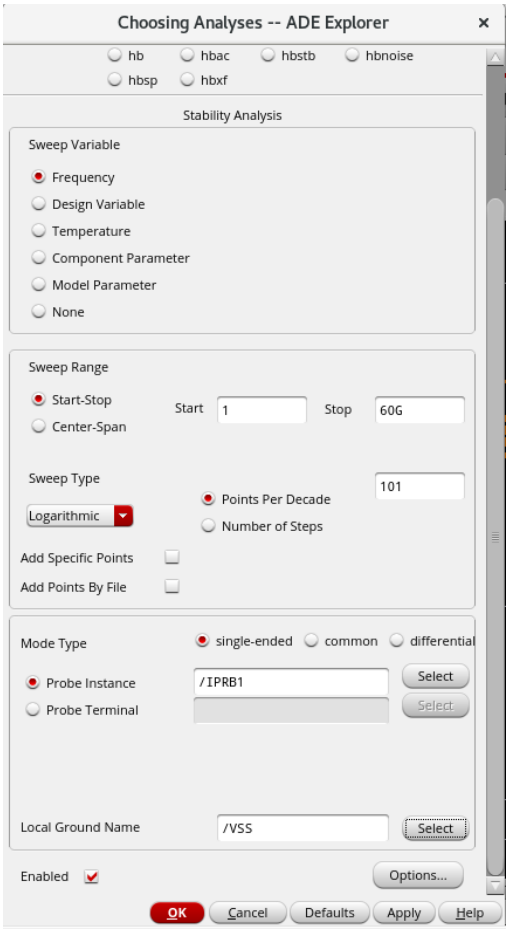

Figure 3.3: Stability Settings

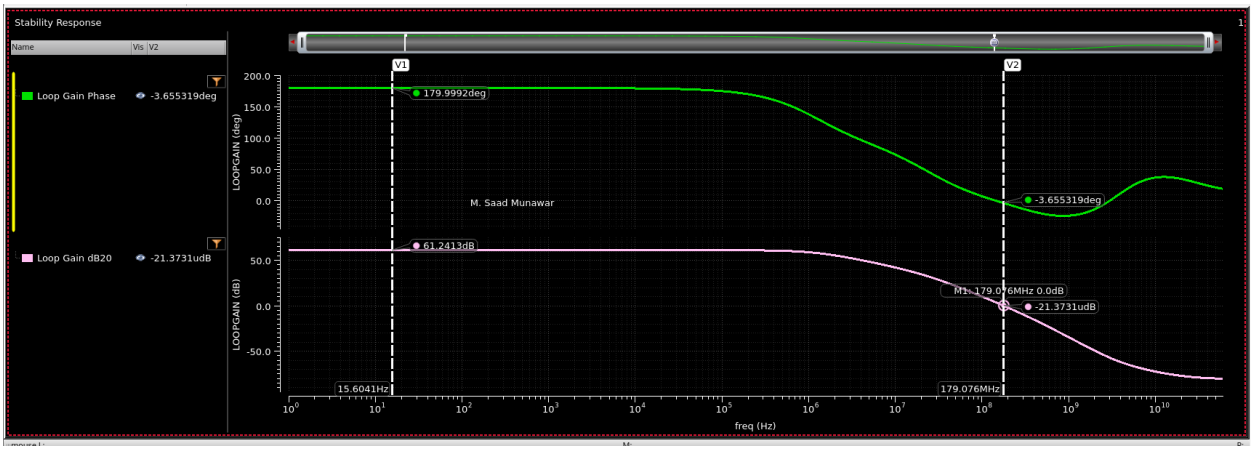

Figure 3.4: Feed Back Gain = 61.24 dB; Band Width = 179M Hz; Phase Margin = -3.65

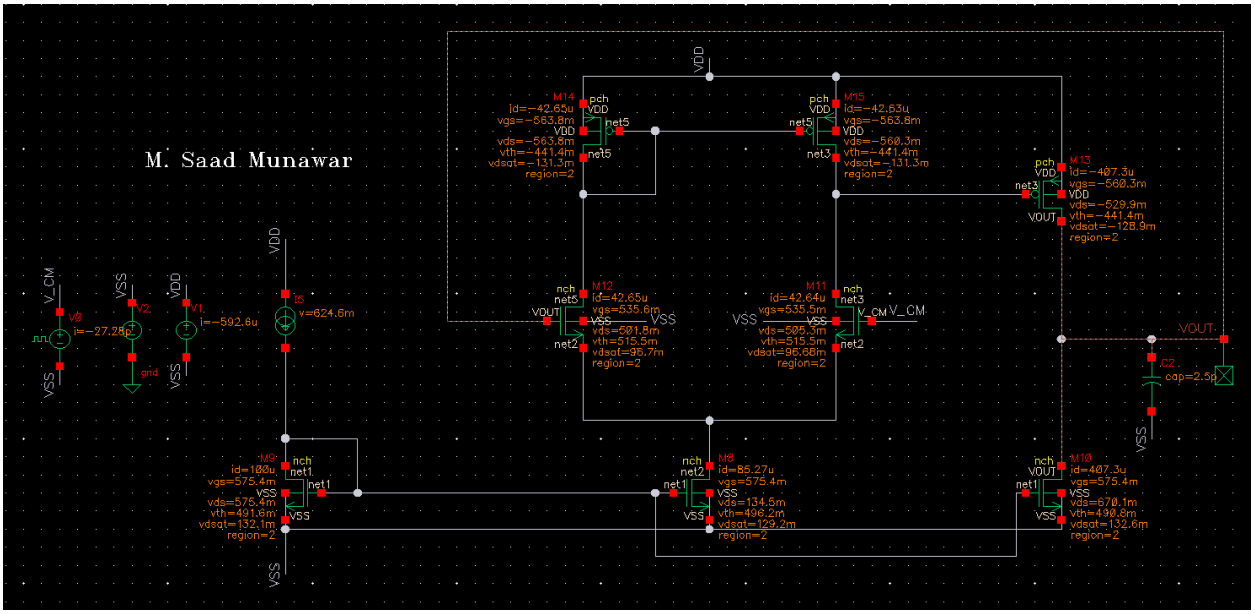

Figure 3.5: Circuit Diagram for Slew Rate

slewRate(VT("/VOUT") -4.7u nil 1.13...

	Expression	Value
1	slewRate(VT("/...	420.5E6

Figure 3.6: Slew Rate

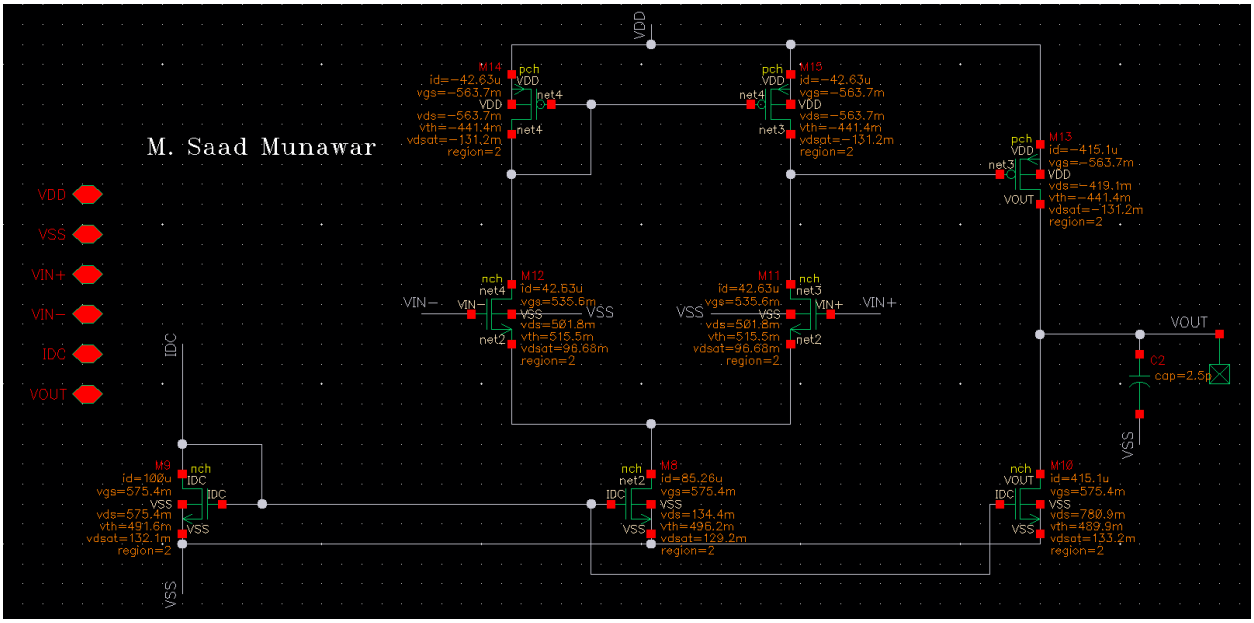

Figure 3.7: Circuit Diagram for Differential Mode

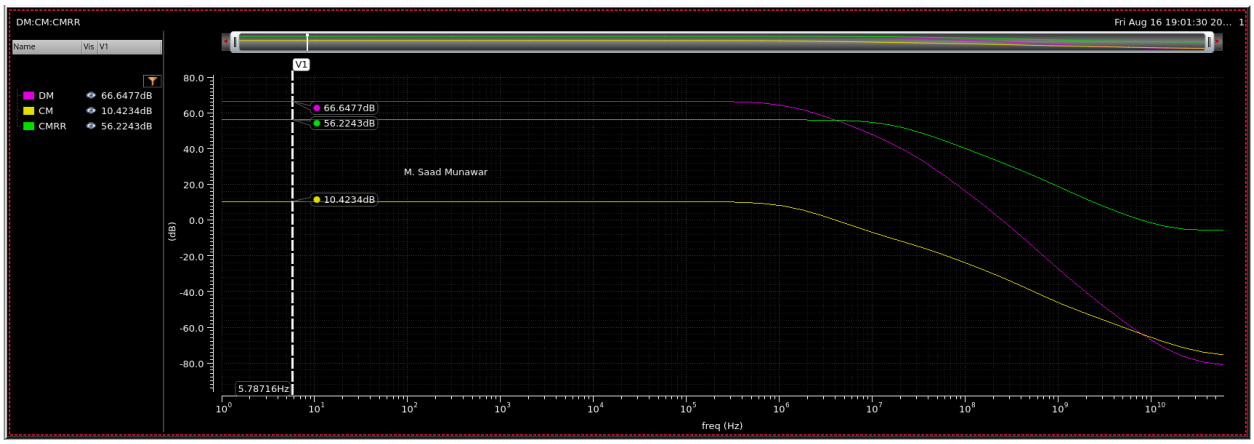

Figure 3.8: ADM, ACM and CMRR

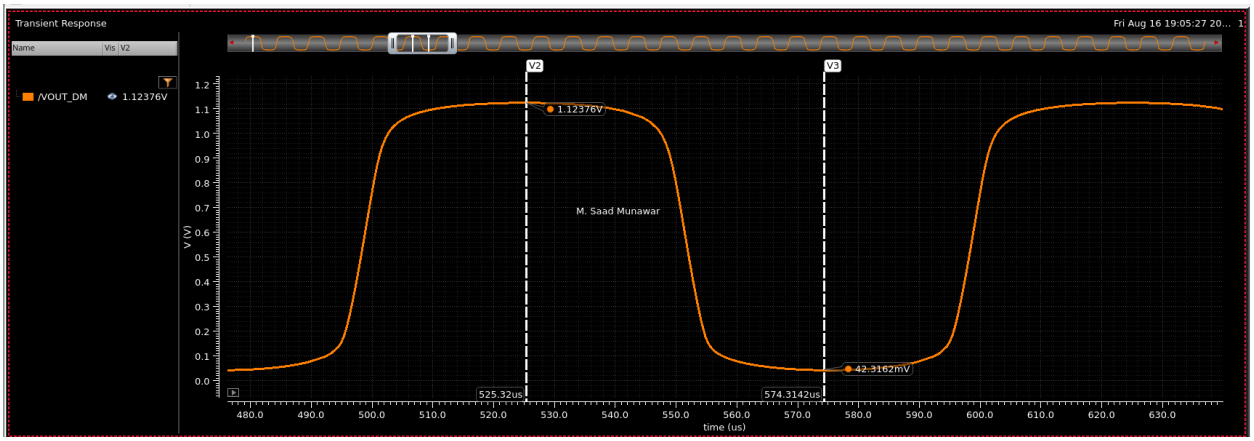

Figure 3.9: Output Swing

3.1.1 ICMR Calculation

From figure 3.7:

$ICMR_{MAX} = VDD - Vsg_{MP\_AL} + Vth_{MN\_DA} = 1.2 - 0.5637 + 0.5155 = 1.1518\ V$

$ICMR_{MIN} = Vds_{MN\_CM2} + Vth_{MN\_DA} = 0.1344 + 0.5155 = 0.6499\ V$

3.1.2 Result Summary

Table 3.1

PARAMETERS	VALUES
Feed Back Gain	61.24 dB
Differential Gain	66.65 dB
Phase Margin	-3.65
Bandwidth	179M Hz
Slew Rate	420.5 V/u sec
ICMR	0.6499 V – 1.1518 V
CMRR	56.2 dB
Output Swing	1.08 V
Bias Current	100u A
Power Consumption	0.6m Watt

4. Phase Margin

- As per table 3.1, we have achieved our required gain and bandwidth. However, our phase margin which should be in the 45-60 degrees range is currently -3.65 degree.
- For Phase Margin, we have:

  For 45 degrees: Cc = 0.122 * C_L; For 60 degrees: Cc = 0.22 * C_L … (8)

- We add a miller capacitor between the output of the OTA and the input of the CS amplifier.
- This miller capacitance increases our phase margin, and from equation (8), we see that increasing the value of the capacitance will increase our phase margin.
- After optimizing the circuit, we set the value of the miller capacitance as **8p F**.

4.1 Results For Achieving Required Phase Margin

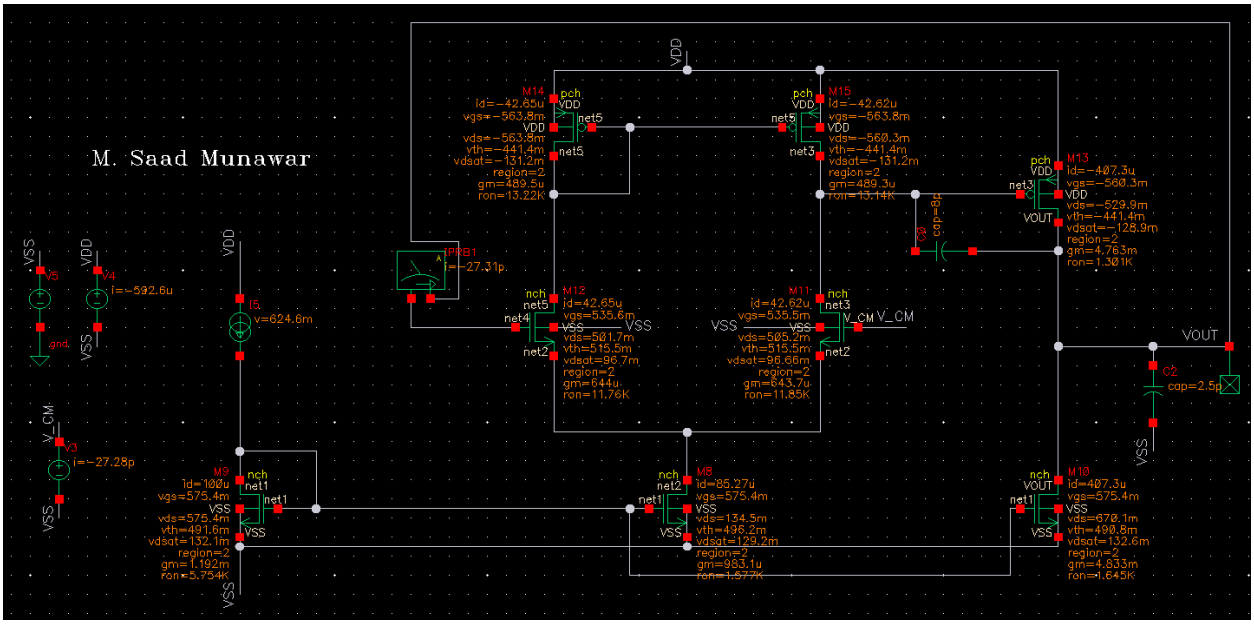

Figure 4.1: Circuit Diagram

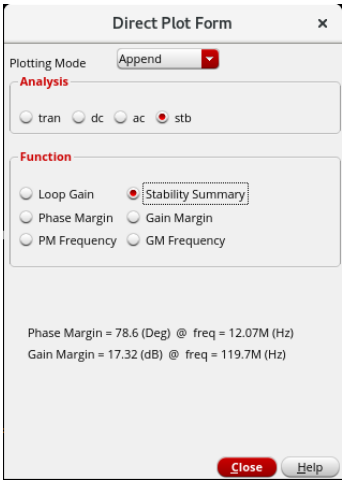

Figure 4.2: Phase Margin: 78.6

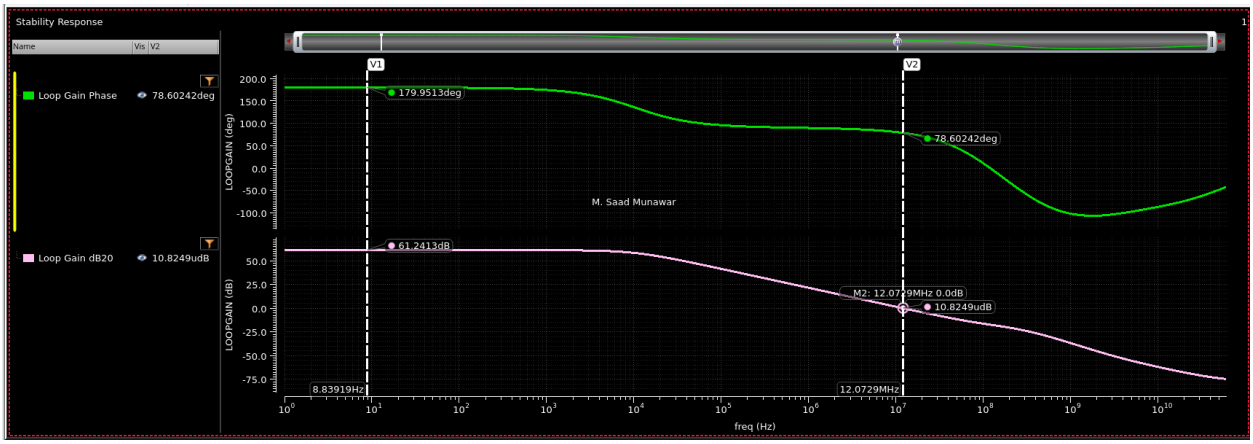

Figure 4.3: Gain: 61.24 dB; Bandwidth: 12.07M Hz

Slew Rate	expr	slewRate(VT("/VOUT") 0.163 nil 1.1315 nil 10 90 nil "time")	11.67M

Figure 4.4: Slew Rate: 11.67 V/u sec

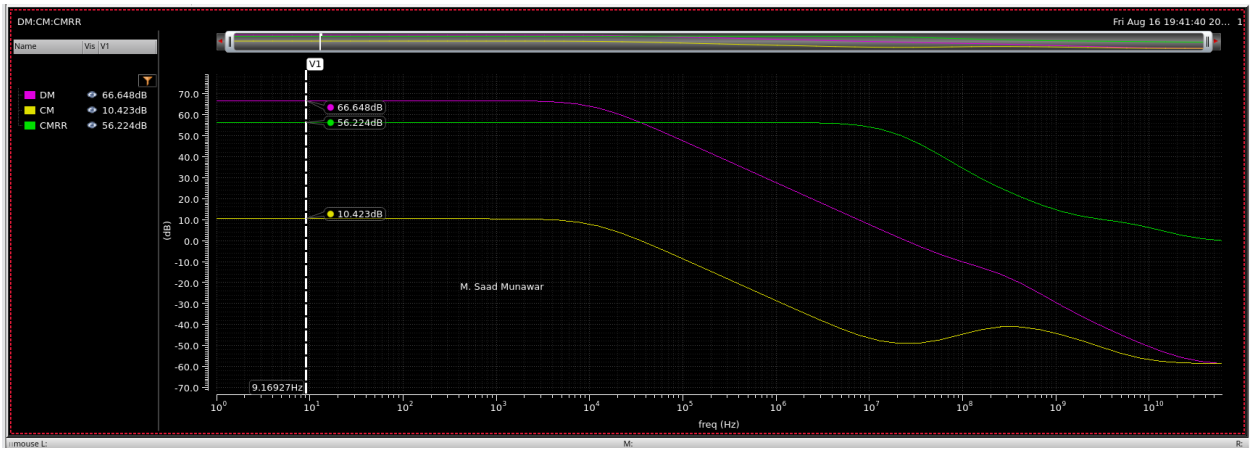

Figure 4.5: ADM: 66.65 dB; CMRR: 56.2 dB

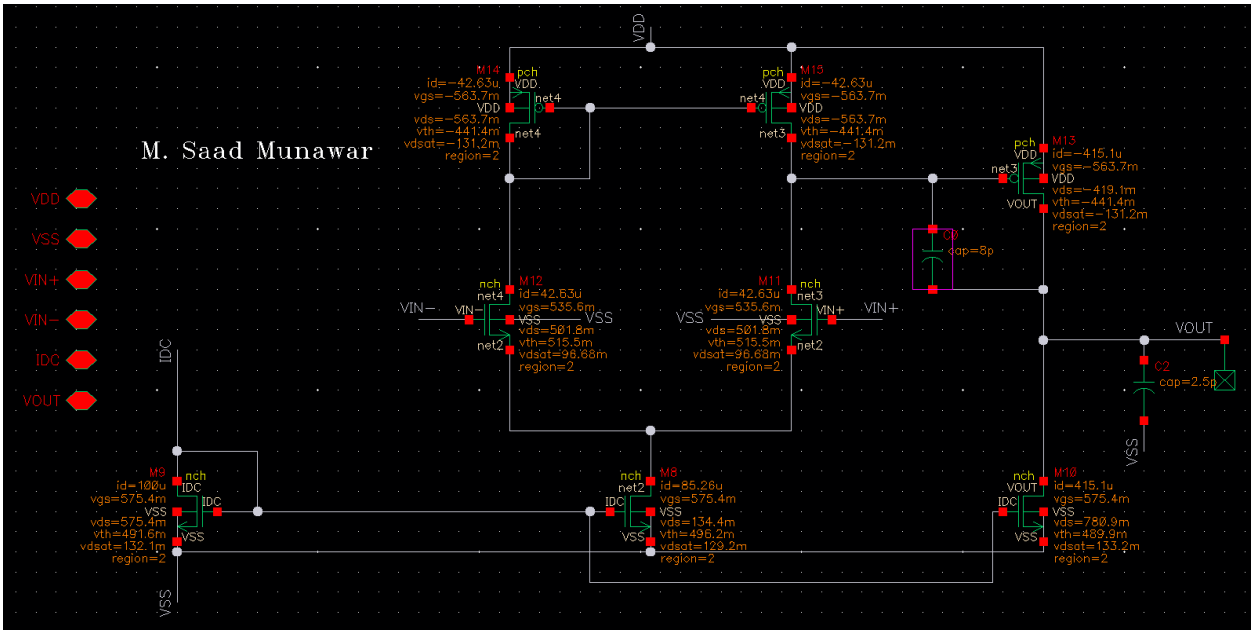

Figure 4.6: Differential Mode Circuit Diagram

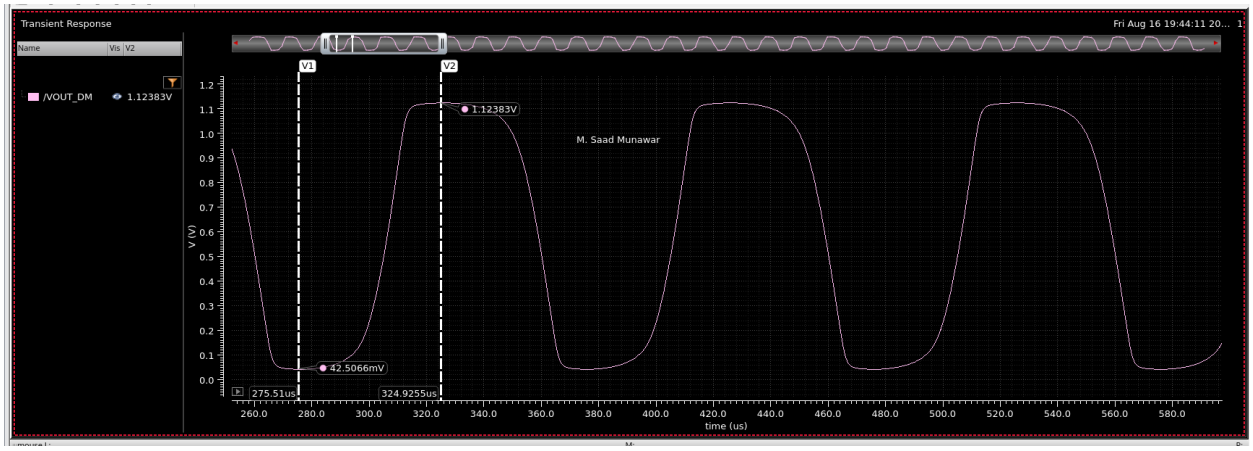

Figure 4.7: Output Swing

4.1.1 ICMR Calculation

From figure 4.6:

$ICMR_{MAX} = VDD - Vsg_{MP\_AL} + Vth_{MN\_DA} = 1.2 - 0.5637 + 0.5155 = 1.1518\ V$

$ICMR_{MIN} = Vds_{MN\_CM2} + Vth_{MN\_DA} = 0.1344 + 0.5155 = 0.6499\ V$

4.1.2 Result Summary

Table 4.1

PARAMETERS	VALUES
Feed Back Gain	61.24 dB
Differential Gain	66.65 dB
Phase Margin	78.6
Bandwidth	12.07M Hz
Slew Rate	11.67 V/u sec
ICMR	0.6499 V – 1.1518 V
CMRR	56.2 dB
Output Swing	1.08 V
Bias Current	100u A
Power Consumption	0.6m Watt

- We observe that the only values that change are Phase Margin, Band width and Slew Rate.
- Phase Margin increases to our required 78.6.
- Bandwidth however decreases from our required 179M Hz to 12.07M Hz. Which is quite less than our required specification.
- This is because adding the Miller capacitance moves the first pole closer to the origin by a significant amount.

$$P_1 = -(gds2 + gds4)(gds6 + gds7)/(gm6C_C)$$

- The second pole is moved away from the origin.

$$P_2 = -gm6/C_2$$

- Adding in the miller capacitance introduces a zero.

$$Z = gm6/C_C$$

- Formula wise, the unity gain bandwidth is given as:

$$GB = gm2/C_C$$

- Our slew rate also decreases tremendously from 420.5 to 11.67. Where the slew rate has an inverse relationship with the miller capacitance defined as:

$$\textbf{Slew Rate} = I_{Bias}/C_C$$

5. Band Width

- Now, we want to reclaim the bandwidth we have lost. For this purpose, we add a nulling resistance Rz in series with the miller capacitor.
- This Rz introduces another pole in the system. However, since that pole is away from the 0 dB point, so it is not a concern for us.

$$\mathbf{P = -1/(Rz*C_1)}$$

- What Rz mainly does is it puts the zero in our control. Using this zero we can extend our bandwidth to reclaim the bandwidth that we have lost.

$$\mathbf{Z = 1/(C_C((1/gm_{11})-Rz))}$$

- Our required bandwidth is achieved at **Rz = 2k ohms**.
- The general trend seen for bandwidth was, increasing the multipliers of CS increases our bandwidth a bit but reduces our phase margin. Then reducing Rz increases our phase margin again but also reduces our bandwidth but only a bit. Finally increasing I_{BIAS} and setting all the values according to it gives us a good boost in the bandwidth.

5.1 Results For Achieving Required Bandwidth

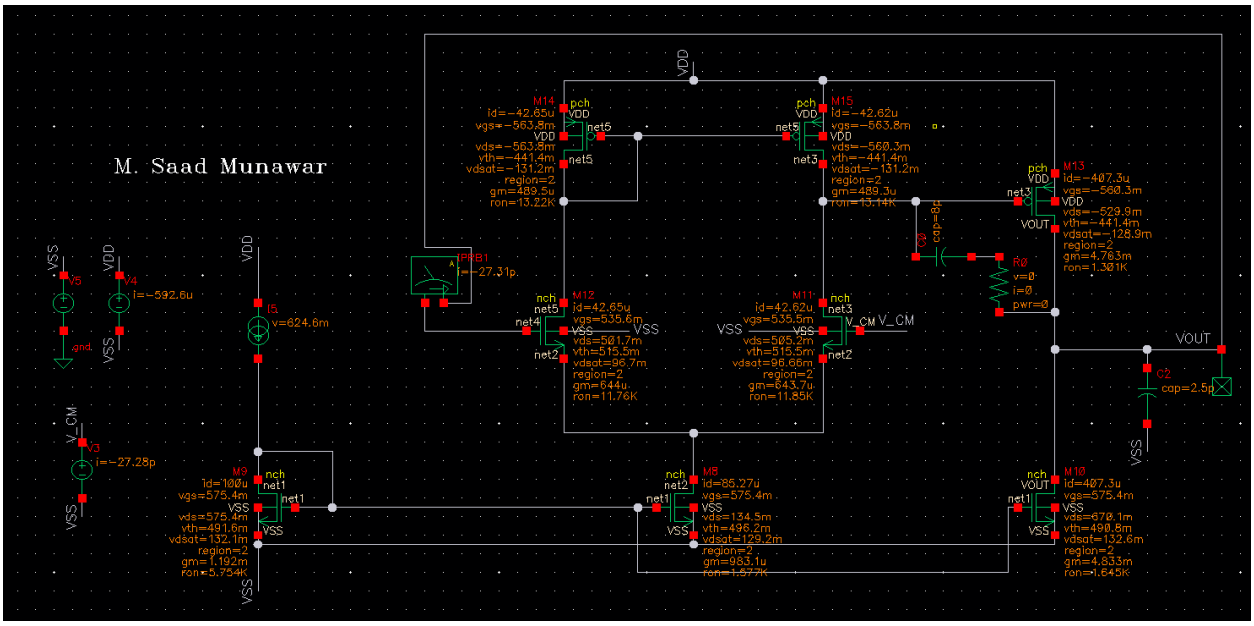

Figure 5.1: Circuit Diagram

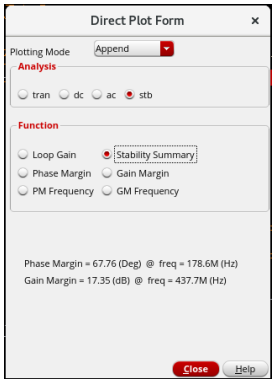

Figure 5.2: Stability: Phase Margin = 67.76

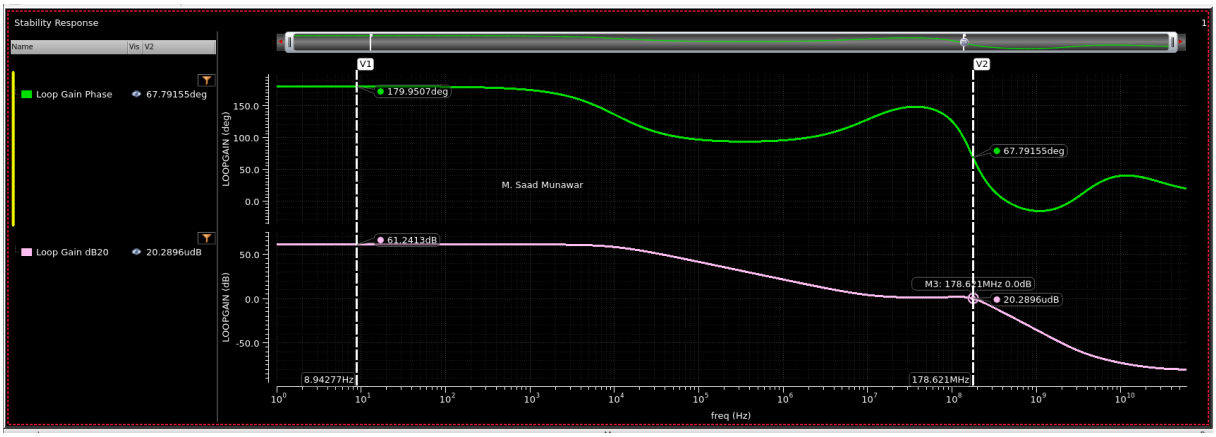

Figure 5.3: Gain = 61.24 dB; Bandwidth = 178.6M Hz

Slew Rate	expr	slewRate(VT("/VOUT") 0.163 nil 1.1315 nil 10 90 nil "time")	11.08M

Figure 5.4: Slew Rate

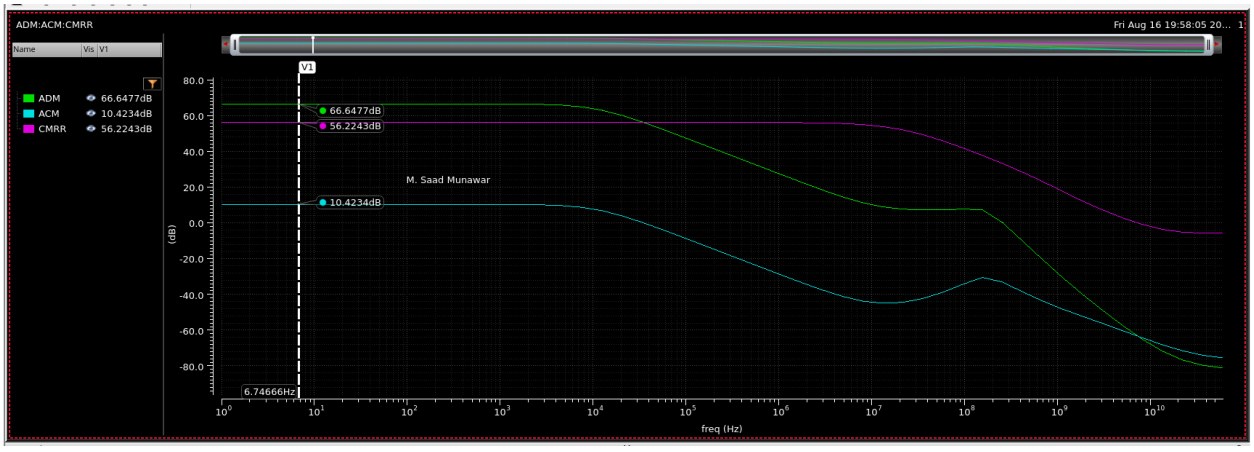

Figure 5.5: ADM = 66.65 dB; CMRR = 56.2 dB

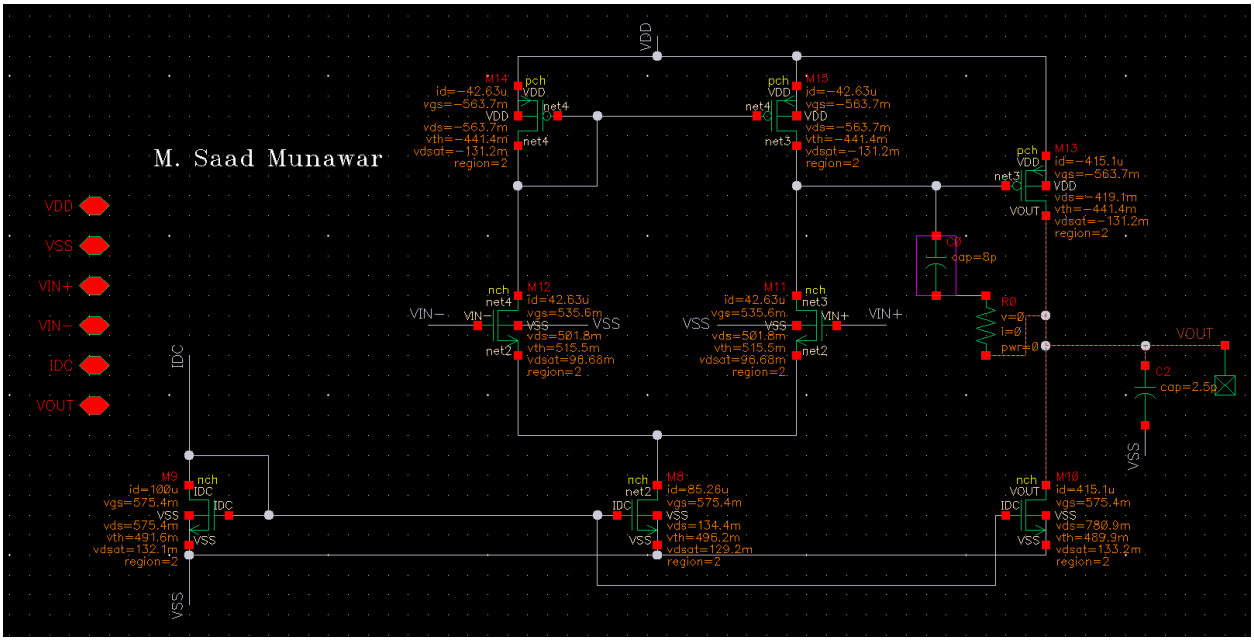

Figure 5.6: Differential Mode Circuit Diagram

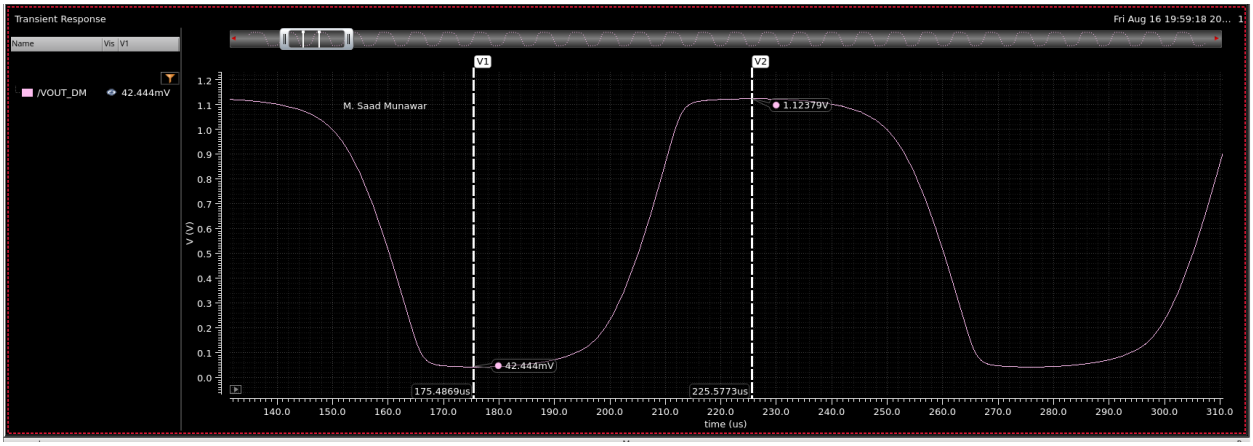

Figure 5.7: Output Swing

5.1.1 ICMR Calculation

From figure 5.6:

$ICMR_{MAX} = VDD - Vsg_{MP\_AL} + Vth_{MN\_DA} = 1.2 - 0.5637 + 0.5155 = 1.1518\ V$

$ICMR_{MIN} = Vds_{MN\_CM2} + Vth_{MN\_DA} = 0.1344 + 0.5155 = 0.6499\ V$

5.1.2 Final Result Summary

Table 5.1

PARAMETERS	VALUES
Feed Back Gain	61.24 dB
Differential Gain	66.65 dB
Phase Margin	67.76
Bandwidth	178.6M Hz
Slew Rate	11.08 V/u sec
ICMR	0.6499 V – 1.1518 V
CMRR	56.2 dB
Output Swing	1.08 V
Bias Current	100u A
Power Consumption	0.6m Watt

- Our phase margin has decreased a bit, but we have recovered the entirety of our bandwidth.

6. Comparison of OTA without Cc and Rz, with Cc and with both Cc and Rz

PARAMETERS	No Capacitor and Resistance	C_C = 8p F	C_C = 8p F and Rz = 2k ohms
Feed Back Gain	61.24 dB	61.24 dB	61.24 dB
Differential Gain	66.65 dB	66.65 dB	66.65 dB
Phase Margin	-3.65	78.6	67.76
Bandwidth	179M Hz	12.07M Hz	178.6M Hz
Slew Rate	420.5 V/u sec	11.67 V/u sec	11.08 V/u sec
ICMR	0.6499 V – 1.1518 V	0.6499 V – 1.1518 V	0.6499 V – 1.1518 V
CMRR	56.2 dB	56.2 dB	56.2 dB
Output Swing	1.08 V	1.08 V	1.08 V
Bias Current	100u A	100u A	100u A
Power Consumption	0.6m Watt	0.6m Watt	0.6m Watt

- We see that after setting our gain, the only values that undergo any change are the slew rate, phase margin and the bandwidth. All these parameters depend on our miller's capacitance. Our phase margin and bandwidth are also affected by Rz.
- We can also cancel our p1 with z if we set a very high value of Rz. This increases our corner frequency. This can be achieved by replacing Rz with a transistor acting as a resistor. However, keep in mind that in this case, we give up our control on the phase margin, and it changes with our gain.

7. Layout

7.1 Pre-Layout Changes

- For the layout, the common centroid configuration is used. To make the **common centroid** configuration easier some changes were made in the schematic.

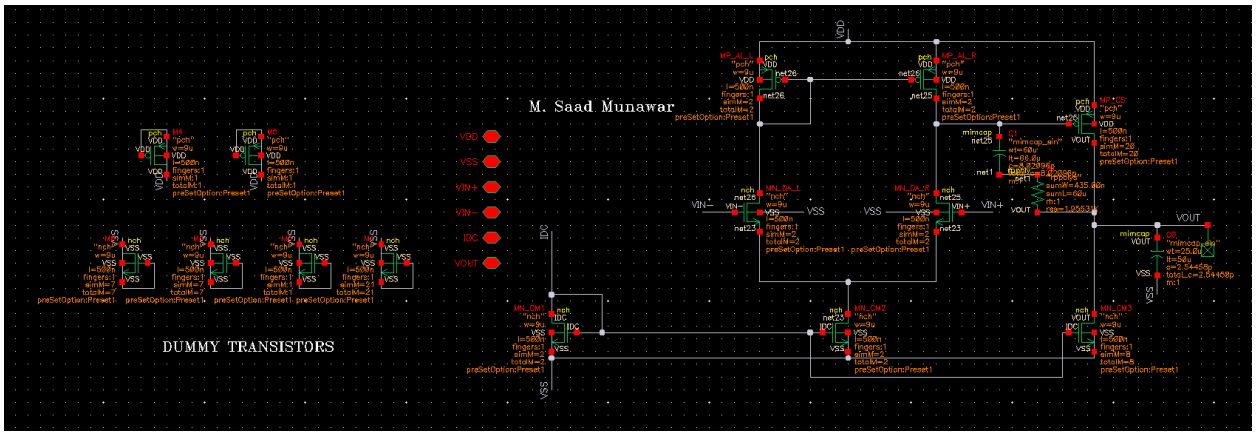

Figure 7.1: Schematic used for Layout

- For common centroid it is better to have your multiples in even numbers.
- For the schematic, following **changes** were made:
    - Unit Transistor Width: 18um -> 9um
    - MP_AL, MN_DA, MN_CM1, MN_CM2 multipliers: 1 -> 2
    - MN_CM3 multipliers: 4 -> 8
    - MP_CS multipliers: 10 -> 20
- Furthermore, to keep the environment same, we add **dummy transistors** on both side of the active transistors. And then to maintain a good shape and symmetry we add more dummy transistors on the left and right of active transistors. In total we add 2 PMOS dummy transistors and 36 NMOS dummy transistors.

- For the **resistor**, we use an 'rppoly' resistor from 'tsmcN65' library.

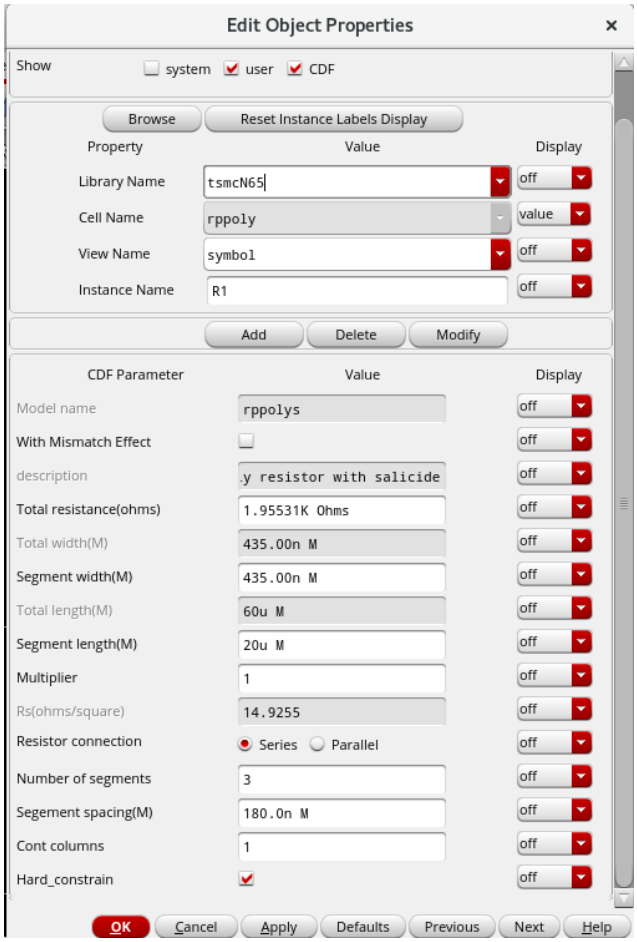

Figure 7.2: Resistor specifications

- For the **capacitor** we use a 'mimcap' capacitor from the 'tsmcN65' library. It should be noted that it is better to use a small capacitor with many multiples as opposed to one big capacitor.

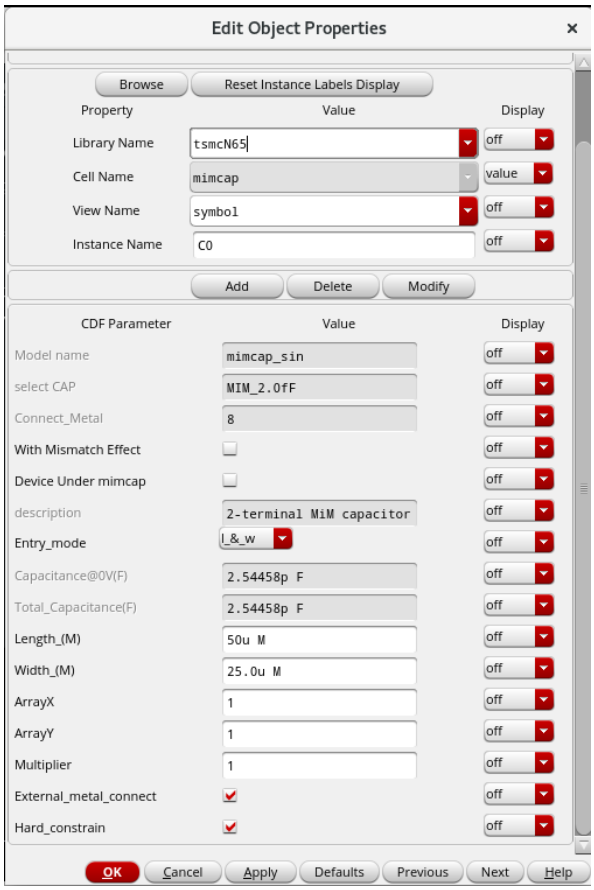

Figure 7.3: 2.5p F Load Capacitor specifications

- Another thing that should be noted is that we make the layout for the symbol. So voltage/current sources will NOT be included in layout.

7.2 Centroids

- In the layout, **3 common centroids** have been formed. For bigger circuits, it is sometimes better to use Inter Digitization, but generally, we use common centroid for making our layout as it provides us with same environment on both sides of the centroid.

7.2.1 Common Centroid 1: MP_AL and MP_CS

- A common centroid has been formed for all the PMOSes of the circuit. The layout for the common centroid is as follows:

(L denotes transistor on left side and R denotes transistor on right side, e.g. MP_AL_R will denote the MP_AL transistor on right side in the schematic**)**

Dummy PMOS: MP_CS_1: MP_CS_2: MP_CS_3: MP_CS_4: MP_CS_5: MP_CS_6: MP_CS_7: MP_CS_8: MP_CS_9: MP_CS_10 **:**

MP_AL_R1: MP_AL_L1: MP_AL_L2: MP_AL_R2:

MP_CS_11: MP_CS_12: MP_CS_13: MP_CS_14: MP_CS_15: MP_CS_16: MP_CS_17: MP_CS_18: MP_CS_19: MP_CS_20: Dummy PMOS

- We add the VDD, which also acts as the body for all the PMOS transistors on top of centroid 1. All of the connections of the dummy PMOSes are to the VDD body as well.

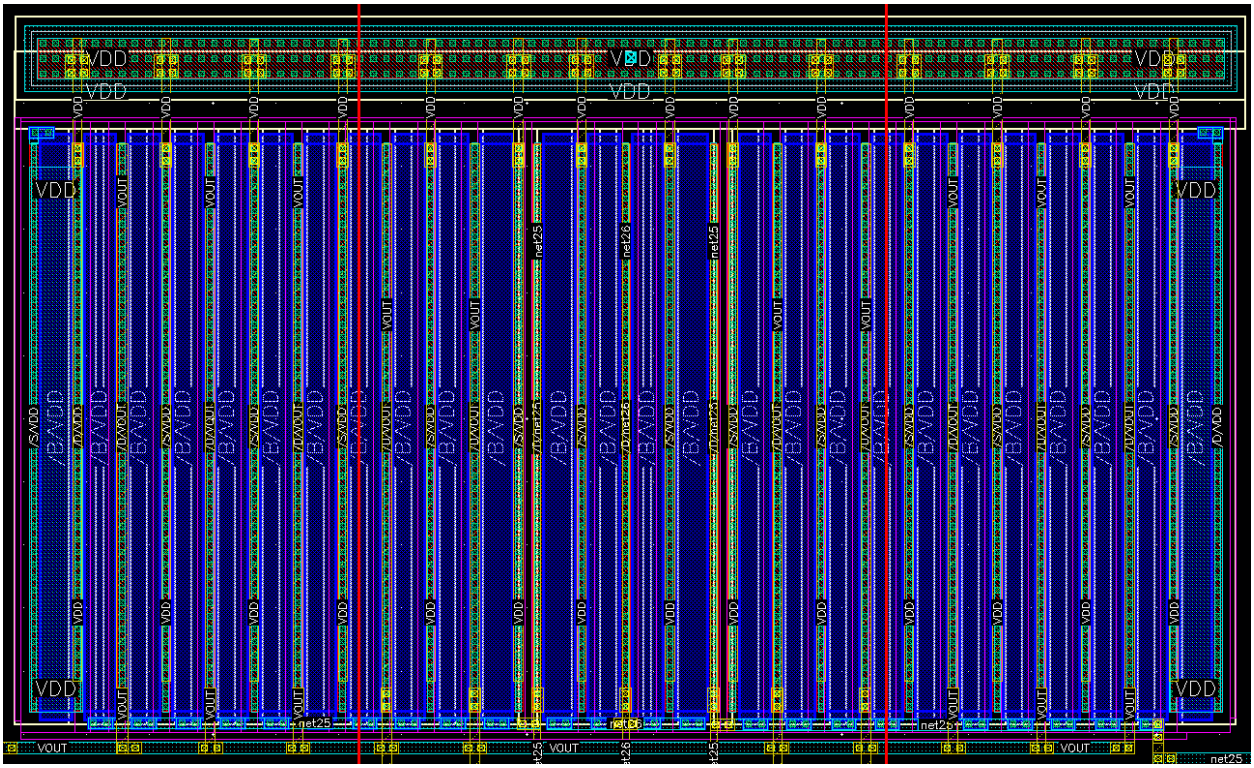

Figure 7.4: Centroid 1: Of MP_AL and MP_CS

7.2.2 Common Centroid 2: MN_DA

- The layout for the MN_DA is as follows:

  Dummy NMOSes: MN_DA_R1:MN_DA_L1:MN_DA_L2:MN_DA_R2: Dummy NMOSes

- Extra dummies are added here to maintain a rectangular symmetry.

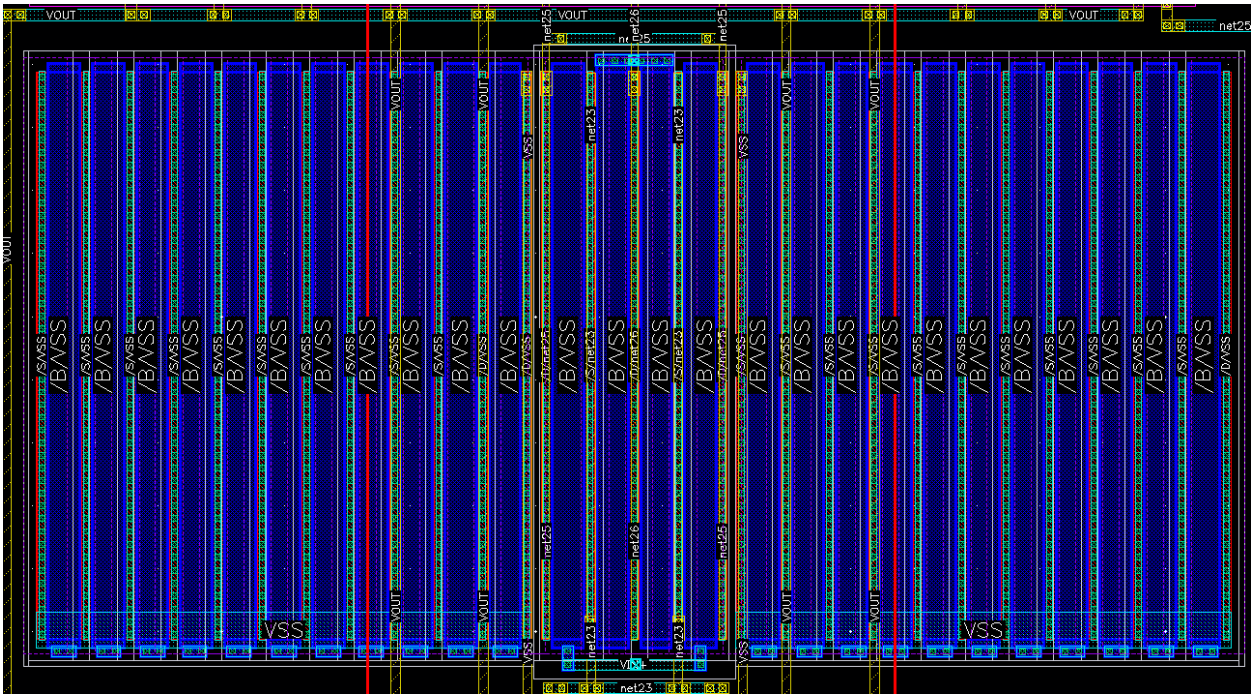

Figure 7.5: Centroid 2: Of MN_DA

7.2.3 Common Centroid 3: MN_CM1, MN_CM2, MN_CM3

- The layout for the 3rd centroid is as follows:

  Dummy NMOSes: MN_CM3_1: MN_CM3_2: MN_CM3_3: MN_CM3_4:

  MN_CM2_1:MN_CM1_1:MN_CM1_2:MN_CM2_2:

  MN_CM3_5: MN_CM3_6: MN_CM3_7: MN_CM3_8: Dummy NMOSes

- Extra dummies are added here as well to provide same environment and maintain symmetry.
- We add VSS at the bottom of centroid 3. VSS acts as the body of all the NMOSes, all the terminals of the NMOS dummies are also connected at the VSS body.

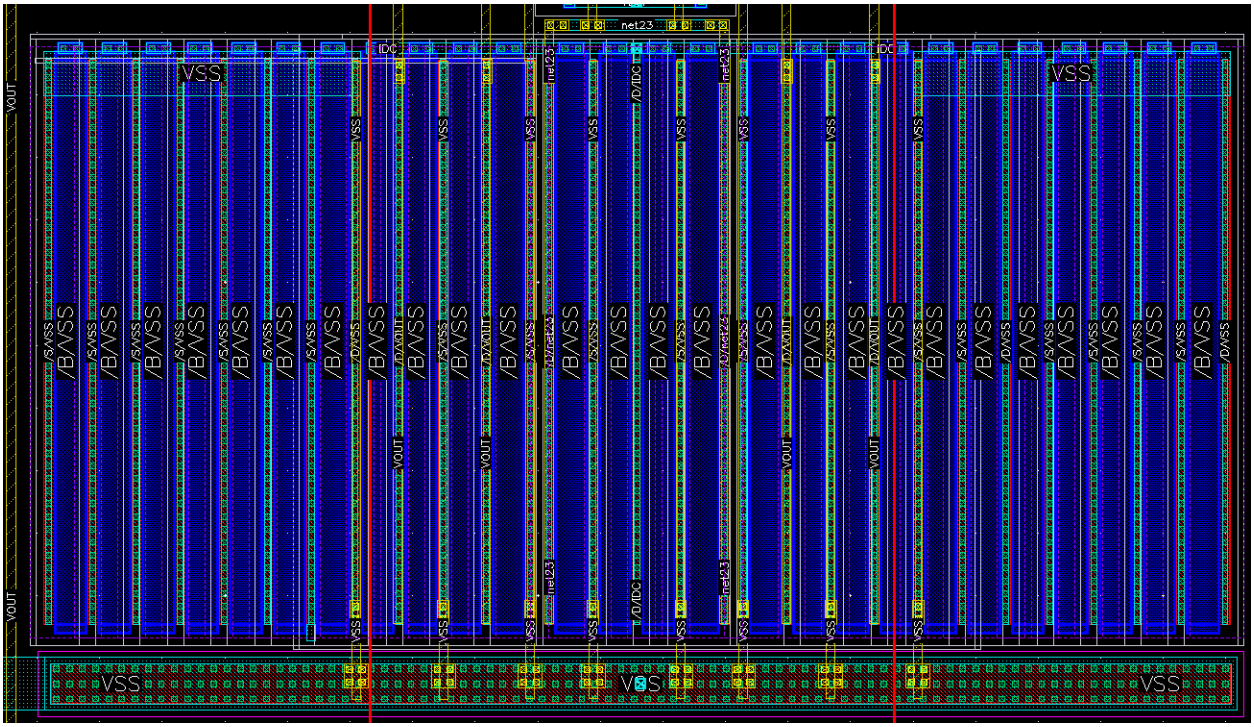

Figure 7.6: Centroid 3: Of MN_CM1, MN_CM2 and MN_CM3

7.3 Overall Layout

- The two capacitors (2.5p F and 8p F) capacitors are added on either side of the transistors. For capacitors you can form the connection anywhere, not necessarily at the two end points.
- The resistor is added at the bottom.
- Make sure to cover the entire circuit with the purple rectangle at the end.

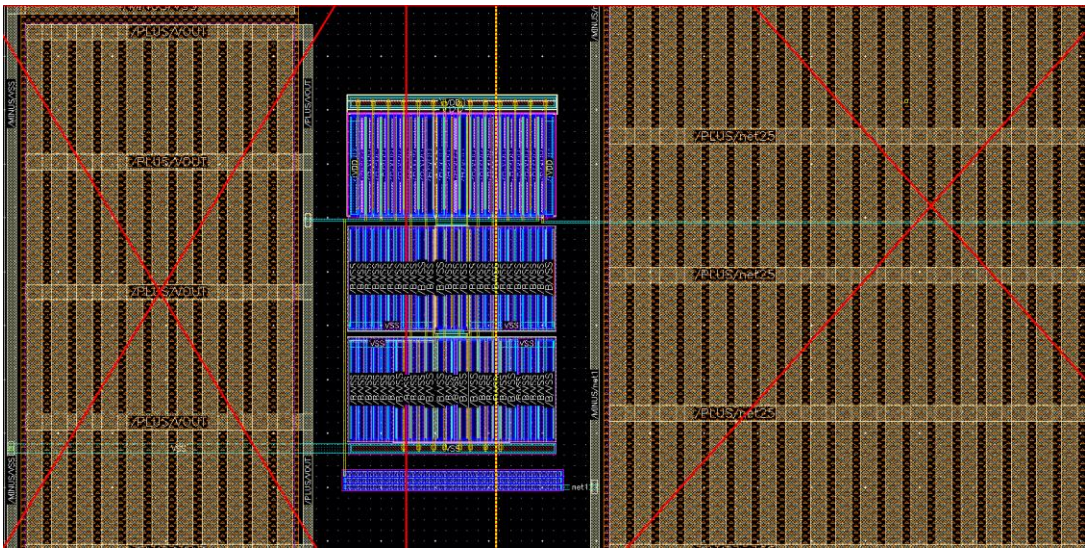

Figure 7.7: Resistor at the bottom and the two capacitors on each side

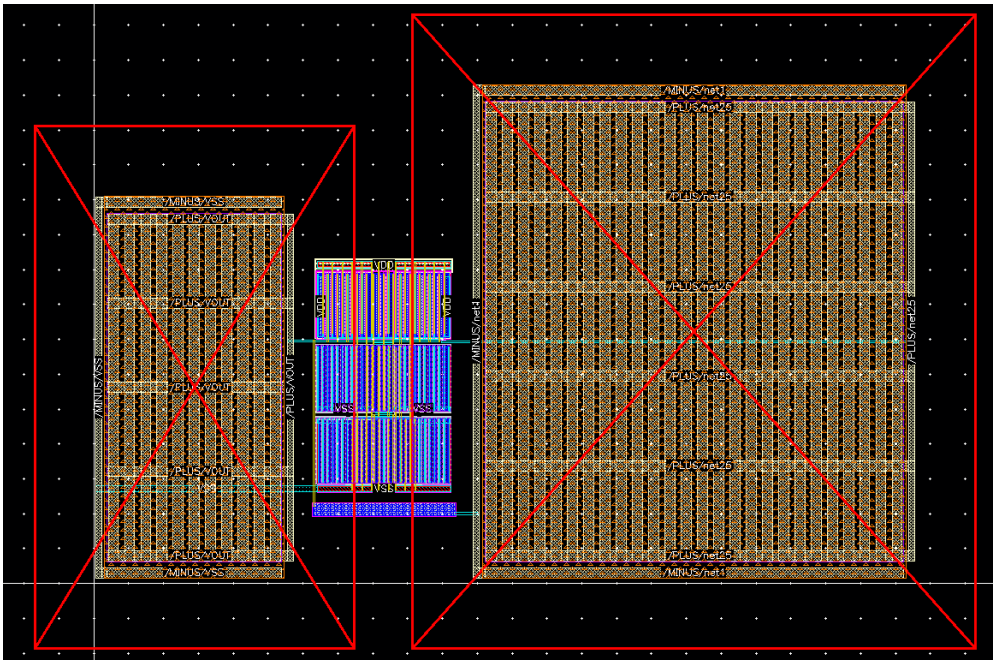

Figure 7.8: Overall Layout

7.4 Checks

- The **DRC checks** were all cleared at the end apart from the density errors (denoted by DN).

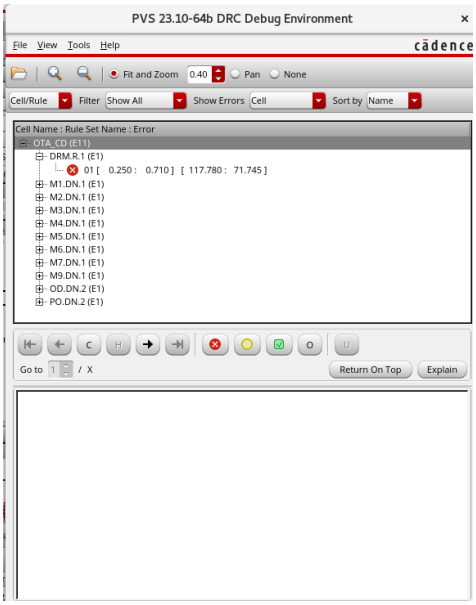

Figure 7.9: DRC Check

- After adding the pins in their proper places, the **LVS check** was cleared as well. Keep in mind that the names of the pins must have the same metal pin as that of the pin itself.

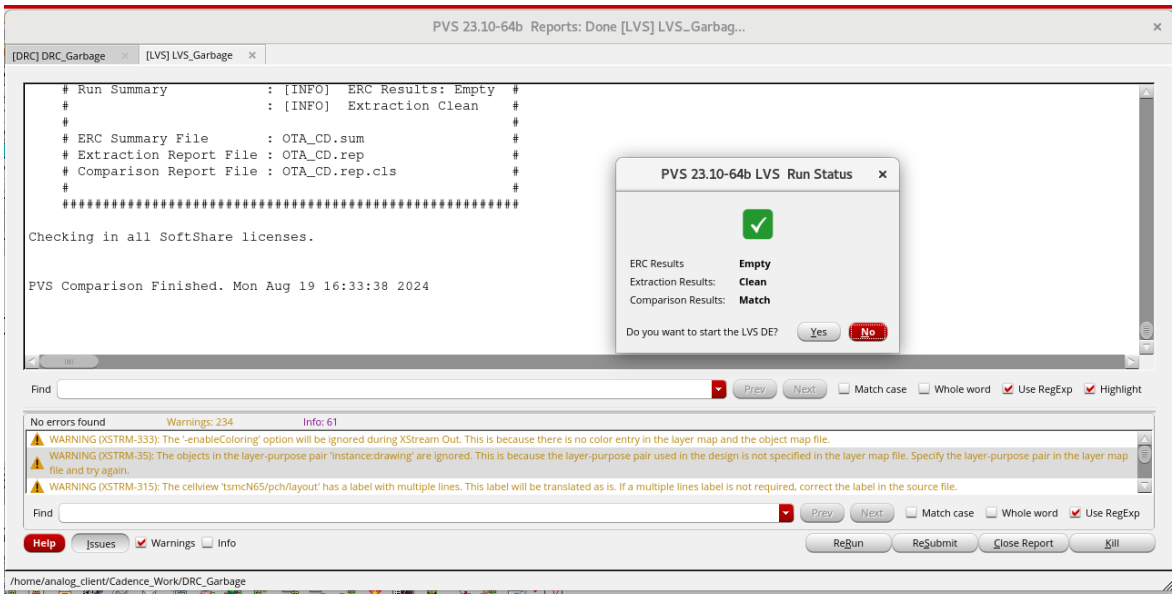

Figure 7.10: LVS Check

- Then we run the LVS_QRC check, which was also successful.

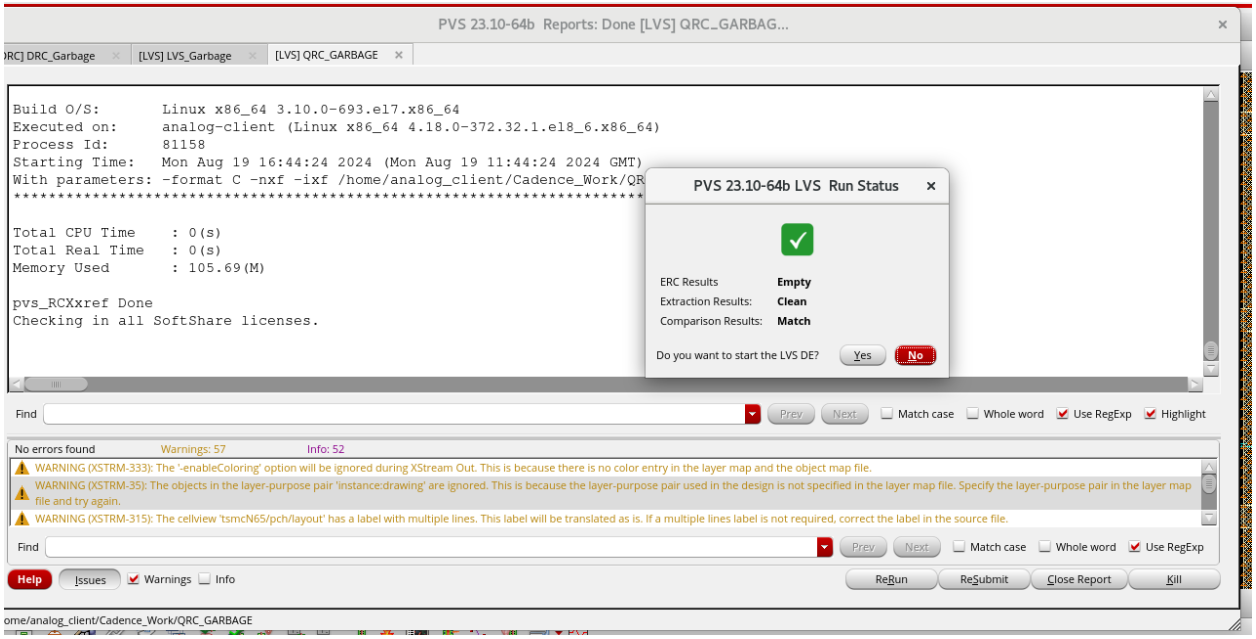

Figure 7.11: LVS_QRC Check

- After this we **setup Quantus**, then run **PVS Quantus** and generate the **.sp** file.
- A new library is created in which a new spice format cell view is made.
- The last two lines are replaced with the contents of the .sp file created previously, and then the symbol for the post-layout OTA is made.

7.5 Post Layout Simulation

- We make the schematic for the feedback, slew rate and differential mode with the post-layout symbol for the post-layout simulation. We set the source values same as before.
- Keep in mind to set the **environment** in Maestro window, by adding spiceText with a space at the end.

7.5.1 Feedback

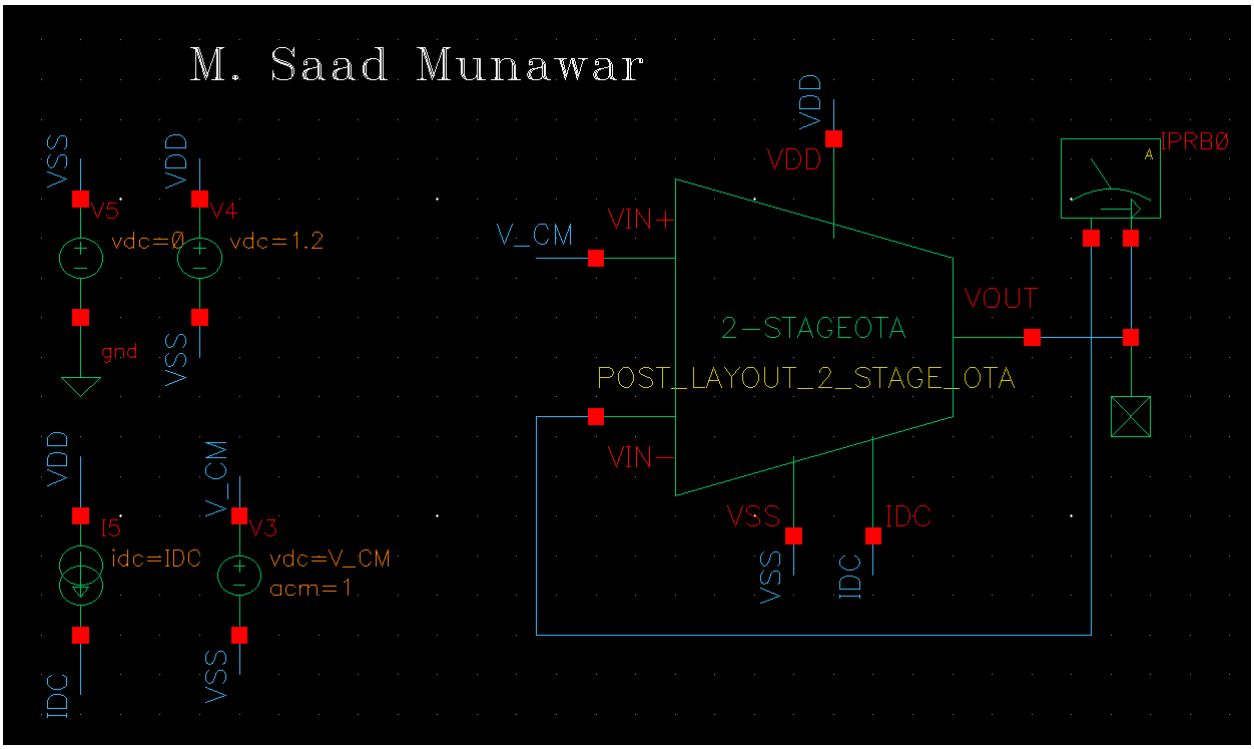

Figure 7.12: Feedback Schematic

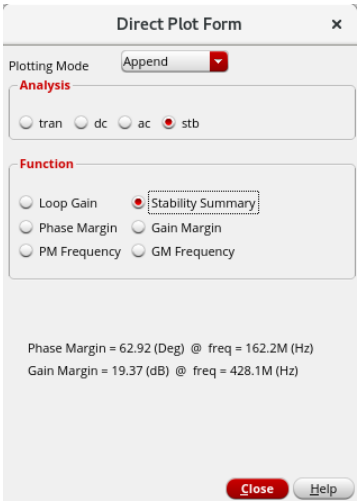

Figure 7.13: Phase Margin = 62.92; Unity Gain Bandwidth = 162.2M Hz

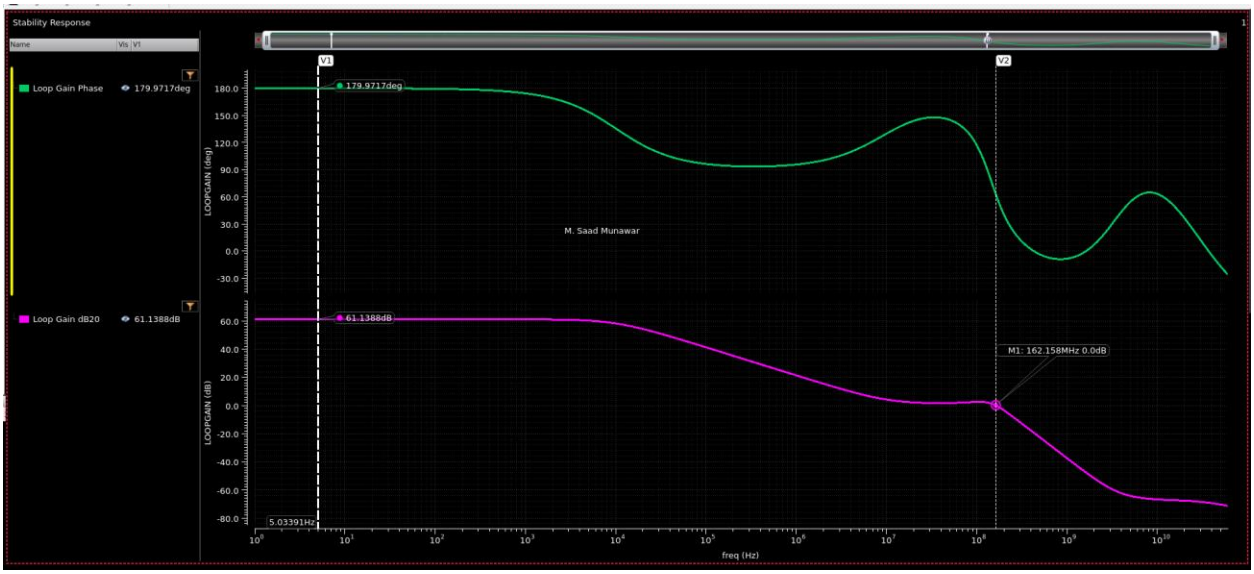

Figure 7.14: Gain = 61.14 dB

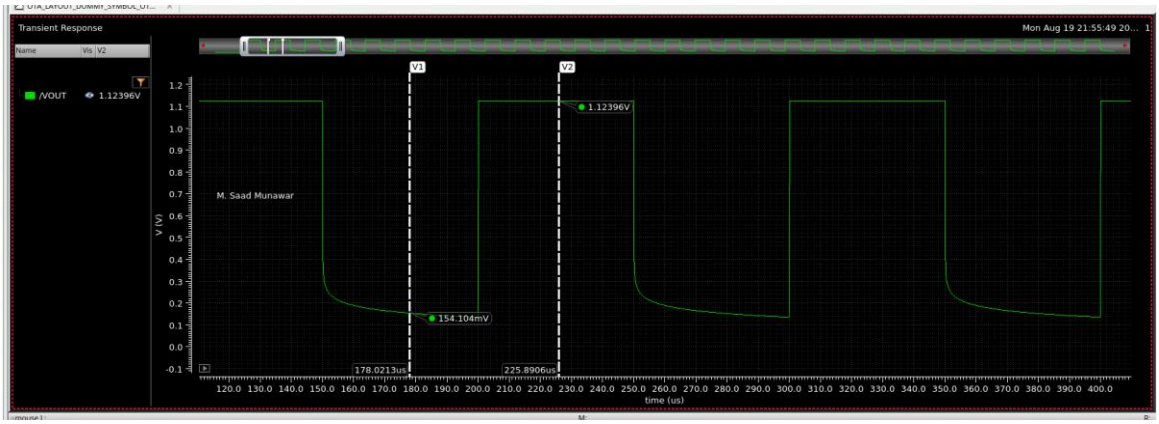

Figure 7.15: VOUT plot in feedback

	Expression	Value
1	slewRate(VT("/...	10.31E6

Figure 7.16: Slew Rate = 10.31 V/u sec

7.5.2 Differential Mode

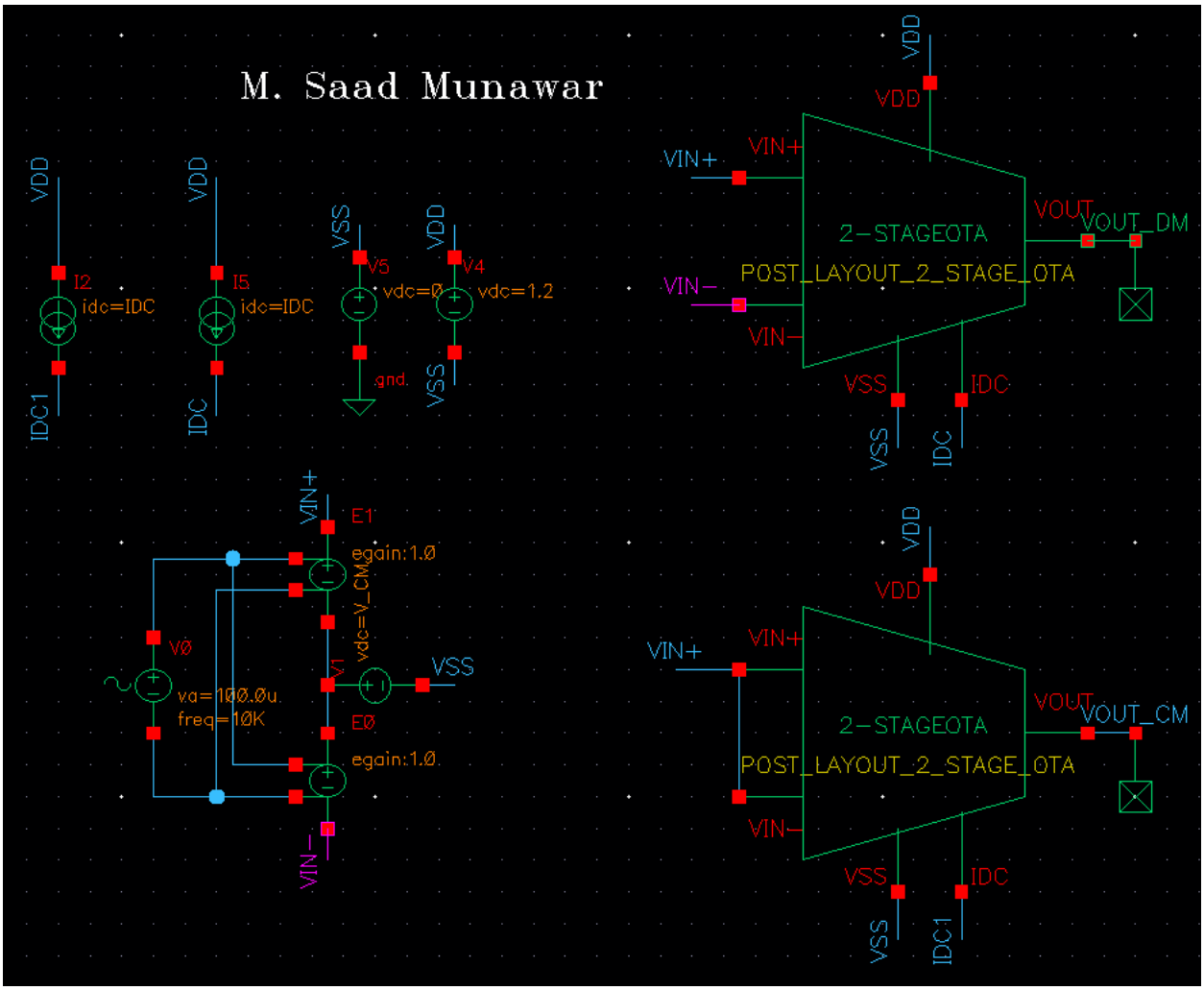

Figure 7.17: Differential Mode Schematic

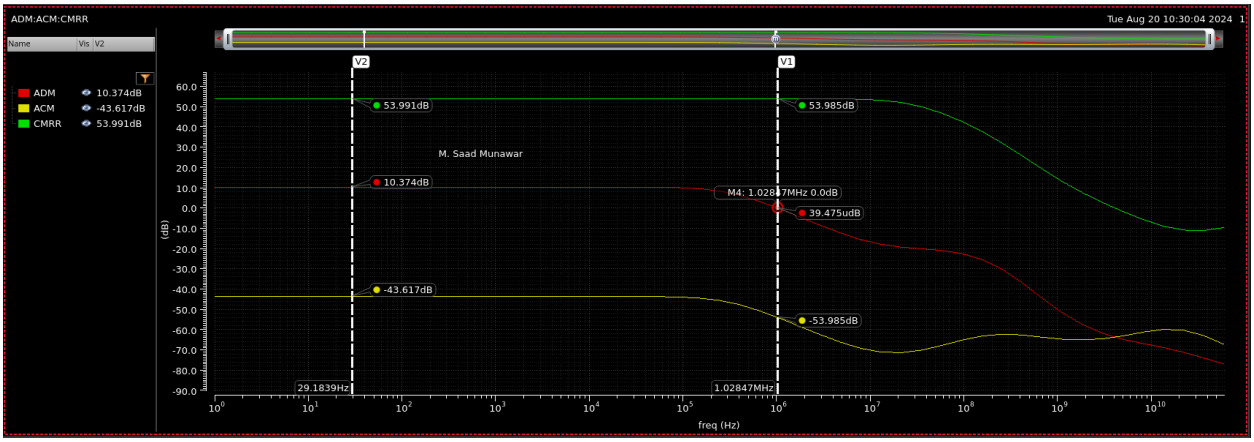

Figure 7.18: ADM = 10.37 dB; CMRR = 54 dB; Bandwidth = 1M Hz

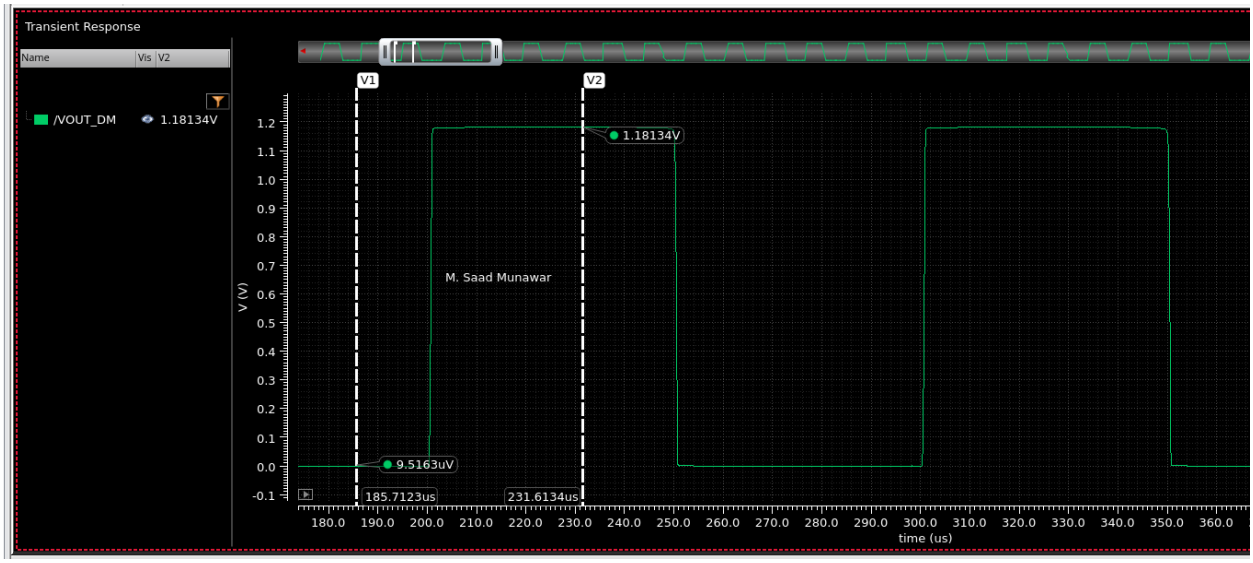

Figure 7.19: Maximum Output Swing = 1.18 V

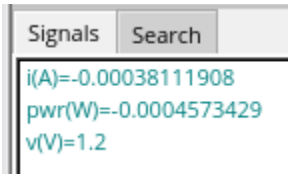

Figure 7.20: Power Consumption

7.6 Layout Summary

PARAMETERS	VALUES
Feed Back Gain	61.24 -> 61.14 dB
Bandwidth Feedback	178.6M -> 162.2M Hz
Phase Margin	67.76 -> 62.92
Differential Gain	**66.65 -> 10.37 dB**
Bandwidth Differential Mode	**259.4M -> 1M Hz**
Slew Rate	11.08 -> 10.31 V/u sec
CMRR	54 dB
Output Swing	1.18 V
Bias Current	100u A
Power Consumption	0.46m Watt

- In the post layout simulation, we see a drastic decrease in the gain and bandwidth in the differential mode. This may be due to not implementing layout techniques effectively enough.
- Our feedback gain and bandwidth, decreases only a bit, and still manages to fulfill our requirements.

8. Result Comparison

PARAMETERS	No Capacitor and Resistance	C_C = 8p F	C_C = 8p F and Rz = 2k ohms	Post Layout
Feed Back Gain	61.24 dB	61.24 dB	61.24 dB	61.14 dB
Differential Gain	66.65 dB	66.65 dB	66.65 dB	**10.37 dB**
Phase Margin	**-3.65**	78.6	67.76	62.92
Bandwidth	179M Hz	**12.07M Hz**	178.6M Hz	162.2M Hz
Slew Rate	420.5 V/u sec	11.67 V/u sec	11.08 V/u sec	10.31 V/u sec
ICMR	0.6499 V – 1.1518 V	0.6499 V – 1.1518 V	0.6499 V – 1.1518 V	**1M Hz DM UG Bandwidth**
CMRR	56.2 dB	56.2 dB	56.2 dB	54 dB
Output Swing	1.08 V	1.08 V	1.08 V	1.18 V
Bias Current	100u A	100u A	100u A	100u A
Power Consumption	0.6m Watt	0.6m Watt	0.6m Watt	0.46m Watt