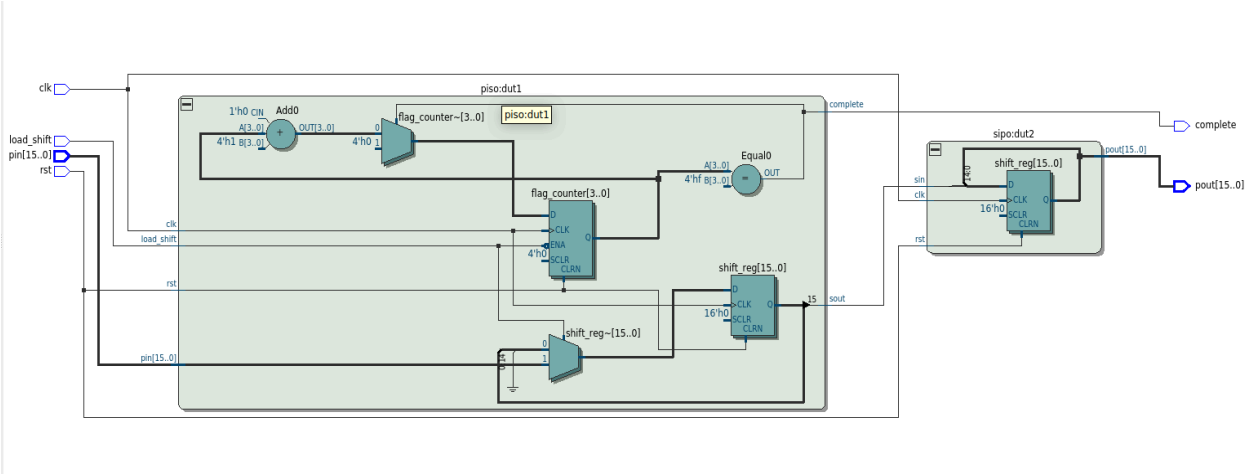
“2. Chaining of Shift Registers”

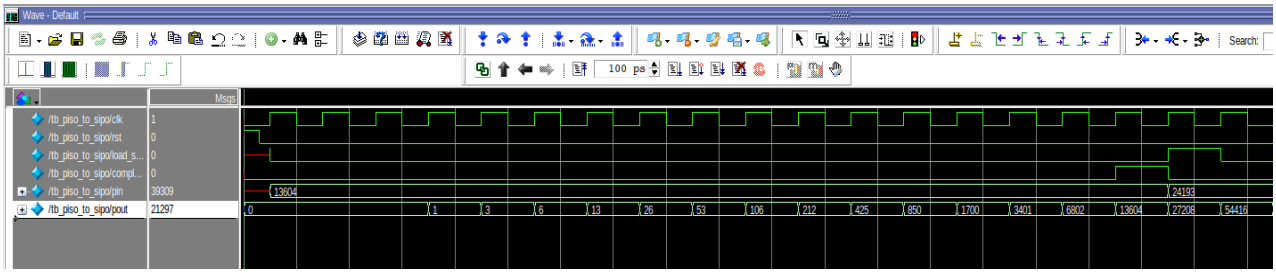
1. Testbench -> PISO -> SIPO -> Testbench Configuration:

Design:



- The piso module loads 16 bit parallel data and shifts it out serially one bit per clock.
- The sipo module collects incoming serial bits and reconstructs them into a 16 bit parallel output.
- A counter in piso tracks the shifting process and signals completion after all bits are sent.
- The combined piso_to_sipo module connects piso output to sipo input, enabling end to end transfer.
- Reset inputs clear registers in both modules, ensuring proper initialization before data transmission begins.

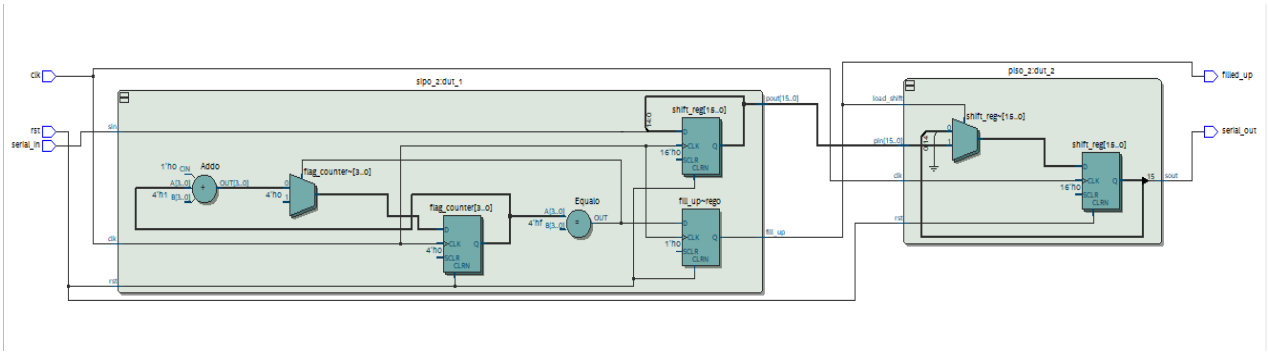
Verification:



- The testbench instantiates the combined piso_to_sipo module and connects all required signals.
- A clock generator with 10 ns period and reset initialization ensures proper timing.
- Random 16 bit words are loaded into piso when complete is asserted, driving serial transfer into sipo.
- The simulation runs for 1000 ns, repeatedly checking word transfers on each clock edge until stop is called.

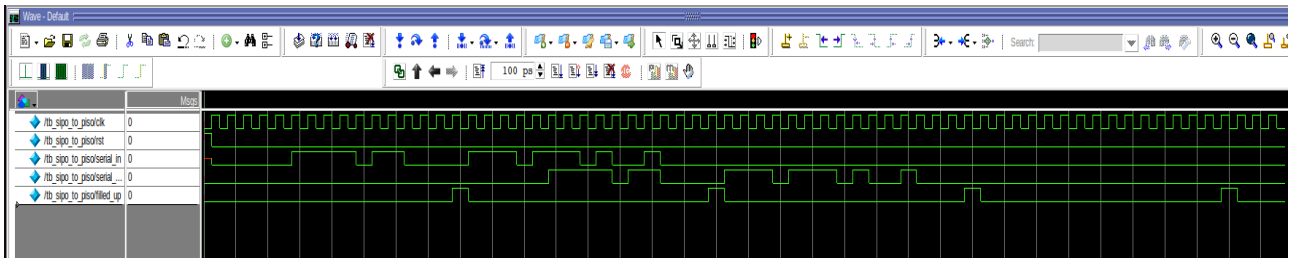
2. Testbench -> SIPO -> PISO -> Testbench Configuration:

Design:



- The piso_2 module loads 16 bit parallel data and shifts it out serially one bit per clock.
- The sipo_2 module receives serial input, reconstructs it into 16 bit parallel output, and signals when full.
- A counter in sipo_2 tracks received bits and asserts fill_up after 16 bits are collected.
- The sipo_to_piso module connects sipo_2 output to piso_2 input, enabling serial to parallel to serial transfer.
- Reset inputs clear registers and counters, ensuring proper initialization before data transmission and reception.

Verification:



- The testbench instantiates the sipo_to_piso module and connects clock, reset, serial input, and outputs.
- A clock generator with 10 ns period and reset initialization ensures proper timing.
- Random serial bits are applied to the input for 32 cycles to test data transfer through both modules.
- The simulation runs for 350 ns before stopping, allowing observation of serial in to out behavior and fill signal.