NE-3102: Electronics-II Laboratory

Roll _____ Date _____ Experiment No. _____

Name of the experiment

Design an Ex-OR gate using NAND gates.

Contents

1 Objective

1. To design an Ex-OR using only NAND gates.

2 Theory

The full form of Ex-OR gate is Exclusive-OR gate. Its function is the same as that of OR gate except for the case when the inputs have an even number of ones. The logic circuit of Ex-OR gate is given in Figure 1 (a). The accompanying truth table shows that $x = 1$ for two cases: $A = 0, B = 1$ (the $\bar{A}B$ term) and $A = 1, B = 0$ (the $A\bar{B}$ term).

This particular combination of logic gates occurs quite often and is very useful in certain applications. In fact, the XOR circuit has been given a symbol of its own, shown in Figure 1 (b). This symbol is assumed to contain all of the logic contained in the XOR circuit and therefore has the same logic expression and truth table. This XOR circuit is commonly referred to as an XOR gate, and we consider it as another type of logic gate. The IEEE/ANSI symbol for an XOR gate is shown in Figure Figure 1 (c). The dependency notation (= 1) inside the block indicates that the output will be active-HIGH only when a single input is HIGH.

An XOR gate has only two inputs; there are no three-input or four-input XOR gates. The two inputs are combined so that $x = \bar{A}B + A\bar{B}$. A shorthand way that is sometimes used to indicate the XOR output expression is

$$x = \mathrm{A} \oplus B$$

where the symbol $\oplus$ represents the XOR gate operation. The characteristics of an XOR gate are summarized as follows:

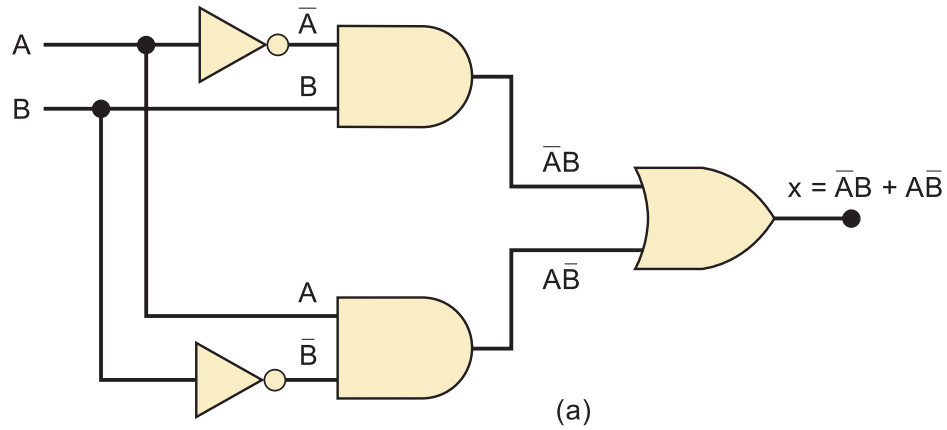
1. It has only two inputs and its output is

$$x = \bar{A}B + A\bar{B} = A \oplus B$$

2. Its output is HIGH only when the two inputs are at different levels.

3 Components and apparatus

1. 74LS00 TTL integrated circuit (quad NAND)
2. Passive components
3. Breadboard and connecting wires
4. Bench power supply



A	B	x
0	0	0
0	1	1
1	0	1
1	1	0

XOR gate symbols

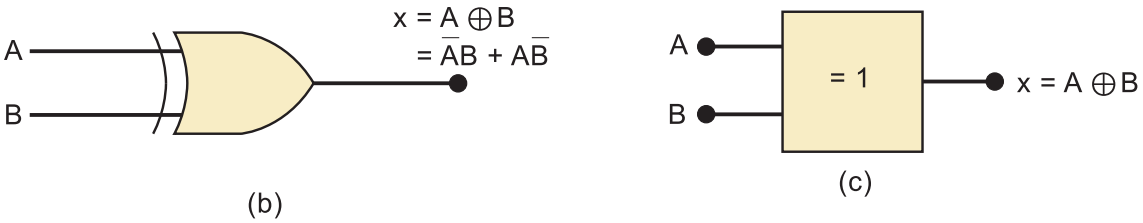


Figure 1: (a) Exclusive-OR circuit and truth table; (b) traditional XOR gate symbol; (c) IEEE/ANSI symbol or XOR gate.

4 Data collection and analysis

Input		Output	
A	B	$Y = A \oplus B$	Voltage, $V_0(v)$
0	0	0	0
0	1	1	4.90
1	0	1	4.91
1	1	0	0

Table 1: Truth table for OR gate.

5 Result

6 Discussion

7 References

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

Appendix