

# NE-3102: Electronics-II Laboratory

Roll Date Experiment No.	
--------------------------	--

#### Name of the experiment

Circuit realization of logic expression using logic gates.

#### Contents

1	Objective	2
2	Theory	2
3	Components and apparatus	2
4	Determination of the logic expression using K map	3
5	Circuit diagram/setup	4
6	Data collection and analysis	5
7	Result	6
8	Discussion	7
9	References	8

#### 1 Objective

- 1. Usage of K map to simplify/synthesize logic expressions.
- 2. To implement and verify a logic circuit that performs a predefined task (given as a truth table).

#### 2 Theory

The Karnaugh map (K map) is a graphical tool used to simplify a logic equation or to convert a truth table to its corresponding logic circuit in a simple, orderly process. Although a K map can be used for problems involving any number of input variables, its practical use is limited to five or six variables.

Like a truth table, a k-map contains all the possible values of input variables and their corresponding output values. However, in k-map, the values are stored in cells of the array. In each cell, a binary value of each input variable is stored.

The procedure will first be outlined and then applied to several examples. The steps below are followed in using the K-map method for simplifying a Boolean expression:

- 1. Construct the K map and place 1s in those squares corresponding to the 1s in the truth table. Place 0s in the other squares.
- 2. Examine the map for adjacent 1s and loop those 1s that are not adjacent to any other 1s.

  These are called isolated 1s.
- 3. Next, look for those 1s that are adjacent to only one other 1. Loop any pair containing such a 1.
- 4. Loop any octet, even if it contains some 1s that have already been looped.
- 5. Loop any pairs necessary to include any 1s that have not yet been looped, making sure to use the minimum number of loops.
- 6. Loop any quad that contains one or more 1s that have not already been looped, making sure to use the minimum number of loops.
- 7. Form the OR sum of all the terms generated by each loop.

These steps will be followed exactly and referred to in the analysis of the logic expression. In each case, the resulting logic expression will be in its simplest SOP form.

### 3 Components and apparatus

- 1. TTL logic ICs
- 2. Passive components
- 3. Breadboard and connecting wires
- 4. Bench power supply

### 4 Determination of the logic expression using K map

A	B	C	D	x
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Table 1: Truth table.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	0	0
$\bar{A}B$	0	1	0	0
AB	0	1	1	0
$A\bar{B}$	0	0	0	0

Table 2: K map.

Looping the K map, the output logic expression is found to be,

$$x = \bar{A}\bar{C}D + ABD$$

$$= D(\bar{A}\bar{C} + AB)$$

$$= D[(\bar{A} + \bar{C}) + AB]$$
(1)

## $5 \quad {\rm Circuit~diagram/setup}$

## 6 Data collection and analysis

### 7 Result

### 8 Discussion

## 9 References

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

## Appendix