

# NE-3102: Electronics-II Laboratory

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### Name of the experiment

To study and verify NAND as a Universal Gate.

### Contents

1	Objective	2
2	Theory	2
	2.1 Implementing an inverter using NAND gate	. 2
	2.2 Implementing AND using NAND gate	. 3
	2.3 Implementing OR using NAND gate	. 3
	2.4 Note on integrated packages	. 3
3	Components and apparatus	3
4	Circuit diagram/setup	4
5	Data collection and analysis	5
6	Result	6
7	Discussion	7
8	References	8

### 1 Objective

- 1. To study the universality of the NAND gate by implementing basic gates using only NAND gate.
- 2. To verify the mentioned implementation by checking the truth table.

### 2 Theory

The NAND gate represents the complement of the AND operation. Its name is an abbreviation of NOT AND.

The graphic symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on the output of the AND gate. All Boolean expressions consist of various combinations of the basic operations of OR, AND, and INVERT. Therefore, any expression can be implemented using combinations of OR gates, AND gates, and INVERTERs. It is possible, however, to implement any logic expression using only NAND gates and no other type of gate. This is because NAND gates, in the proper combination, can be used to perform each of the Boolean operations OR, AND, and NOT. Since any of the Boolean operations can be implemented using only NAND gates, any logic circuit can be constructed using only NAND gates. To prove that any Boolean function can be implemented using only NAND gates, we will show that the AND, OR and NOT operations can be performed using only these gates.

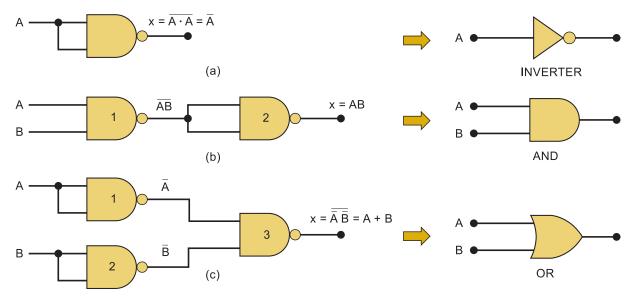


Figure 1: NAND gates can be used to implement any Boolean function.

#### 2.1 Implementing an inverter using NAND gate

The figure shows the way in which a NAND gate can be used as an inverter, as shown in Figure 1 (a). We have a two-input NAND gate whose inputs are purposely connected together so that the variable A is applied to both. In this configuration, the NAND simply acts as INVERTER because its output is  $x = \overline{A \cdot A} = \overline{A}$ .

#### 2.2 Implementing AND using NAND gate

An AND gate can be replaced by NAND gates, as shown in Figure 1 (b). We have two NAND gates connected so that the AND operation is performed. NAND gate 2 is used as an INVERTER to change  $\overline{AB}$  to  $\overline{\overline{AB}} = AB$ , which is the desired AND function.

#### 2.3 Implementing OR using NAND gate

The OR operation can be implemented using NAND gates connected, as shown in Figure 1 (c). Here NAND gates 1 and 2 are used as INVERTERs to invert the inputs, so that the final output is  $x = \overline{A} \cdot \overline{B}$ , which can be simplified to x = A + B using DeMorgan's theorem.

#### 2.4 Note on integrated packages

Basic logic gates can be constructed from diodes, transistors, and resistors. However, more practically, these basic logic gates are implemented as small-scale integrated circuits (SSICs) or as part of the more complex medium-scale (MSI) or very large-scale (VLSI) integrated circuits. Digital IC gates are classified not only by their logic operation but also by the specific logic circuit family to which they belong. Each logic family has its own basic electronic circuit upon which more complex digital circuits and functions are developed. The following logic families are the most frequently used.

- TTL Transistor-transistor logic
- ECL Emitter-coupled logic
- MOS Metal-oxide semiconductor
- CMOS Complementary metal-oxide semiconductor

TTL and ECL are based on bipolar transistors. TTL has popularity among logic families. ECL is used only in systems requiring a high-speed operation. MOS and CMOS are based on field effect transistors. They are widely used in large-scale integrated circuits because of their high component density and relatively low power consumption. CMOS logic consumes far less power than MOS logic. There are various commercial integrated circuit chips available. TTL ICs are usually distinguished by numerical designation as the 5400 and 7400 series.

### 3 Components and apparatus

- 1. 74LS00 TTL integrated circuit (quad NAND)
- 2. Passive components
- 3. Breadboard and connecting wires
- 4. Bench power supply

## ${\it 4~Circuit~diagram/setup}$

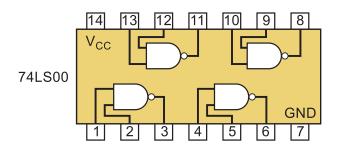


Figure 2: 74LS00 IC.

## 5 Data collection and analysis

Inp	Input		Output	
A	В	X	Voltage, $V_0(v)$	
0	0	0	0.57	
0	1	1	4.34	
1	0	1	4.34	
1	1	1	4.39	

Table 1: Truth table for OR gate.

Input		Output	
A	В	X	Voltage, $V_o(v)$
0	0	0	0.70
0	1	0	0.78
1	0	0	0.79
1	1	1	4.97

Table 2: Truth table for AND gate.

Input	Output	
A	X	Voltage, $V_o(v)$
0	1	4.56
1	0	0.42

Table 3: Truth table for NOT gate.

## 6 Result

## 7 Discussion

## 8 References

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

## Appendix