NE-3102: Electronics-II Laboratory

Roll ____________ Date ____________ Experiment No. ____________

Name of the experiment

Truth Table verification of S-R, T, D, J-K flip-flop.

Contents

1 Objective 2

2 Theory 2

2.1 S-R latch 2

2.2 S-R flip-flop 2

2.3 Conversion of S-R flip-flop to T flip-flop 2

2.4 Conversion of S-R flip-flop to D flip-flop 3

2.5 Conversion of S-R flip-flop to J-K flip-flop 4

2.6 Timing generator/clock 4

3 Components and apparatus 6

4 Circuit diagram/setup 7

5 Data collection and analysis 8

6 Result 9

7 Discussion 10

8 References 11

1 Objective

1. To implement a S-R latch using NAND/NOR[1] gates.
2. To design a generic astable multivibrator with 0.2 Hz and 50% duly cycle square wave output as timing generator/clock
3. To implement a S-R flip-flop based on the S-R NAND/NOR latch
4. To convert the S-R flip-flow to a T flip-flop
5. To convert the S-R flip-flow to a D flip-flop
6. To verify the associated truth tables

2 Theory

A latch or a flip-flop is an electric circuit with two stable states that can store binary data. This stored data can be changed by applying one or more inputs. Latches and flip-flops are fundamental building blocks of logic circuits that incorporate memory cells; their output depends on the present value of the input and also on the previous values. These circuits, also called sequential logic circuits, often require a timing generator (a clock) for their operation. Usually there are two outputs, Q and its complementary value $\bar{Q}$.

2.1 S-R latch

(description)

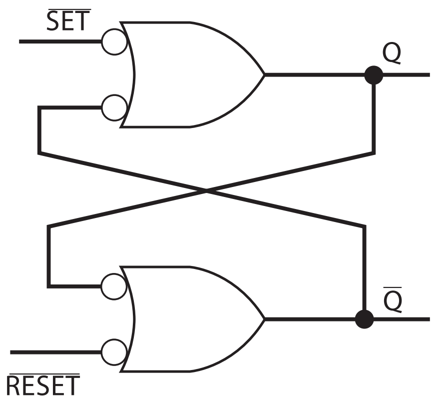

Figure 1: S-R latch.

2.2 S-R flip-flop

(description)

2.3 Conversion of S-R flip-flop to T flip-flop

(description)

[1]Either use NAND or NOR gates; this will affect your input/output active sates, e.g., a NAND S-R latch will have active LOW inputs, so you have to pull your inputs HIGH with pull-up resitors for the resting state

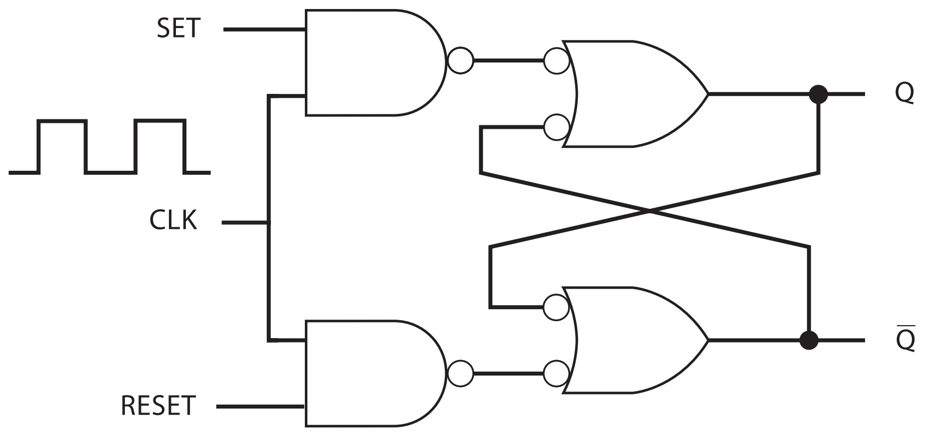

Figure 2: S-R flip-flop.

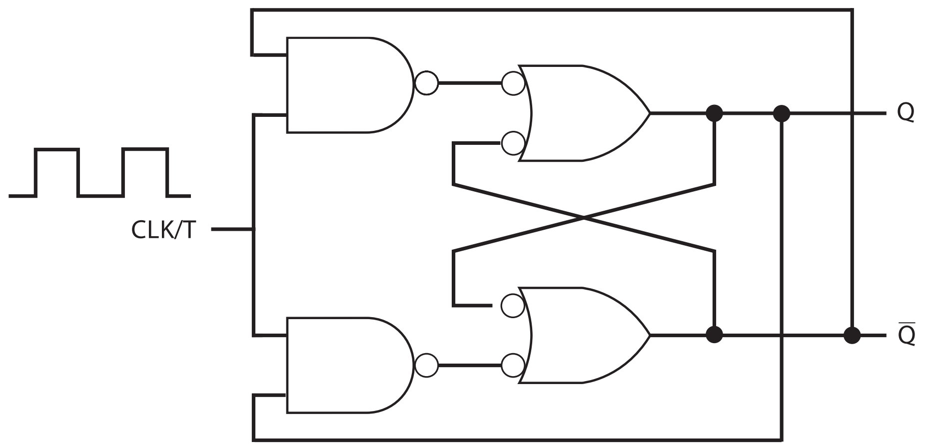

Figure 3: T flip-flop.

2.4 Conversion of S-R flip-flop to D flip-flop

(description)

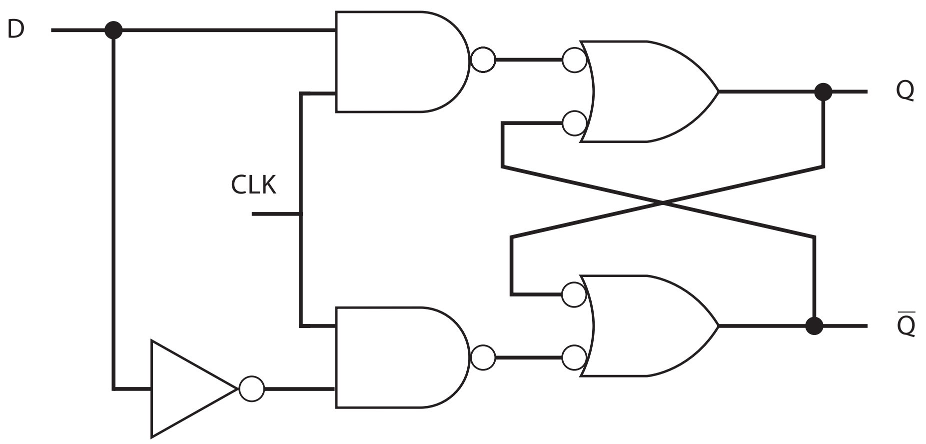

Figure 4: D flip-flop.

2.5 Conversion of S-R flip-flop to J-K flip-flop

(description)

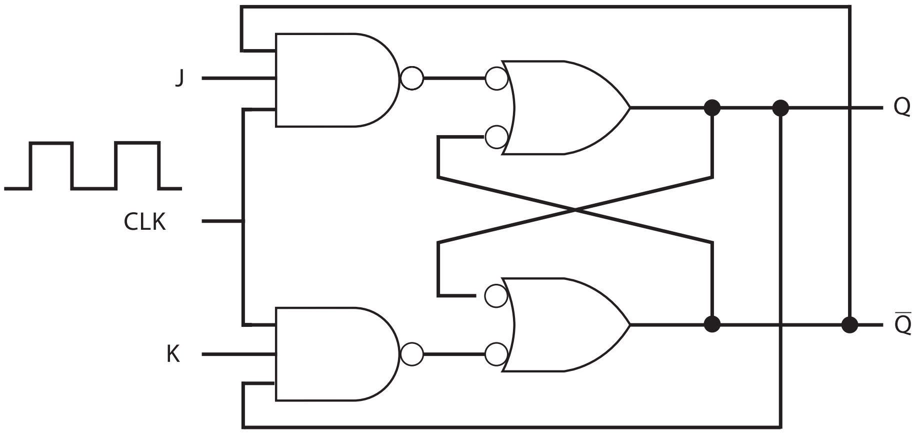

Figure 5: D flip-flop.

2.6 Timing generator/clock

555 timer is made up of two voltage comparators and an S-R latch as shown in Figure 6. The voltage comparators are devices that produce a HIGH out whenever the voltage on the + input is greater than the voltage on the - input. The external capacitor (C) charges up until its voltage exceeds $2/3 \times V_{CC}$ as determined by the upper voltage comparator monitoring V_{T+}. When this comparator output goes HIGH, it resets the SR latch, causing the output pin (3) to go LOW. At the same time, $\bar{Q}$ goes HIGH, closing the discharge switch and causing the capacitor to begin to discharge through R_B. It will continue to discharge until the capacitor voltage drops below $\frac{1}{3} \times V_{CC}$ as determined by the lower-voltage comparator monitoring V_{T-}. When this comparator output goes HIGH, it sets the SR latch, causing the output pin to go HIGH, opening the discharge switch, and allowing the capacitor to start charging again as the cycle repeats.

The formulas for these time intervals, t_{L} and t_{H}, and the overall period of the oscillations, T, are given in the figure. The frequency of the oscillations is, of course, the reciprocal of T. As the formulas in the diagram indicate, the t_{L} and t_{H} intervals cannot be equal unless R_A is made zero. This cannot be done without producing excess current through the device. This means that it is impossible to produce a perfect 50 percent duty-cycle square wave output with this circuit. It is possible, however, to get very close to a 50 percent duty cycle by making $R_B \gg R_A$ (while keeping R_A greater than 1kΩ), so that $t_{\mathrm{L}} \approx t_{\mathrm{H}}$.

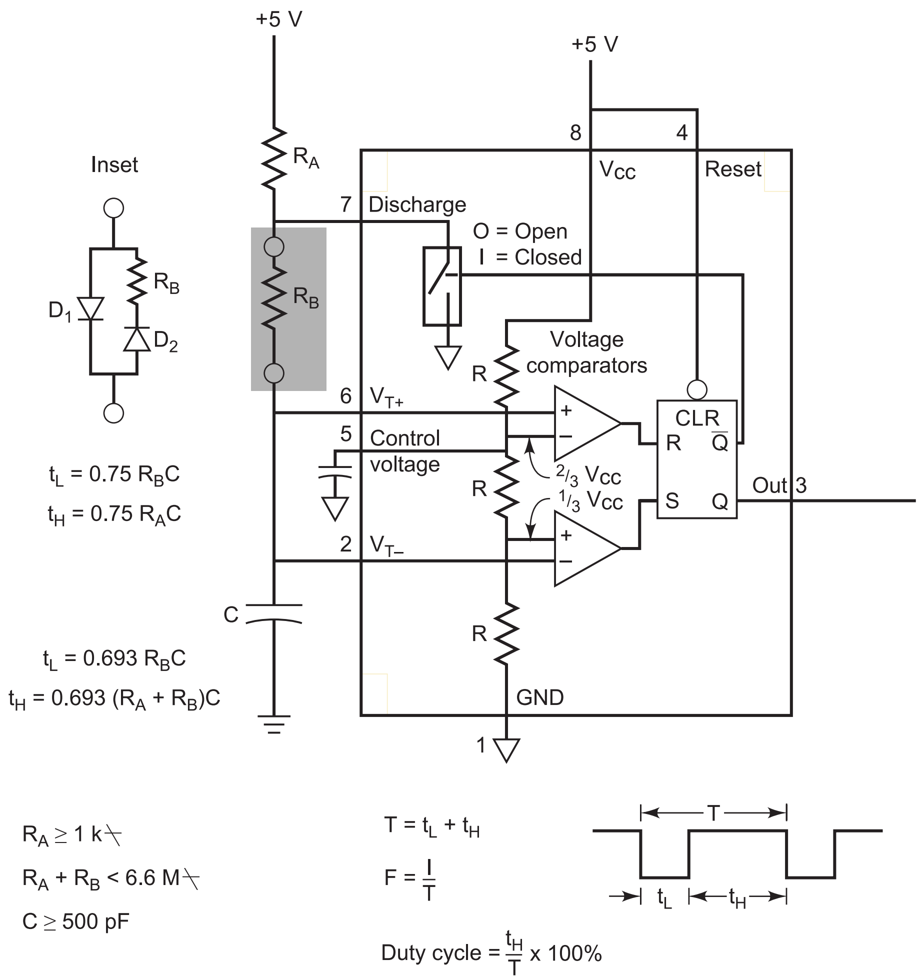

Figure 6: 555 astable multivibrator.

3 Components and apparatus

1. Logic[2] ICs
2. Passive components
3. Breadboard and connecting wires
4. Bench power supply

[2]Specify exactly what ICs you are using in your build

4 Circuit diagram/setup

5 Data collection and analysis

S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	(ambiguous)

Table 1: Function table for S-R flip-flop with active low inputs and PGT triggering.

T	CLK	Q
0	↑	Q_0 (no change)
1	↑	$\overline{Q_0}$ (toggle)
1	↑	1

Table 2: Function table for T flip-flop with active low inputs and PGT triggering.

D	CLK	Q
0	↑	0
1	↑	1

Table 3: Function table for D flip-flop with active low inputs and PGT triggering.

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggle)

Table 4: Function table for J-K flip-flop with active low inputs and PGT triggering.

6 Result

7 Discussion

(You are expected to elaborated on possible timing implications and reflect on your setup-specific details.)

8 References

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

Appendix