NE-3102: Electronics-II Laboratory

Roll _____ Date _____ Experiment No. _____

Name of the experiment

Truth Table verification of J-K flip-flop.

Contents

1 Objective

1. To verify the truth table of a J-K flip-flop.

2 Theory

A flip-flop is an electric circuit with two stable states that can store binary data. This stored data can be changed by applying various inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in many applications. Both are used as data storage elements. It is the primary storage element in sequential logic. But first, we have to know the difference between a latch and a flip-flop.

The basic difference between a latch and a flip-flop is a gating or clocking mechanism. In simple words, a flip-flop is edge-triggered, and a latch is level-triggered. In an SR latch and SR Flip-flops, when we set S as active, the output Q would be HIGH and $\bar{Q}$ would be low. This is irrespective of anything else. On the other hand, a flip-flop is synchronous and also known as a gated or clocked SR latch. The circuit output is changed only when we give an active clock signal. Otherwise, even if the S or R is active, the data will not change.

Due to the undefined state in the SR flip-flop, another flip-flop is required in electronics. The J-K flip-flops are an improvement of the S-R flip-flops. Where S=R=1 is not a problem. The input condition of J=K=1 gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

In simple words, if J and K data input are different (i.e., high and low), then the output Q takes the value of J to the next clock edge. If J and K are both high at the clock edge, then the output will toggle from one state to another. J-K flip-flops can function as set or reset flip-flops.

3 Components and apparatus

1. 74LS76 IC (dual J-K flip-flop)
2. Passive components
3. Breadboard and connecting wires
4. Bench power supply

4 Circuit diagram/setup

5 Data collection and analysis

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggle)

Table 1: Function table for J-K flip-flop.

6 Result

7 Discussion

8 References

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

Appendix