NE-3102: Electronics-II Laboratory

Roll _____ Date _____ Experiment No. _____

Name of the experiment

Design a 4-bit shift register using J-K flip-flops and verify its operation.

Contents

1 Objective

1. To design a 4-bit shift register using J-K flip-flops and verify its operation.

2 Theory

A shift register is a group of flip-flops so arranged that the binary numbers stored in the flip-flops are shifted from one flip-flop to the next for every (active) clock pulse. Figure 1(a) shows the arrangement of J-K flip-flops to operate as a four-bit shift register. Note that the flip-flops are connected so that the output of X_3 transfers into X_2, X_2 into X_1, and X_1 into X_0. This means that upon the NGT of a shift pulse, each flip-flop takes on the value stored previously in the flip-flop on its left. Flip-flop X_3 takes on a value determined by the conditions present on its J and K inputs when the NGT occurs. For now, we will assume that X_3's J and K inputs are fed by the DATA IN waveform shown in Figure 1(b). We will also assume that all flip-flops are in the 0 states before shift pulses are applied .

The waveforms in Figure 1(b) show how the input data are shifted from left to right from flip-flop to flip-flop as shift pulses are applied. When the first NGT occurs at T_1, each of the flip-flops X_2, X_1, and X_0 will have the $J = 0$, $K = 1$ condition present at its inputs because of the state of the flip-flop on its left. Flip-flop X_3 will have $J = 1$, $K = 0$ because of DATA IN. Thus, at T_1, only X_3 will go HIGH, while all the other flip-flops remain LOW. When the second NGT occurs at T_2, flip-flop X_3 will have $J = 0$, $K = 1$ because of DATA IN. Flip-flop X_2 will have $J = 1$, $K = 0$ because of the current HIGH at X_3. Flip-flops X_1 and X_0 will still have $J = 0, K = 1$. Thus, at T_2, only flip-flop X_2 will go HIGH, flip-flop X_3 will go LOW, and flip-flops X_1 and X_0 will remain LOW.

Similar reasoning can be used to determine how the waveforms change at T_3 and T_4. Note that on each NGT of the shift pulses, each flip-flop output takes on the level that was present at the output of the flip-flop on its left just prior to the NGT. Of course, X_3 takes on the level present at DATA IN just before the NGT.

3 Components and apparatus

1. 74LS76A IC
2. Timing generator/clock[1]
3. Passive components
4. Breadboard and connecting wires
5. Bench power supply

4 Circuit diagram/setup

[1] Use the same one from the previous experiment

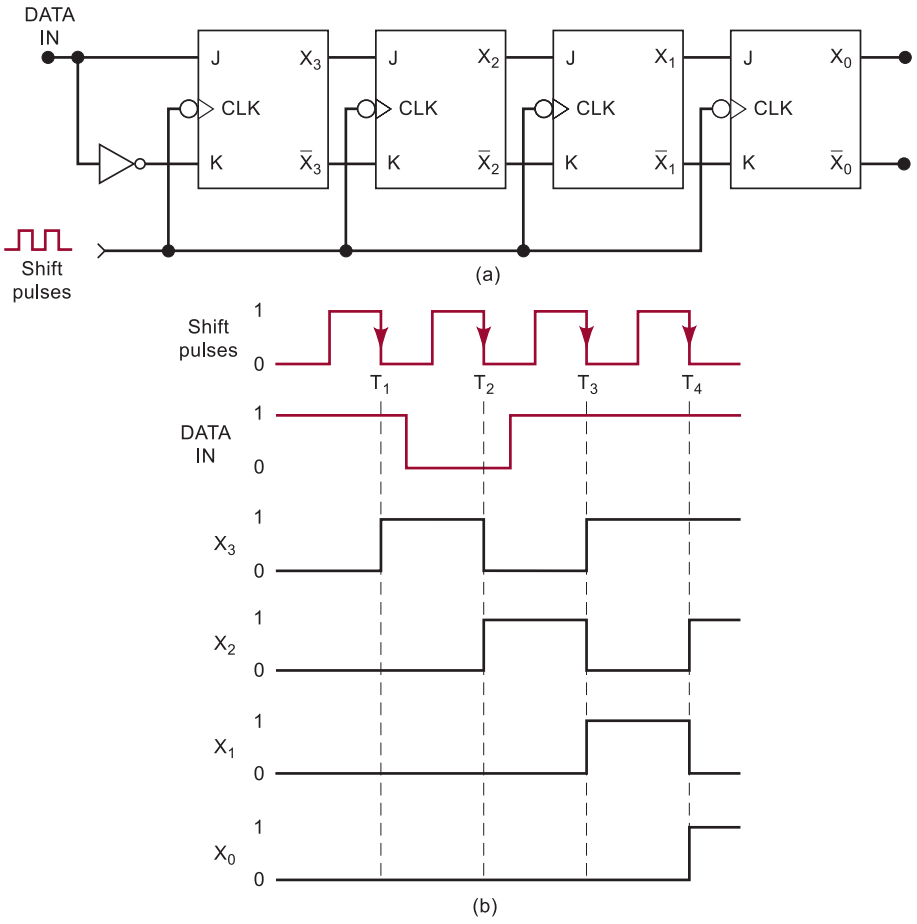

Figure 1: Four-bit shift register; J-K flip-flops with active HIGH inputs and NGT triggering .

5 Data collection and analysis

6 Result

7 Discussion

(You are expected to elaborated on the implications of hold time and propagation delay and reflect on your setup-specific details.)

8 References

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

Appendix