



## NE-3102: Electronics-II Laboratory

Roll \_\_\_\_\_ Date \_\_\_\_\_ Experiment No. \_\_\_\_\_

### Name of the experiment

Implementation of a 4-bit parallel adder using 7483 IC.

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## 1 Objective

1. To implement a 4-bit parallel adder using 7483 IC.

## 2 Theory

A parallel adder can be constructed using any number of full adders (FA) by connecting them parallelly. An FA circuit adds two inputs and a carry input and generates one sum and a carry output. One FA's carry output is carry input to the next higher order FA. Thus, all the bits of both augend and addend are tied into the circuit parallelly and addition in each adder always happens simultaneously. For a 4-bit parallel adder, 4 FAs are required. In Figure 2, the variables  $A_0, A_3, A_2, A_1$ , represent the bits of the augend which is stored in the accumulator register, and the variables  $B_3, B_2, B_1, B_0$  represents the bits of the addend which is stored in the B register. variables  $C_3, C_2, C_1, C_0$  represents carry bits into the corresponding FAs. Sum appears at  $S_3, S_2, S_1, S_0$  outputs.

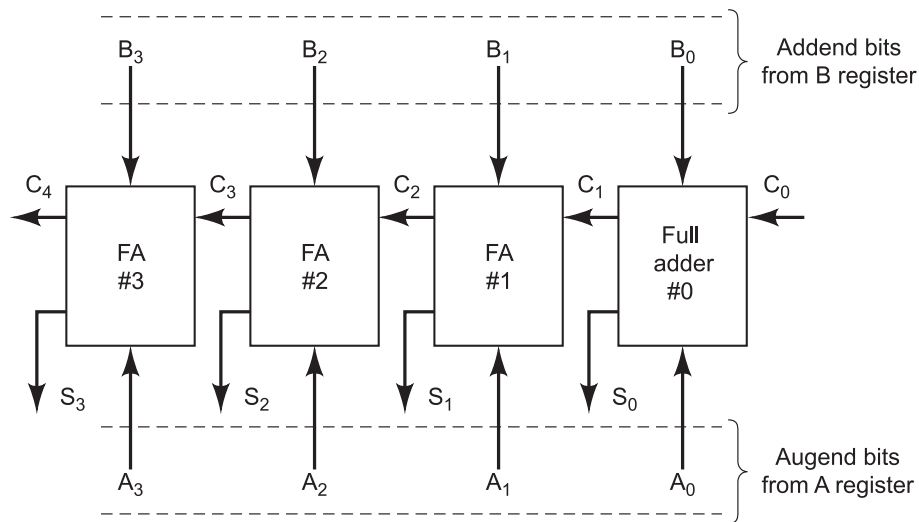


Figure 1: Block diagram of a four-bit parallel adder circuit using full adders.

A				B				Sum				Carry
$A_3$	$A_2$	$A_1$	$A_0$	$B_3$	$B_2$	$B_1$	$B_0$	$S_3$	$S_2$	$S_1$	$S_0$	$C_4$
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0
0	1	0	0	0	1	0	0	1	0	0	0	0
0	1	0	1	0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	1	0	1	1	0	0	0
0	1	1	1	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	1	0	0	1	0	0	1	0	1
1	0	1	0	1	0	1	0	0	1	0	0	1
1	0	1	1	1	0	1	1	0	1	1	0	1
1	1	0	0	1	1	0	0	1	0	0	0	1
1	1	0	1	1	1	0	1	1	0	1	0	1
1	1	1	0	1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1

Table 1: Truth table for 4-bit parallel adder.

### 3 Components and apparatus

1. 7483 IC
2. Passive components
3. Breadboard and connecting wires
4. Bench power supply

### 4 Circuit diagram/setup

The following is the implementation of a four-bit parallel adder circuit:<sup>1</sup>

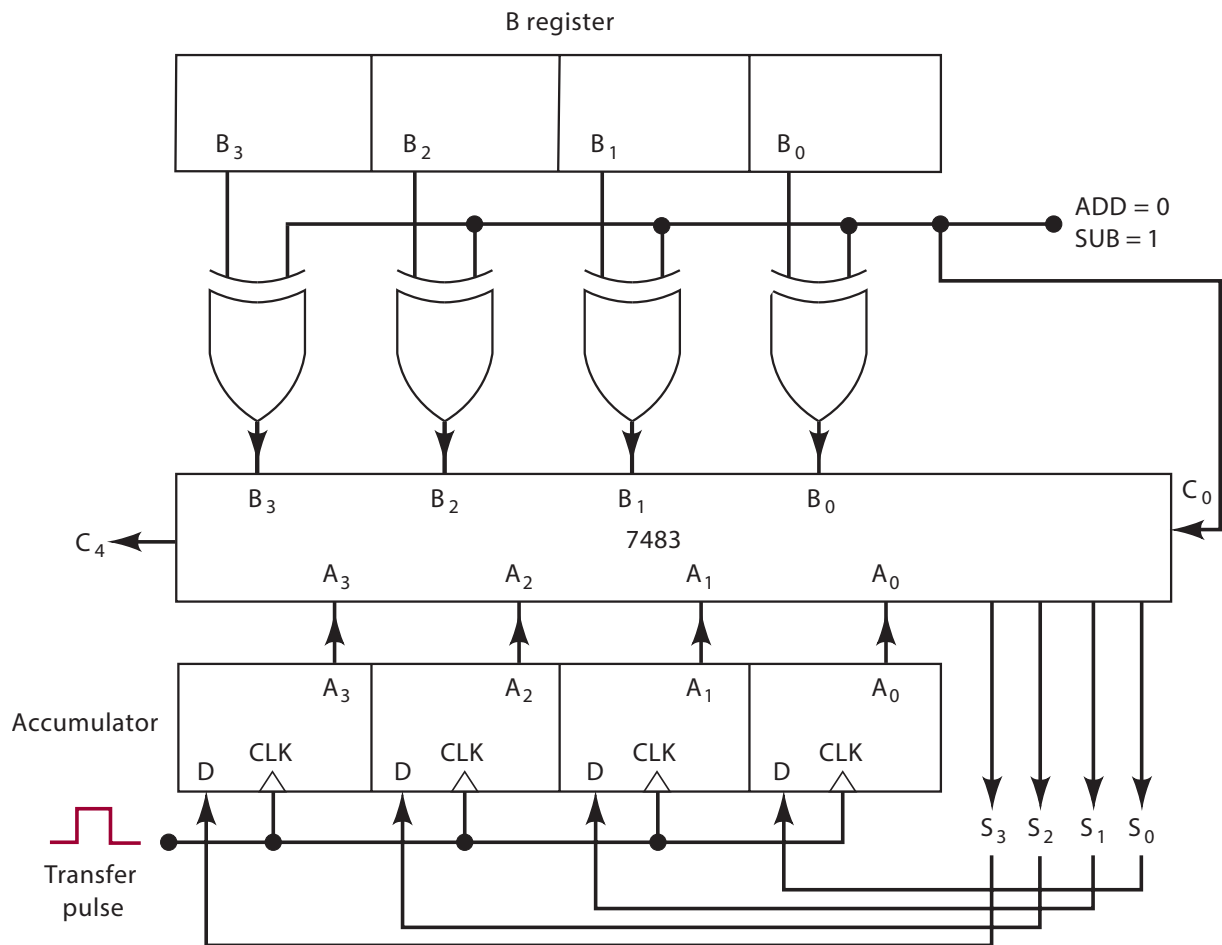


Figure 2: Implementation of a four-bit parallel adder circuit using a 7483 IC.

<sup>1</sup>Perform the arithmetic operation  $6 + 1 - 4$  (or any other) in the 2's-complement system using the adder. The operation should be done in 2 steps: first perform  $6 + 1$  and then perform  $7 - 4$ . Values in the intermediate and final steps should be stored/accumulated in the Accumulator or the A register. Manually simulate the B register by applying HIGH/LOW on the bits. Use two 7474 D flip-flop ICs for constructing the Accumulator register and asynchronously load the initial augend/minuend: in this case, the value is 6 in 4-bit binary, including the sign bit. Do not put a timing generator/clock; manually synchronize the transfer instead. Note that an array of Ex-OR gates performs the plain binary to 2's-complement conversion between the B register and the points where the values are actually input to the 7483 IC, meaning that you do not need to perform the 2's-complement conversion; the circuit will do that for you. The implementation is essentially a 4-bit arithmetic logic unit (ALU).

## **5 Data collection and analysis**

## **6 Result**

## **7 Discussion**

## **8 References**

1. Tocci Ronald J, Neal W, Greg M. Digital Systems Principles and Applications.

## **Appendix**