

COAL Lab-00

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Literature Review:

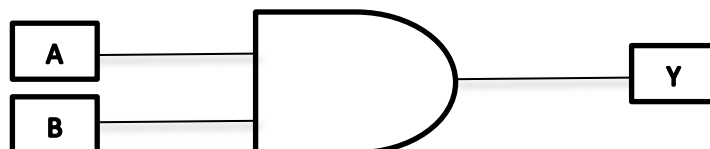
In this lab, we learned the basic knowledge of how hardware performs basic logic functions. RISC-V is an international open instruction set architecture to implement in microprocessors. HDL (Hardware Description Language) is used to describe structure and behaviors of circuits. Verilog is a Hardware Description Language to design digital systems. It follows gate-level, dataflow and behavioral modeling.

Task:

Implement AND gate function using Verilog code.

AND GATE:

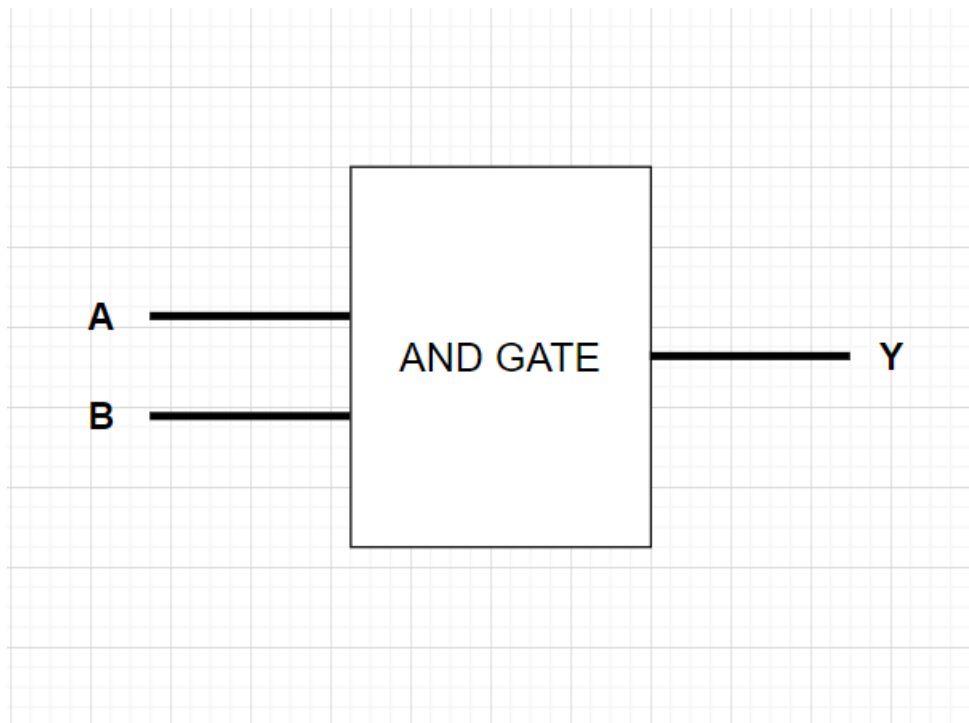
And gate is a basic logic gate which gives high if bth of the inputs are high or low if any of the inputs is low



Truth Table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Block Diagram:



Boolean Equation

$$Y = A \cdot B$$

Verilog Code:

design.v

```
module gate(A,B,Y);  
  
    // Declaring inputs  
    input A,B;  
    // Declaring output  
    output Y;  
  
    // Using gate level modeling  
    and(Y,A,B);  
  
endmodule
```

testbench.v

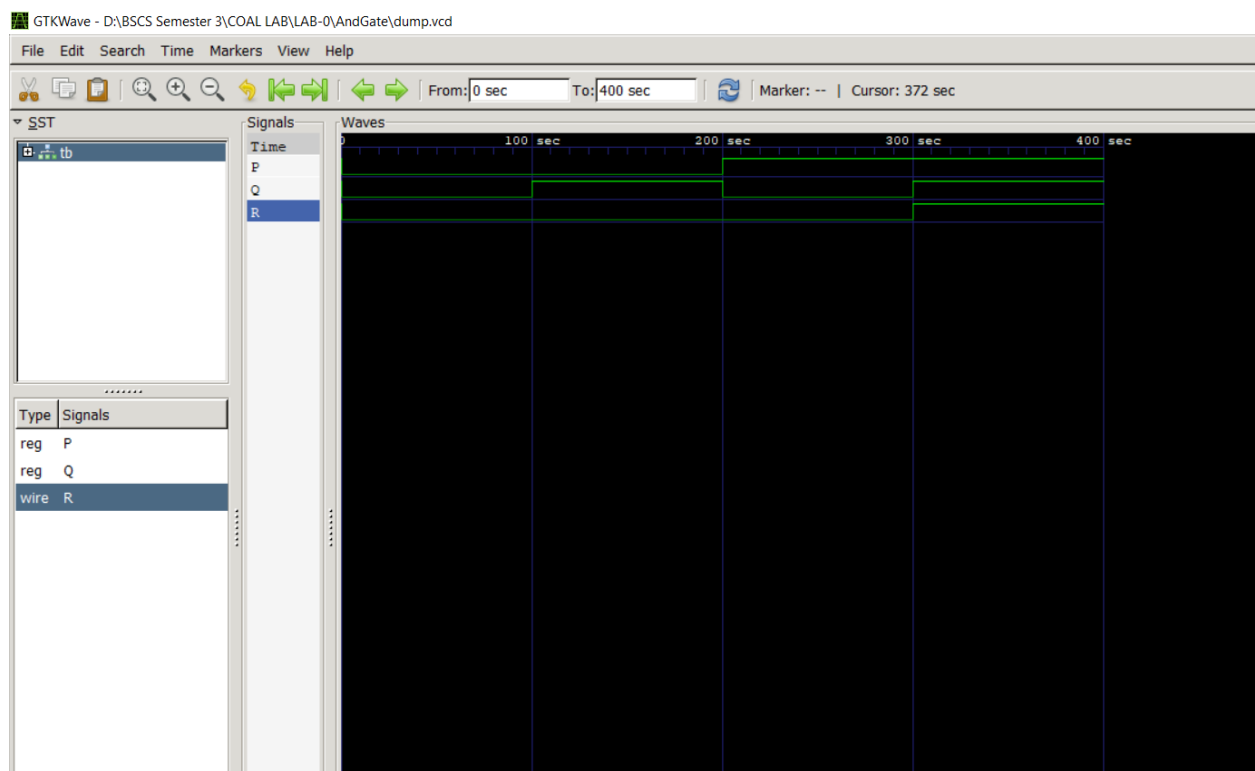
```
module tb();  
  
    // variables  
    reg P, Q;  
    wire R;  
  
    // declaring design // dut (Design Under Test)  
    gate dut(.A(P),.B(Q),.Y(R));  
  
    // All possible input value for and gate  
    initial begin  
        P <= 1'b0;  
        Q <= 1'b0;  
        #100;  
  
        P <= 1'b0;  
        Q <= 1'b1;  
        #100;  
  
        P <= 1'b1;  
        Q <= 1'b0;  
        #100;  
  
        P <= 1'b1;  
        Q <= 1'b1;  
        #100;  
    end  
endmodule
```

```
end

initial begin
    $dumpfile("dump.vcd"); // value change dump // variable change dump
    $dumpvars(0);
end

endmodule
```

Waveforms:



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