Programmed I/O

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Book Chapter

- “Computer Organization and Architecture”
- Author “William Stallings”
- 8th Edition
- Chapter 7
  - Section 7.3

I/O Techniques

- Three major I/O techniques
  - Programmed I/O
  - Interrupt-driven I/O
  - Direct Memory Access (DMA)

Programmed I/O

- Data are exchanged between the processor and I/O module
- Processor takes direct control of I/O operation by executing a program
  - Sensing status
  - Read/Write commands
  - Transferring data
- Processor waits for I/O module to complete operation
- If processor is faster than I/O module, then much of the processor time is wasted

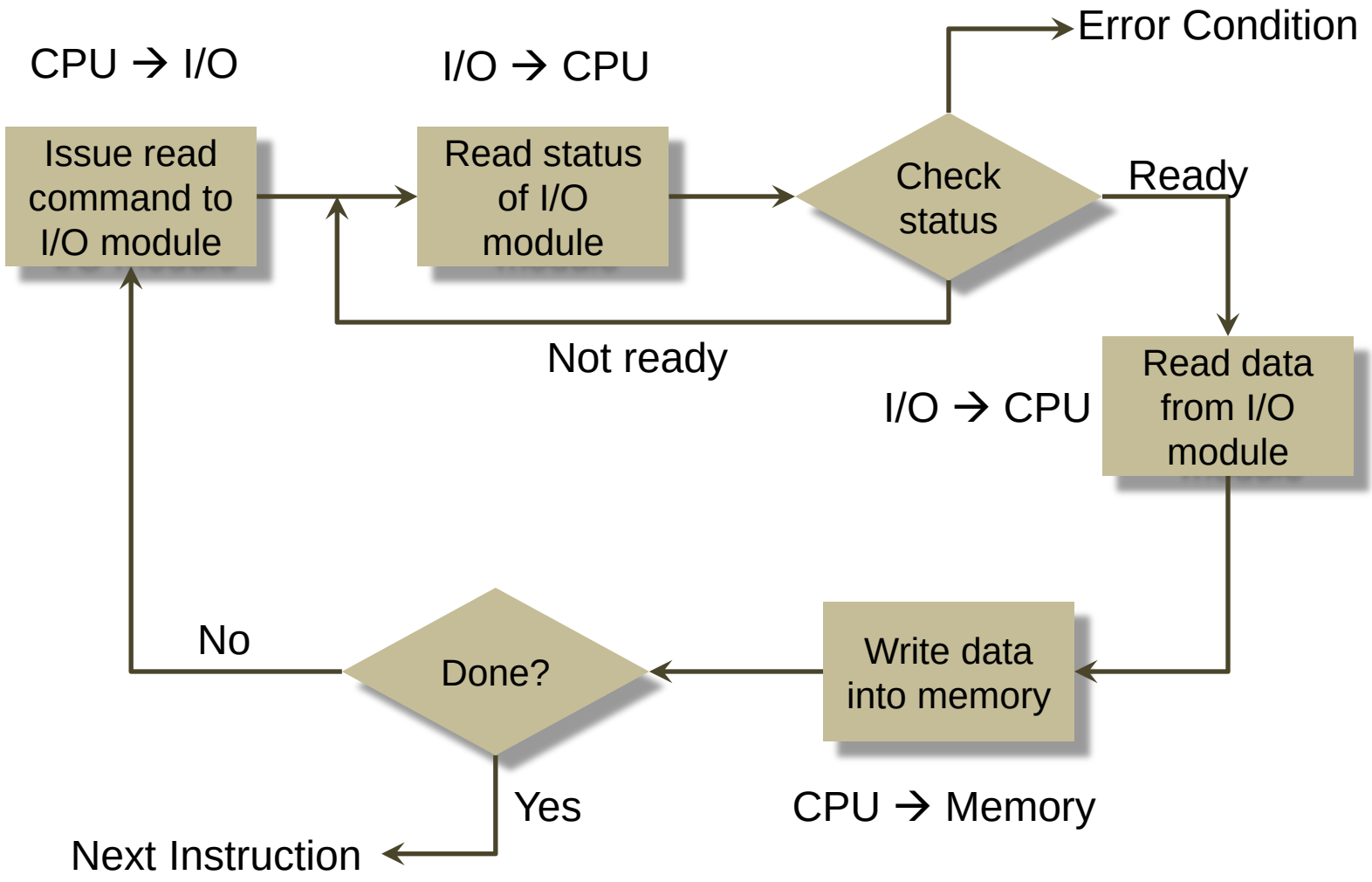
Programmed I/O – Details

- CPU requests I/O operation
- I/O module performs operation
- I/O module sets status bits
- CPU checks status bits periodically
- I/O module does not inform CPU directly
- I/O module does not interrupt CPU
- CPU may wait or come back later

I/O Commands

- CPU issues address of particular I/O module and external device
- CPU issues one of four I/O commands
  - Control – used to activate a peripheral and telling what to do e.g. spin up disk, rewind magnetic tape etc.
  - Test – checks status e.g. is the device powered on?
  - Read – I/O module obtains data from peripheral and places in internal buffer (data register)
  - Write – I/O module takes data from data bus and transmits to the peripheral

Programmed I/O Block Diagram



I/O Mapping (1/2)

- Often a one-to-one relationship between I/O related instructions and I/O commands
- One or more peripherals connected to each I/O module
- Each peripheral has a unique identifier or address
- I/O command issued by processor contains the address of desired peripheral
- … each I/O module must interpret the address lines to determine if the command contains address of peripheral connected to it

I/O Mapping (2/2)

- When processor, main memory and I/O share a common bus, two modes of addressing are possible
  - Memory-mapped I/O
  - Isolated I/O

Memory-mapped I/O

- Single address space for memory locations and I/O devices
- Processor treats data and status registers of I/O modules as memory locations
- With 8 address lines, a total of $2^8 = 256$ memory locations and I/O address can be supported in any combination

Isolated I/O

- Separate address space
- Address bus equipped with
  - Memory read/write lines to select memory
  - Input/Output lines to select I/O module
- Command line specifies whether address refers to memory location or I/O device
- With 8 address lines
  - 256 memory locations can be referenced
  - 256 I/O addresses are supported