Interconnection Structures

Muhammad Afzaal
m.afzaal@nu.edu.pk

Book Chapter

- “Computer Organization and Architecture”
- Author “William Stallings”
- 8th Edition
- Chapter 3
  - Section 3.3
  - Section 3.4

Interconnection Structures

- Three basic computer components
  - Processor
  - Main memory
  - I/O Devices
- They need to interact with each other to perform their functions
- Collection of paths connecting above modules is called Interconnection Structures
- Type of connection depends upon the module
  - Memory Connection
  - I/O Module Connection
  - CPU Connection

Memory Connection

- Receives and send data
- Receives addresses of memory locations
- Receives control signals
  - Read
  - Write
  - Timing

I/O Module Connection

- Similar to memory from computer's viewpoint
- Input connection
  - Receives data from peripheral
  - Sends data to computer
- Output connection
  - Receives data from computer
  - Sends data to peripheral

CPU Connection

- Reads instructions and data
- Writes out data after processing
- Sends control signals to other units
- Receives and acts on interrupts

Bus Interconnection

- A Bus is a communication path connecting two or more devices
- Each bus consists of single/multiple lines
- Bus that connects major computer components like processor, memory and I/O, is called System Bus
- Bus lines can be classified into three different types depending upon their functionality
  - Data Lines
  - Address Lines
  - Control Lines

Data Lines

- Used to move data between system modules
- Called Data Bus altogether
- Carries data
  - Remember that there is not any difference between “data” and “instruction” at this level
  - Width is a key determinant of performance
    - 32, 64 or 128 data lines
- Number of lines is equal to the number of bits transferred at one time

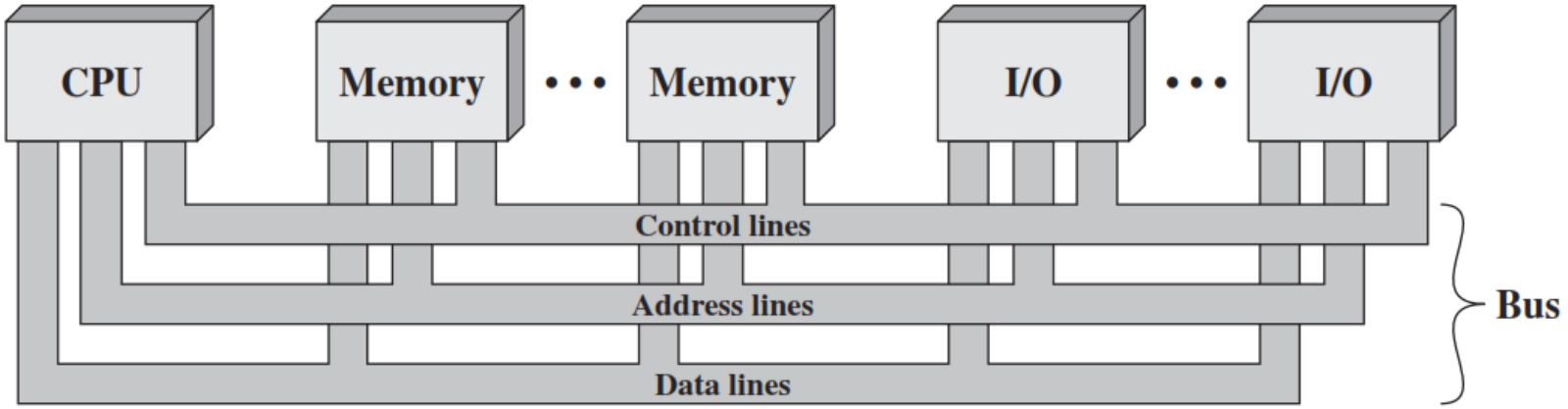
Address Lines

- Identify the source or destination of data
  - e.g. CPU needs to read an instruction from a given location in memory
- Bus width determines maximum memory capacity of system

Control Lines

- Control the use of data and address lines
- Used to transmit command and timing signals
- Timing signals indicate the validity of data and address information
- Command signals specify operation to be executed
- Typical control signals include
  - Memory read/write signal
  - Interrupt request
  - Clock signal

Bus Interconnection Scheme



Speed Issues

- Different devices have different transfer/operate speed
- If the speed of bus is bounded by the slowest device connected to it, the efficiency will be very low
- How to solve it?
  - A common approach is using buffers

Single Bus Problems

- Lots of devices on one bus leads to
  - Propagation delay
    - Long data paths mean that coordination of bus use can adversely affect performance
    - Aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Bus Types

- Dedicated Bus
  - Permanently assigned one function
  - Separate Data and Address lines
- Multiplexed Bus
  - Shares lines
  - Address valid or Data valid control line
  - Advantage – fewer lines
  - Disadvantage
    - More complex circuitry
    - Potential reduction in performance

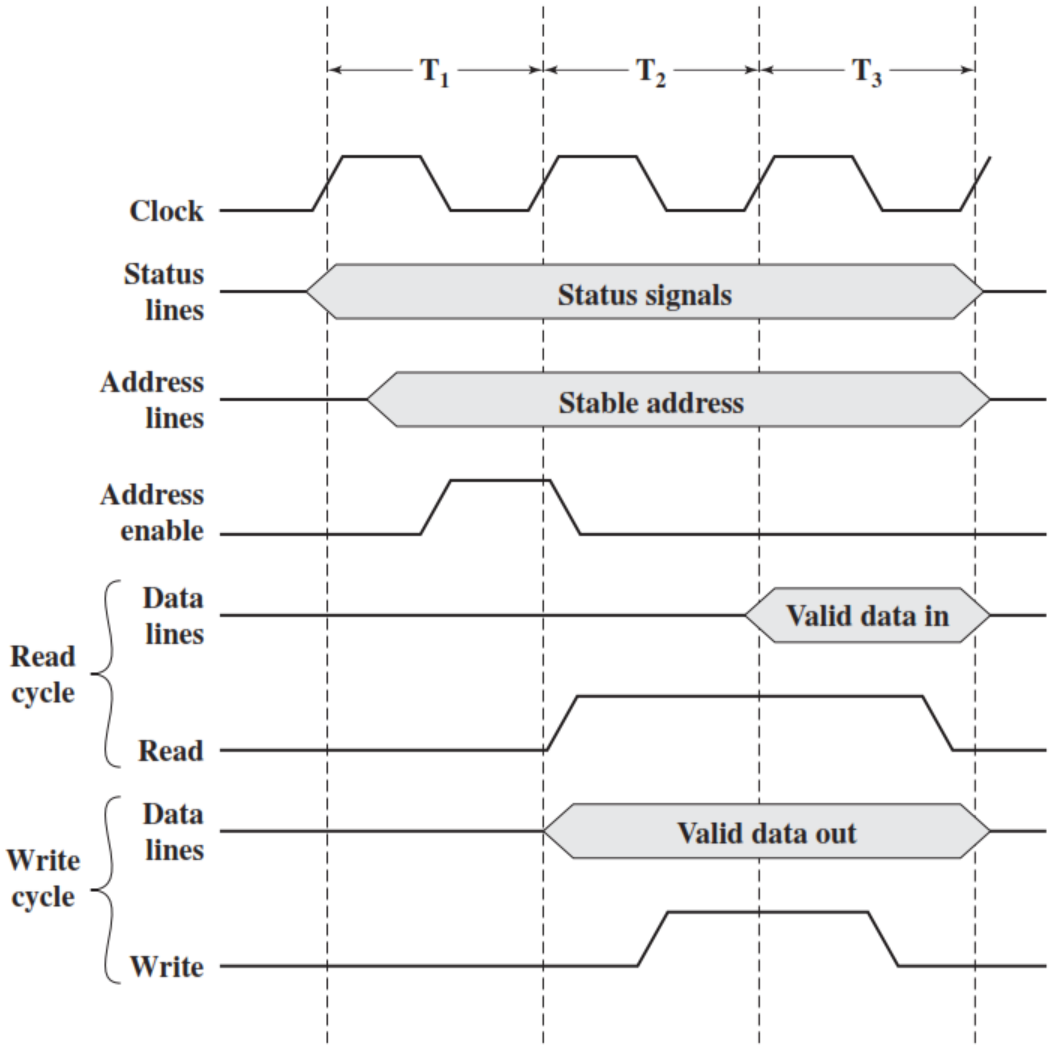
Bus Arbitration

- More than one modules may need control of the bus
- Only one unit at a time can successfully transmit over the bus
- Arbitration may be
  - Centralized
    - Single hardware device controlling the bus access
  - Distributed
    - Each module may claim the bus
    - Control logic on all modules

Timing

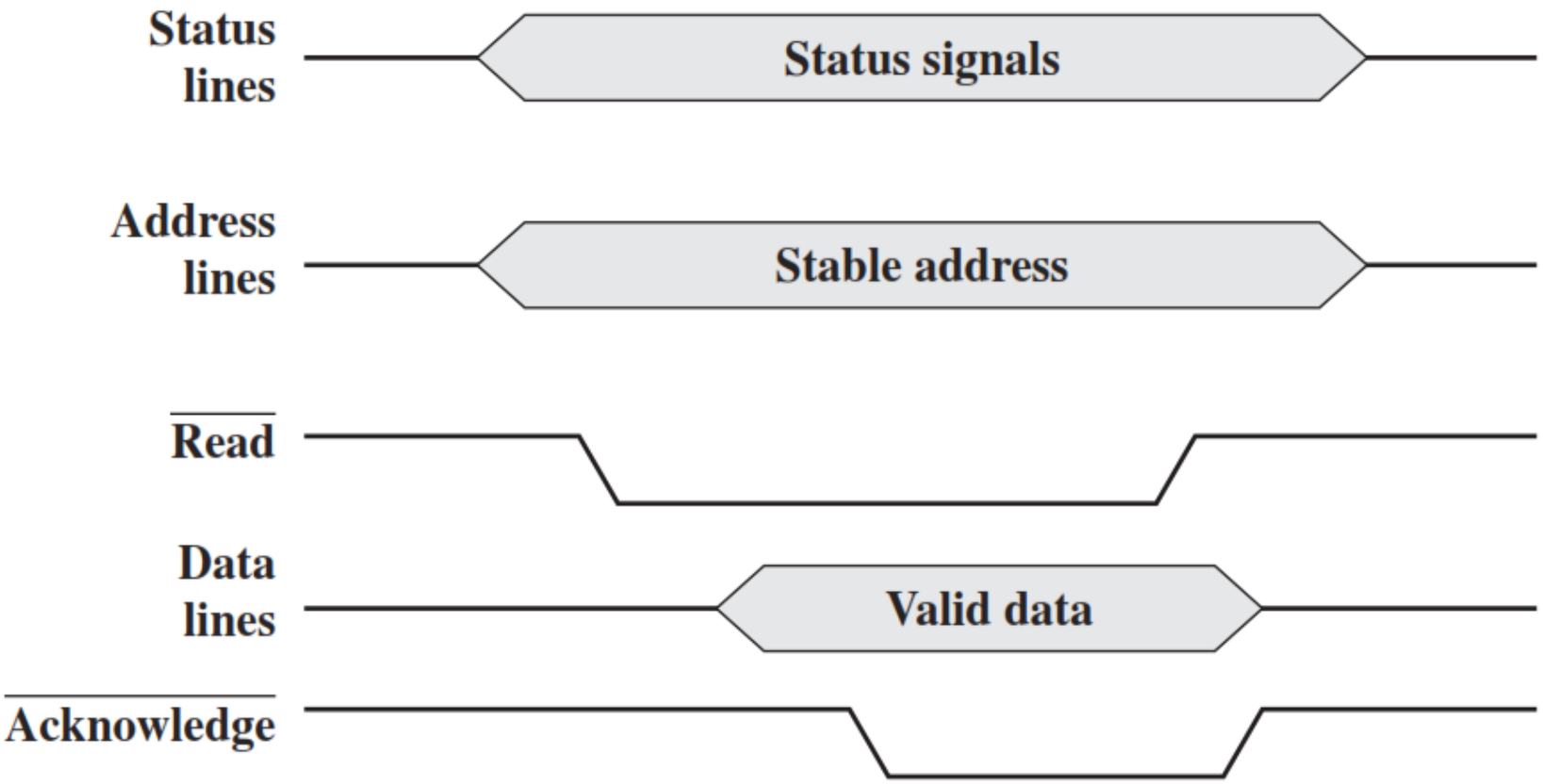
- Coordination of events on bus
- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - All devices can read clock line
  - Usually a single cycle for an event

Synchronous Timing Diagram



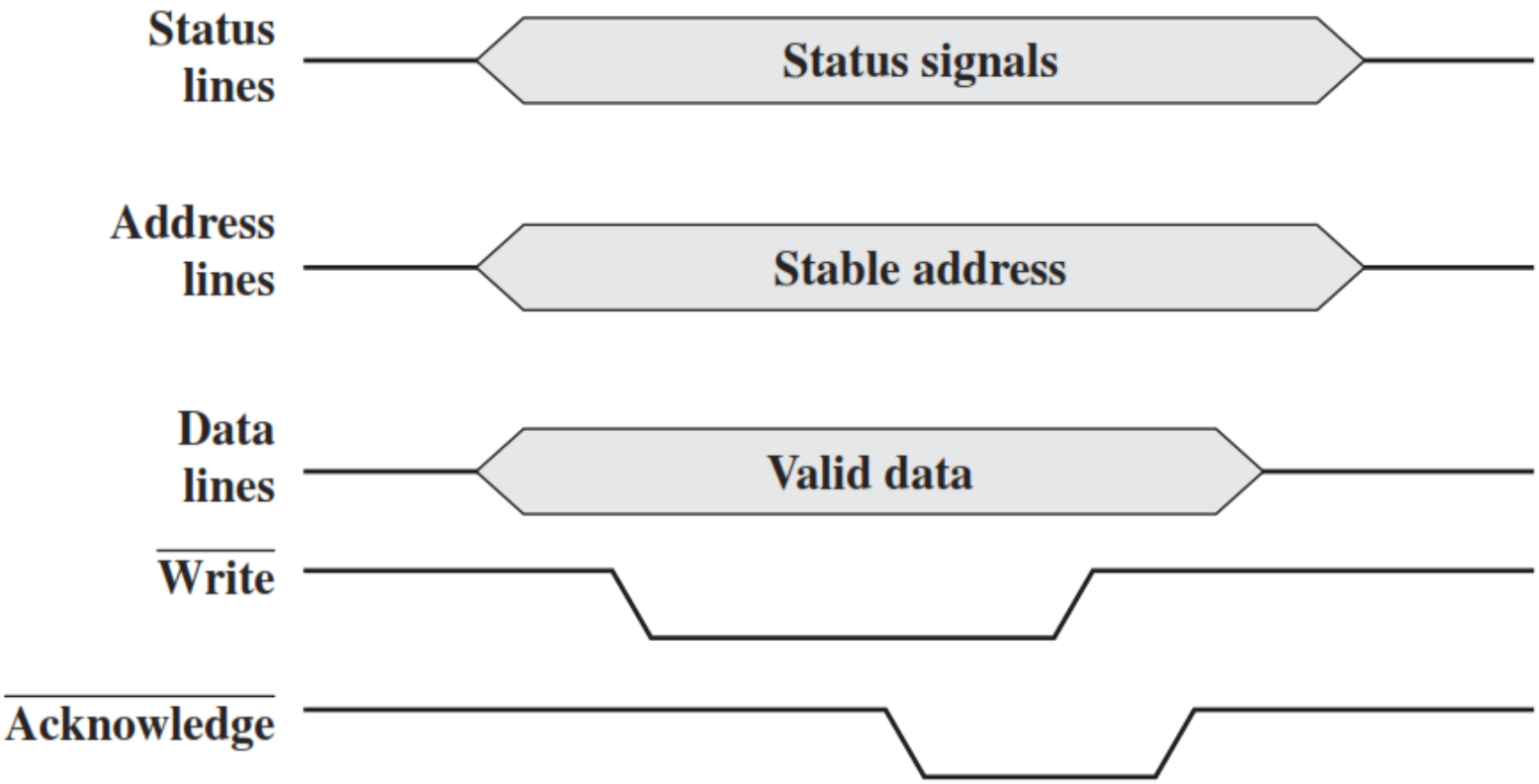
Asynchronous Timing Diagram

- System bus read cycle



Asynchronous Timing Diagram

- System bus write cycle



Synchronous vs. Asynchronous

- Synchronous timing is simpler to implement
- Less flexible than asynchronous timing
- Because all devices on synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance
- With asynchronous timing, a mixture of slow and fast devices, using older and newer technology, can share a bus