

Basic Computer Organization

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Book Chapter

- “Assembly Language for x86 processors”
- Author “Kip R. Irvine”
- 6th Edition
- Chapter 2
 - Section 2.1

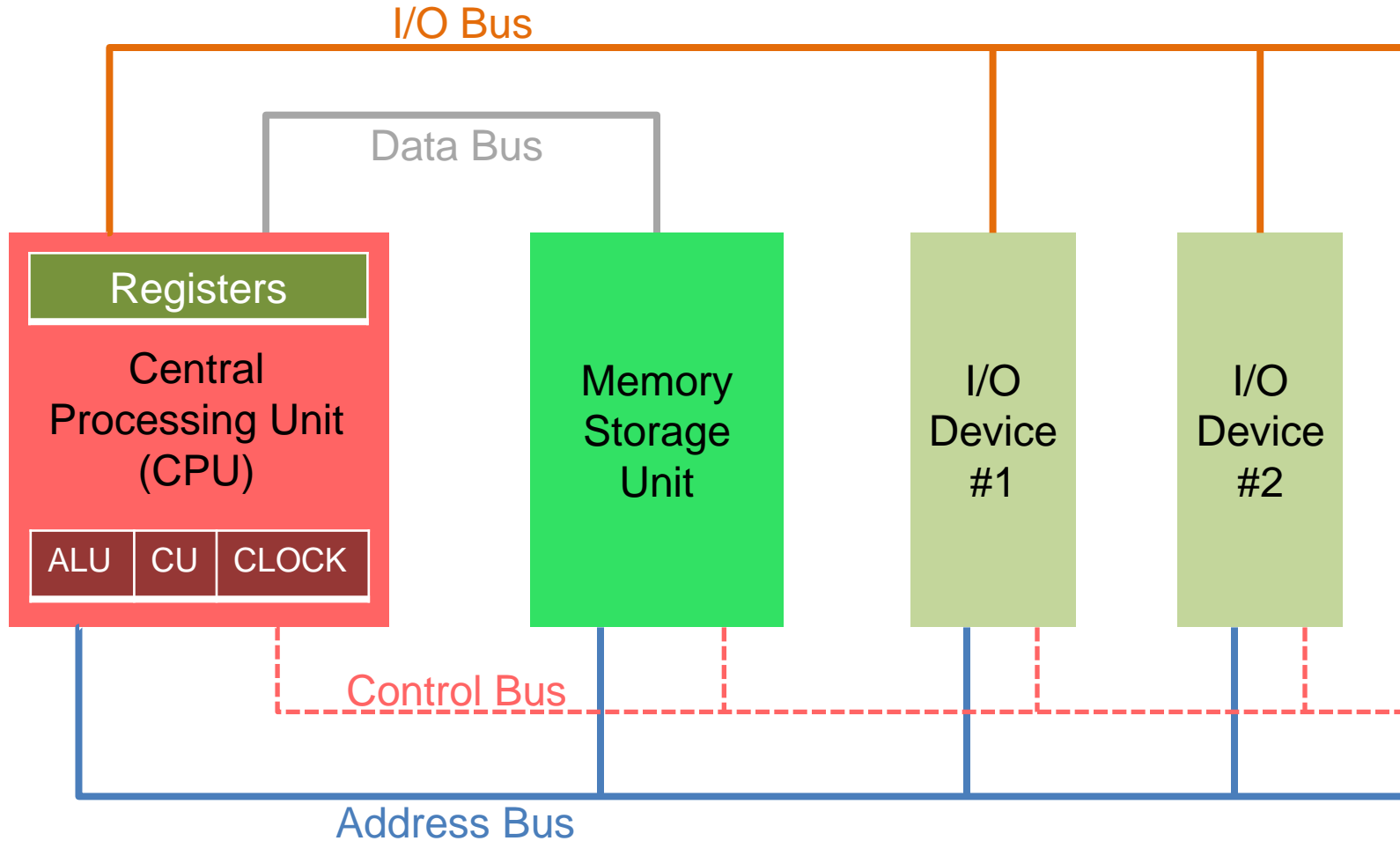
Organization and Architecture

- Computer Architecture
 - Attributes of a computer that have a direct impact on the logical program execution
 - e.g. I/O mechanisms, memory addressing techniques
- Computer Organization
 - Operational units and their interconnection that realizes the architectural specifications
 - e.g. control signals, interconnection between computer and its peripherals

Basic Computer Organization (1/2)

- Computer has 3 main components
 - Processor, also called Central Processing Unit (CPU)
 - Memory and Storage Devices
 - I/O Devices
- These components communicate with each other through
 - Data Bus
 - I/O Bus
 - Address Bus
 - Control Bus

Basic Computer Organization (2/2)



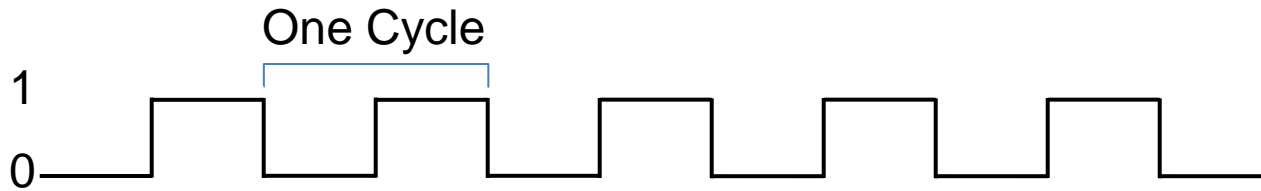
Central Processing Unit (CPU)

- Generally called Processor
- Contains
 - Clock
 - Registers
 - Arithmetic Logic Unit (ALU)
 - Performs arithmetic and logic instructions
 - Control Unit (CU)
 - Generates the control signals required to execute the instructions

Clock (1/2)

- Clock cycle is basic unit of time for machine instructions
- Synchronizes Processor and Bus operations
- $\text{Clock cycle} = \text{Clock period} = 1/(\text{Clock Rate})$
- $\text{Clock Rate} = \text{Clock Frequency} = \text{Cycles per sec}$
 - 1 Hz clock produces 1 Clock Cycle in 1 second
 - 1 KHz clock produces 1000 Clock Cycles in 1 second
 - 1 MHz clock produces 1,000,000 cycles in 1 second
 - 1 GHz clock produces 1,000,000,000 cycles in 1 second

Clock (2/2)



Clock Frequency	Clock Period (sec)	Time to execute one instruction
1 Hz	1	1 sec
1 KHz	0.001	1 ms (millisecond)
1 MHz	0.000,001	1 μ s (microsecond)
1 GHz	0.000,000,001	1 ns (nanosecond)

Memory (1/2)

- Ordered sequence of bytes
 - Sequence number is called memory address
- Byte addressable memory
 - Each byte has a unique address
- Physical address space
 - Determined by the address bus width
 - Pentium has 32-bit address bus
 - Physical address space of Pentium = 2^{32} bytes = 4 GB
 - Itanium with 64-bit address bus can support up to 2^{64} bytes of physical address space

Memory (2/2)

- Address of location to be read/written is placed on the address bus
- Data to be read/written is places on the data bus by memory/processor
- Two control signals read and write decide the reading or writing operations



Physical Address Space

- Address space is the set of addressable memory locations (bytes)

Address in decimal		Address in hex
$2^{32}-1$		FFFFFFFF
		FFFFFFFE
		FFFFFFFD
	• • •	
2		00000002
1		00000001
0		00000000

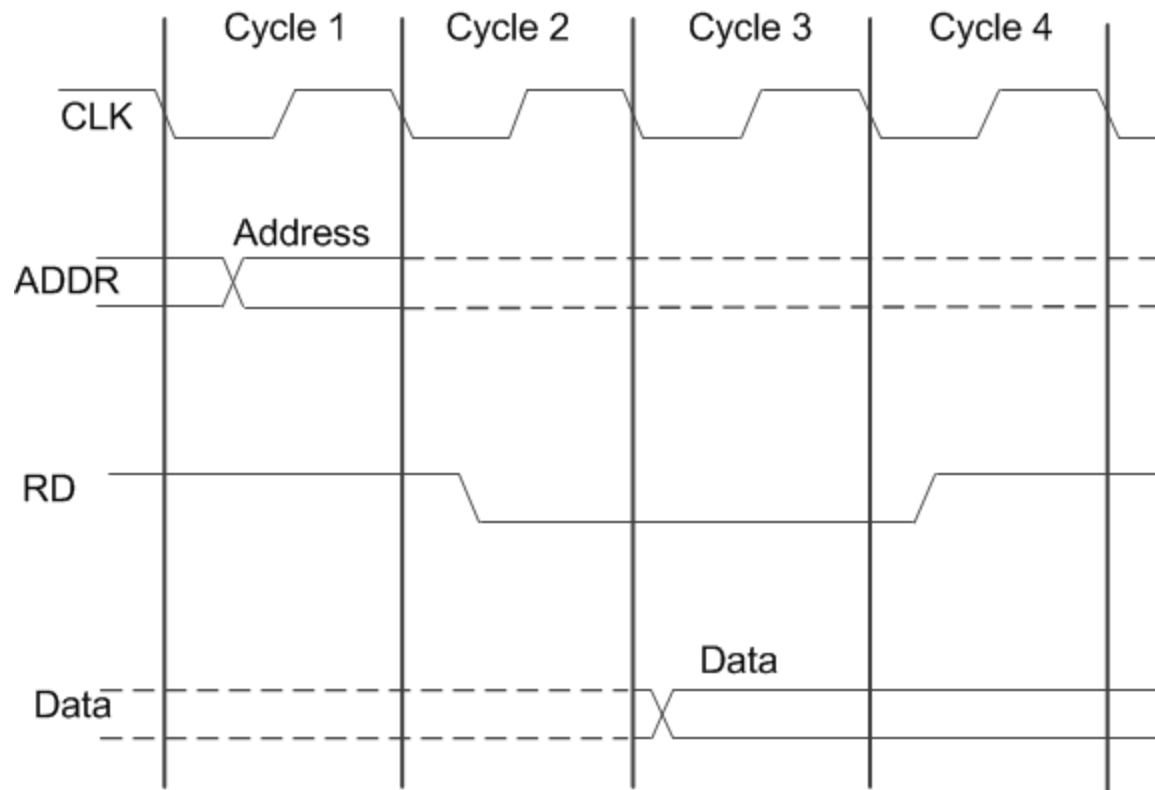
Reading from Memory

- Multiple clock cycles are required
- Memory responds much more slowly than CPU
- Reading process is carried out in this way
 - Address is placed on the address bus
 - Read Line (RL) goes low indicating that processor wants to read
 - CPU waits for memory to respond
 - Read Line (RL) goes high indicating that data has been placed on the data bus

Memory Read and Write Cycles

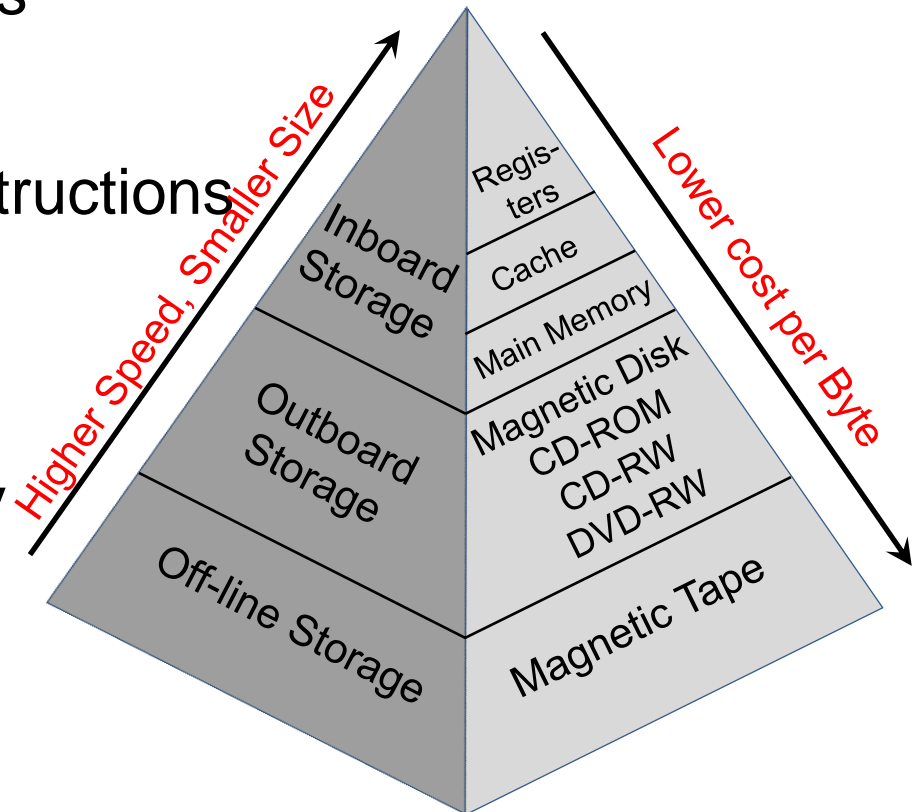
- In Read Cycle, the Processor
 - places **address on address bus**
 - asserts the memory **read control signal**
 - waits for memory to place **data on the data bus**
 - **reads the data** from data bus
 - **drops** the memory read signal
- In Write Cycle, the Processor
 - places **address on the address bus**
 - asserts the memory **write control signal**
 - places the **data on the data bus**
 - waits for memory to **store the data**
 - **drops** the memory write signal

Reading from Memory



Memory Hierarchy

- Registers
 - Fastest storage elements
- Cache Memory
 - Stores recently used instructions
- Main Memory
- Magnetic Disk
 - Stores data permanently
- Magnetic Tape



Next Lecture

- IA-32 Registers
 - General Purpose Registers
 - Special-Purpose and Segment Registers
 - EFLAGS Registers