Syed Noorul Saad

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Education

University of Waterloo — Waterloo, ON
Candidate for B.A.Sc Computer Engineering — Sep 2022 - May 2027
Relevant courses: Reconfigurable Computing (Master's Level), Real Time Operating Systems, Digital Hardware Systems, Computer Architecture, Compilers, Embedded Microprocessor Systems

Projects

RISC-V CPU + NPU Machine Learning Co-Processor *RISC-V ISA, Verilog, AMD Vivado, FPGA*

- Designing a **5-stage pipelined RV32I RISC-V core** and a **Neural Processing Unit (NPU)** with dedicated **ML acceleration** hardware for **MNIST digit classification**.
- **Integrating** CPU and NPU in a **co-processor achitecture** on FPGA, and extending the RISC-V ISA to include **custom instructions** to offload neural-network operations to the NPU.

Matrix-Vector Multiplication Engine + Activation Unit *SystemVerilog, AMD Vivado, FPGA*

- Designed and implemented a pipelined **Matrix-Vector Multiplication (MVM) engine** in SystemVerilog, inspired by Microsoft Brainwave's deep learning inference accelerator.
- Optimized for throughput and latency using **DSP48e1 slices**, capable of calculating **27 outputs in parallel at 280 MHz**.
- Built a fully pipelined hyperbolic tangent (tanh) approximation unit based on a Taylor series approximation for nonlinear activation. **Improved performance from 170 MHz to 320 MHz**.

UVM Design Verification Project (Aligner) *SystemVerilog*
Designed and implemented a comprehensive **UVM testbench** for a data aligner module in SystemVerilog, based on a Udemy course. Developed **reusable agent classes, a model, and a scoreboard** to ensure thorough verification.

Shell Jr *C++, OpenAI API*
Implemented a lightweight Unix-like shell in C++ with support for **command parsing, process creation, and I/O redirection**. Integrated an **AI-powered explain command** via the **OpenAI API**, enabling natural-language explanations of CLI commands directly within the shell.

Experience

UW ASIC Design Team — Waterloo, ON
Digital Design Engineer — August 2025 - Ongoing

- Leading a **mixed-signal design** team to implement a lightweight **RISC-V core** with **custom instructions** to communicate with an **AXI crossbar** for integration into an **analog MVM engine**.
- Implemented a **Serial Peripheral Interface (SPI)** module in Verilog, incorporating flip-flop synchronizers to handle **clock domain crossing** and prevent metastability.
- Developed and executed verification tests using **CocoTB**, a Python-based testbench framework, as part of the team's **TinyTapeout** ASIC flow.

VCast Online — Dubai, UAE
Software Engineer — January 2025 - May 2025

- Led the full-stack development of a collaborative mind-map platform, enabling real-time feedback and map sharing, **driving community engagement up by 25%**.
- Built and deployed a **scalable SvelteKit + Node.js web app** from scratch, integrating **dynamic graph editing** (Cytoscape.js), Google OAuth, JWT authentication, and enforced access control logic (owner vs viewer privileges).
- Architected and integrated a Mongoose-based feedback system, **enabling structured insight** collection on nodes, edges, and the graph as a whole — **improving data access times by 18%**.

Dematic — Waterloo, ON
Technical Writer — May 2024 - August 2024

- Developed comprehensive technical documentation for Dematic's mechanical and control systems, enhancing user understanding and supporting the seamless integration of advanced automation technologies.
- Authored detailed user manuals and technical guides for Dematic's InSights logistics software, ensuring clarity in functionality and facilitating efficient software deployment across multiple industries.

Languages and Tools

Languages:	C/C++, SystemVerilog/Verilog, JavaScript, Python
Tools:	Git, AMD Vivado, Quartus, GTKWave, VTR, OpenFPGA, Visual Studio Code, JIRA