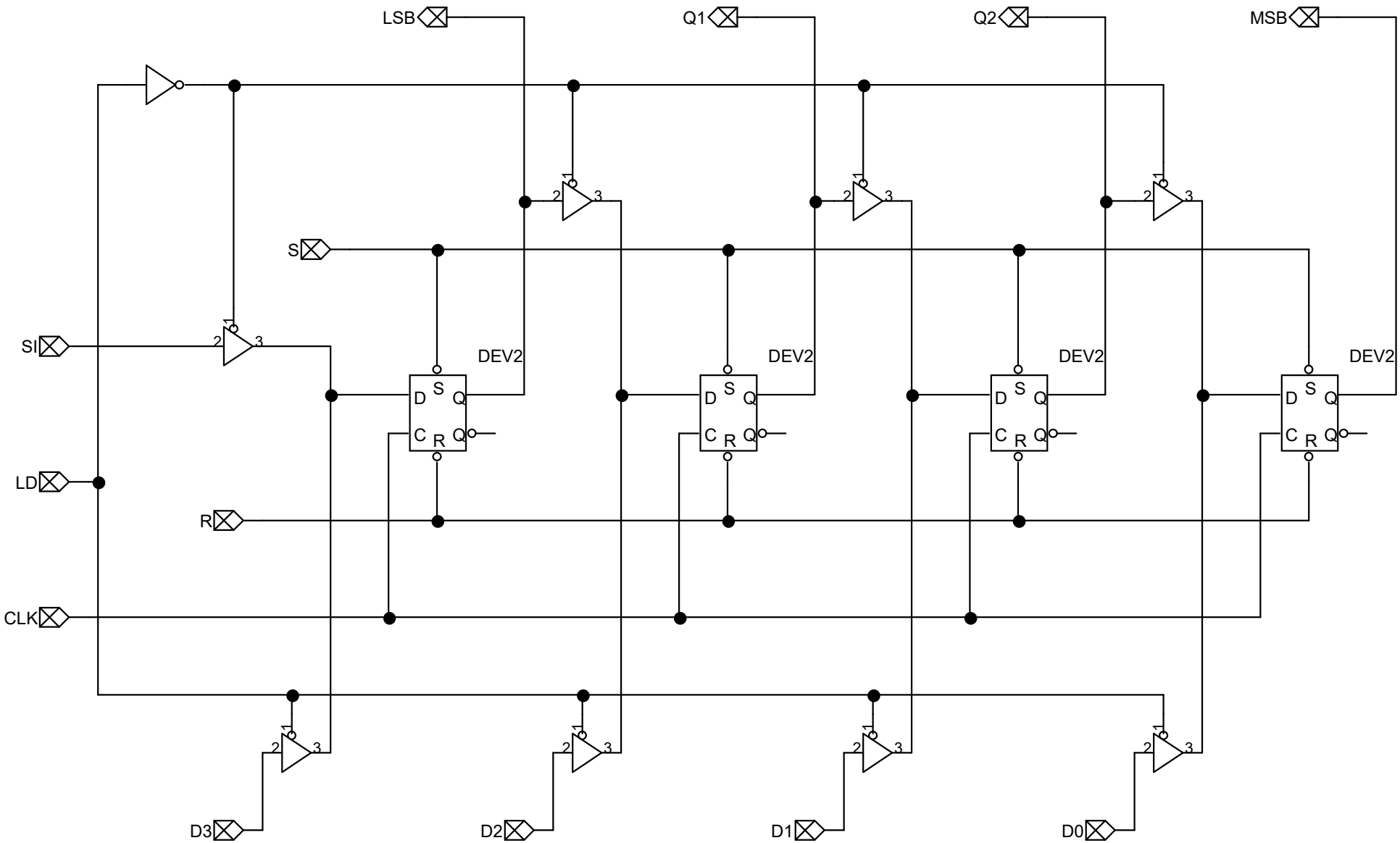
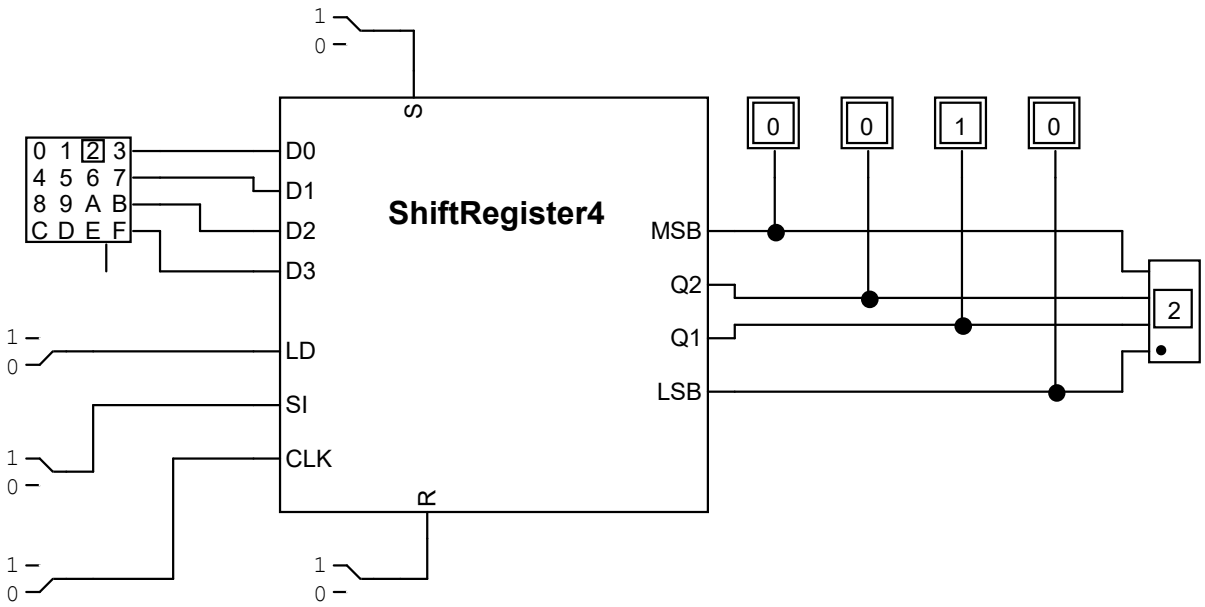
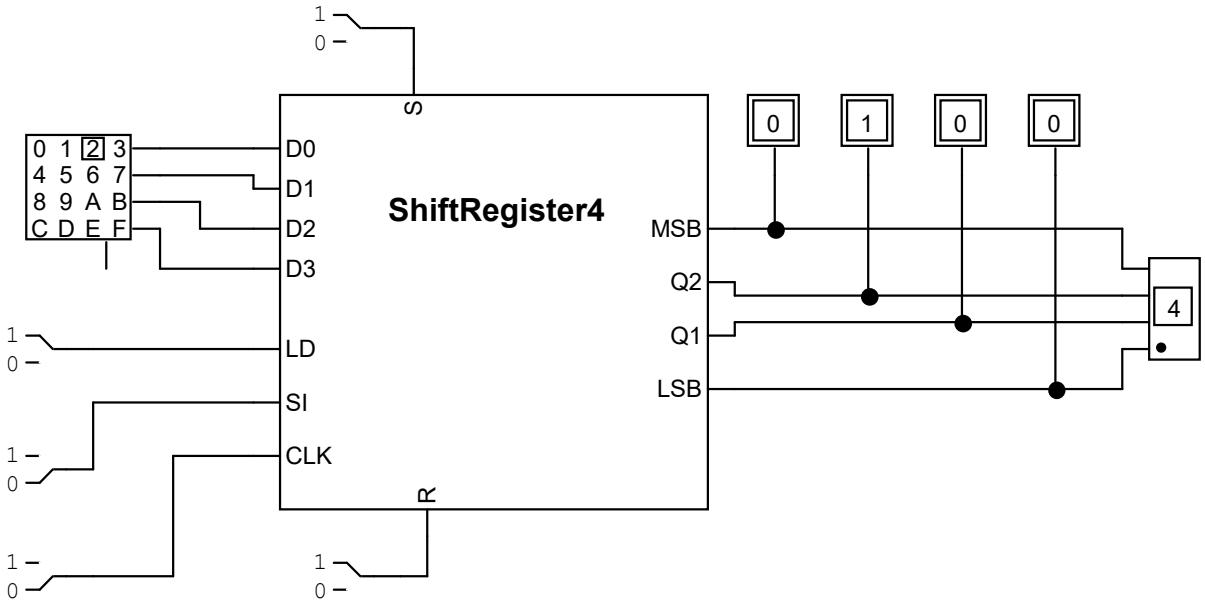

LSB
Q1
Q2
MSB
S
SI
LD
R
CLK
D3
D2
D1
D0
DEV2
DEV2
DEV2
DEV2
D
S
Q
C
R
Q

Testing Circuit of the 4-bit right shift register

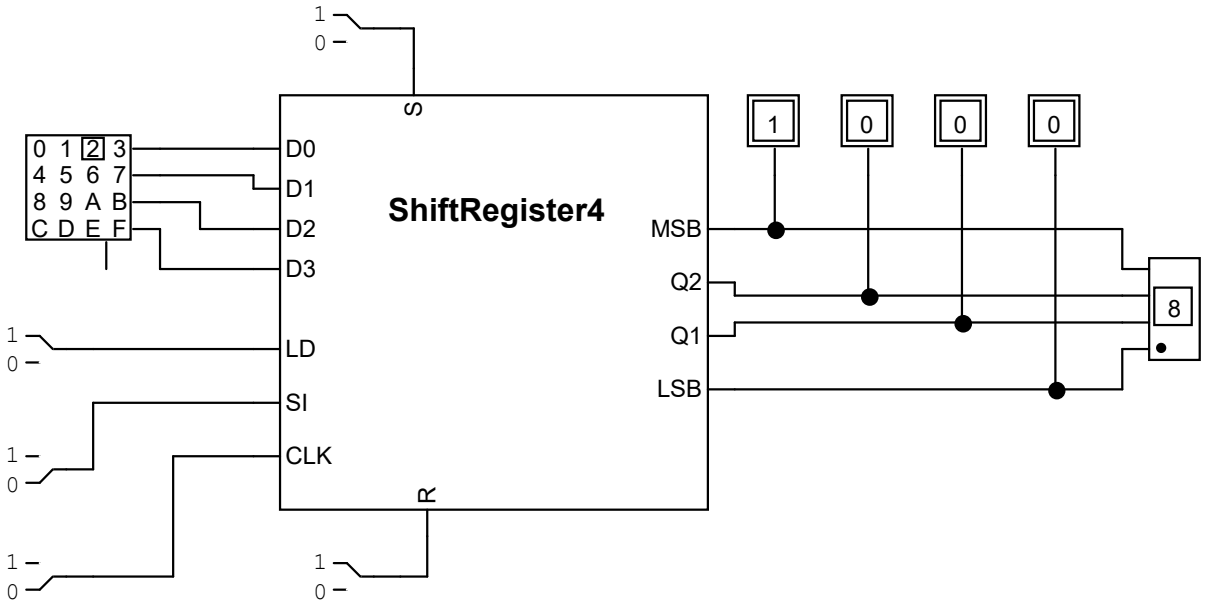
Load Mode (Storing Input)

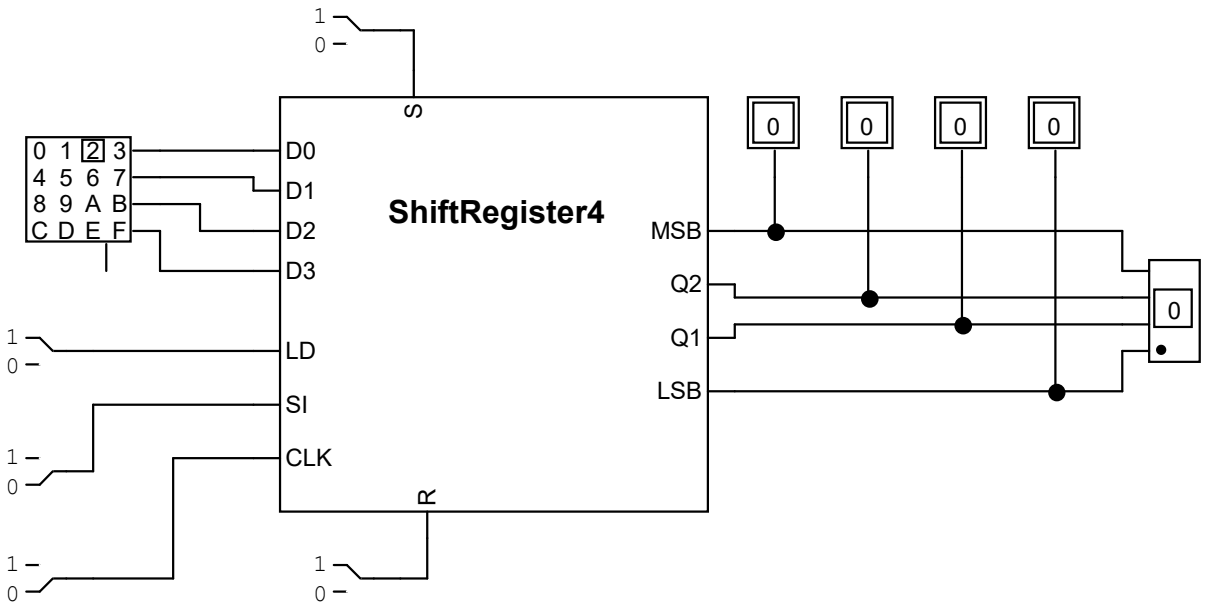


Shift Mode (Shifting One-by-One)



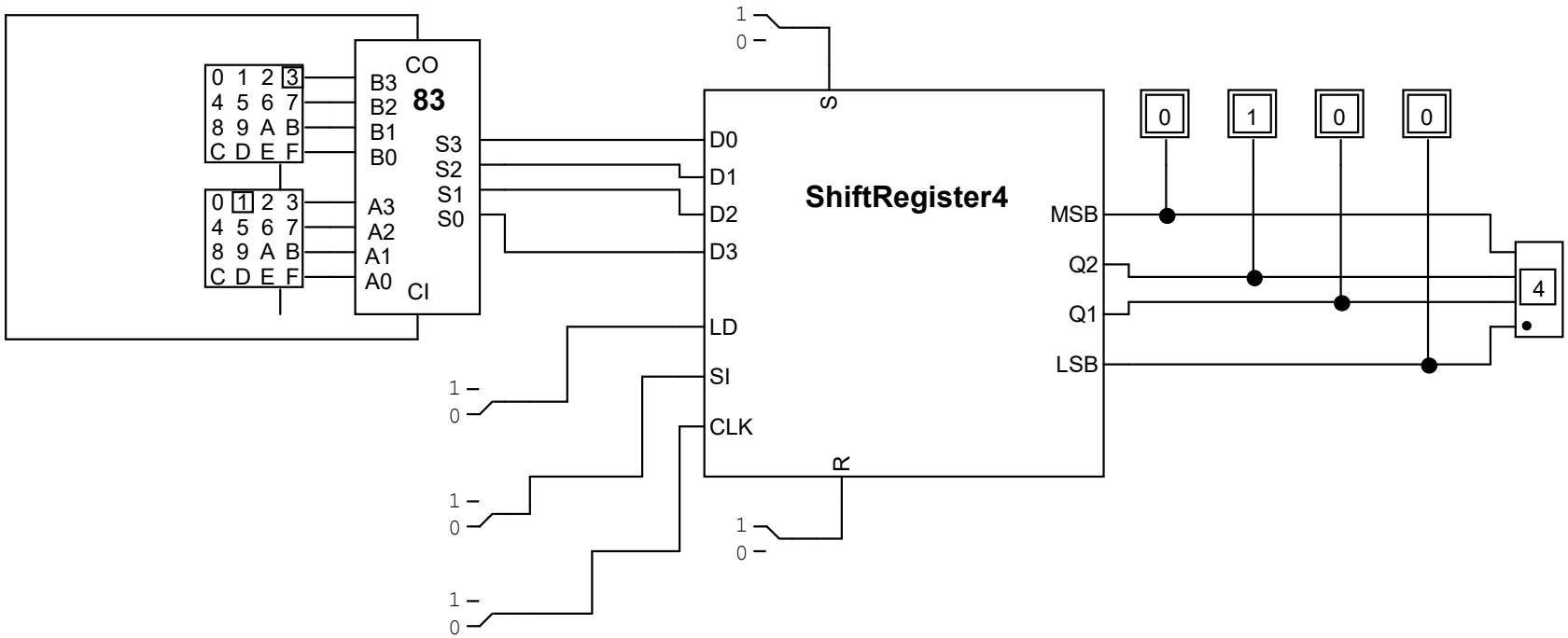
Shift Mode (Shifting One-by-One)





B = 0011
A = 0001

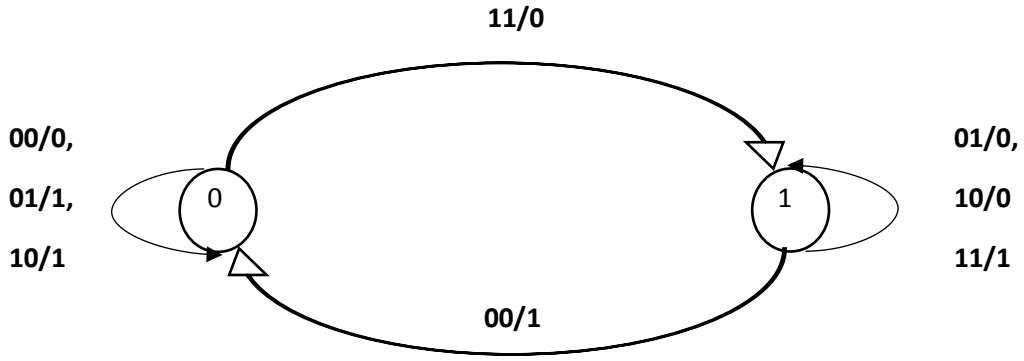
\+ 0100



- **State Table**

Present State	Input		Next State	Output
Ci	A	B	Ci+1	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- **State Diagram**



- **K – maps**

C_{i+1}

	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$C_{i+1} = AB + C_iB + C_iA$

$= AB + C_i (A + B)$

S

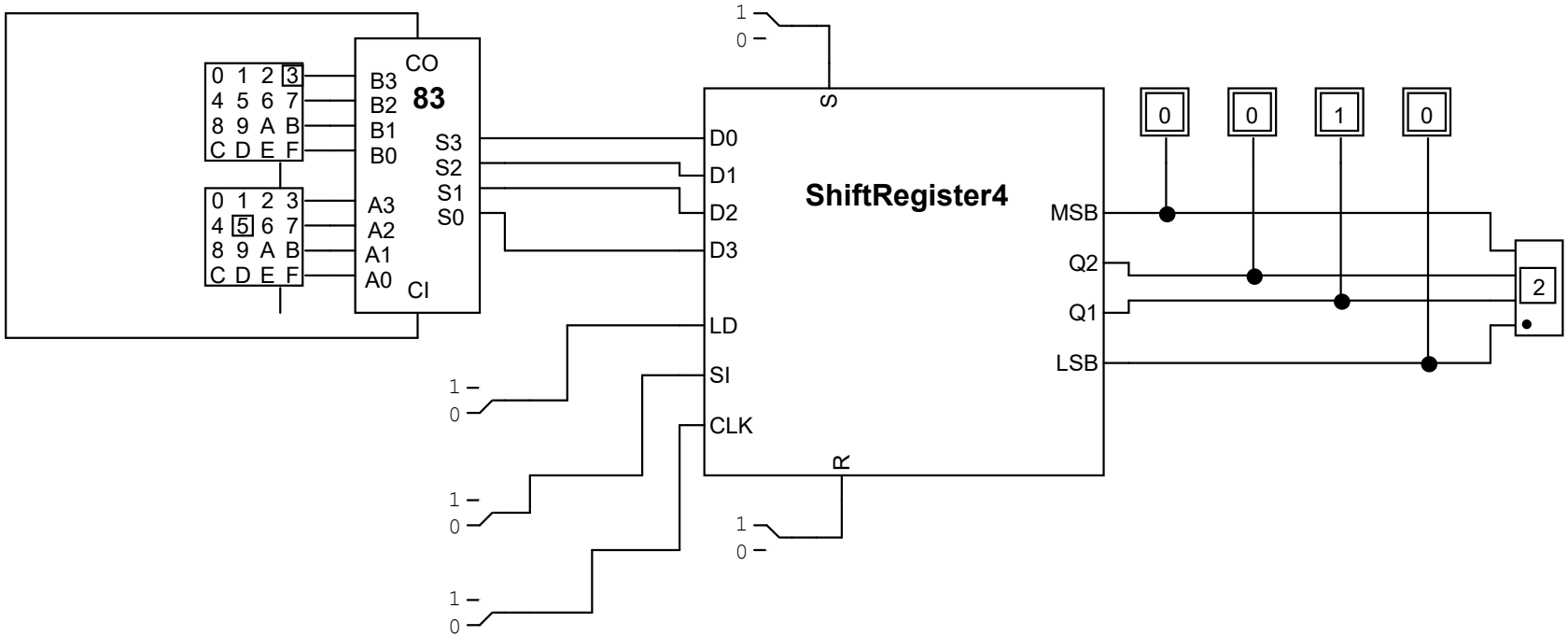
	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$S = C_i A'B' + C_i AB' + C'_i A'B + C'_i AB$

$= C_iB'(A' + A) + C_i B (A' + A)$

$= C_i$ XOR B

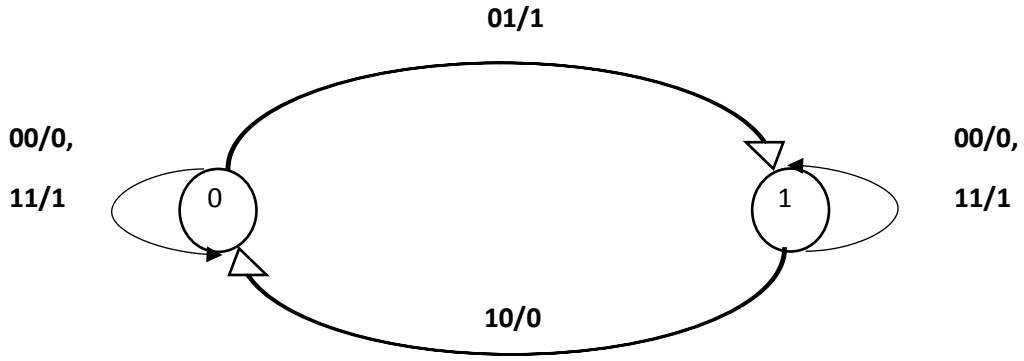
$$
\begin{array}{r}
B = 0011 \\
A = 0101 \\
\hline
+ \quad 0010
\end{array}
$$



- **State Table**

Present State	Input		Next State	Output
Ci	A	B	Ci+1	S
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

- **State Diagram**



- **K – maps**

B_{i+1}

	00	01	11	10
0	0	1	0	0
1	1	0	1	0

$B_{i+1} = B_iA'B' + B'_iA'B + B_iAB$

$= B'_iA'B + B_i$

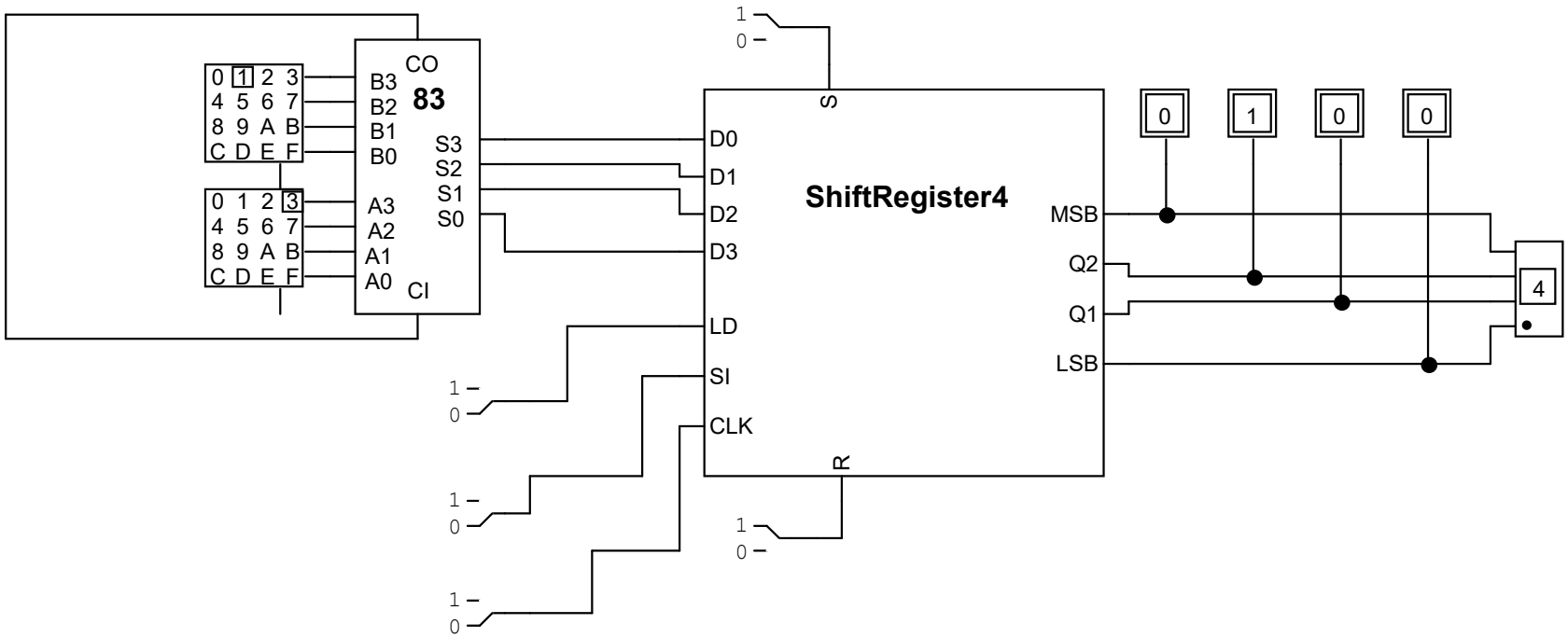
D

	00	01	11	10
0	0	1	1	1
1	1	0	1	0

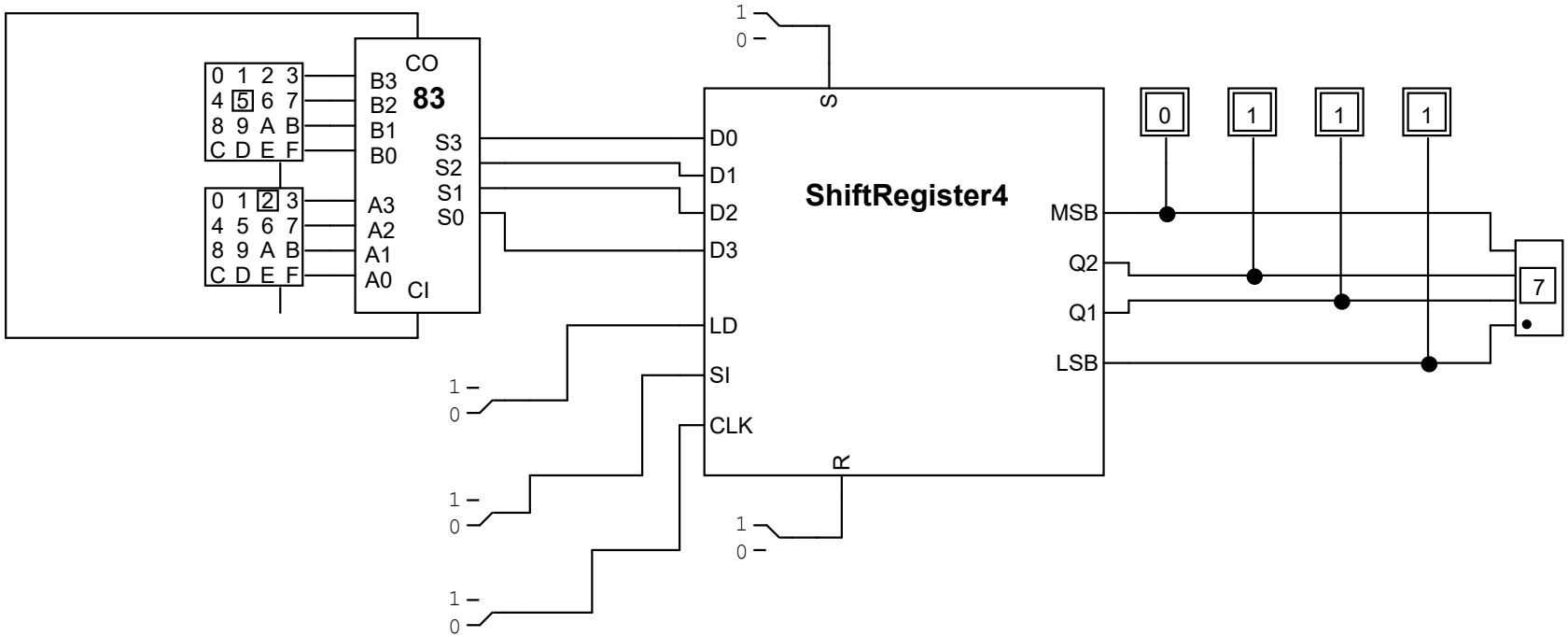
$D = B'_iB + B'_i A + AB + B'_iA'B'$

Test Cases for Q-3

B = 0001
A = 0011
\+ 0100

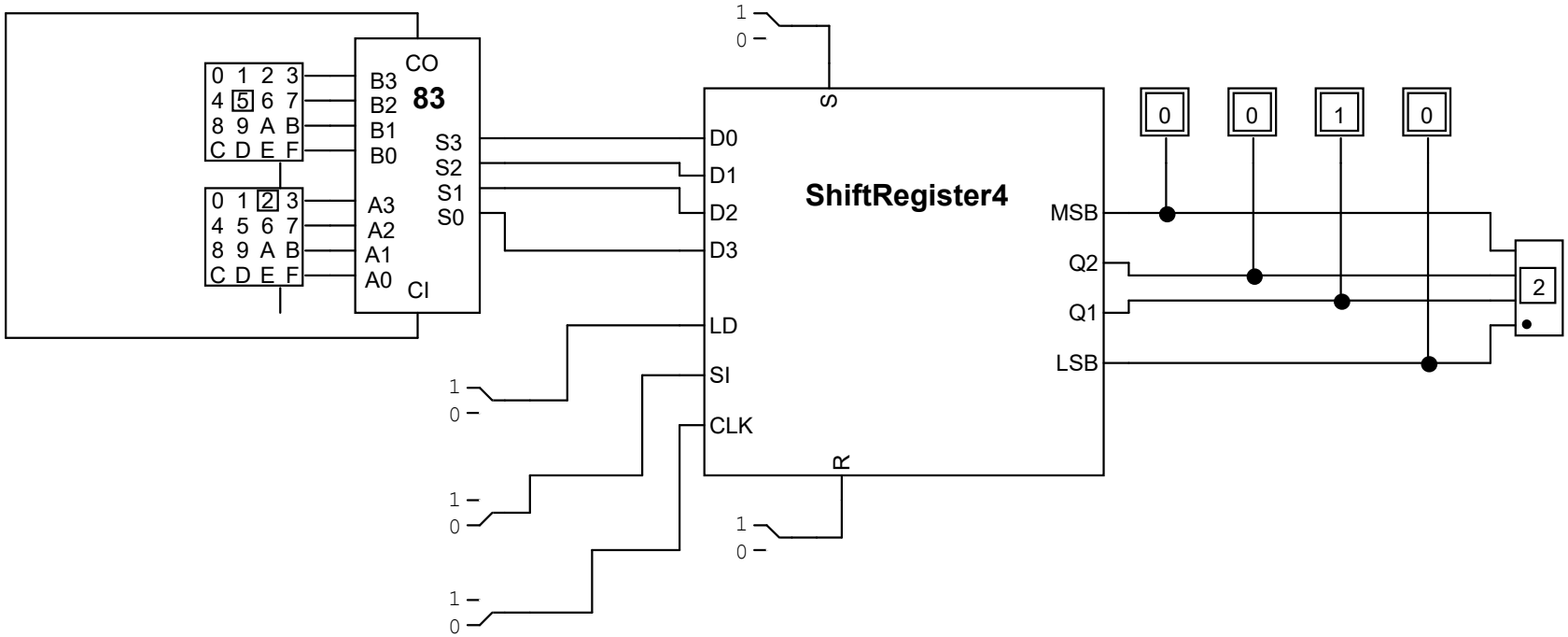


B = 0101
A = 0010
+ 0111



B = 0101
A = 0011

\- 0010



B = 0011
A = 0101
- 1010