FINAL REPORT

COMP.CE.400 System Design

Group - 18

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Overview of the System

In the following set of exercises we implemented a complete embedded system capable of capturing, encoding, streaming and playing a video. The implementation was performed using FPGA board as a major hardware component, following all actual phases of a SoC Design. Picture below is taken from slide 12 of Lecture 0, depicts the system's overview.

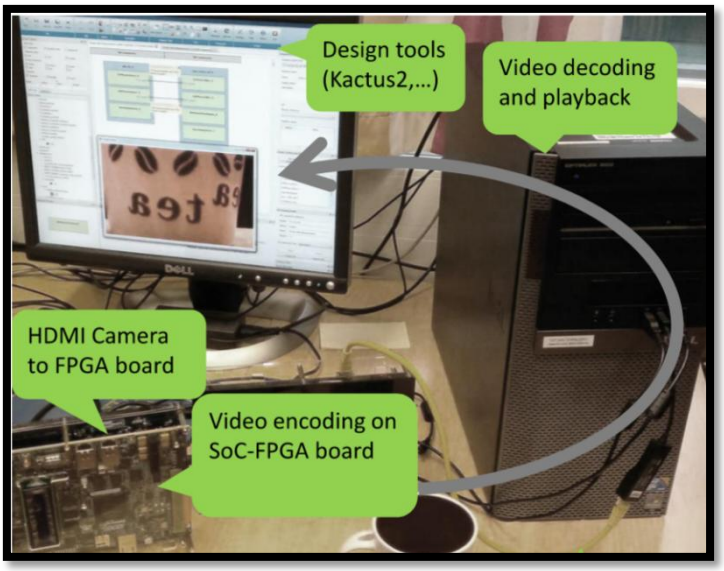

Figure 1: SOC System Overview for the Exercise

Hardware

The complete implementation uses various hardware components such as an FPGA Soc board, a camera and a PC as shown in *Figure 1.*

The FPGA SoC board used has integrated multiple IP blocks such as the **processor (ARM based), some memory, IO interface communication and some HW accelerated blocks**. All those blocks are interconnected by bus segments of different speeds and can exchange and share data by using different protocols.

Software

Choice of an operating system (OS) is **linux based**. Therefore it uses a HAL **(HW Abstraction Layer)** to do the link between the HW and the OS. The OS offers an API to programme the application. Here the application is **Kvazaar** and it is running as a **process**. Finally the streaming is handled thanks to the SW streaming libraries and tools ffmpeg.

Summary of the Exercises

Exercise 1

In this first exercise the objectives were to get familiar with the tools used in this project like Kactus2 and the environment such as the virtual machine. We also have a first contact with Kvazaar, the open source video encoder used during this project. It consisted in profiling the application to select one function that could be a good candidate to accelerated with HW acceleration.

Exercise 2

The focus of this exercise was first of all to get familiar with SystemC. To do so we had implemented intercommunication, both timed and untimed, between process with SystemC in an already existing application. The goal here was mainly to discover modeling in SystemC.

Exercise 3

The main focuses of the exercise was to implement both task division and communication with data transfers between them. Once again we start from an existing application that we divided into different modules capable of communicate ans synchronize thanks to TLM.

Exercise 4

During this exercise we had a first taste of FPGA plateform and its associated tools. To do so we interface both the FPGA design (with Qsys) and the implementation of blinker demo application. Therefore it is the first real intercation between hardware and software during this project.

Exercise 5

This exercice aims at benchmarking various IO operations of the FPGA platform like transfer rates or available memory. Those measurements were used to estimate the performances of the final system design. Also Kvazaar was run for the first time on the FPGA platform.

Exercise 6

During this exercises we continue the performance measurements started in previous exercise but more accurately. We also profile Kvazaar while using hardware acceleration to know the percentages of each parts of the encoder. The last step consisted in evaluating the performances needed for real time encoding at 25fps in full HD.

Exercise 7

Here in this exercice we implemented the hardware accelerated Kvazaar design with Qsys and then connected to the rest of the design using Kactus2. We finished by testing the HW design with both the Kvazaar HW accelerator driver and with a camera driver used in an userspace application.

Exercise 8

In this final exercise, we profile the hardware accelerated Kvazaar driver used in previous exercise. Finally we test the streaming functionnality both from files and from Kvazaar output directly to the PC.

Suggestions and Feedback

What did we learn?

We learn a lot of things in this exercises. We followed the roadmap of Soc development while implementing a video encoder system based on Kvazaar. Therefore we learn various skills such as modelling systems, measuring performance, integration of HW and SW and basics of SystemC and linux driver.

What was Easy/Hard?

Globally the exercices were not too difficult because the instructions were very clear for each exercices. However most of the tasks were time consuming. It might be nice to have more planned exercices session per week as the current scheduling does not reflect the actual work required. It also could be useful because one won't need to wait a week to ask question(s) to staff.

What Needs Improvement?

Some of the FPGAs were not working properly (broken camera, screen or both) and it was annoying to use them especially in the last exercices.