# TPS568330 4.5-V to 23-V Input, 8-A Synchronous Step-Down Voltage Regulator

*TI Information — Selective Disclosure*

## 1 Features

- Input Voltage Range: 4.5 V to 23 V
- D-CAP3™ Architecture Control for Fast Transient Response
- Output Voltage Range: 0.6 V to 7 V
- 1% Feedback Voltage Accuracy (25°C)
- Continual Output Current: 8 A
- Integrated 19.5-mΩ / 9.5-mΩ $R_{DS(on)}$ Internal Power Switch
- ULQ™ Operation to Enable Long Battery Life During System Standby
- Eco-Mode™/OOA/FCCM Mode Selectable for Light Load Running by MODE Pin
- 600 kHz/800 kHz/1MHz Selectable Switching Frequency by MODE Pin
- OOA Light Load Operation with Switching Frequency over 25 kHz
- Large Duty Operation Support
- Adjustable Soft Start Time by SS Pin
- Power Good Indicator
- Built-in Output Discharge Function
- Cycle-by-Cycle Over Current Protection
- Non-Latched for OC/OV/UV/OT/UVLO Protections
- Small 3.0-mm × 3.0-mm HotRod™ QFN Package

## 2 Applications

- DTV and STB, Server and Storage
- Telecom & Networking, Point-of-Load (POL)
- IPCs, Factory Automation
- Distributed Power Systems

## 3 Description

The TPS568330 is a cost effective, high-voltage input, high efficiency synchronous buck converter with integrated FETs.

The key feature of the TPS568330 is its ULQ™ (Ultra Low Quiescent) feature to enable low-bias current and large duty operation. The ULQ™ feature is extremely beneficial for long battery life in low power operation. The TPS568330 operates with supply input voltage ranging from 4.5V to 23V. It uses DCAP3™ control mode to provide a fast transient response, good line, load regulation, no requirement for external compensation, and supports low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors.

The TPS568330 provides complete protection OVP, UVP, OCP, OTP and UVLO. It is combined power good signal and output discharge function.

MODE pin in TPS568330 can be used to set Eco-mode™, OOA mode or FCCM mode for light load operation. And OOA mode operations with switching frequency larger than 25 kHz even no loading.

The TPS568330 supports both internal and external soft-start time option. It has the internal fixed soft-start time 1.3 ms, if the application needs longer soft-start time, the external SS pin can be used to achieve it by connecting the external capacitor.

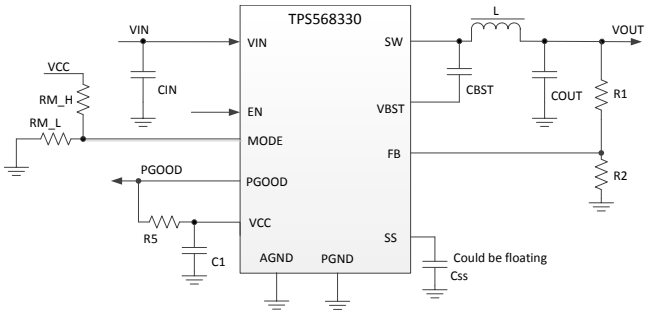
The TPS568330 is available in a 20-pin 3.0-mm x 3.0-mm HotRod™ package and the junction temperature is specified from -40°C to 125°C.

**Device Information(1)**

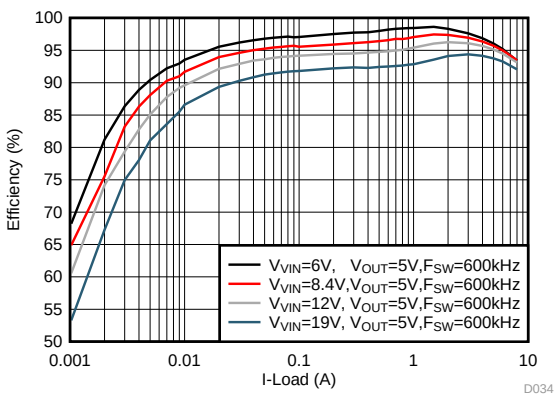
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS568330 | VQFN (20) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application**




**Efficiency vs Output Current ECO-mode**



# Table of Contents



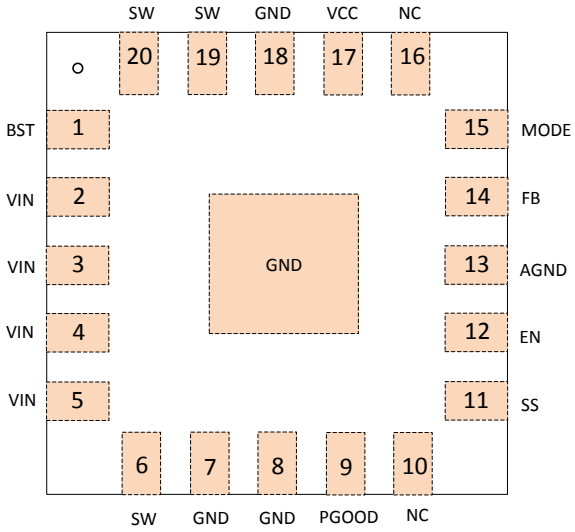
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| September 2018 | A | Initial release. |

# 5 Pin Configuration and Functions

**RJE Package**
**20-Pin VQFN**
**Top View**




## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BST | 1 | I | Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW, 0.1uF is recommended. |
| VIN | 2,3,4,5 | P | Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and GND. |
| SW | 6,19,20 | O | Switch node terminal. Connect the output inductor to this pin. |
| GND | 7,8,18,Pad | G | Power GND terminal for the controller circuit and the internal circuitry. |
| PGOOD | 9 | O | Open drain power good indicator. It is asserted low if output voltage is out of PGOOD threshold, over voltage or if the device is under thermal shutdown, EN shutdown or during soft start. |
| SS | 11 | I | Soft-start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the soft-start time is about 1.3ms. |
| NC | 10,16 | | Not connect. Can be connected to GND plane for better thermal achieved. |
| EN | 12 | I | Enable pin of buck converter. EN pin is a digital input pin, decides turn on or off buck converter. Internal pull down current to disable converter if leave this pin open. |
| AGND | 13 | G | Ground of internal analog circuitry. Connect AGND to GND plane with a short trace. |
| FB | 14 | I | Converter feedback input. Connect to the center tap of the resistor divider between output voltage and AGND. |
| MODE | 15 | I | Switching frequency and light load operation mode selection pin. Connect this pin to a resistor divider from VCC and AGND, the different MODE options are shown in Table 1 |
| VCC | 17 | O | 5.0-V internal VCC LDO output. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 1-μF capacitor. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN | –0.3 | 26 | V |
| | VBST | –0.3 | 31 | V |
| | VBST-SW | –0.3 | 6 | V |
| | EN, MODE, FB, SS | –0.3 | 6 | V |
| | PGND, AGND | –0.3 | 0.3 | V |
| Output voltage | SW | –2 | 26 | V |
| | SW (10-ns transient) | –3 | 28 | V |
| | PGOOD | –0.3 | 6 | V |
| $T_J$ | Operating junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22- V C101 (2) | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN | 4.5 | 23 | V |
| | VBST | –0.3 | 28 | V |
| | VBST-SW | –0.3 | 5.5 | V |
| | EN, MODE, FB, SS | –0.3 | 5.5 | V |
| | PGND, AGND | –0.3 | 0.3 | V |
| Output voltage | SW | –2 | 24 | V |
| | SW (10-ns transient) | –3 | 26 | V |
| | PGOOD | –0.3 | 5.5 | V |
| $I_{OUT}$ | Output current | | 8 | A |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TPS568330 RJE (VQFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 44.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 32.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

## Thermal Information (continued)

| THERMAL METRIC(1) | | TPS568330 RJE (VQFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 16.1 | °C/W |

## 6.5 Electrical Characteristics

$T_J$ =-40°C to 125°C, $V_{VIN}$ = 12 V, unless otherwise noted

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| VIN | Input voltage range | VIN | 4.5 | | 23 | V |
| $I_{VIN}$ | $V_{IN}$ supply current | No load, $V_{EN}$=5V,switching | | 110 | | uA |
| $I_{VINSDN}$ | Shutdown supply current | No load, $V_{EN}$=0V | | 2 | | uA |
| **VCC OUTPUT** | | | | | | |
| $V_{CC}$ | VCC output voltage | $V_{VIN}$>5.0V | 4.85 | 5 | 5.15 | V |
| | | $V_{VIN}$=4.5V | | 4.5 | | |
| $I_{CC}$ | VCC current limit | | 20 | | | mA |
| **FEEDBACK VOLTAGE** | | | | | | |
| $V_{FB}$ | FB voltage | $T_J$ = 25°C | 594 | 600 | 606 | mV |
| | | $T_J$ = -40°C to 125°C | 592 | 600 | 611 | mV |
| **DUTY CYCLE AND FREQUENCY CONTROL** | | | | | | |
| $F_{SW}$ | Switching frequency | $T_J$ = 25°C , Set MODE with $F_{SW}$=600kHz,$V_{OUT}$=5V | | 600 | | kHz |
| $T_{ON(MIN)}$ | Minimum on time | $T_J$ = 25°C | | 60 | | ns |
| $T_{OFF(MIN)}$ | Minimum off time | $T_J$ = 25°C, $V_{FB}$ = 0.5 V | | | 190 | ns |
| **MOSFET AND DRIVERS** | | | | | | |
| $R_{DS(ON)H}$ | High side switch resistance | $T_J$ = 25°C | | 19.5 | | mΩ |
| $R_{DS(ON)L}$ | Low side switch resistance | $T_J$ = 25°C | | 9.5 | | mΩ |
| **OOA FUNCTION** | | | | | | |
| $T_{OOA}$ | OOA mode operation period | | | 28 | | us |
| **OUTPUT DISCHARGE AND SOFT START** | | | | | | |
| $R_{DIS}$ | Discharge resistance | $T_J$=25°C, $V_{EN}$=0V | | 420 | | Ω |
| $T_{SS}$ | Soft start time | Internal soft-start time,SS floating | | 1.3 | | ms |
| $I_{SS}$ | Soft start charge current | | | 5 | | uA |
| **POWER GOOD** | | | | | | |
| $T_{PGDLY}$ | PG start-up delay | PG from low to high | | 1 | | ms |
| $V_{PGTH}$ | PG threshold | VFB falling (fault) | | 85 | | % |
| | | VFB rising (good) | | 90 | | % |
| | | VFB rising (fault) | | 115 | | % |
| | | VFB falling (good) | | 110 | | % |
| $V_{PG}$ | PG sink current capability | $I_{OL}$ =4mA | | | 0.4 | V |
| $I_{PGLK}$ | PG leak current | $V_{PGOOD}$ =5.5V | | | 1 | uA |
| **CURRENT LIMIT** | | | | | | |
| $I_{OCL}$ | Over current threshold | Valley current set point | 8.1 | 9.8 | 11.3 | A |
| $I_{NOCL}$ | Negative over current threshold | | | 3.9 | | A |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN high-level input voltage | | 1.21 | 1.31 | 1.4 | V |
| $V_{ENL}$ | EN low-level input voltage | | 0.95 | 1.12 | 1.19 | V |
| $I_{EN}$ | Enable internal pull down current | $V_{EN}$=0.8V | | 2 | | µA |

## Electrical Characteristics (continued)

$T_J$ =-40°C to 125°C, $V_{VIN}$ = 12 V, unless otherwise noted

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | OVP trip threshold | | | 125 | | % |
| $t_{OVPDLY}$ | OVP prop deglitch | $T_J$=25°C | | 20 | | us |
| $V_{UVP}$ | UVP trip threshold | | | 60 | | % |
| $t_{UVPDLY}$ | UVP prop deglitch | | | 256 | | us |
| $T_{UVPDEL}$ | Output hiccup delay relative to SS time | | | 256 | | us |
| $T_{UVPEN}$ | Output hiccup enable delay relative to SS time | | | 7 | | cycle |
| **UVLO** | | | | | | |
| $V_{UVLOVIN}$ | VIN UVLO threshold | Wake up | | 4.2 | 4.4 | V |
| | | Shutdown | 3.6 | 3.8 | | V |
| | | Hysteresis | | 0.4 | | V |
| **OVER TEMPERATURE PROTECTION** | | | | | | |
| $T_{OTP}$ | OTP trip threshold(1) | Shutdown temperature | | 150 | | °C |
| $T_{OTPHSY}$ | OTP hysteresis(1) | Hysteresis | | 20 | | °C |

(1) Not production tested

## 6.6 Typical Characteristics

$T_J$=-40°C to 125°C, $V_{VIN}$=12V(unless otherwise noted)

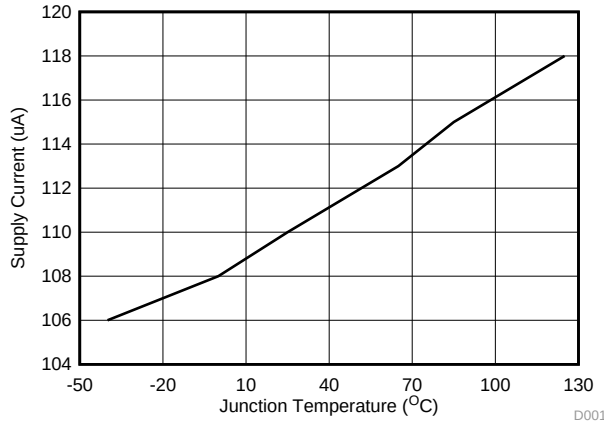



**Figure 1. Supply Current vs Junction Temperature**

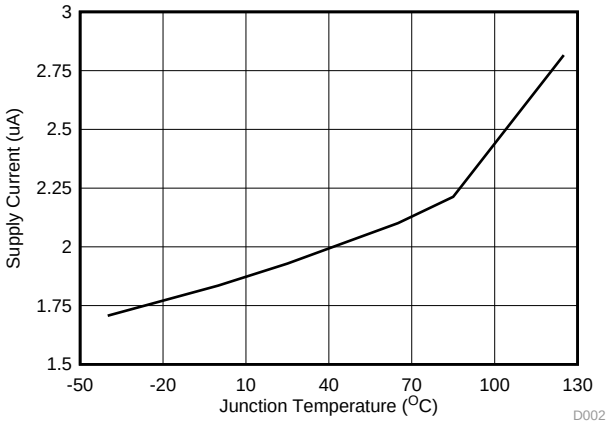



**Figure 2. Shutdown Current vs Temperature**

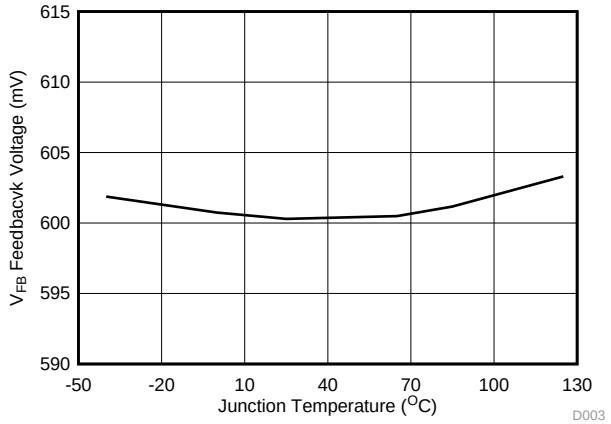



**Figure 3. Feedback Voltage vs Junction Temperature**

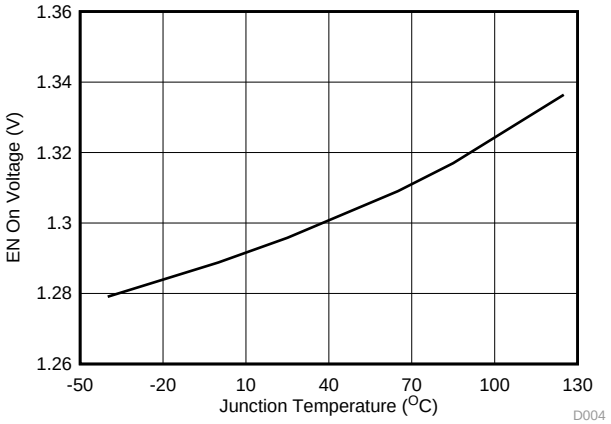



**Figure 4. Enable On Voltage vs Junction Temperature**

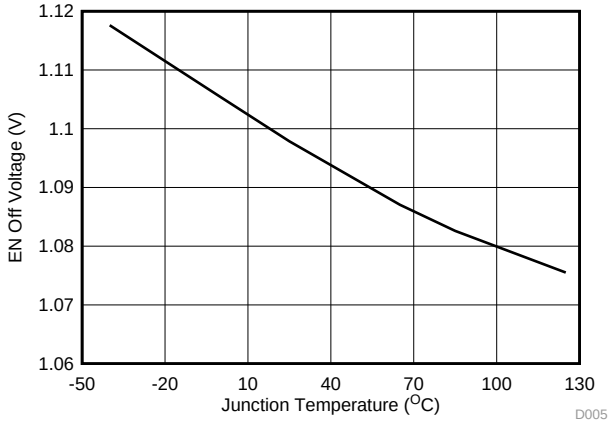



**Figure 5. Enable Off Voltage vs Junction Temperature**

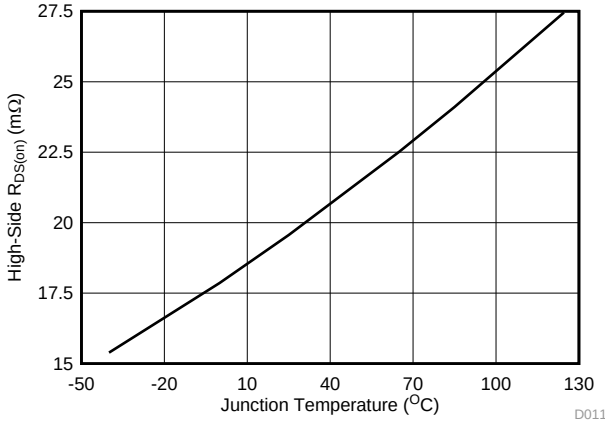



**Figure 6. High-Side $R_{DS}$(on) vs Junction Temperature**

## Typical Characteristics (continued)

$T_J$=-40°C to 125°C, $V_{VIN}$=12V(unless otherwise noted)

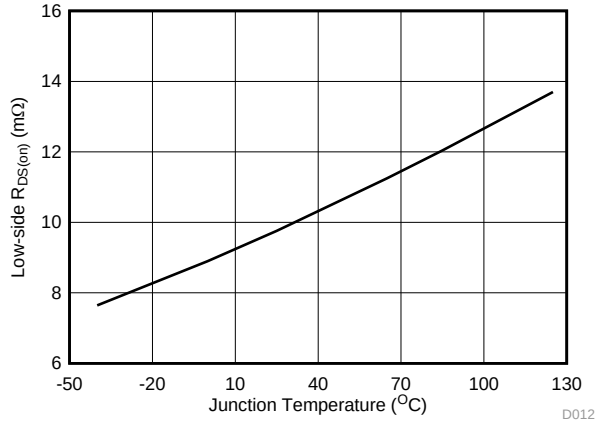



**Figure 7. Low-Side $R_{DS(on)}$ vs Junction Temperature**

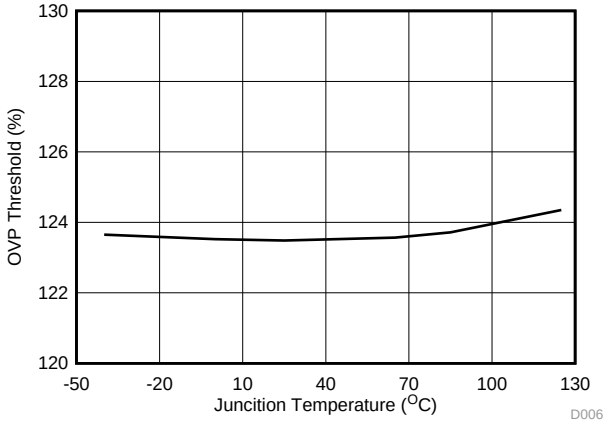



**Figure 8. OVP Threshold vs Junction Temperature**

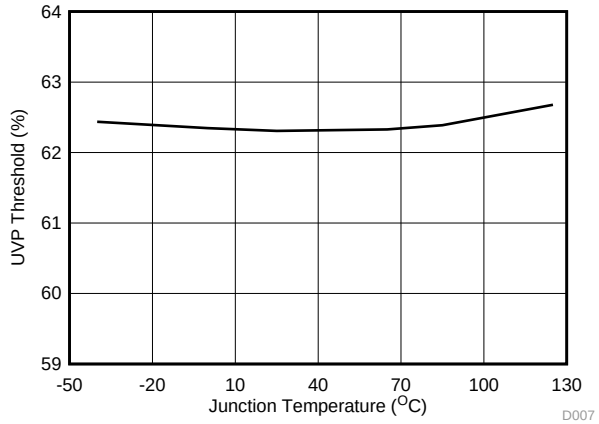



**Figure 9. UVP Threshold vs Junction Temperature**

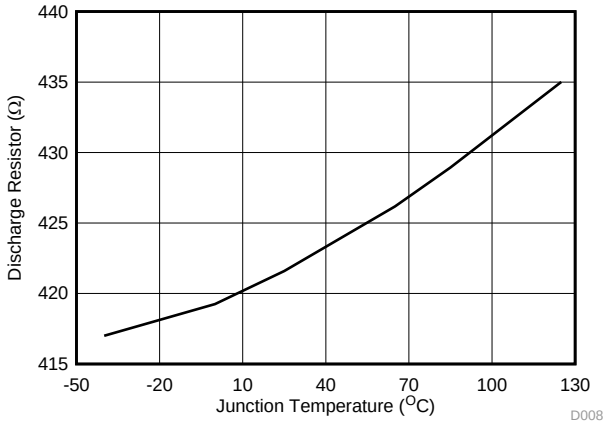



**Figure 10. Discharge Resistor vs Junction Temperature**

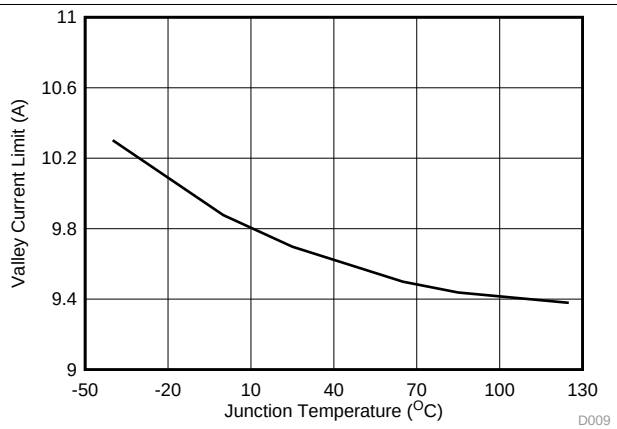



**Figure 11. Valley Current Limit vs Junction Temperature**

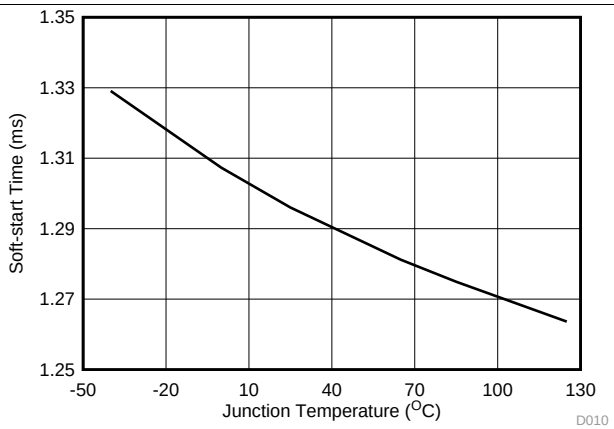



**Figure 12. Soft-Start Time vs Junction Temperature**

## Typical Characteristics (continued)

$T_J$=-40°C to 125°C, $V_{VIN}$=12V(unless otherwise noted)

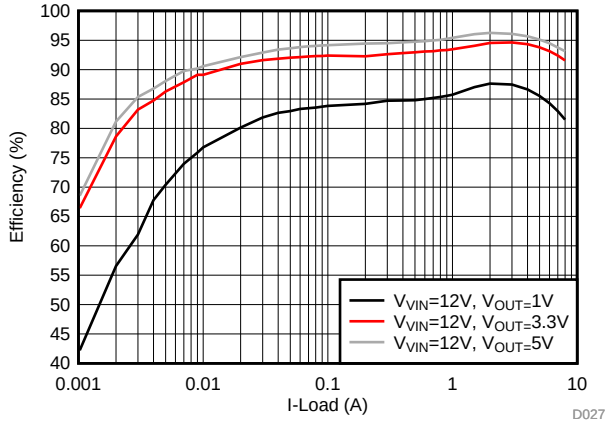



**Figure 13. Efficiency, Eco-mode, $F_{SW}$ = 600 kHz**

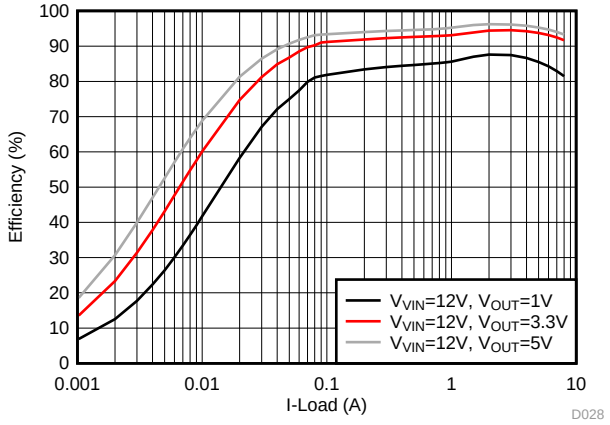



**Figure 14. Efficiency, OOA-mode, $F_{SW}$ = 600 kHz**

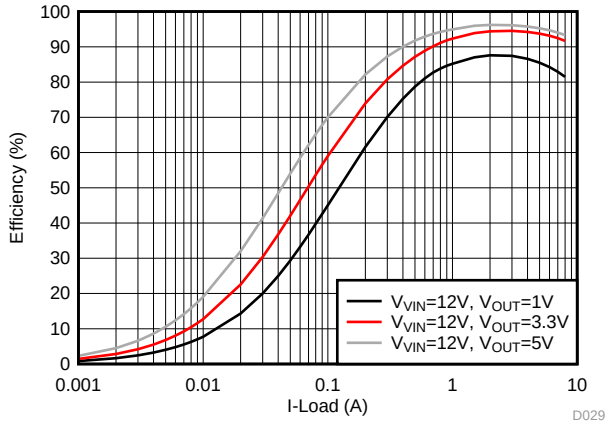



**Figure 15. Efficiency, FCCM, $F_{SW}$ = 600 kHz**

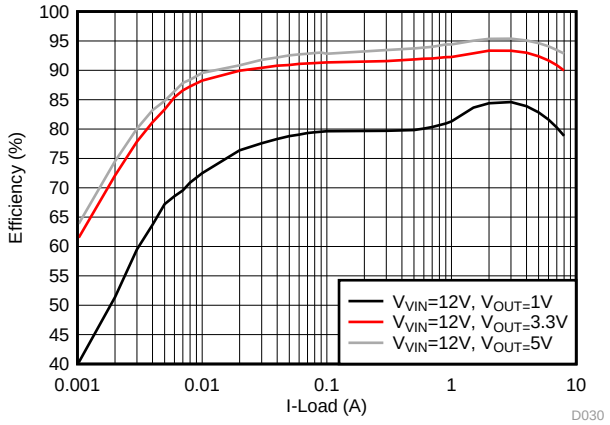



**Figure 16. Efficiency, Eco-mode, $F_{SW}$ = 1 MHz**

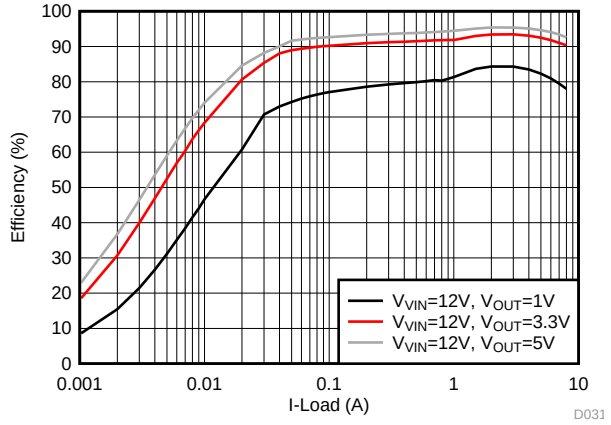



**Figure 17. Efficiency, OOA-mode, $F_{SW}$ = 1 MHz**

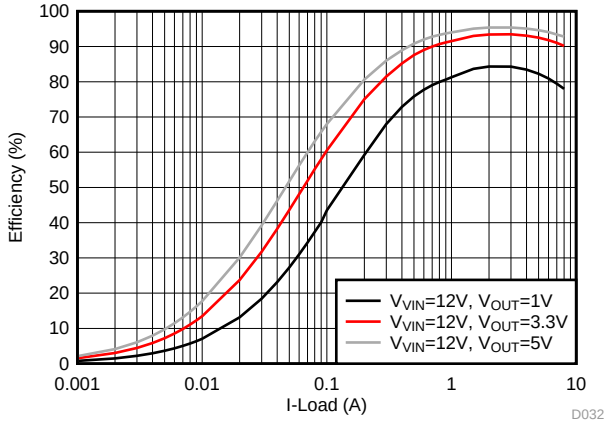



**Figure 18. Efficiency, FCCM, $F_{SW}$ = 1 MHz**

## Typical Characteristics (continued)

$T_J$=-40°C to 125°C, $V_{VIN}$=12V(unless otherwise noted)

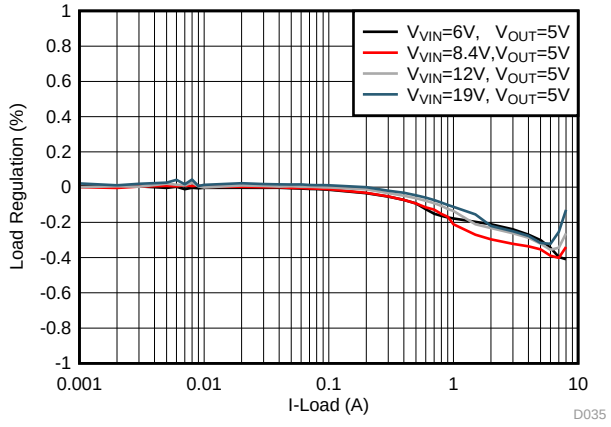



**Figure 19. Load Regulation, Eco-mode, $F_{SW}$ = 600 kHz**

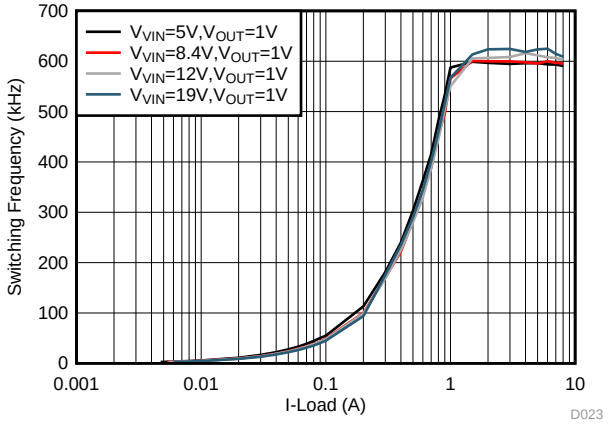



**Figure 20. $F_{SW}$ Load Regulation, Eco-mode, $F_{SW}$ = 600 kHz**

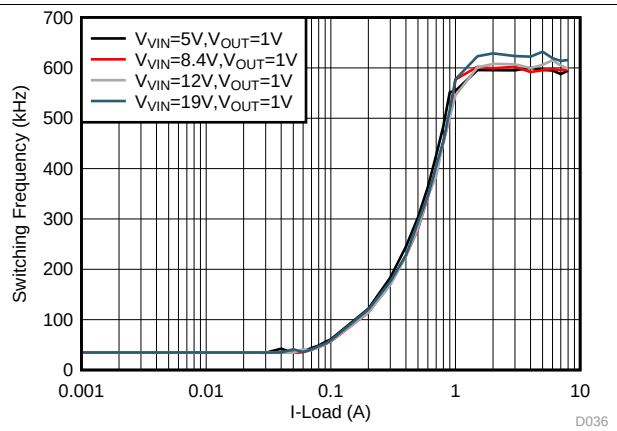



**Figure 21. $F_{SW}$ Load Regulation, OOA-mode, $F_{SW}$ = 600 kHz**

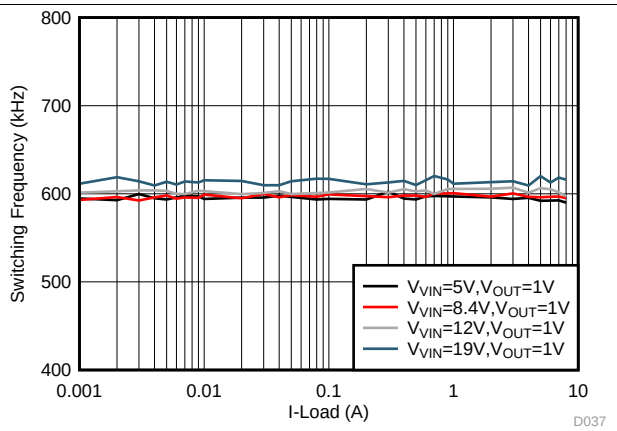



**Figure 22. $F_{SW}$ Load Regulation, FCCM, $F_{SW}$ = 600 kHz**

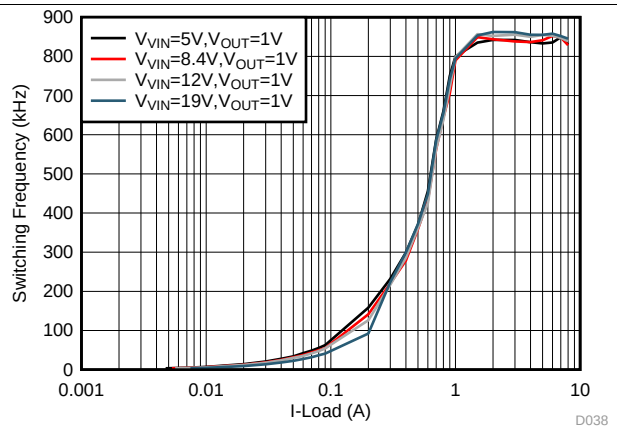



**Figure 23. $F_{SW}$ Load Regulation, Eco-mode, $F_{SW}$ = 800 kHz**

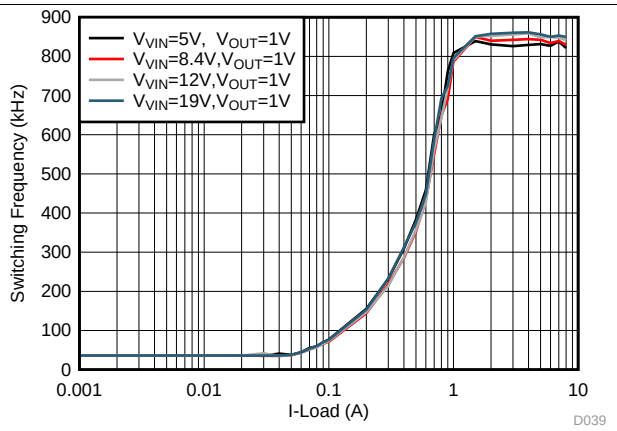



**Figure 24. $F_{SW}$ Load Regulation, OOA-mode, $F_{SW}$ = 800 kHz**

## Typical Characteristics (continued)

$T_J$=-40°C to 125°C, $V_{VIN}$=12V(unless otherwise noted)

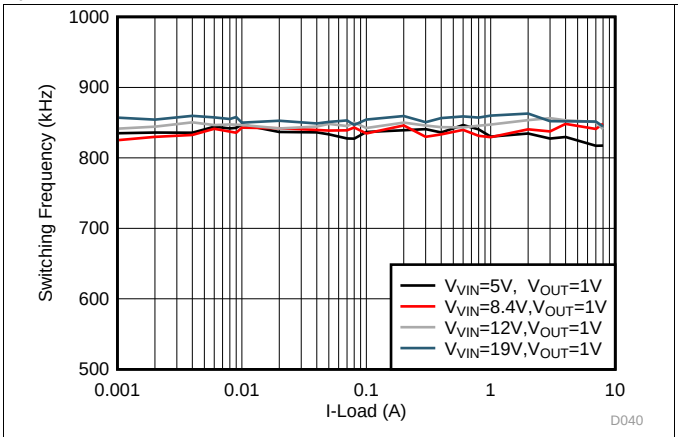



**Figure 25. $F_{SW}$ Load Regulation, FCCM, $F_{SW}$ = 800 kHz**

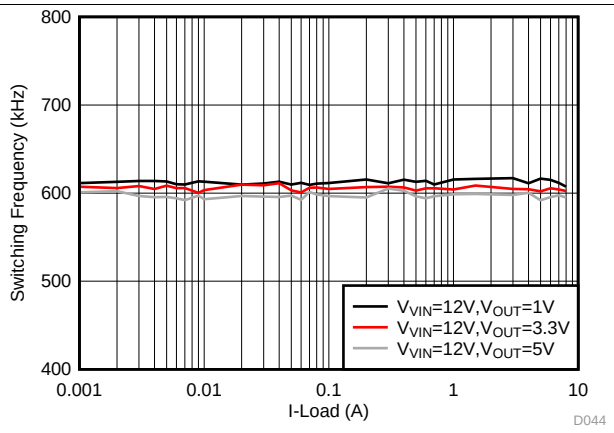



**Figure 26. $F_{SW}$ Load Regulation, FCCM, $F_{SW}$ = 600 kHz**

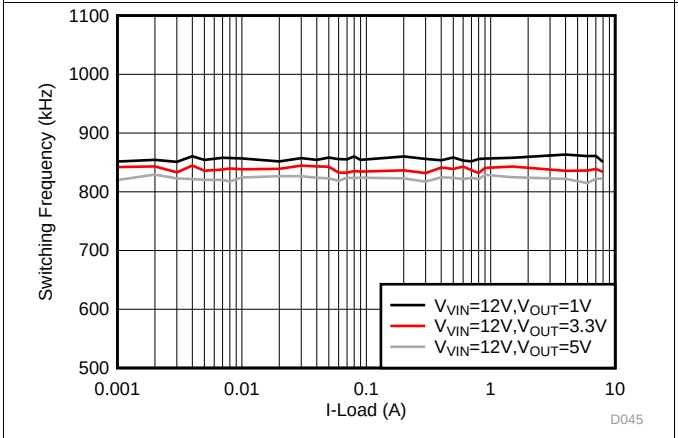



**Figure 27. $F_{SW}$ Load Regulation, FCCM, $F_{SW}$ = 800 kHz**

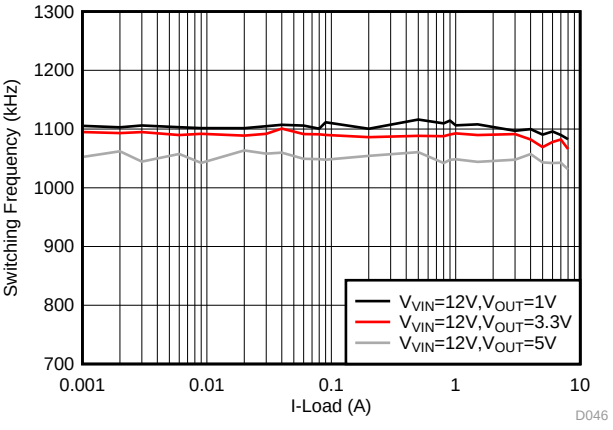


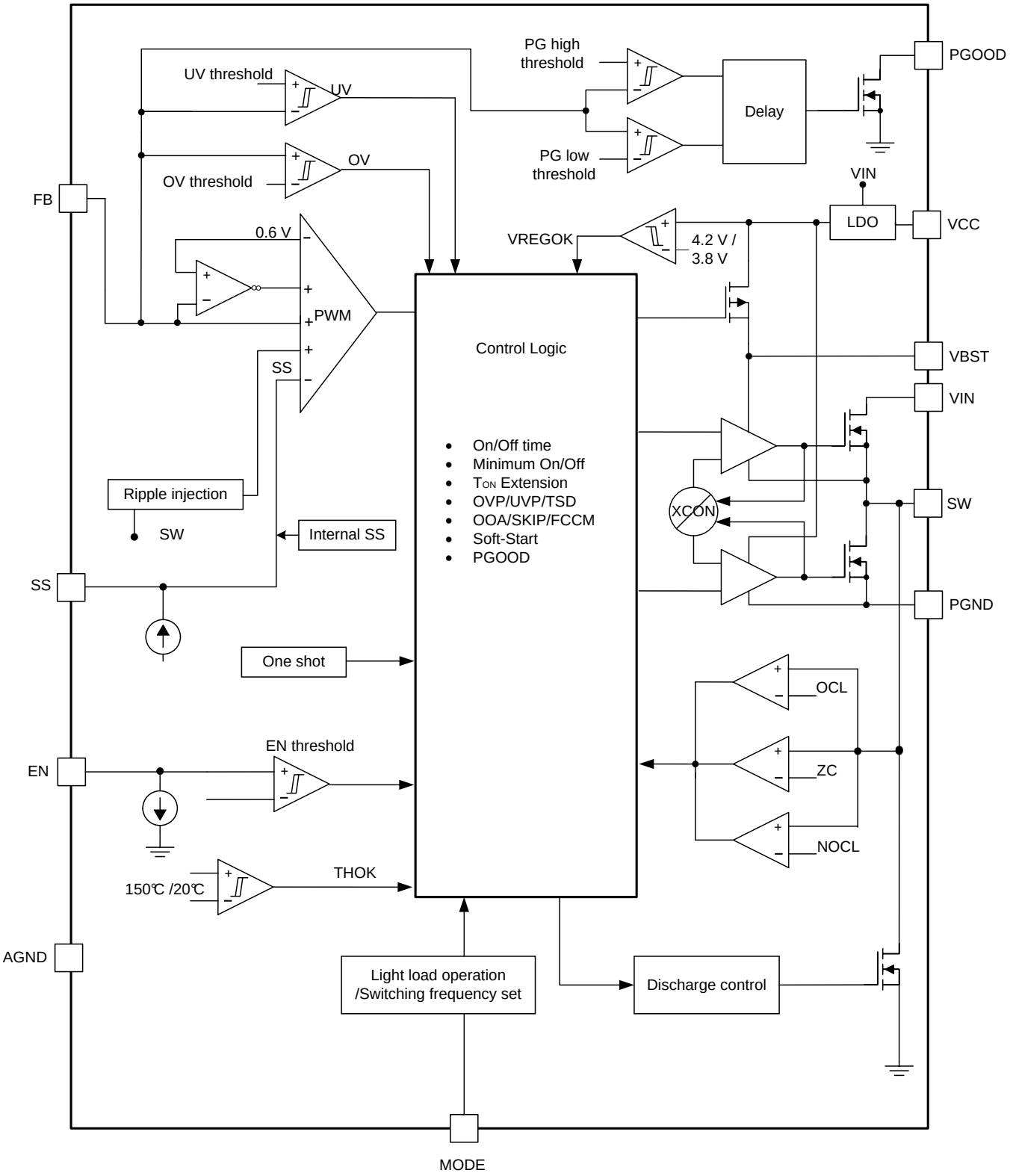

**Figure 28. $F_{SW}$ Load Regulation, FCCM, $F_{SW}$ = 1 MHz**

# 7 Detailed Description

## 7.1 Overview

The TPS568330 is 8-A integrated FET synchronous buck converter which operates from 4.5V to 23V input voltage ($V_{IN}$), and the output is from 0.6V to 7V. The proprietary D-CAP3™ mode enables low external component count, ease of design, optimization of the power design for cost, size and efficiency. The key feature of the TPS568330 is ultra-low quiescent current (ULQ™) mode. This feature is beneficial for long battery life in system standby mode. The device employs D-CAP3™ mode control that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition. Eco-mode™ allows the TPS568330 to maintain high efficiency at light load. OOA (out of audio) mode makes switching frequency above audible frequency larger than 25 kHz, even there is no loading at output side. FCCM mode has the constant switching frequency at both light and heavy load. The TPS568330 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the buck is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS568330 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, $V_{OUT}$, and is inversely proportional to the converter input voltage, $V_{IN}$, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS568330 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in Equation 1.

$$f_p = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS568330. The low-frequency L-C double pole has a 180 degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is related to the switching frequency. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency ($F_{SW}$).

### 7.3.2 Soft Start

The TPS568330 has an internal 1.3-ms soft start, and also an external SS pin is provided for setting higher soft-start time if needed. When the EN pin becomes high, the soft-start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a larger soft start time, it can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current ($I_{SS}$) begins charging the external capacitor ($C_{SS}$) connected between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time ($T_{SS}$) is shown in Equation 2:

$$T_{ss} = \frac{C_{ss}(nF) \times V_{REF}(V)}{I_{ss}(\mu A)} \quad (2)$$

where

- $V_{REF}$ is 0.6 V and $I_{SS}$ is 5 μA

### 7.3.3 Large Duty Operation

The TPS568330 can support large duty operations by its internal $T_{ON}$ extension function. When the $V_{IN}/V_{OUT}$ <1.6, and the $V_{FB}$ is lower than internal $V_{REF}$, the $T_{ON}$ will be extended to implement the large duty operation and also improve the performance of the load transient performance.

### 7.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the $V_{FB}$ is between 90% and 110% of the target output voltage, the PGOOD is de-asserted and floats after a 1-ms de-glitch time. A 100 kΩ pullup resistor is recommended to pull the voltage up to VCC. The PGOOD pin is pulled low when:

## Feature Description (continued)

- the FB pin voltage is lower than 85% or greater than 115% of the target output voltage
- in an OVP, UVP, or thermal shutdown event
- during the soft-start period.

### 7.3.5 Over Current Protection and Undervoltage Protection

The TPS568330 has the over current protection and undervoltage protection. The output over current limit (OCL) is implemented using a cycle-by-cycle valley detect circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OUT}$. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over current protection. When the load current is higher than the over current threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the device will shut off after a wait time of 256us and then re-start after the hiccup time (typically 7*Tss). When the over current condition is removed, the output will be recovered.

### 7.3.6 Over Voltage Protection

The TPS568330 has the over voltage protection feature. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, the output will be discharged after a wait time of 20 µs. When the over voltage condition is removed, the output voltage will be recovered.

### 7.3.7 UVLO Protection

Undervoltage Lockout protection (UVLO) monitors the $V_{IN}$ power input. When the voltage is lower than UVLO threshold voltage, the device is shut off and output is discharged. This is a non-latch protection.

### 7.3.8 Output Voltage Discharge

The TPS568330 has the discharge function by using internal MOSFET about 420Ω $R_{DS(on)}$, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET.

### 7.3.9 Thermal Shutdown

The TPS568330 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device is shut off and the output will be discharged. This is a non-latched protection, the device restarts switching when the temperature goes below the thermal shutdown threshold.

## 7.4 Device Functional Modes

### 7.4.1 Light Load Operation

TPS568330 has a MODE pin which can setup three different modes of operation for light load running and 600 kHz/800 kHz/1 MHz switching frequency at heavy load .The light load running includes Out-of-Audio mode , Advanced Eco-mode and Force CCM mode.

## Device Functional Modes (continued)

### 7.4.2 Advanced Eco-mode™ Control

The advanced Eco-mode™ control scheme to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode™ operation happens ( $I_{OUT(LL)}$ ) can be calculated from Equation 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

After identifying the application requirements, design the output inductance ($L_{OUT}$) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

### 7.4.3 Out of Audio Mode

Out-of-Audio (OOA) light-load mode is a unique control feature that keeps the switching frequency above audible frequency towards a virtual no-load condition. During Out-of-Audio operation, the OOA control circuit monitors the states of both high-side and low-side MOSFETs and forces them switching if both MOSFETs are off for more than 28 μs. When both high-side and low-side MOSFETs are off for more than 28 μs during a light-load condition, the lowside FET will be on for discharge till reverse OC happens or output voltage drops to trigger the high-side FET on. This mode initiates one cycle of the low-side MOSFET and the high-side MOSFET turning on. Then, both MOSFETs stay turned off waiting for another 28 μs.

If the MODE pin is selected to operate in OOA mode, when the device works at light load, the minimum switching frequency is above 25 kHz which avoids the audible noise in the system.

### 7.4.4 Force CCM Mode

Force CCM(FCCM) mode keeps the converter to operate in continuous conduction mode during light-load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency ($F_{SW}$) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

### 7.4.5 Mode Selection

The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in Table 1 . The voltage on the MODE pin can be set by connecting this pin to the center tap of a resistor divider connected between VCC and AGND. A guideline for the top resistor ($R_{M\_H}$) and the bottom resistor ($R_{M\_L}$) is shown in Table 1, and 1% resistors are recommended. It is important that the voltage for the MODE pin is derived from the VCC rail only since internally this voltage is referenced to detect the MODE option. The MODE pin setting can be reset only by a VIN power cycling or EN toggle.

**Table 1. MODE Pin Resistor Settings**

| $R_{M\_H}$(kΩ) | $R_{M\_L}$ (kΩ) | Light Load Operation | Switching Frequency (kHz) |
|---|---|---|---|
| 330 | 5.1 | Eco-mode | 600 |
| 330 | 15 | Eco-mode | 800 |
| 330 | 27 | Eco-mode | 1000 |
| 300 | 43 | OOA mode | 600 |
| 150 | 33 | OOA mode | 800 |
| 160 | 51 | OOA mode | 1000 |
| 110 | 51 | FCCM | 600 |

## Device Functional Modes (continued)

**Table 1. MODE Pin Resistor Settings (continued)**

| $R_{M\_H}$(kΩ) | $R_{M\_L}$ (kΩ) | Light Load Operation | Switching Frequency (kHz) |
|---|---|---|---|
| 75 | 51 | FCCM | 800 |
| 51 | 51 | FCCM | 1000 |

Figure 29 below shows the typical start-up sequence of the device once the enable signal crosses the EN turn on threshold. After the voltage on VCC crosses the rising UVLO threshold it takes about 500us to read the first mode setting and approximately 100us from there to finish the last mode setting. The output voltage starts ramping after the mode reading is done.

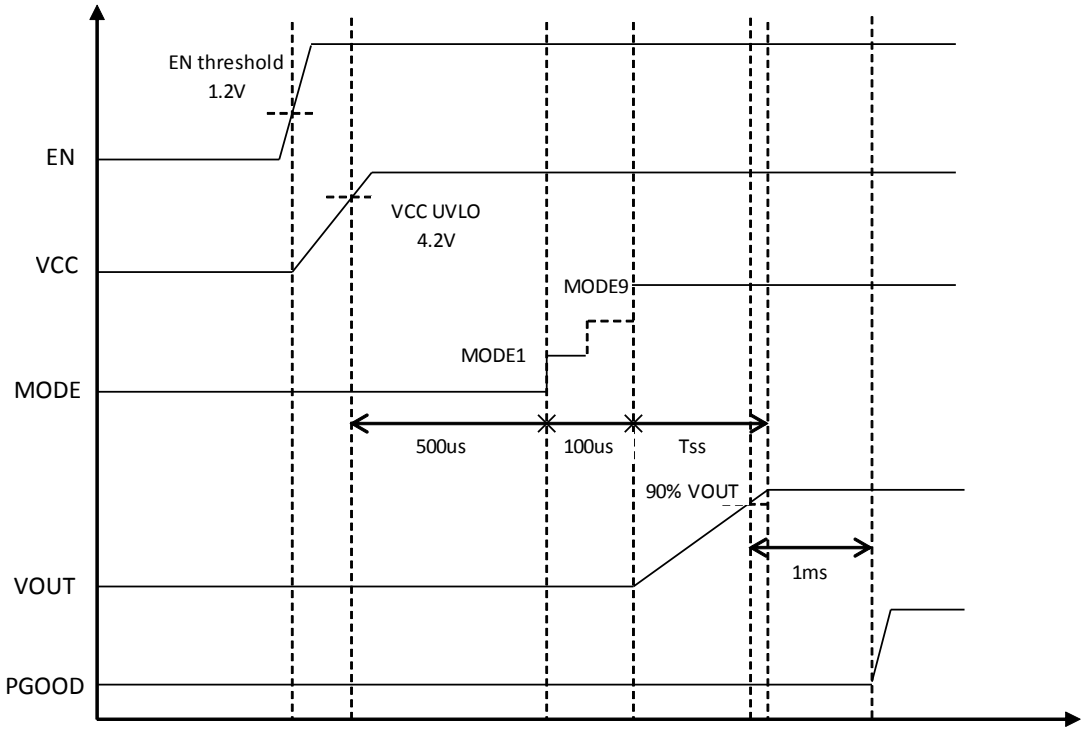



**Figure 29. Power-Up Sequence**

### 7.4.6 Standby Operation

The TPS568330 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2 µA when in standby condition. EN pin is pulled low internally, when float, the part is disabled by default.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The schematic of Figure 30 shows a typical application for TPS568330 with 1-V output. This design converts an input voltage range of 4.5 V to 23 V down to 1 V with a maximum output current of 8 A.

## 8.2 1V Output Typical Application

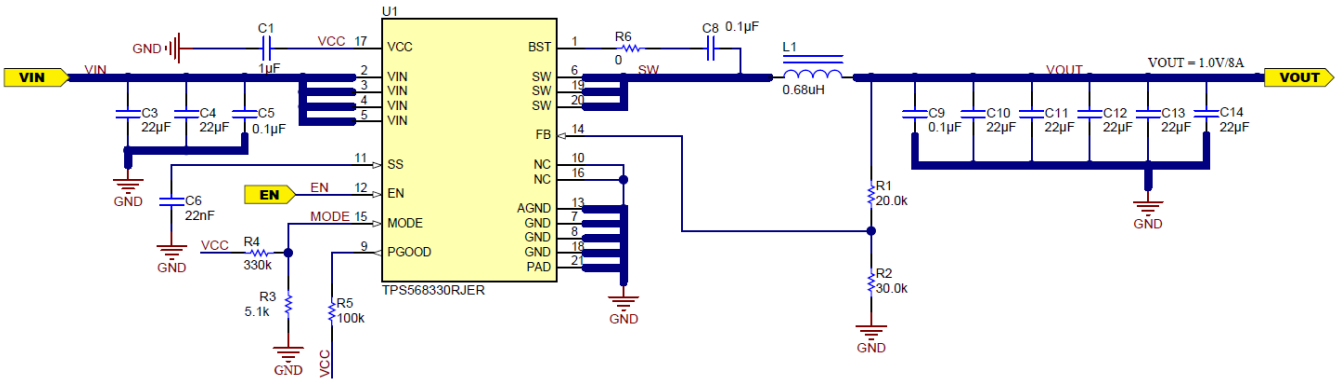



**Figure 30. 1V/8A Reference Design with Eco-mode, $F_{SW}$=600 kHz**

### 8.2.1 Design Requirements

Table 2 lists the design parameters for this example.

**Table 2. Design Parameters**

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 1 | | V |
| $I_{OUT}$ | Output current | | | 8 | | A |
| $\Delta V_{OUT}$ | Transient response | 0 A - 8 A load step,2.5A/us | | ±40 | | mV |
| $V_{IN}$ | Input voltage | | 4.5 | 12 | 23 | V |
| $V_{OUT(ripple)}$ | Output voltage ripple | | | 18 | | $mV_{(P-P)}$ |
| $F_{SW}$ | Switching frequency | | | 600 | | kHz |
| | Light load operating mode | | | Eco-mode | | |
| $T_A$ | Ambient temperature | | | 25 | | °C |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 External Component Selection*

##### 8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See Equation 4

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}}) \quad (4)$$

#### 8.2.2.1.2 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 5 and Equation 6. It is important that the inductor is rated to handle these currents.

$$I_{L(RMS)} = \sqrt{\left( I^2_{OUT} + \frac{1}{12} \times \left( \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (5)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{L(ripple)}}{2} \quad (6)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

#### 8.2.2.1.3 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In DCAP3™, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 3.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

**Table 3. Recommended Component Values**

| $V_{OUT}$ (V) | $R_{LOWER}$ (kΩ) | $R_{UPPER}$ (kΩ) | $F_{sw}$ (kHz) | $L_{OUT}$ (µH) | $C_{OUT(min)}$ (µF) | $C_{OUT(max)}$ (µF) | $C_{FF}$ (PF) |
|---|---|---|---|---|---|---|---|
| 0.6 | 10 | 0 | 600 | 0.47 | 66 | 500 | - |
| | | | 800 | 0.33 | 66 | 500 | - |
| | | | 1000 | 0.27 | 66 | 500 | - |
| 1 | 30 | 20 | 600 | 0.68 | 66 | 500 | - |
| | | | 800 | 0.47 | 66 | 500 | - |
| | | | 1000 | 0.33 | 66 | 500 | - |
| 3.3 | 20 | 90 | 600 | 1.5 | 66 | 500 | 47-330 |
| | | | 800 | 1.2 | 66 | 500 | 47-330 |
| | | | 1000 | 1 | 66 | 500 | 47-330 |
| 5.0 | 30 | 220 | 600 | 2.2 | 66 | 500 | 47-330 |
| | | | 800 | 1.5 | 66 | 500 | 47-330 |
| | | | 1000 | 1.2 | 66 | 500 | 47-330 |

#### 8.2.2.1.4 Input Capacitor Selection

The TPS568330 requires input decoupling capacitors on power supply input VIN, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in Equation 7.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (7)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 8:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (8)$$

A 1-µF ceramic capacitor is needed for the decoupling capacitor on VCC pin.

### 8.2.3 Application Curves

Figure 31 through Figure 44 apply to the circuit of Figure 30. $V_{IN}$ = 12 V. $T_J$ = 25°C unless otherwise specified.

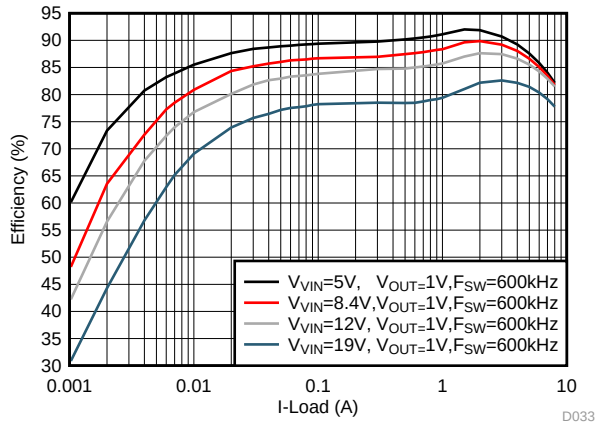



**Figure 31. Efficiency Curve**

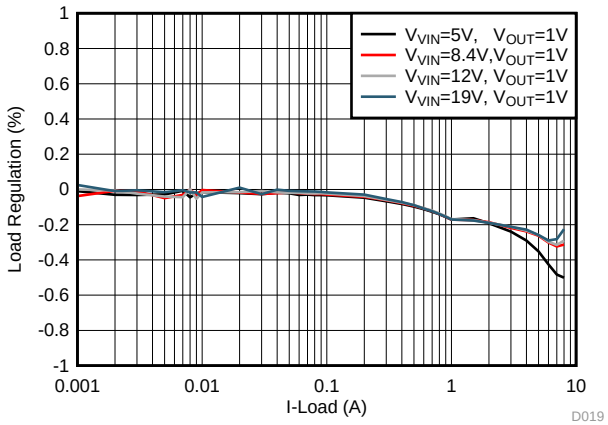
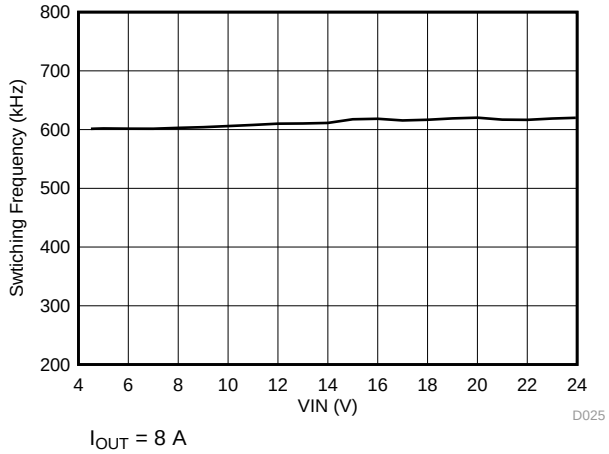



**Figure 32. Load Regulation**




$I_{OUT}$ = 8 A

**Figure 33. Switching Frequency vs Input Voltage**

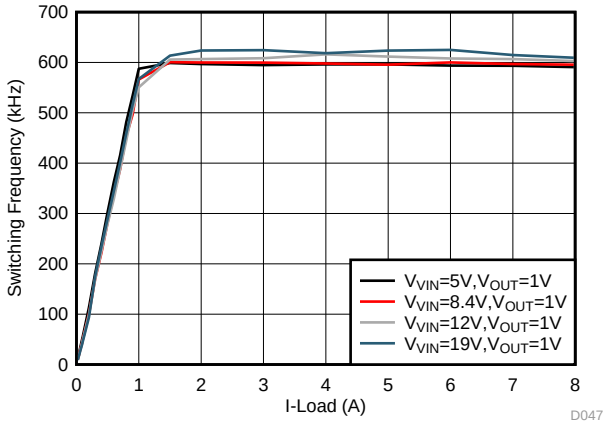



**Figure 34. Switching Frequency vs Output Load**

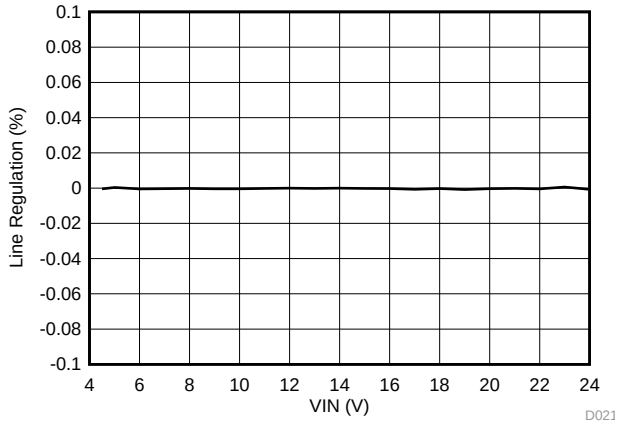



**Figure 35. Line Regulation,$I_{OUT}$ = 0.01 A**

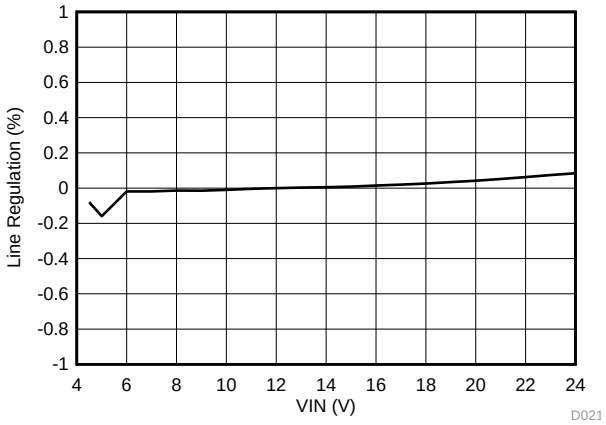



**Figure 36. Line Regulation,$I_{OUT}$ = 8 A**

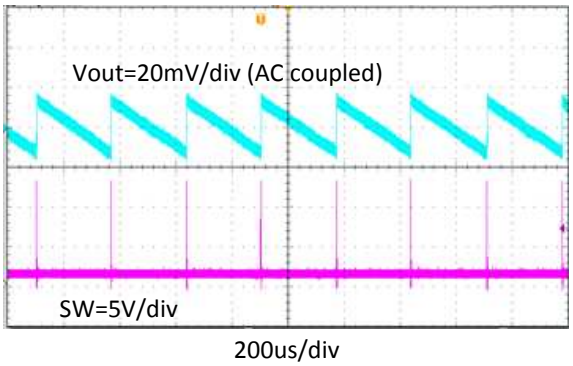



**Figure 37. Output Voltage Ripple, $I_{OUT}$ = 0.01 A**

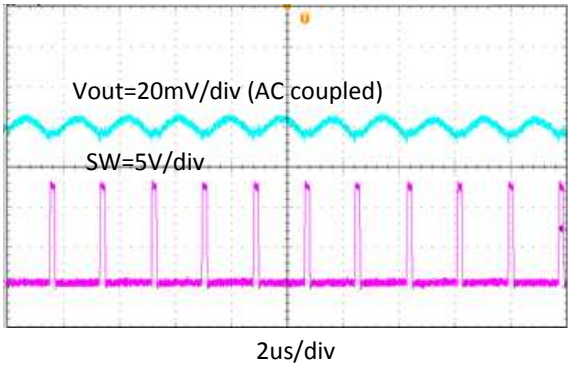



**Figure 38. Output Voltage Ripple, $I_{OUT}$ = 8 A**

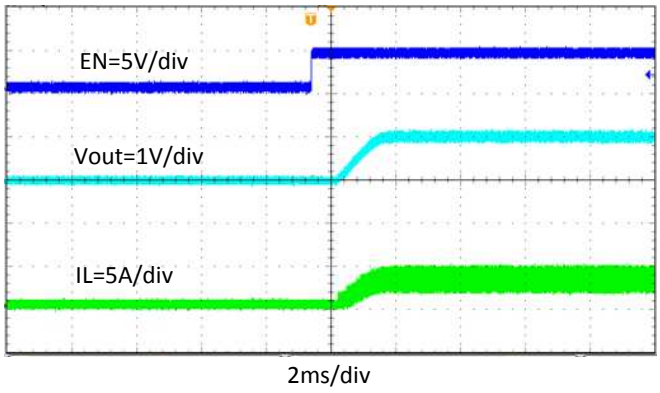



**Figure 39. Start-Up Through EN, $I_{OUT}$ = 4A**

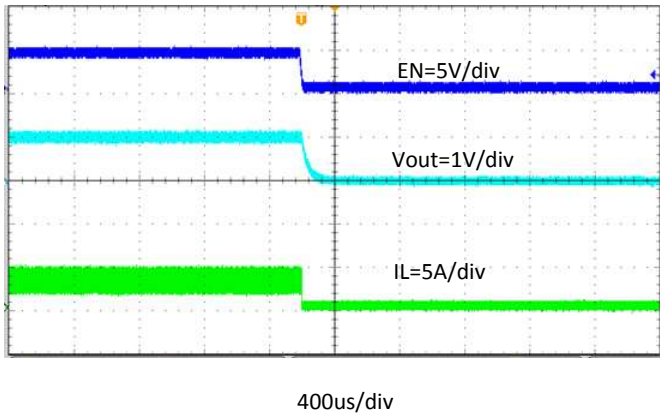



**Figure 40. Shut-down Through EN, $I_{OUT}$ = 4A**

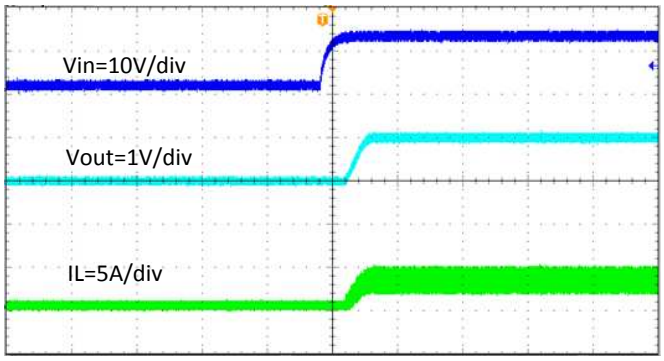



**Figure 41. Start Up Relative to $V_{IN}$ Rising, $I_{OUT}$ = 4 A**

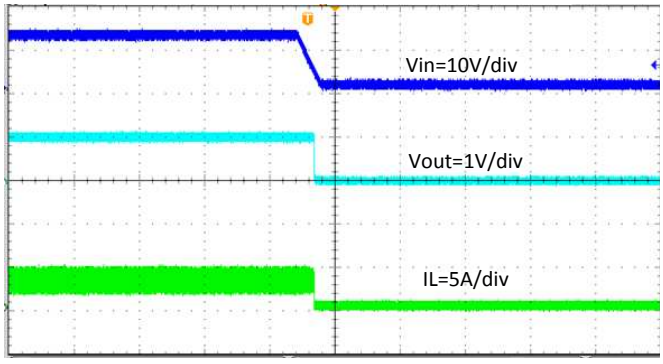



**Figure 42. Start Up Relative to $V_{IN}$ Falling, $I_{OUT}$ = 4 A**

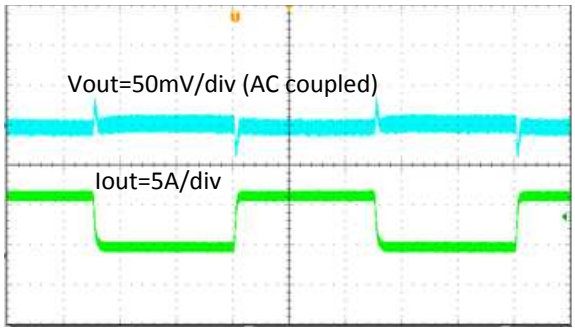



**Figure 43. Transient Response, 0.8 A to 7.2 A**

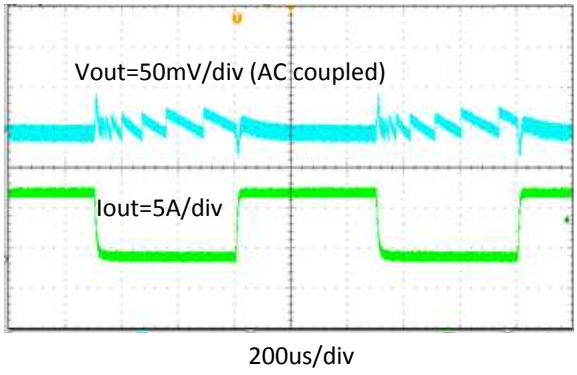



**Figure 44. Transient Response, 0 A to 8 A**

## 9 Power Supply Recommendations

The TPS568330 is intended to be powered by a well regulated dc voltage. The input voltage range is 4.5 to 23 V. TPS568330 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS568330 circuit, additional input bulk capacitance is recommended, typical values are 100 μF to 470 μF.

# 10 Layout

## 10.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch × 3-inch, four-layer PCB with 2-oz copper is used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductor and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the GND connection of output capacitor and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- Feedback could be 20mil and must be routed away from the switching node, BST node or other high efficiency signal.
- VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and GND and near input capacitors to reduce parasitic inductance and improve thermal performance

## 10.2 Layout Example

Figure 45 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in Figure 30. Resistor divider for EN is not used in the circuit of Figure 30, but are shown in the layout for reference.

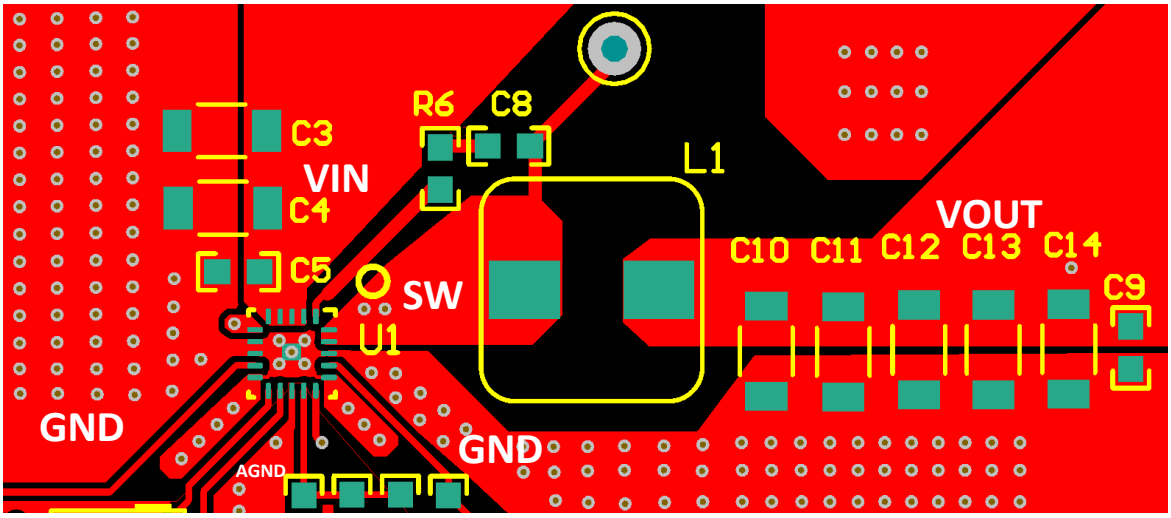



**Figure 45. Top-Layer Layout**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

D-CAP3, ULQ, Eco-Mode, HotRod, DCAP3, Eco-mode, E2E are trademarks of Texas Instruments.

## 11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Package Option Addendum

### 12.1.1 Packaging Information

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (3) | MSL Peak Temp (4) | Op Temp (°C) | Device Marking (5) (6) |
|---|---|---|---|---|---|---|---|---|---|---|
| TPS568330RJER | PREVIEW | VQFN | RJE | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 Year | –40 to 125 | 568330 |
| TPS568330RJET | PREVIEW | VQFN | RJE | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 Year | –40 to 125 | 568330 |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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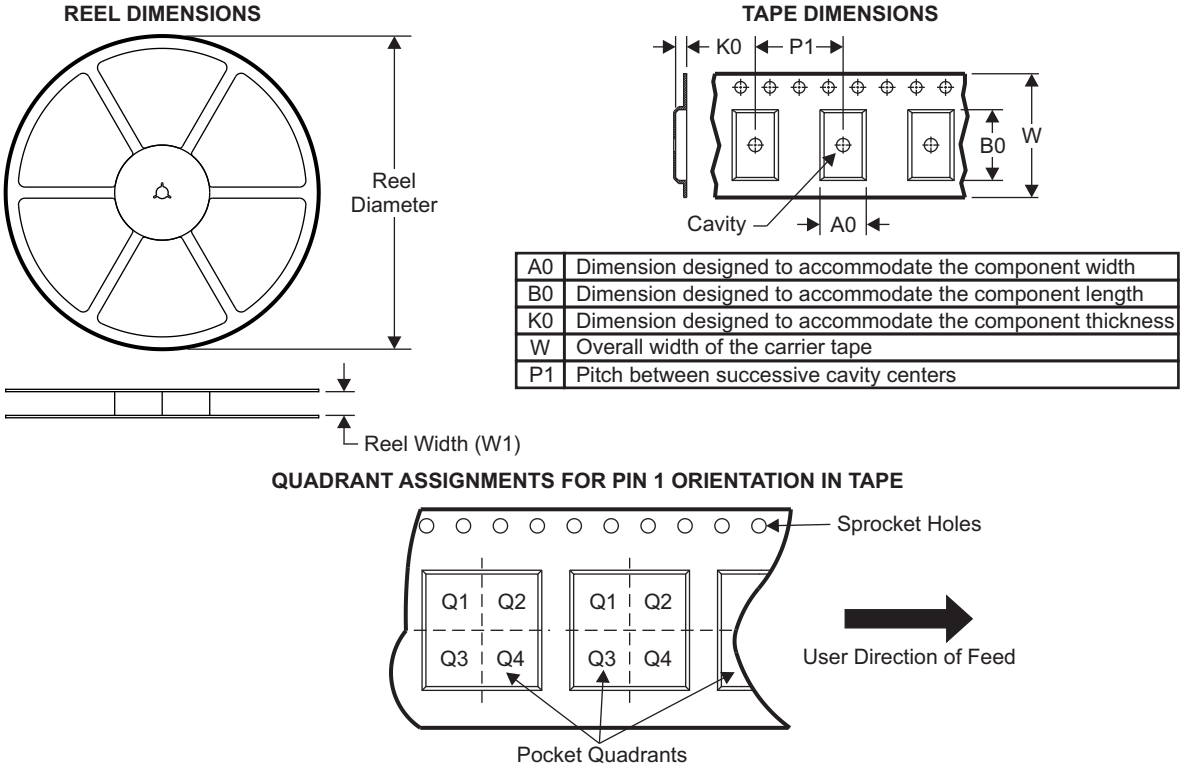
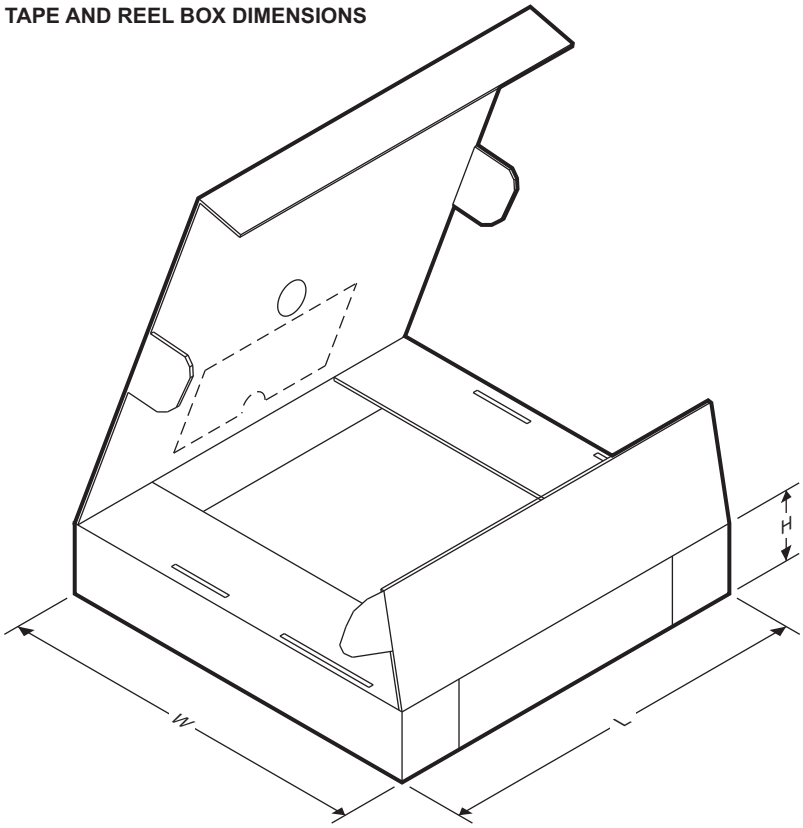
### 12.1.2 Tape and Reel Information




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS568330RJER | VQFN | RJE | 20 | 3000 | 330 | 12.4 | 3.3 | 3.3 | 1.1 | 8 | 12 | 2 |
| TPS568330RJET | VQFN | RJE | 20 | 250 | 180 | 12.4 | 3.3 | 3.3 | 1.1 | 8 | 12 | 2 |

**TAPE AND REEL BOX DIMENSIONS**



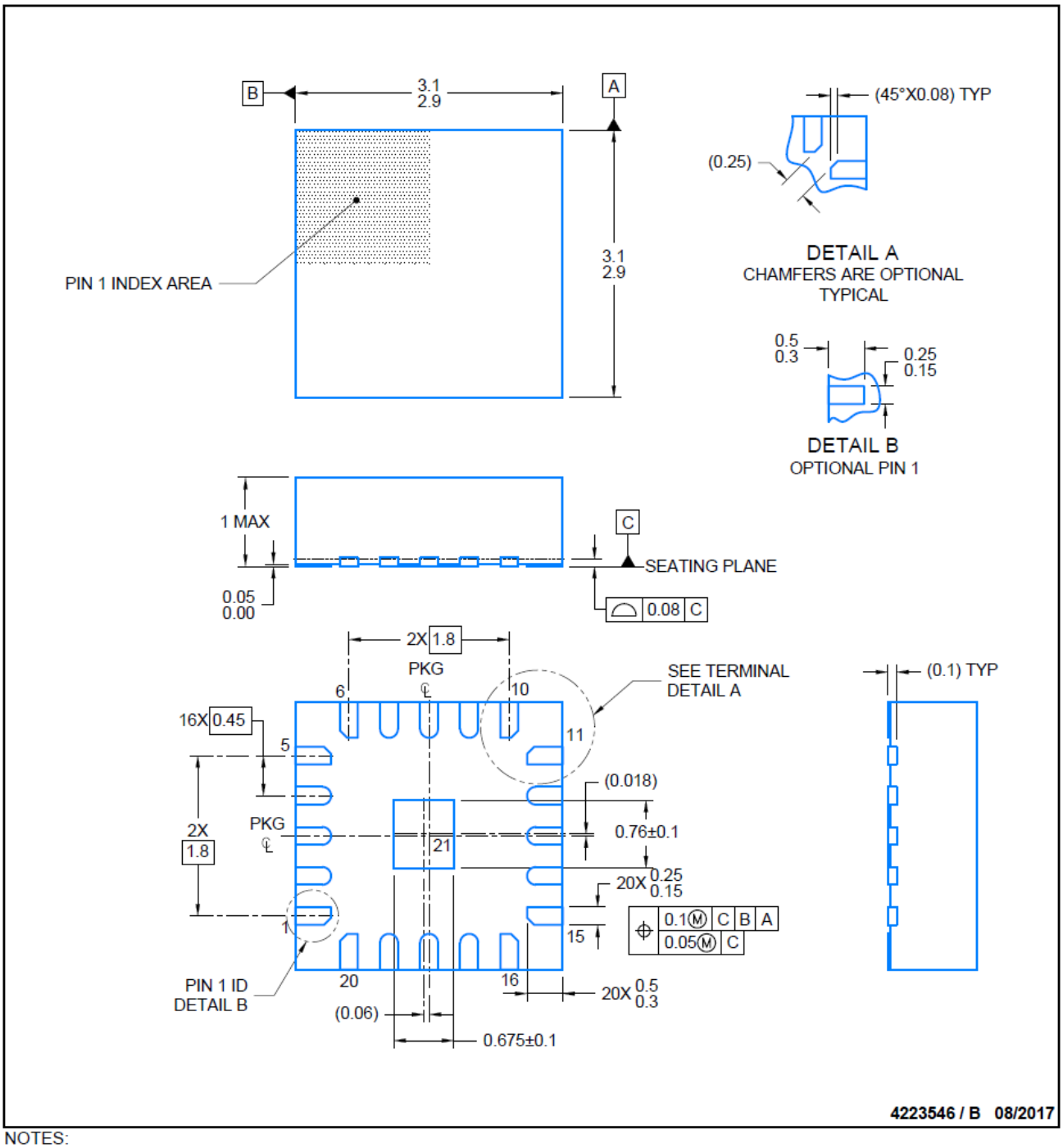

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS568330RJER | VQFN | RJE | 20 | 3000 | 367 | 367 | 35 |
| TPS568330RJET | VQFN | RJE | 20 | 250 | 210 | 185 | 35 |

# PACKAGE OUTLINE

## RJE0020A

## VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD




NOTES:

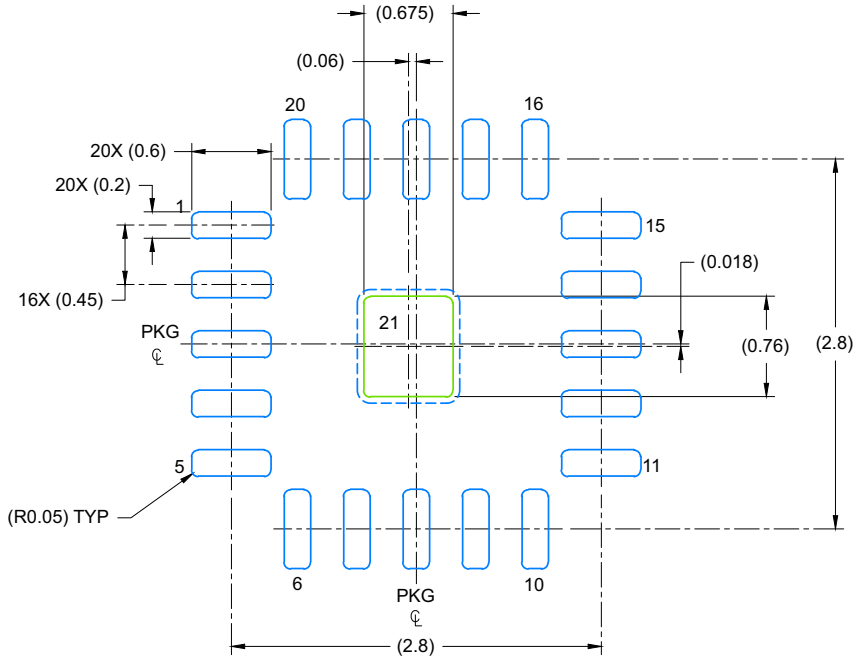
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

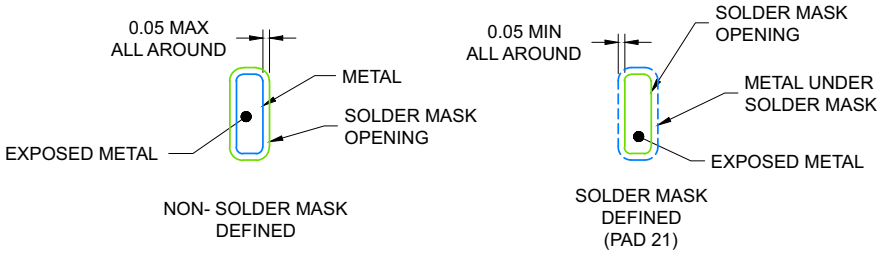
## RJE0020A

### VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




SOLDER MASK DETAILS

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NOTES: (continued)

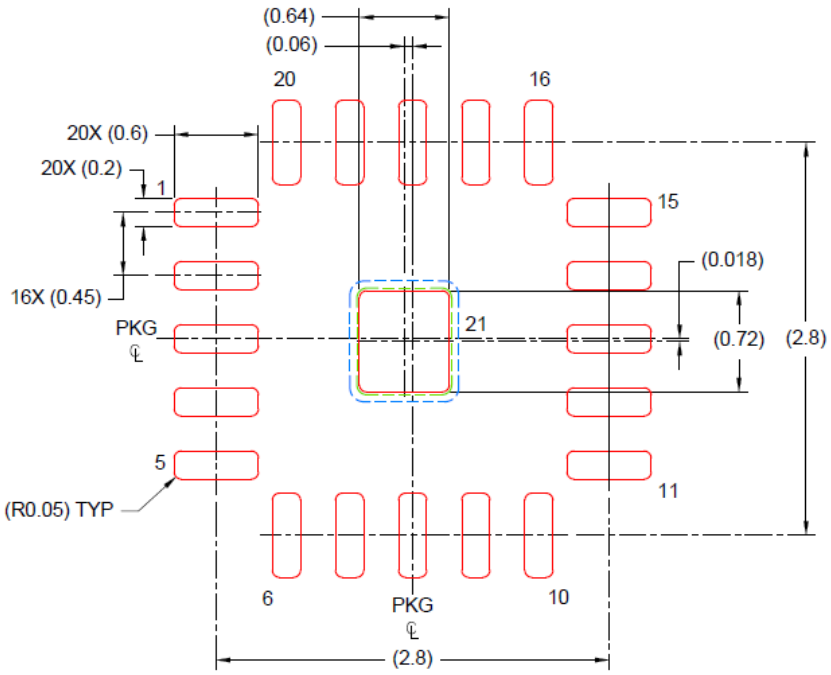
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## RJE0020A

### VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 21: 90%
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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