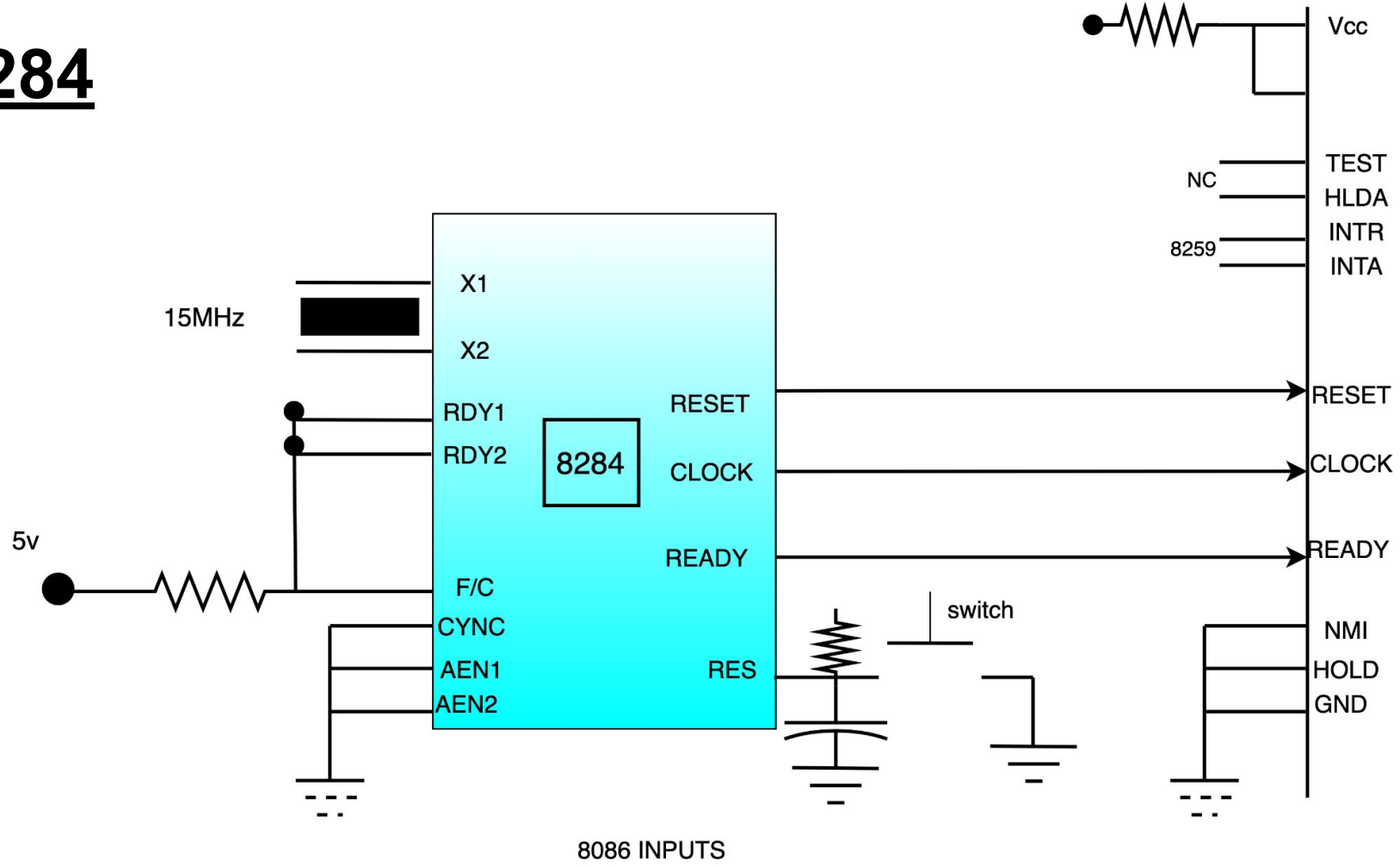
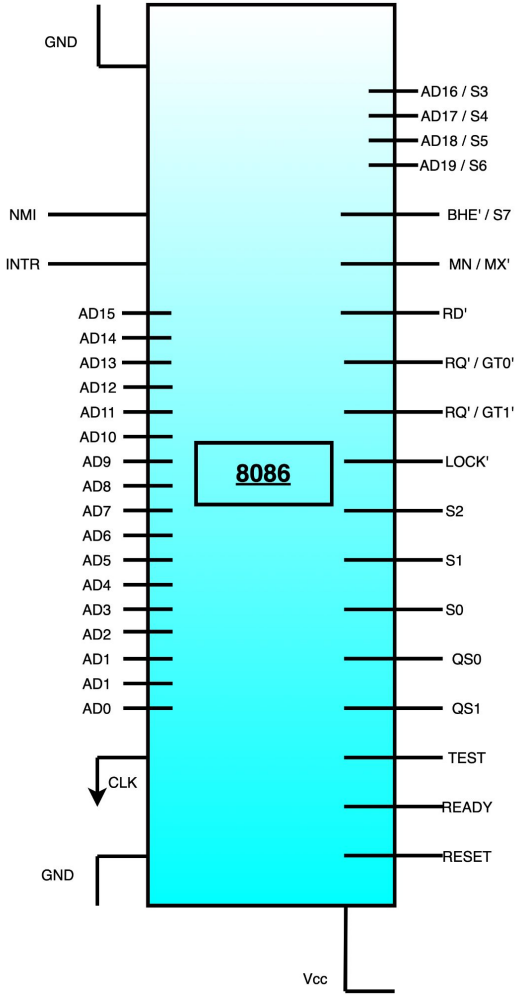
Hardware Design

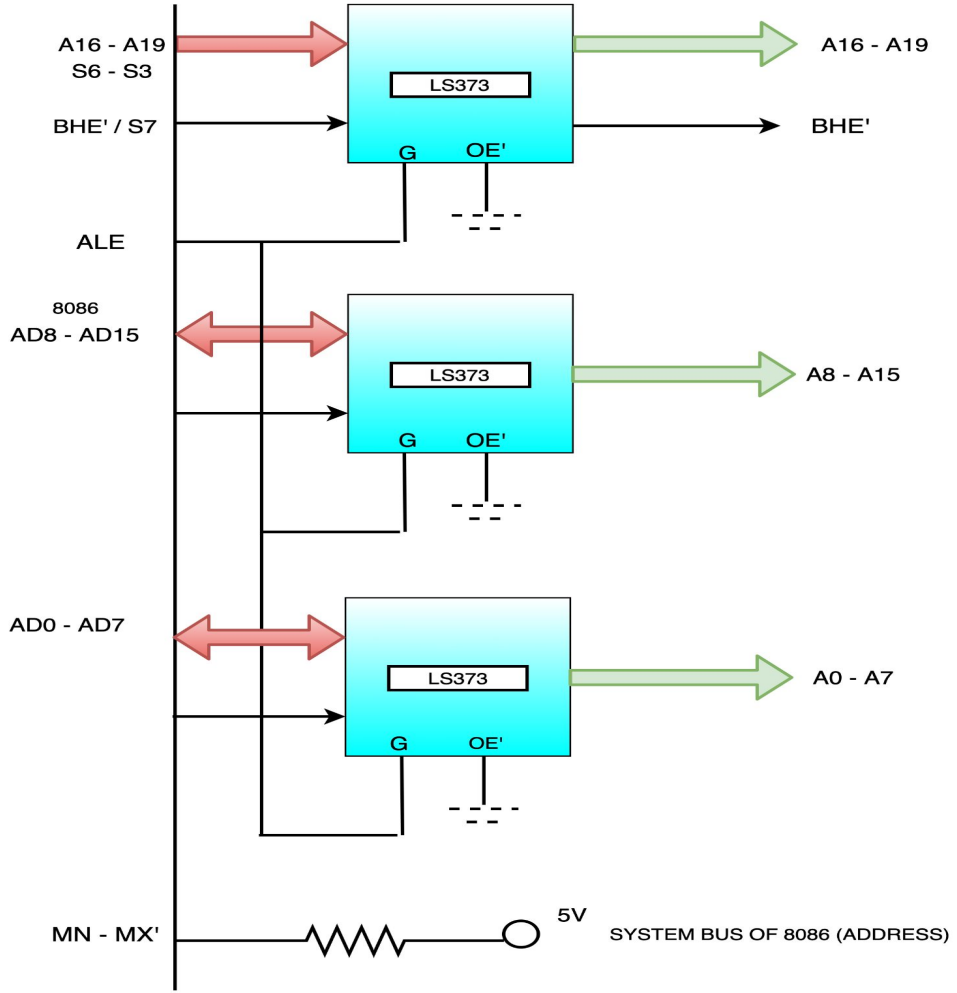
8284


Vcc
TEST
NC
HLDA
INTR
8259
INTA
15MHz
X1
X2
RDY1
RDY2
8284
RESET
CLOCK
READY
RESET
CLOCK
READY
5v
F/C
CYNC
AEN1
AEN2
RES
switch
NMI
HOLD
GND
8086 INPUTS

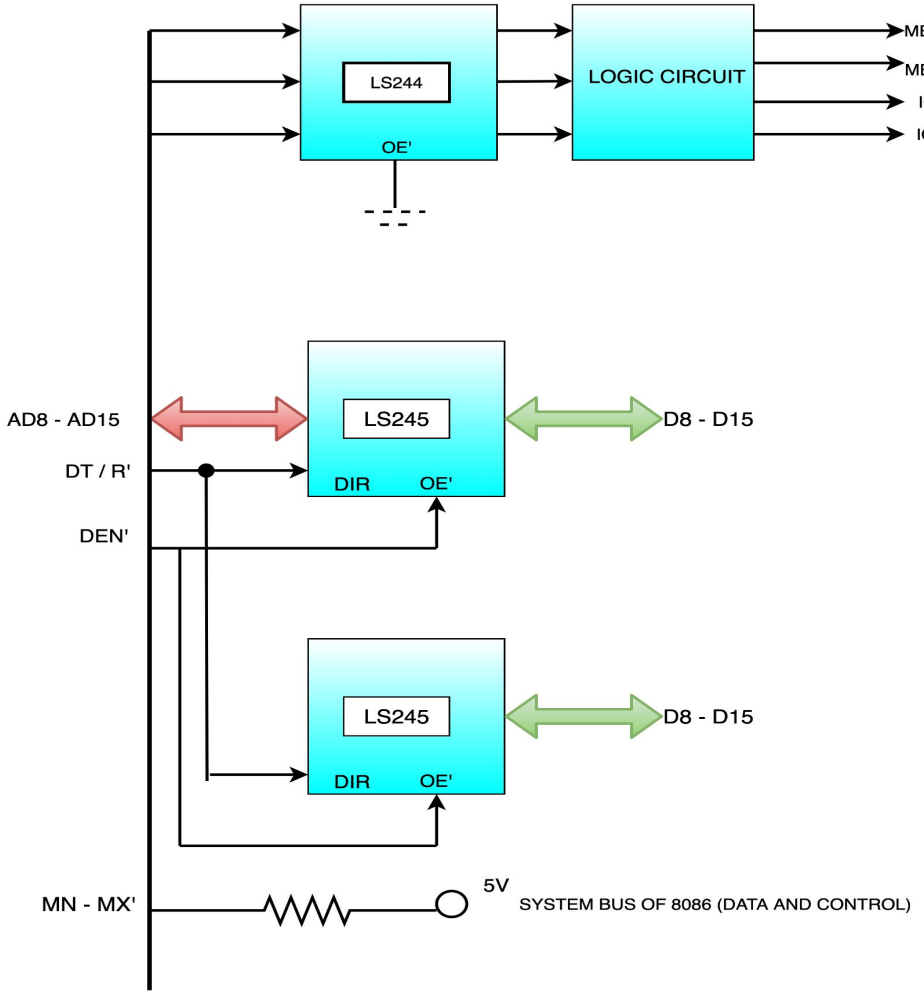
8086

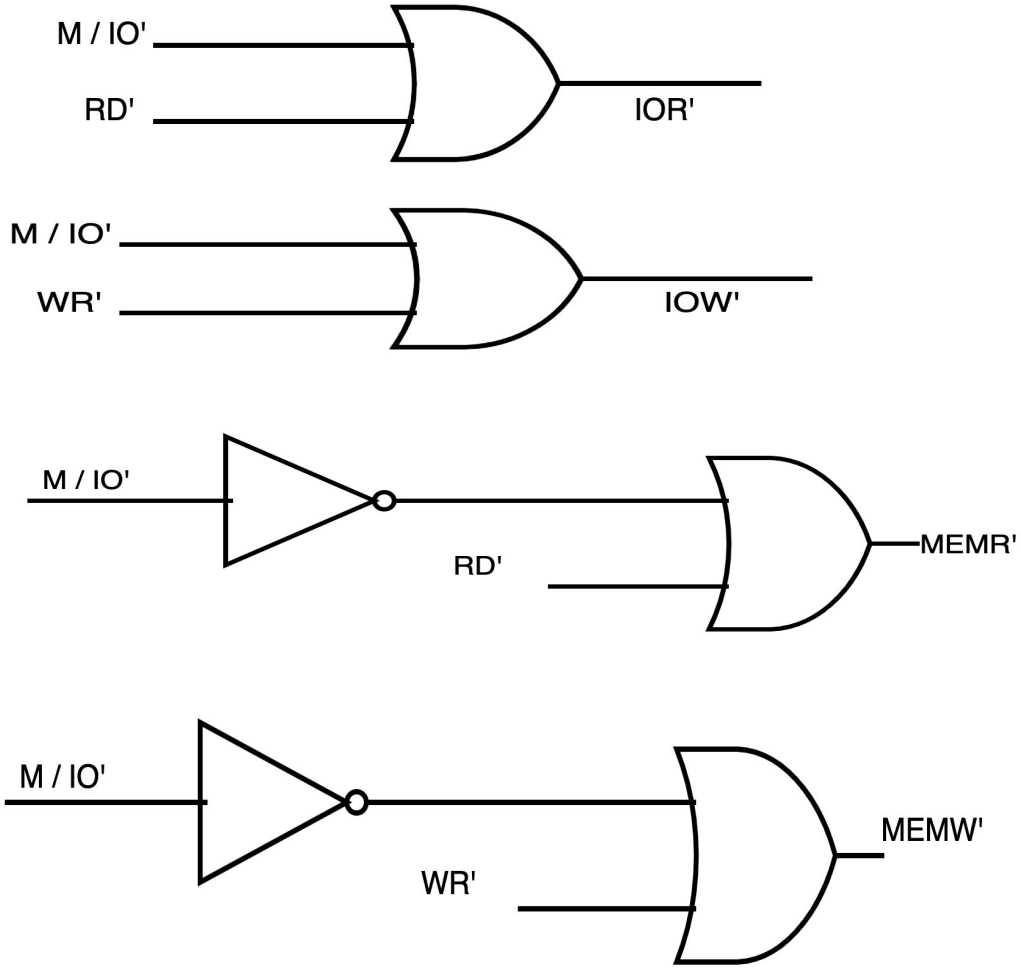

GND
AD16 / S3
AD17 / S4
AD18 / S5
AD19 / S6
NMI
BHE' / S7
INTR
MN / MX'
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD1
AD0
RD'
RQ' / GT0'
RQ' / GT1'
LOCK'
S2
S1
S0
QS0
QS1
TEST
READY
RESET
8086
CLK
GND
Vcc

SYSTEM BUS OF 8086 (ADDRESS)



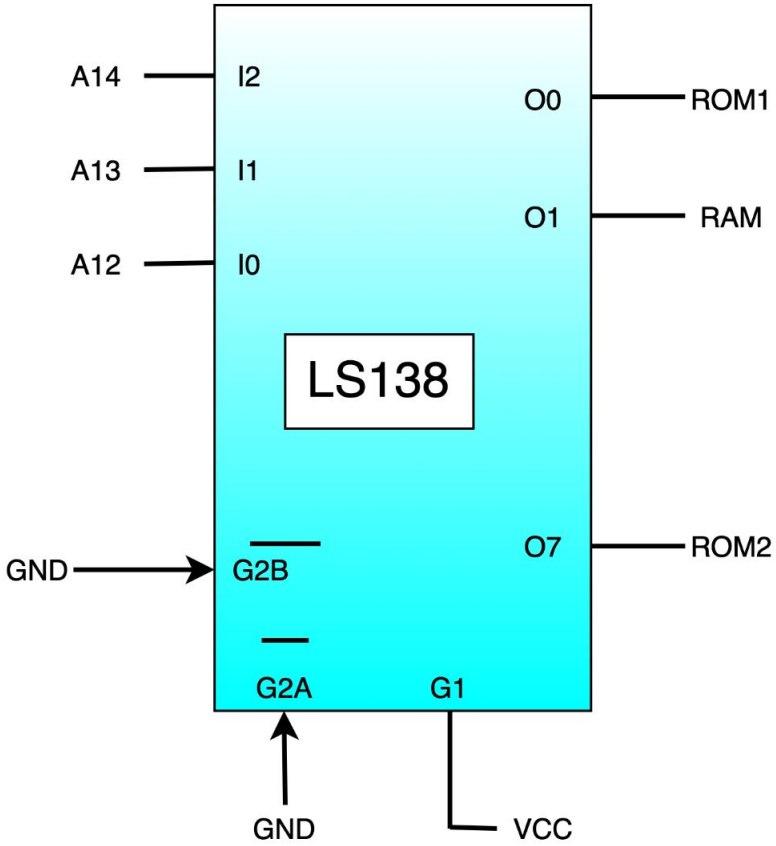
SYSTEM BUS OF 8086 (DATA + CONTROL)

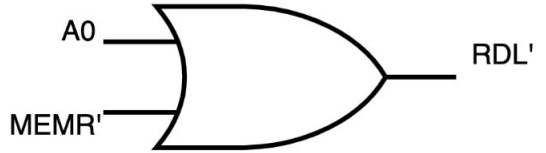


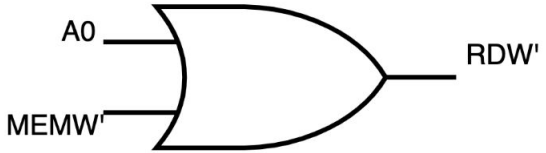


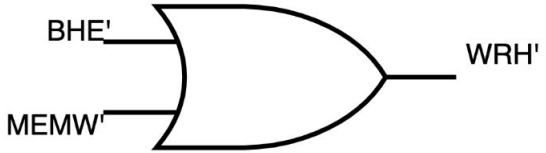
M /IO'	RD'	WR'	BUS CYCLE
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

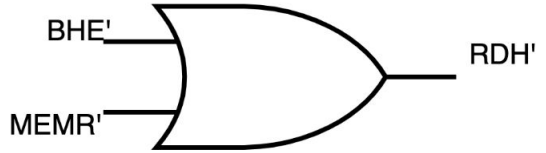
MEMORY DECODER



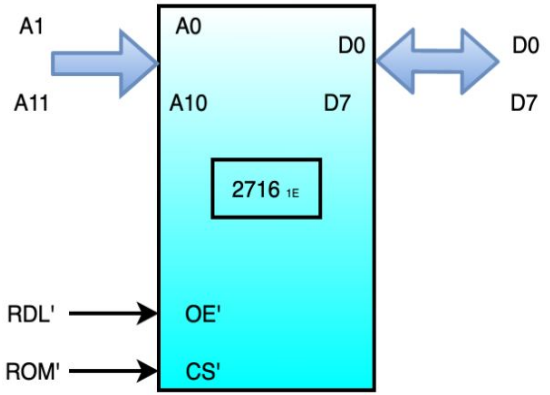


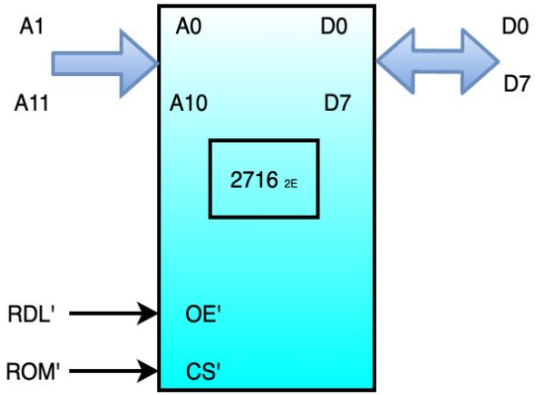


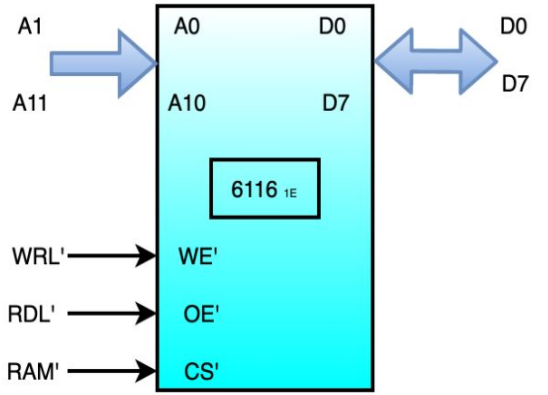


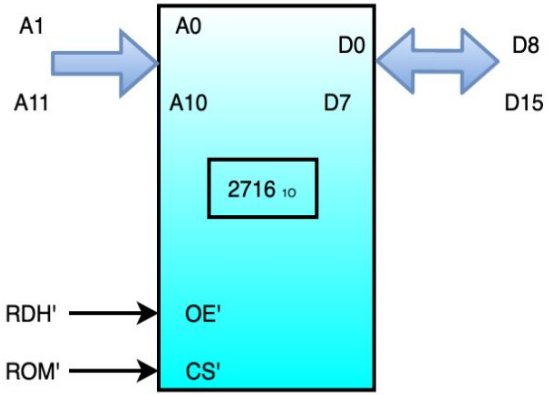


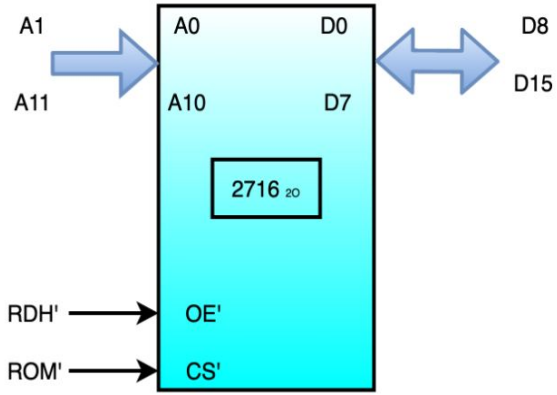
MEMORY INTERFACING

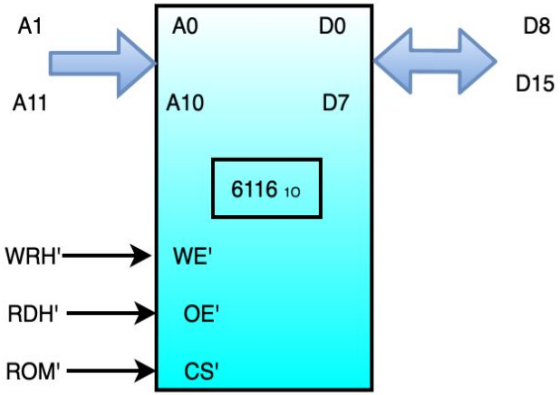




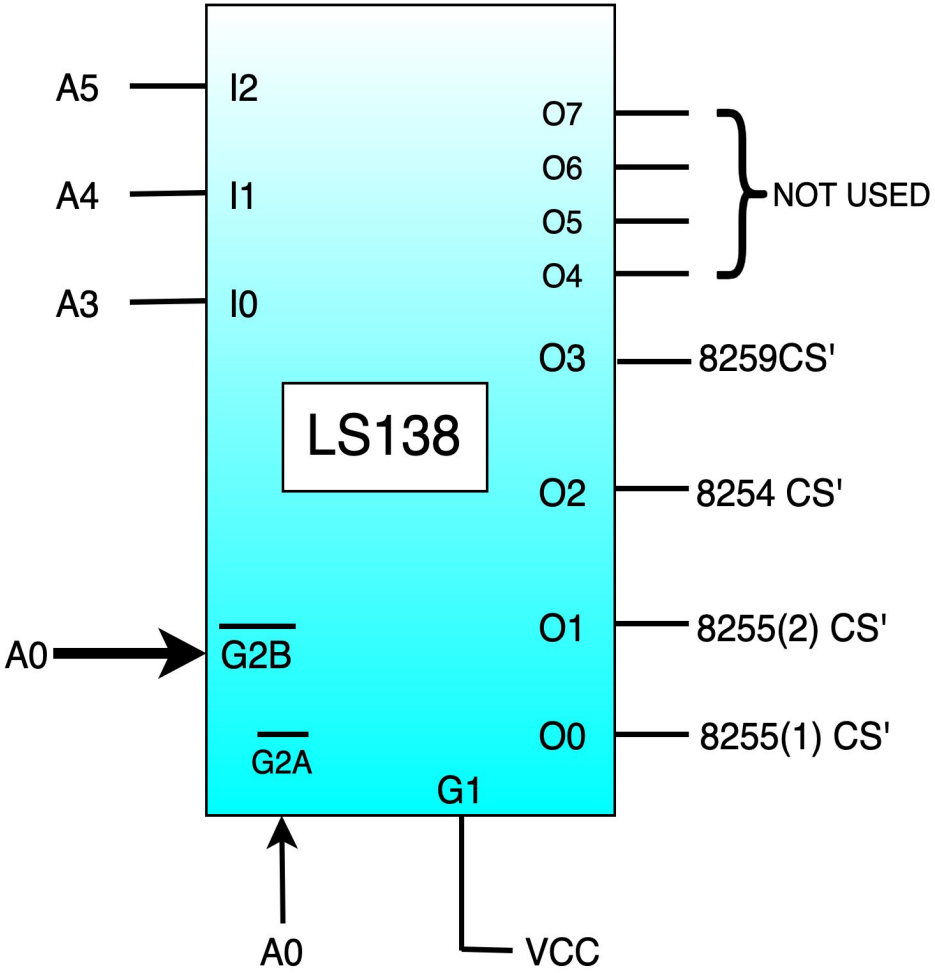




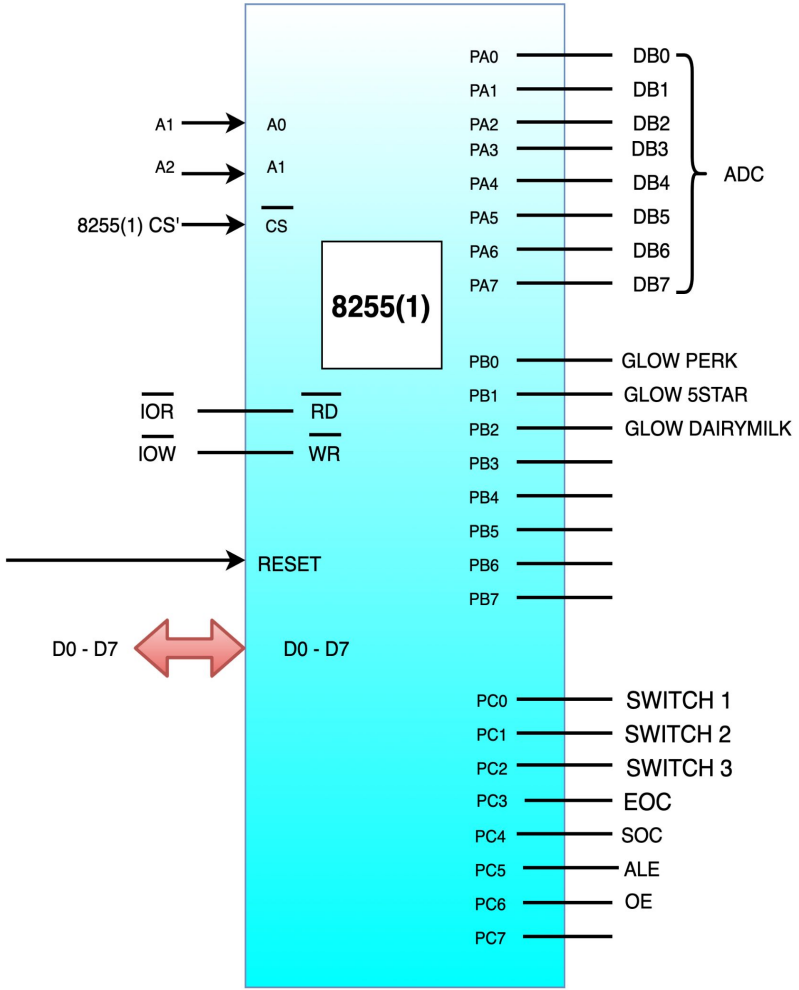




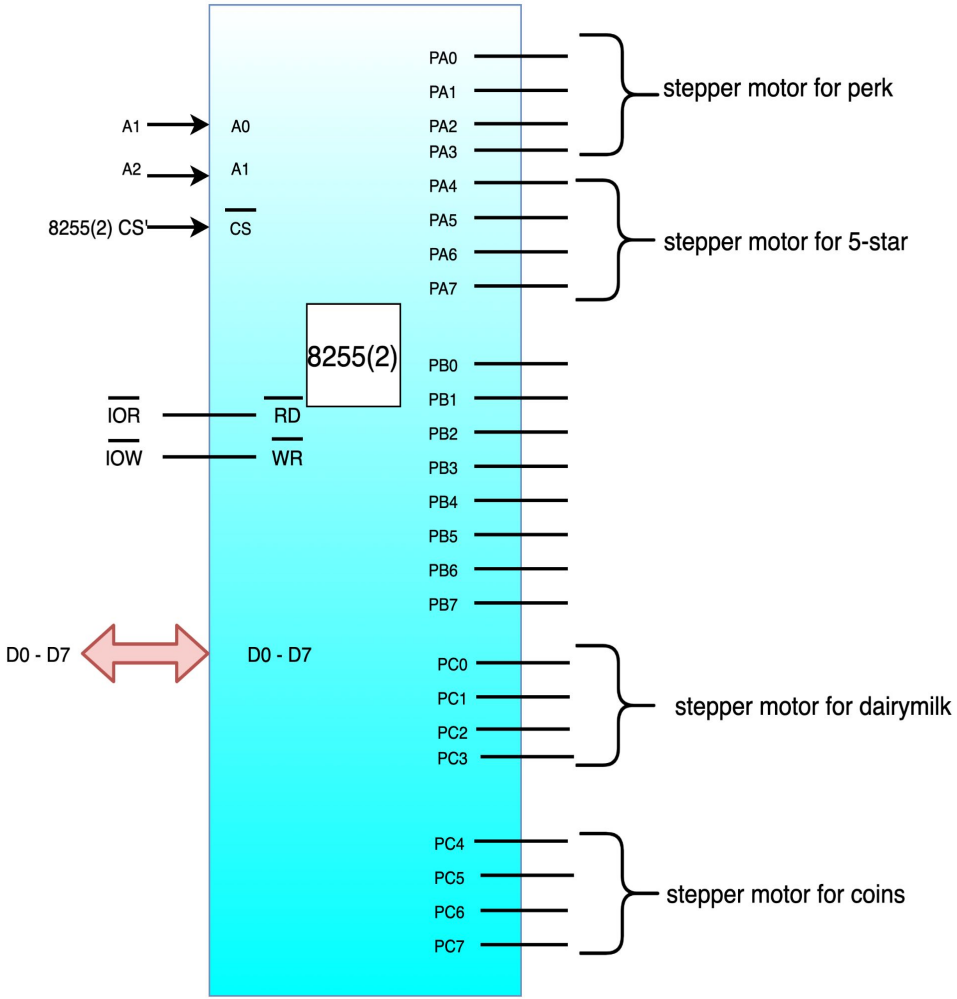
I/O DECODER


A5
I2
A4
I1
A3
I0
LS138
O7
O6
O5
O4
NOT USED
O3
8259CS'
O2
8254 CS'
O1
8255(2) CS'
O0
8255(1) CS'
A0
G2B
G2A
G1
A0
VCC

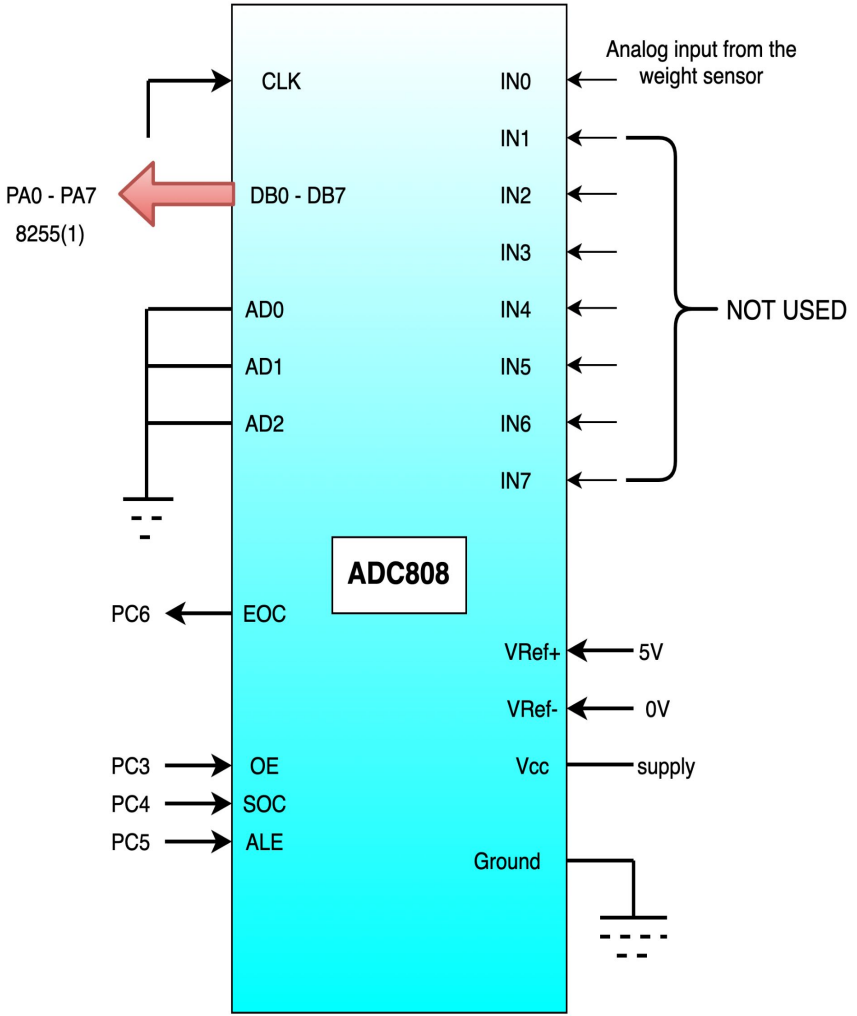
8255 (1)


A1
A0
A2
A1
8255(1) CS'
CS
8255(1)
IOR
RD
IOW
WR
RESET
D0 - D7
D0 - D7
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
ADC
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
GLOW PERK
GLOW 5STAR
GLOW DAIRYMILK
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
SWITCH 1
SWITCH 2
SWITCH 3
EOC
SOC
ALE
OE

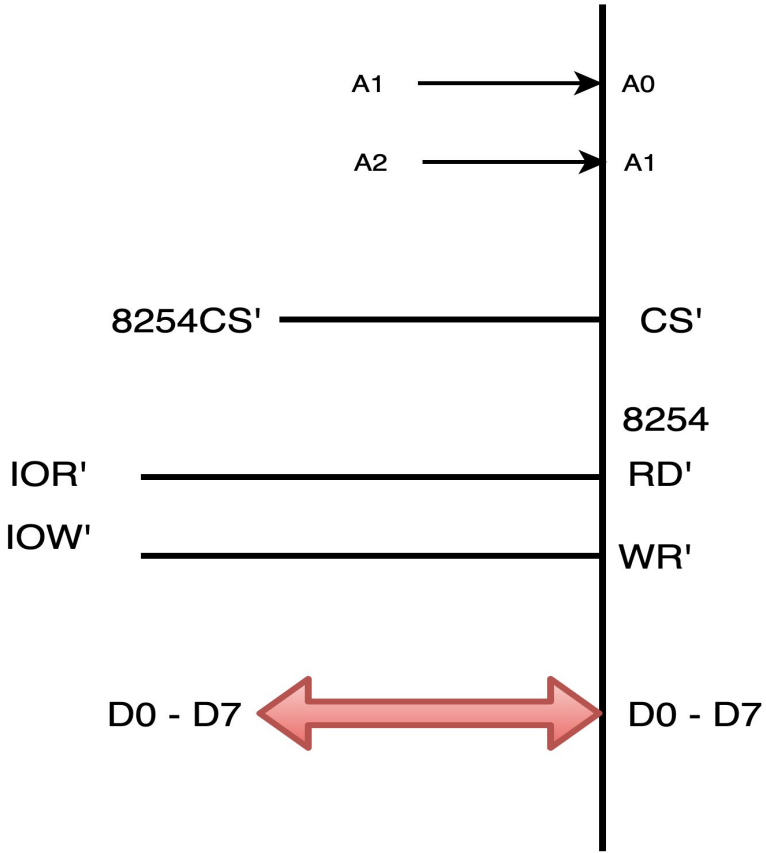
8255 (2)


A1
A0
A2
A1
8255(2) CS'
CS
8255(2)
IOR
RD
IOW
WR
D0 - D7
D0 - D7
PA0
PA1
PA2
PA3
stepper motor for perk
PA4
PA5
PA6
PA7
stepper motor for 5-star
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
stepper motor for dairymilk
PC4
PC5
PC6
PC7
stepper motor for coins

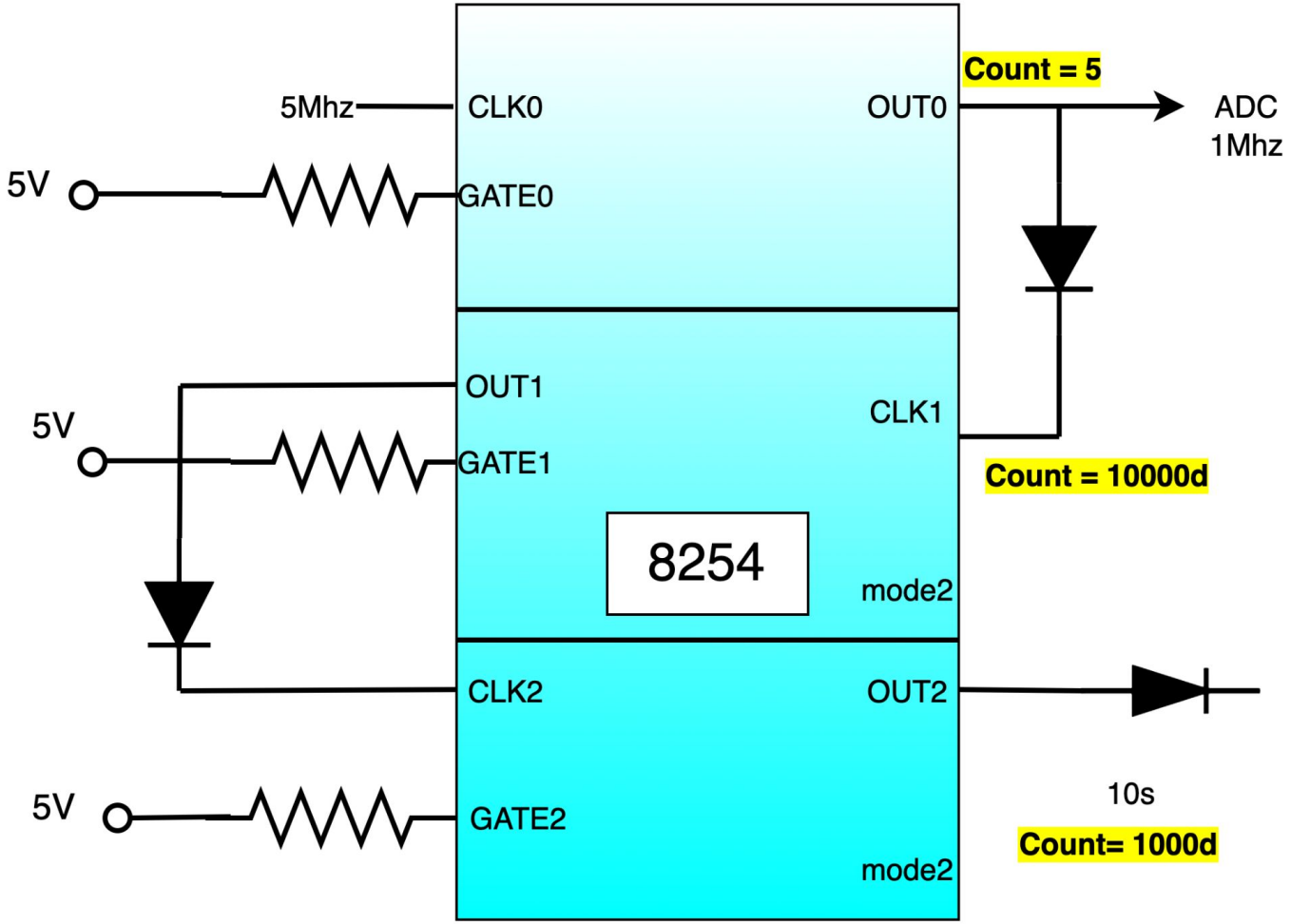
ADC808


Analog input from the weight sensor
CLK
IN0
IN1
PA0 - PA7
8255(1)
DB0 - DB7
IN2
IN3
AD0
IN4
NOT USED
AD1
IN5
AD2
IN6
IN7
ADC808
PC6
EOC
VRef+
5V
VRef-
0V
PC3
OE
Vcc
supply
PC4
SOC
PC5
ALE
Ground

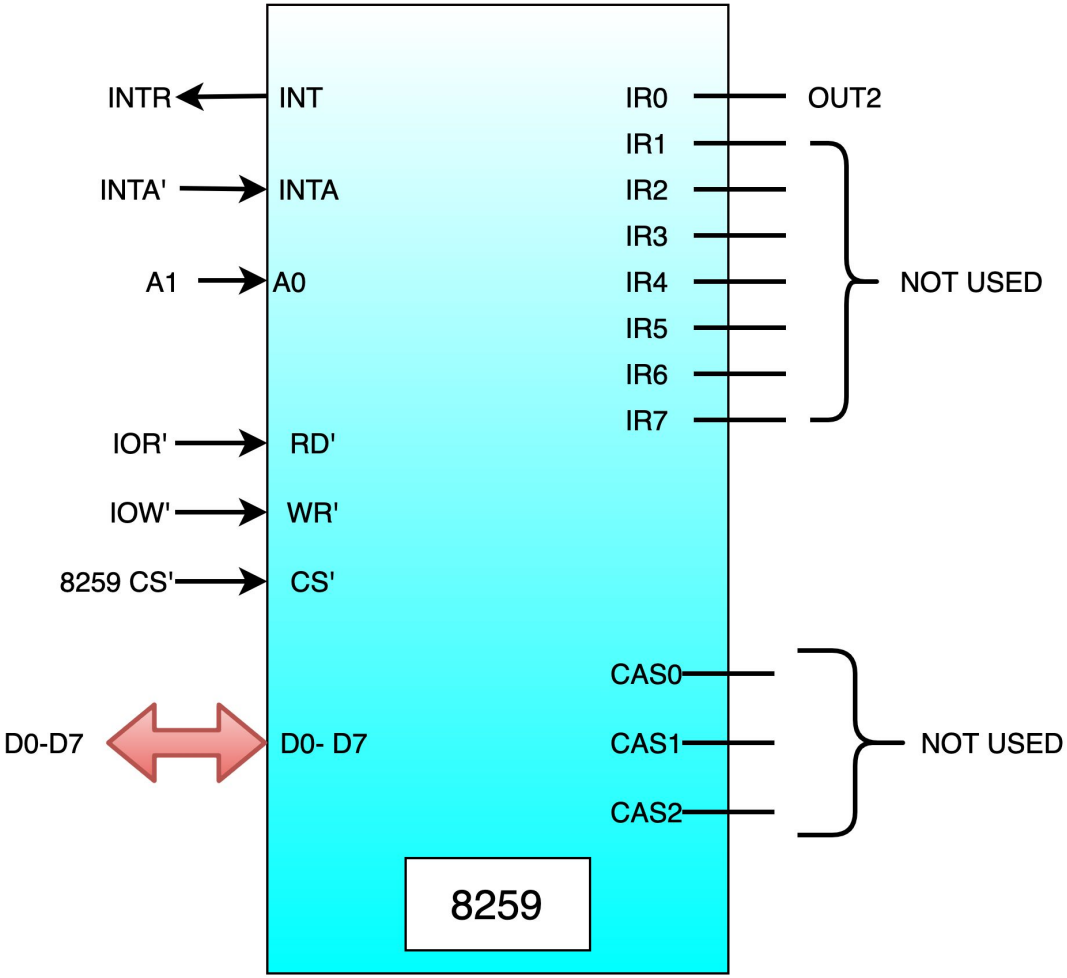
8254 INTERFACE TO THE PROCESSOR



8254


5Mhz
CLK0
OUT0
Count = 5
ADC
1Mhz
5V
GATE0
OUT1
CLK1
5V
GATE1
Count = 10000d
8254
mode2
CLK2
OUT2
5V
GATE2
10s
Count= 1000d
mode2

8259


INTR
INT
INTA'
INTA
A1
A0
IOR'
RD'
IOW'
WR'
8259 CS'
CS'
D0-D7
D0- D7
IR0
OUT2
IR1
IR2
IR3
IR4
IR5
IR6
IR7
NOT USED
CAS0
CAS1
CAS2
NOT USED
8259

STEPPER MOTOR