Summer Fellowship Report

On

Integrated Circuit Design using Subcircuit feature of eSim

Submitted by

Sabarish Mohan JS

Under the guidance of

Prof.Kannan M. Moudgalya
Chemical Engineering Department
IIT Bombay

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Acknowledgment

I would like to express my sincere gratitude to the FOSSEE team at IIT Bombay for the incredible opportunity to be a part of the Summer Fellowship program. This experience has been both intellectually rewarding and personally inspiring. Working on the eSim platform allowed me to dive deep into the process of circuit design, testing, and simulation using open-source EDA tools.

During this fellowship, I had the opportunity to design and contribute multiple subcircuits to the eSim platform, making a tangible contribution to its growing open-source ecosystem. Through this hands-on work, I was able to explore the intricacies of analog and digital design in a practical environment, gaining insight into how simulation tools aid in real-world engineering workflows.

I am grateful to Prof. Kannan M. Moudgalya for his vision in leading the FOSSEE initiative, and for making open-source tools like eSim accessible to students across the country. His efforts in promoting self-reliance in engineering education have created learning platforms that continue to impact thousands of aspiring engineers like me.

A special note of thanks to Mr. Sumant Kar, my mentor during the fellowship, for his continuous guidance and support. His practical advice, clear explanations, and willingness to help whenever I faced roadblocks played a significant role in shaping my project outcomes.

This fellowship has been a defining chapter in my academic journey, and I leave it with not only new skills and knowledge, but also with clarity and excitement for the path that lies ahead in the VLSI domain.

Contents

Chapter 1

Introduction

The FOSSEE (Free/Libre and Open-Source Software for Education) project at IIT Bombay, an initiative of the Ministry of Education, Government of India, is committed to promoting the widespread adoption of open-source software in academic and research institutions. By reducing dependence on expensive proprietary tools, FOSSEE empowers individuals and institutions to explore free/libre alternatives that are equally capable and accessible.

1.1 FOSSEE Summer Fellowship

As part of its mission, FOSSEE conducts the Summer Fellowship Program, which provides students an opportunity to contribute to active open-source projects. The program aims to develop students' technical skills, encourage collaborative development practices, and inspire long-term involvement in the open-source community. I was selected for this fellowship through a selection process that involved technical evaluations and task submissions.

1.2 eSim

eSim is an open-source Electronic Design Automation (EDA) tool developed by FOSSEE for circuit design, simulation, and PCB layout. It serves as a powerful alternative to proprietary tools like OrCAD and PSpice. Built on top of KiCad and Ngspice, eSim is designed to provide a complete and intuitive workflow for analog, digital, and mixed-signal circuit simulation.

1.3 KiCad

KiCad is a popular open-source EDA software suite used for schematic capture and PCB layout design. In the eSim environment, KiCad is used to create the circuit schematics and define component connections. Its graphical interface simplifies

the process of drawing and organizing complex circuit design.

1.4 Ngspice

Ngspice is an open-source mixed-level/mixed-signal electronic circuit simulator based on SPICE. Integrated within eSim, Ngspice is responsible for performing time-domain, frequency-domain, and other simulations based on the circuit designs created in KiCad. It helps in visualizing voltage, current, and other waveform outputs through simulation.

1.5 Key Features of eSim

eSim is designed to be a comprehensive, open-source EDA tool that enables users to design, simulate, and validate electronic circuits efficiently. Its features make it suitable not only for academic learning but also for real-world circuit development and prototyping. Some of its key features include:

- **Integrated Circuit Design and Simulation:** Combines KiCad for schematic capture and Ngspice for simulation, enabling users to design and test analog, digital, and mixed-signal circuits in a unified environment.

- **Subcircuit Modeling and Reuse:** Users can create custom IC models using subcircuits, which can then be saved and reused from the `esim_subckt` libraryideal for modular design and rapid prototyping.

- **PCB Design and Layout Support:** Leveraging KiCads PCB design suite, eSim allows users to not only simulate circuits but also transition directly to PCB layout and fabrication, making it practical for real-time product development and hardware prototyping.

- **Waveform Analysis and Debugging:** Provides interactive waveform plotting for voltage and current through simulation outputs, which helps in verifying and debugging circuits before implementation.

- **Cross-platform and Open-source:** Completely free and compatible with Windows and Linux systems, eSim promotes accessibility and transparency, making it ideal for institutions and individual learners worldwide.

Chapter 2

Subcircuit Modeling of Analog and Digital ICs in eSim

2.1 Problem Statement

To design and implement subcircuit models of various analog and digital Integrated Circuits (ICs) in eSim by utilizing existing device models from the eSim library. The subcircuits are to be developed based on standard IC datasheets and integrated into the `esim_subckt` library. Each IC model must be verified for correct functionality through suitable test circuits. This work aims to expand the reusable IC model base in eSim for future circuit design and simulation purposes.

2.2 Approach

1. **IC Selection and Datasheet Analysis:**
   Begin by selecting commonly used analog and digital ICs. Carefully study their datasheets to extract internal schematic diagrams, pin configurations, electrical characteristics, and application circuits.

2. **Subcircuit Schematic Development:**
   Using the extracted internal circuit from the datasheet, replicate the schematic in eSim. This is done using only the standard device models already available in the eSim library. The circuit is designed with strict adherence to the original datasheet specifications to ensure accurate modeling.

3. **Component Symbol and Pin Configuration Design:**
   Once the subcircuit is created, the corresponding symbol (component) is designed in eSim. The pin configuration and labeling are matched exactly as per the datasheet to ensure easy usability in any circuit design. This new component is saved into the `esim_subckt` library.

4. **Application-Based Test Circuit Design:**
   Typical application circuits provided in the datasheet are recreated to serve as test environments. These circuits help in validating whether the behavior of the modeled IC aligns with its real-world application.

5. **Simulation and Functional Testing:**
   The test circuits are simulated using eSims KiCad-to-Ngspice interface. Expected output waveforms or behaviors are compared against the datasheet's specifications. Multiple test cases are formulated and evaluated to ensure full coverage of the IC's operating conditions.

6. **Verification and Debugging Loop:**

   - If the test results match expectations, the IC model is considered verified and finalized for library inclusion.
   - If discrepancies arise, the model undergoes debuggingeither the subcircuit or the test circuit is reviewed, modified, and re-tested until satisfactory performance is achieved.

7. **Library Integration and Reusability:**
   Successfully verified ICs are added to the `esim_subckt` library with complete symbol, pin mapping, and validated functionality. These components are now available for future use in any circuit simulation within eSim.

This structured approach ensures that each subcircuit model is not only accurate but also practical and reusable for educational and design purposes.

Chapter 3

IC Design and Simulation

3.1 SN74AUP1G58 Low Power Configurable Multiple Function Gate

The SN74AUP1G58 is a low-power configurable multiple-function logic gate IC from Texas Instruments, designed to implement various logic functions (AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer) using just one device. It allows function selection via control pins, operates over a wide supply range, and features 5V-tolerant inputs, making it ideal for battery-powered, portable, and space-constrained digital systems. Its primary purpose is to provide flexible, low-power logic in a compact form factor while maintaining high noise immunity and reliable signal integrity.

3.1.1 Pin Diagram

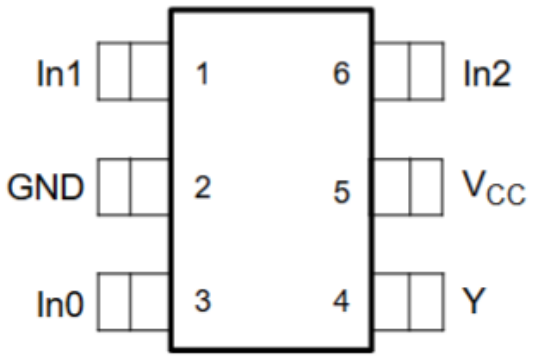


Figure 3.1: Pin configuration of IC SN74AUP1G58

3.1.2 Subcircuit Schematic Diagram

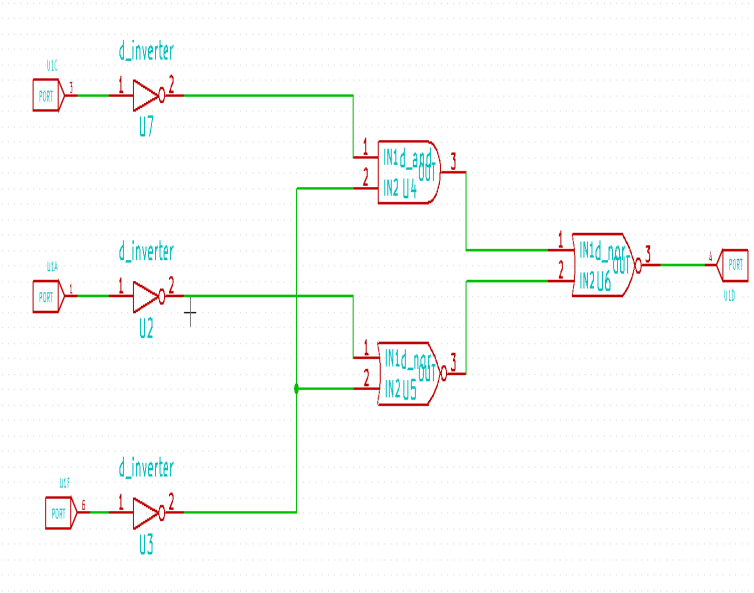


Figure 3.2: Subcircuit schematic diagram

3.1.3 Test Circuit

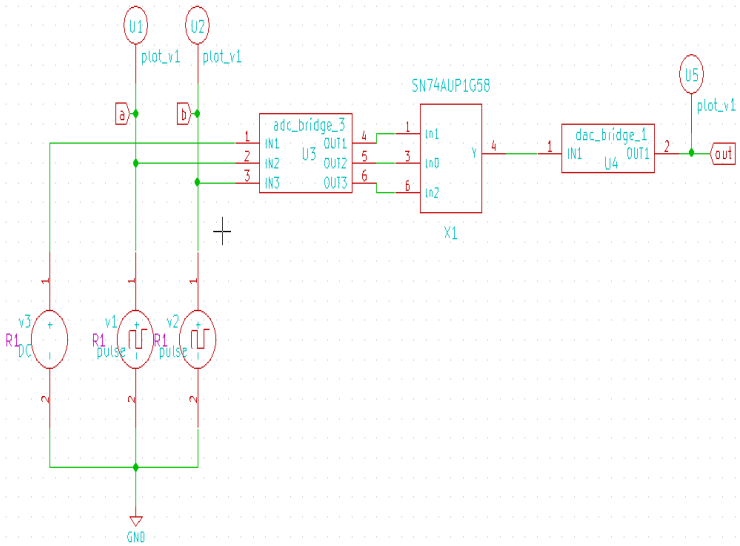
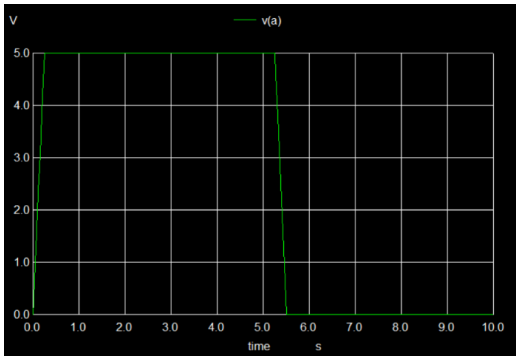
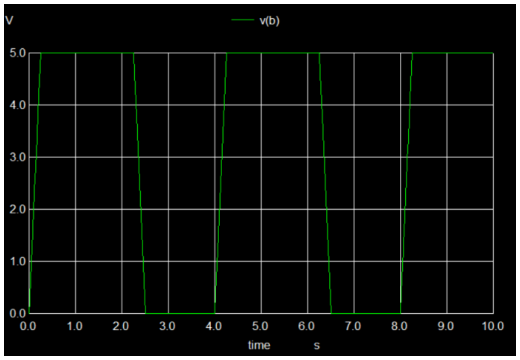


Figure 3.3: IC SN74AUP1G58 test circuit (OR Gate)

3.1.4 Input Plot



(a) Input plot (In0)



(b) Input plot (In2)

Figure 3.4: Input plots of IC SN74AUP1G58

3.1.5 Output Plot

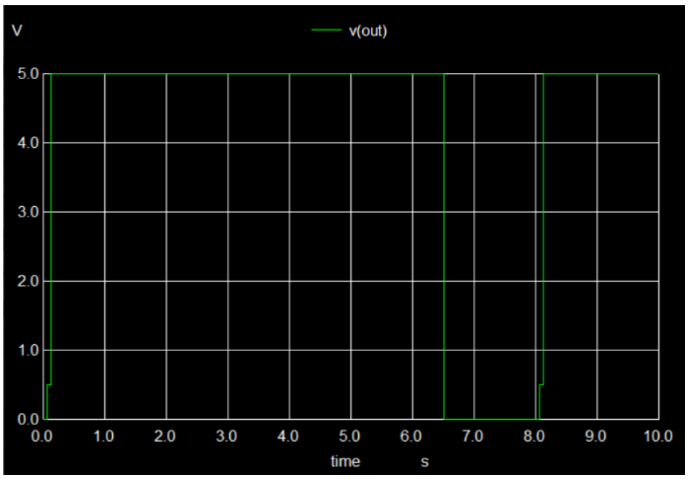


Figure 3.5: Output Plot (Y)

3.2 DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate

The DM74LS51 is a TTL-based dual AND-OR-INVERT (AOI) logic gate IC that integrates two independent logic circuitsone with two 2-input AND gates and one with two 3-input AND gates, both feeding into a NOR structure. This configuration performs complex logic functions by first executing AND operations, then OR-ing the results, and finally inverting the output. It is useful for implementing compact and efficient multi-level logic in digital circuits, reducing gate count and improving timing performance in control and arithmetic logic designs.

3.2.1 Pin Diagram

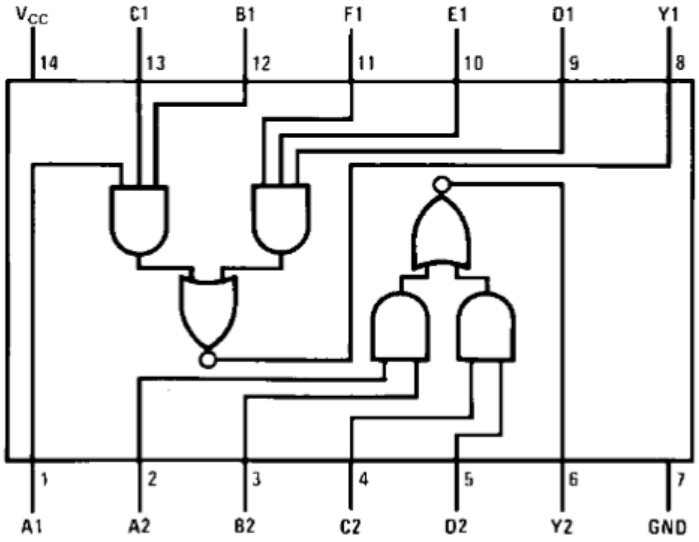


Figure 3.6: Pin configuration of IC DM74LS51

3.2.2 Subcircuit Schematic Diagram

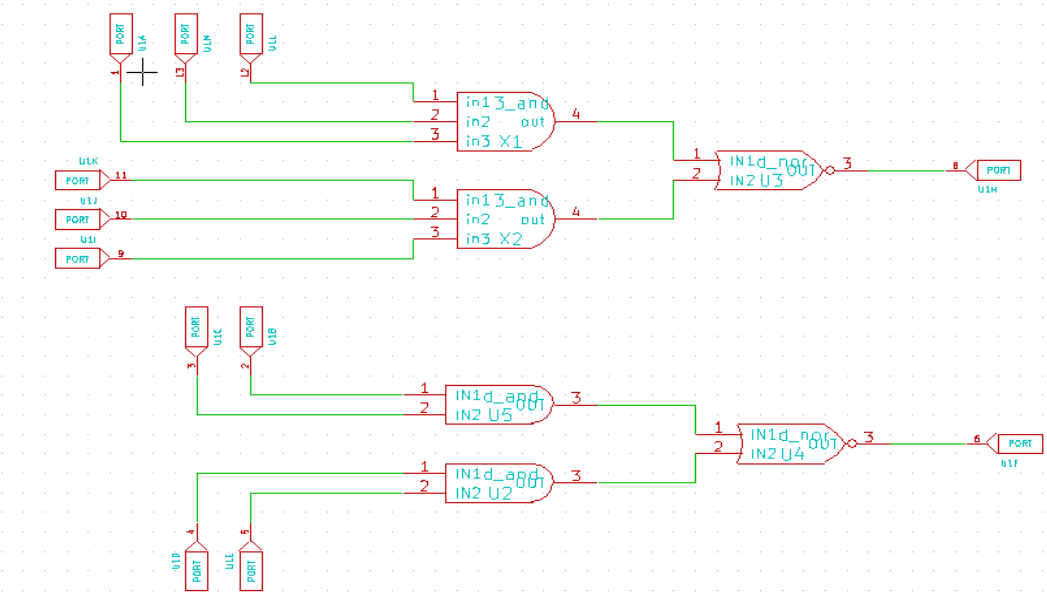


Figure 3.7: Subcircuit schematic diagram

3.2.3 Test Circuit

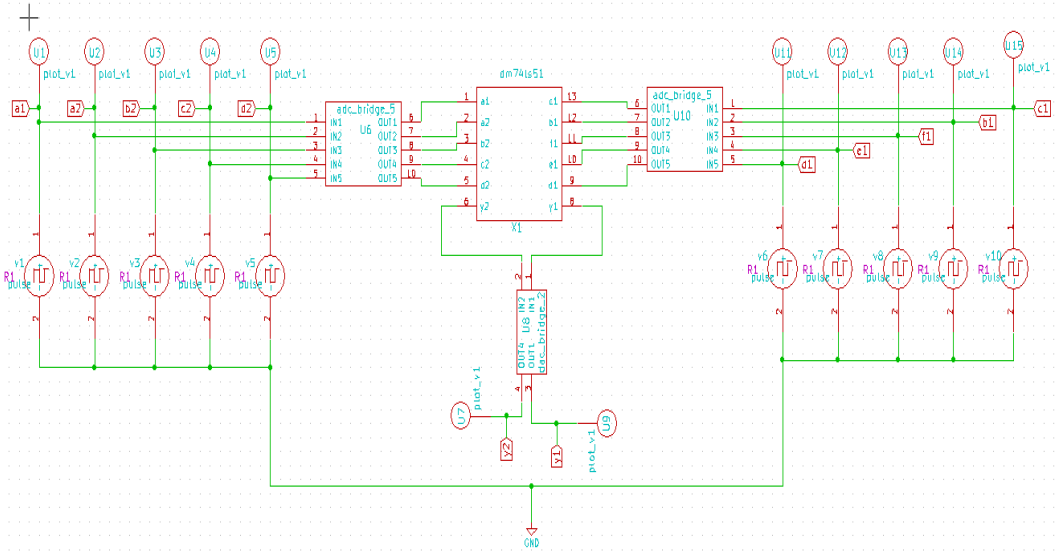
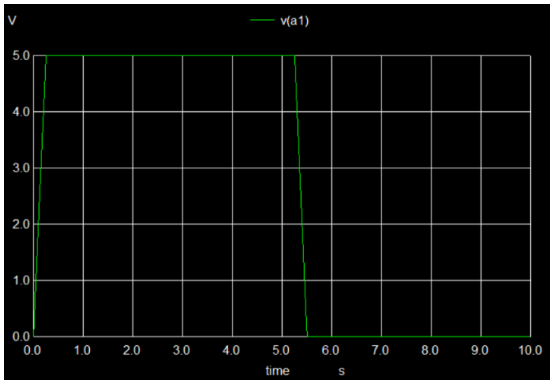
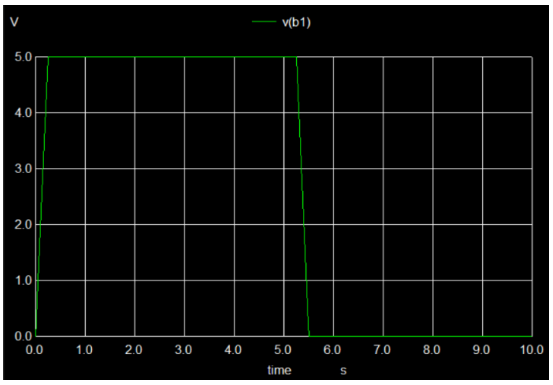


Figure 3.8: IC DM74LS51 test circuit (AOI Logic)

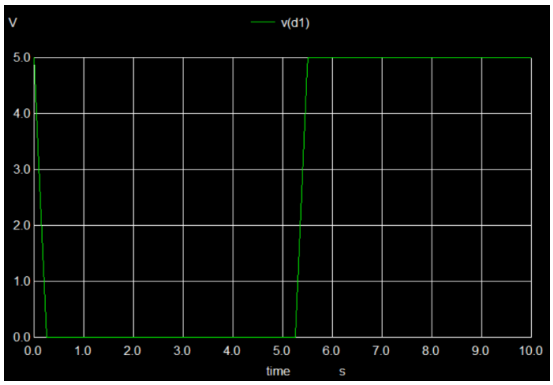
3.2.4 Input Plots



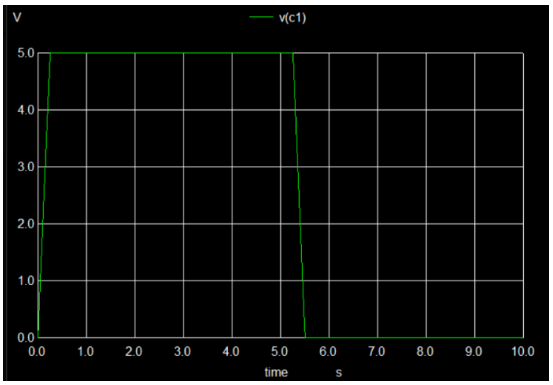
(a) Input plot (a1)



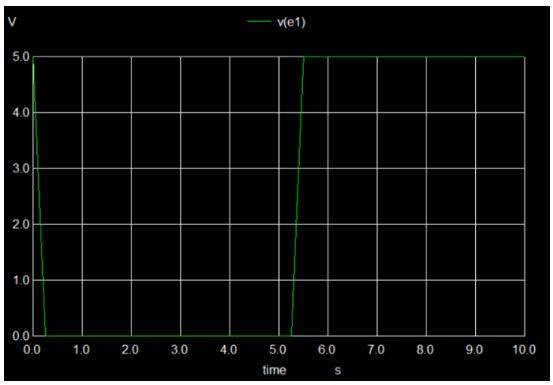
(b) Input plot (b1)



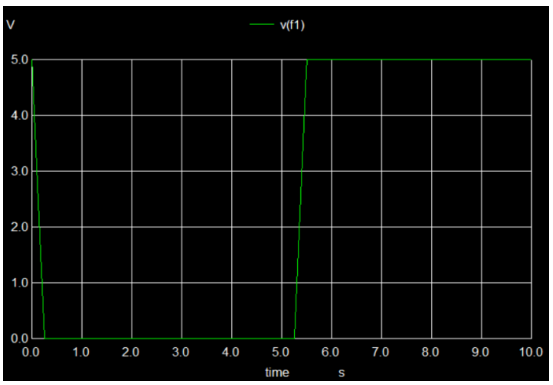
(c) Input plot (c1)



(d) Input plot (d1)



(e) Input plot (e1)



(f) Input plot (f1)

Figure 3.9: Input plots of IC DM74LS51

3.2.5 Output Plot

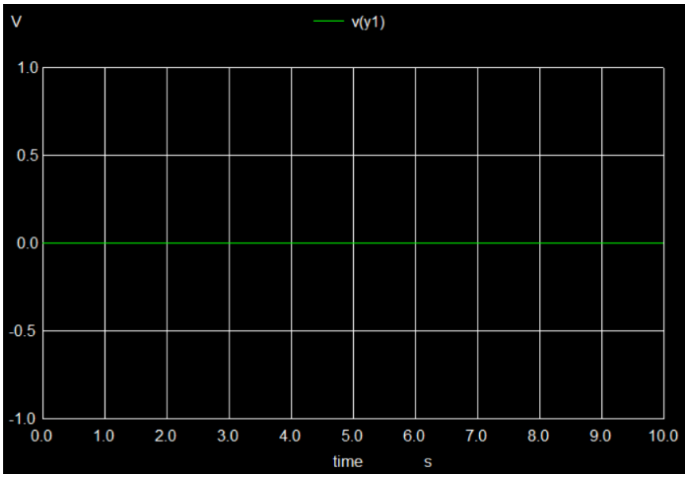


Figure 3.10: Output plot (y1)

3.3 F100102 Quint 2 Input OR/NOR Gate

The F100102 is a TTL-based IC that contains two independent 2-input OR/NOR gates. It features 10 input and 10 output pins, supporting multiple signal combinations with both true (OR) and complemented (NOR) outputs for each gate. Designed for high-speed logic systems, it provides fast response times and is typically used in control logic, data routing, and arithmetic logic units where dual-output logic is beneficial.

3.3.1 Pin Diagram

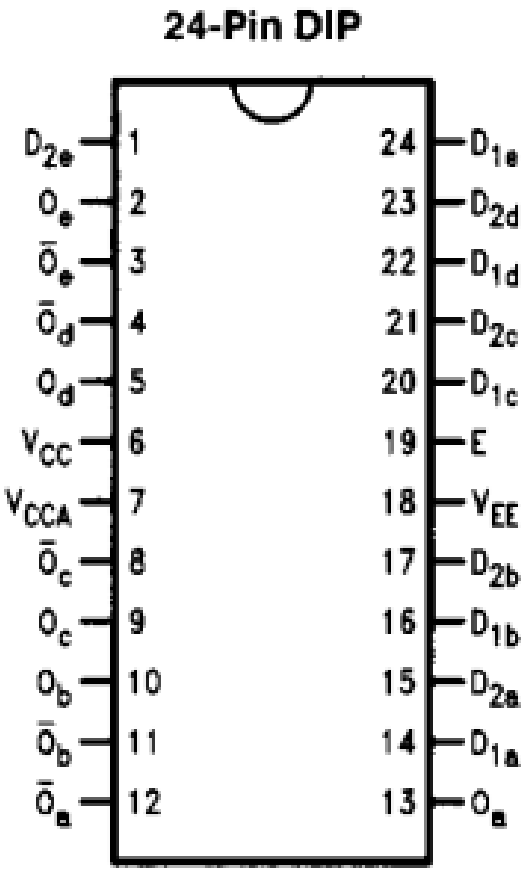


Figure 3.11: Pin configuration of IC F100102

3.3.2 Subcircuit Schematic Diagram

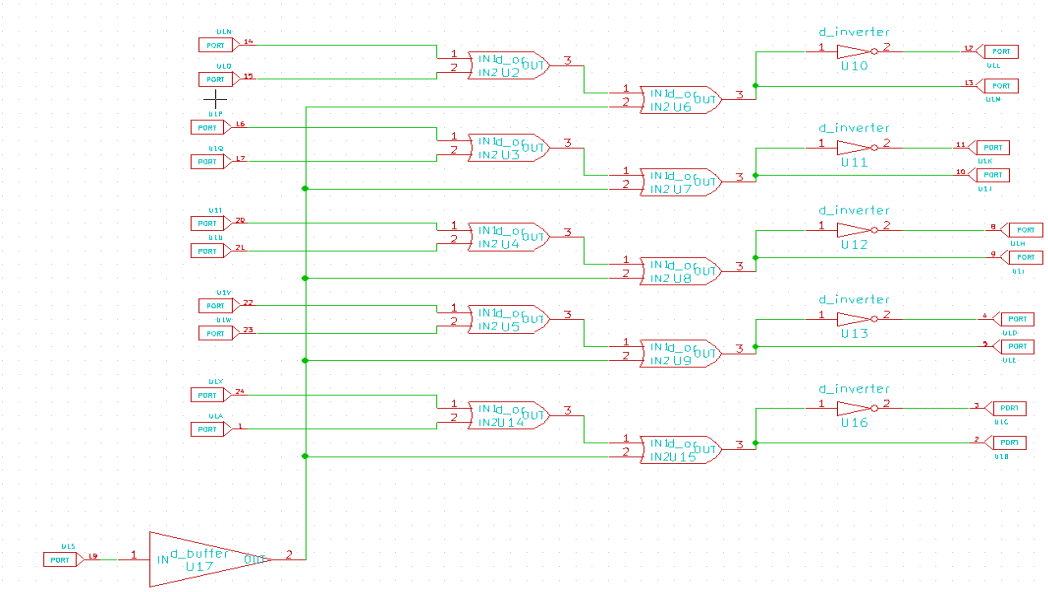


Figure 3.12: Subcircuit schematic diagram of IC F100102

3.3.3 Test Circuit

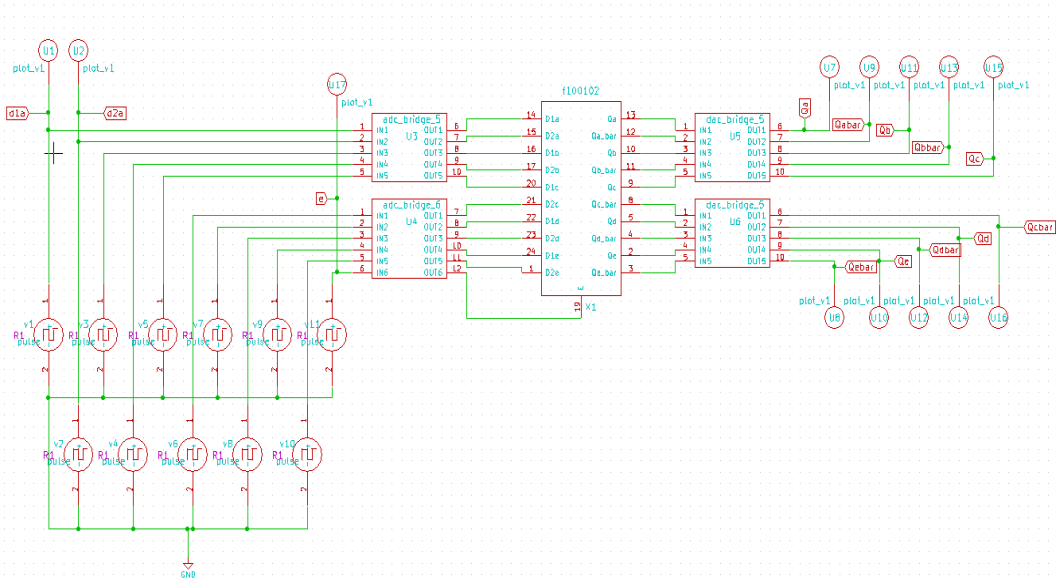
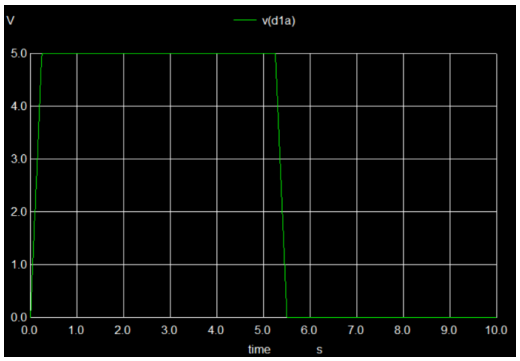
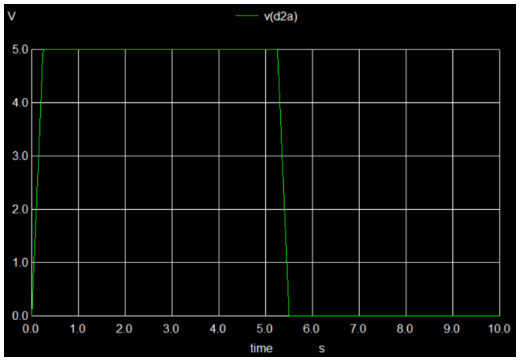


Figure 3.13: Test circuit of IC F100102 (OR Gate)

3.3.4 Input Plot



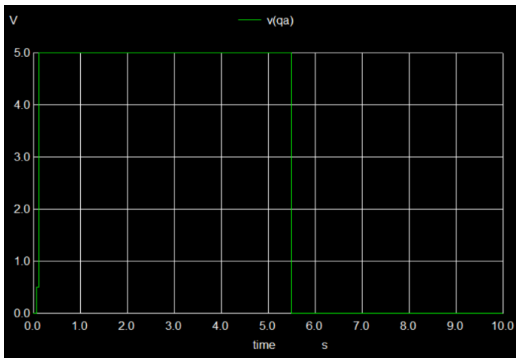
(a) Input plot (d1a)



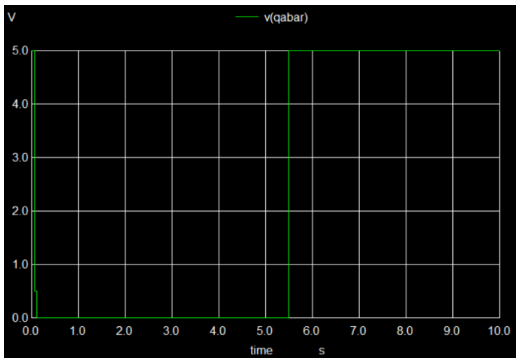
(b) Input plot (d2a)

Figure 3.14: Input plots of IC F100102

3.3.5 Output Plot



(a) Output plot (qa)



(b) Output plot (qabar)

Figure 3.15: Output plots of IC F100102

3.4 MC14560B NBCD Adder

The MC14560B is a 4-bit NBCD (Natural Binary Coded Decimal) adder IC that adds two 4-bit BCD numbers and outputs the result in NBCD format, along with a carry output. It supports active-high logic and is designed for decimal arithmetic operations in digital systems. Subtraction can be performed by pairing it with the MC14561B 9s Complementor. For addition without an input carry, the carry-in for the least significant digit is connected to VSS (logic low). This IC is commonly used in BCD-based calculators, counters, and arithmetic units.

3.4.1 Pin Diagram

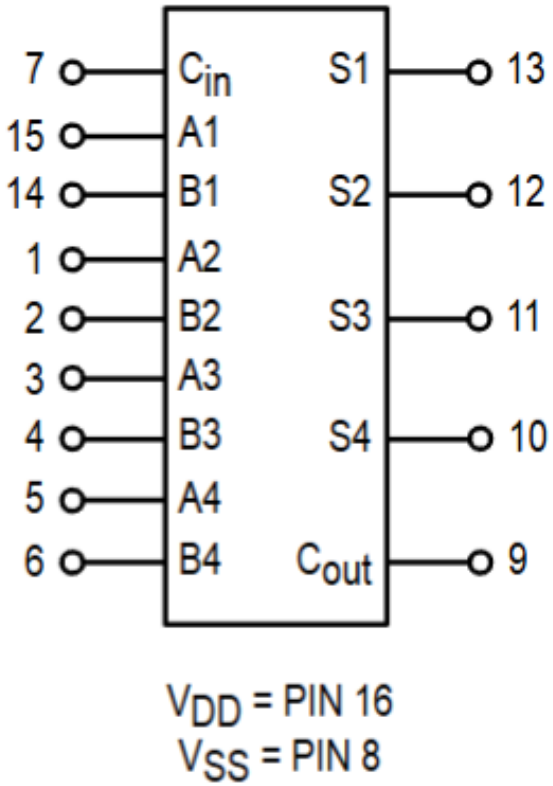


Figure 3.16: Pin configuration of IC MC14560B

3.4.2 Subcircuit Schematic Diagram

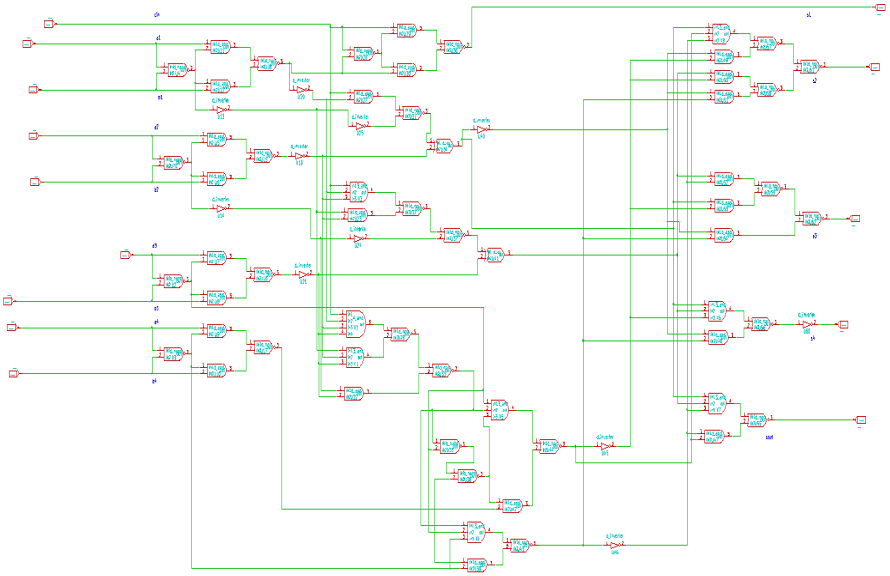


Figure 3.17: Subcircuit schematic diagram of IC MC14560B

3.4.3 Test Circuit

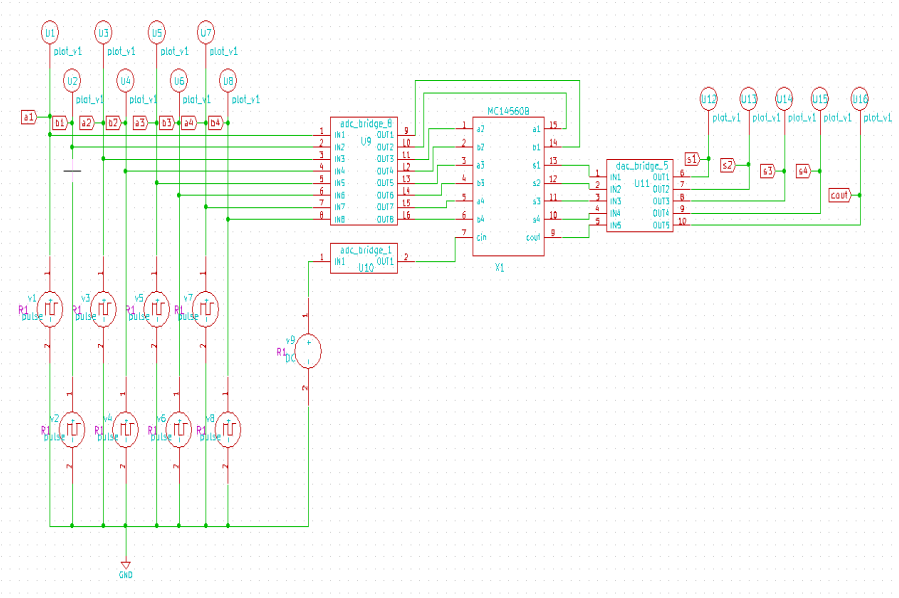
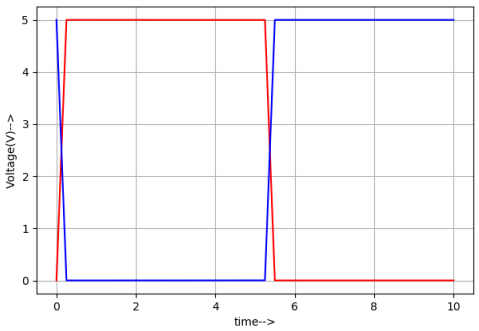
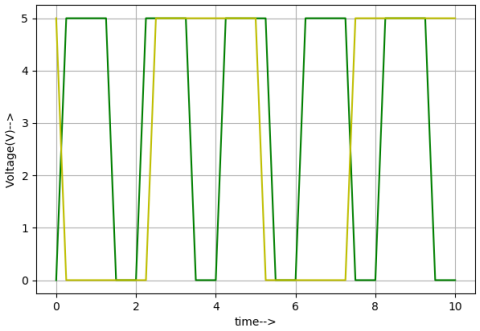


Figure 3.18: Test circuit of IC MC14560B

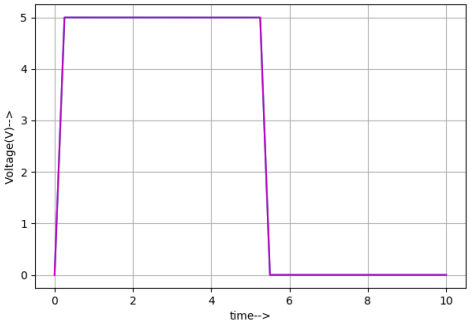
3.4.4 Input Plot



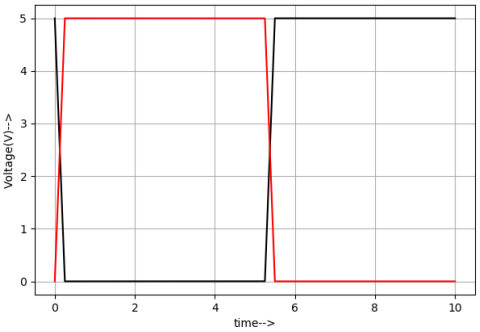
(a) Input plot (a4.1, a4.2)



(b) Input plot (a4.3, a4.4)



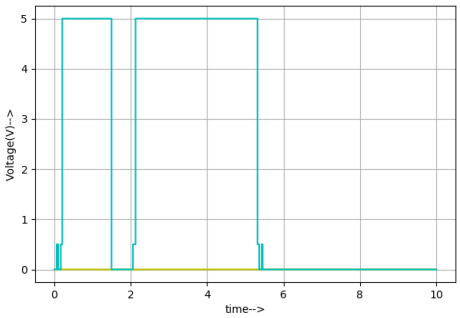
(c) Input plot (b4.1, b4.2)



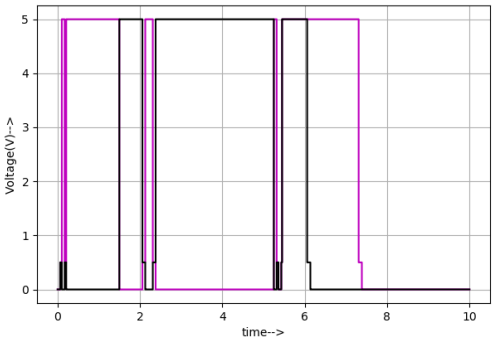
(d) Input plot (b4.3, b4.4)

Figure 3.19: Input plots of IC MC14560B

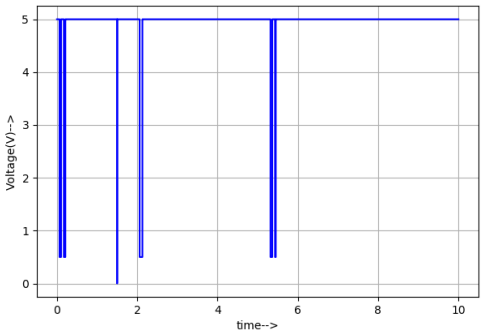
3.4.5 Output Plot



(a) Output plot (s1, s2)



(b) Output plot (s3, s4)



(c) Output plot (cout)

Figure 3.20: Output plots of IC MC14560B

3.5 CD4070B Quad CMOS-based XOR Logic Gate

The CD4070B is a CMOS-based logic IC that contains four independent 2-input Exclusive-OR (XOR) gates in a single 14-pin package. Each gate performs the XOR logic function, outputting HIGH only when the number of HIGH inputs is odd. This makes it useful in digital systems for operations like bit comparison, parity checking, and arithmetic logic implementations. The IC operates over a wide voltage range of 3V to 15V, offers low power consumption, high noise immunity, and is compatible with other CMOS and TTL logic families, making it ideal for both analog-digital interfacing and general-purpose logic design.

3.5.1 Pin Diagram

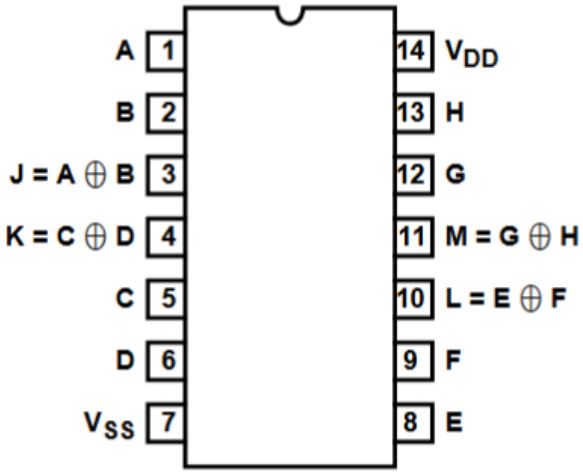


Figure 3.21: Pin configuration of IC CD4070B

3.5.2 Subcircuit Schematic Diagram

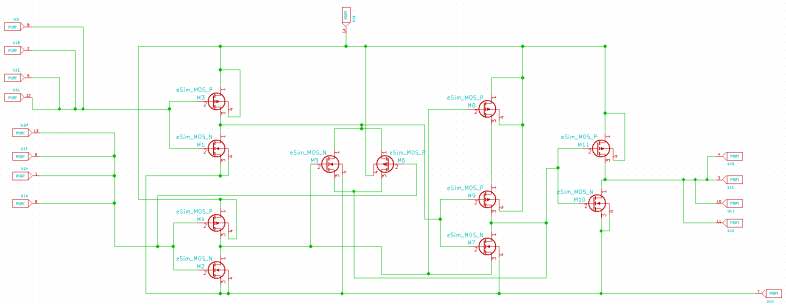


Figure 3.22: Subcircuit schematic diagram of IC CD4070B

3.5.3 Test Circuit

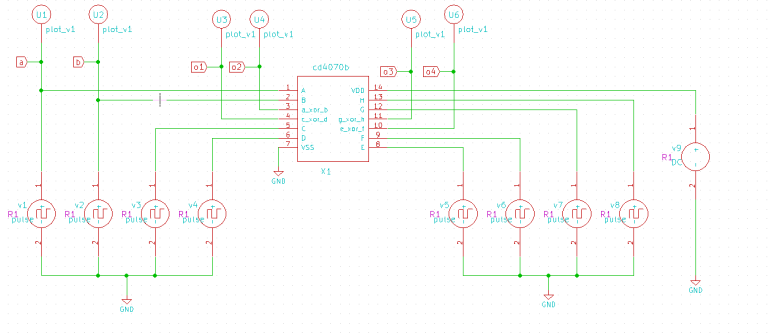
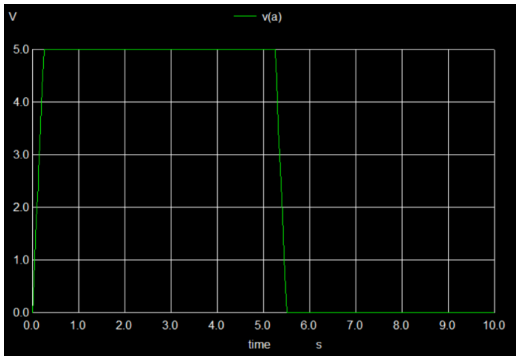
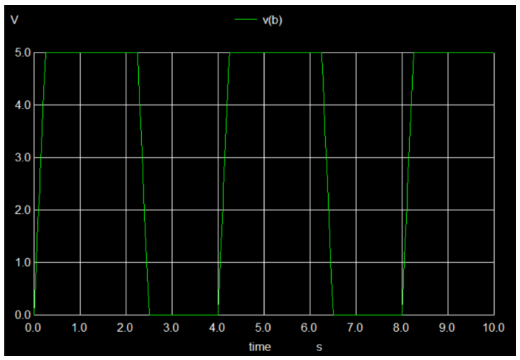


Figure 3.23: Test circuit of IC CD4070B

3.5.4 Input Plot



(a) Input plot (a)



(b) Input plot (b)

Figure 3.24: Input plots of IC CD4070B

3.5.5 Output Plot

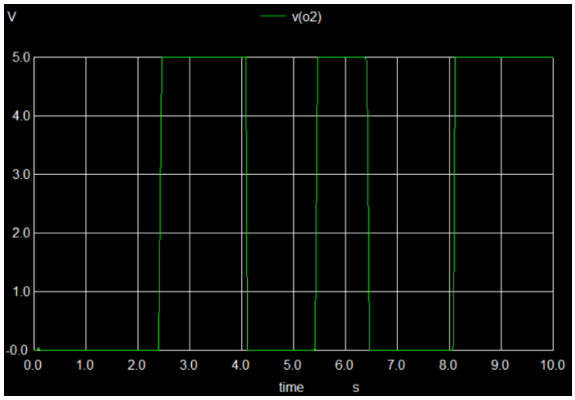


Figure 3.25: Output plot (o2)

3.6 CD4077B Quad CMOS-based XNOR Logic Gate

The CD4077B is a CMOS logic IC that contains four independent 2-input Exclusive-NOR (XNOR) gates in a single 14-pin package. Each gate performs the XNOR logic function, outputting HIGH only when both inputs are the same (either both HIGH or both LOW). It operates over a wide voltage range of 3V to 15V, features low power consumption, and provides high noise immunity. The CD4077B is widely used in equality comparison, logic verification, parity generation, and error detection circuits in digital systems.

3.6.1 Pin Diagram

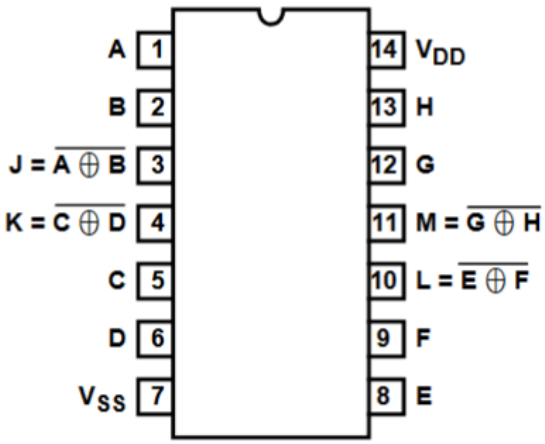


Figure 3.26: Pin configuration of IC CD4077B

3.6.2 Subcircuit Schematic Diagram

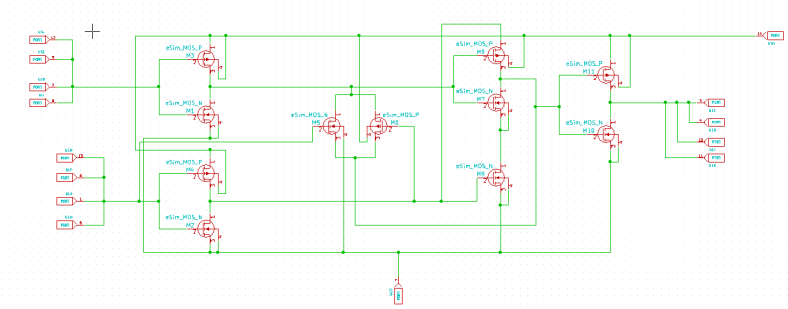


Figure 3.27: Subcircuit schematic diagram of IC CD4077B

3.6.3 Test Circuit

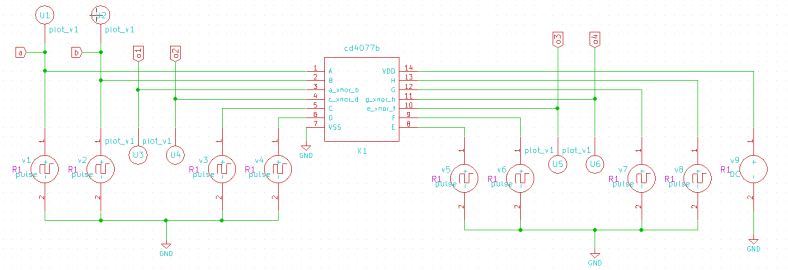
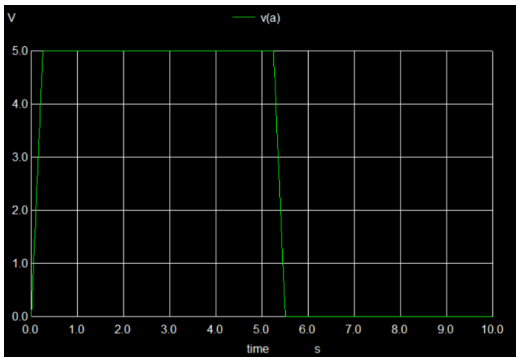
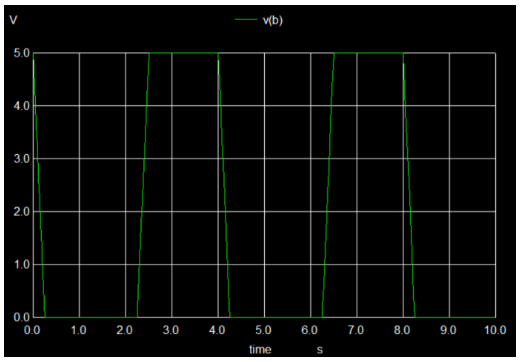


Figure 3.28: Test circuit of IC CD4077B (XNOR Gate)

3.6.4 Input Plot



(a) Input plot (6a)



(b) Input plot (6b)

Figure 3.29: Input plots of IC CD4077B

3.6.5 Output Plot

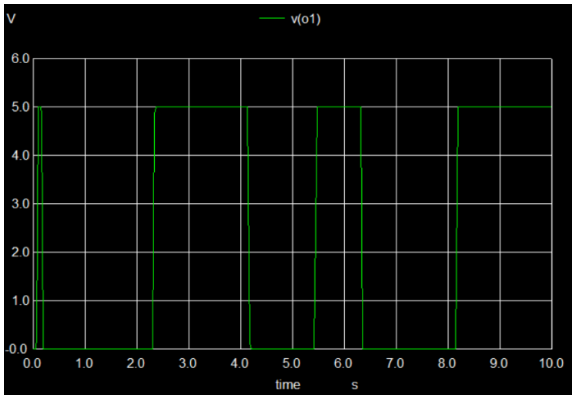


Figure 3.30: Output plot (o1)

3.7 MC1496 Balanced Modulator

The MC1496 / MC1496B is a balanced modulator/demodulator IC designed to produce an output that is the product of two input signalstypically a carrier and a modulating signal. It is widely used in applications requiring signal multiplication, such as amplitude modulation (AM), suppressed carrier modulation, synchronous detection, FM detection, phase detection, and chopper circuits. The IC offers high linearity and good carrier suppression, making it ideal for analog communication systems and signal processing tasks where precise modulation or demodulation is required.

3.7.1 Pin Diagram

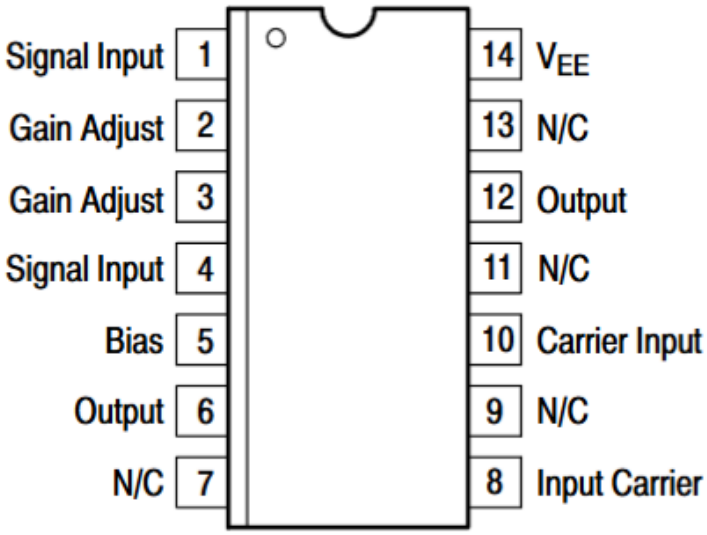


Figure 3.31: Pin configuration of IC MC1496

3.7.2 Subcircuit Schematic Diagram

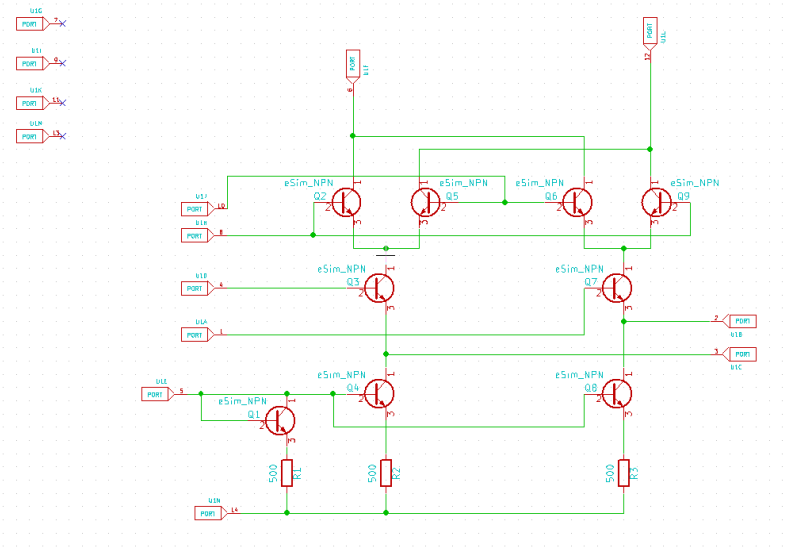


Figure 3.32: Subcircuit schematic diagram of IC MC1496

3.7.3 Test Circuit

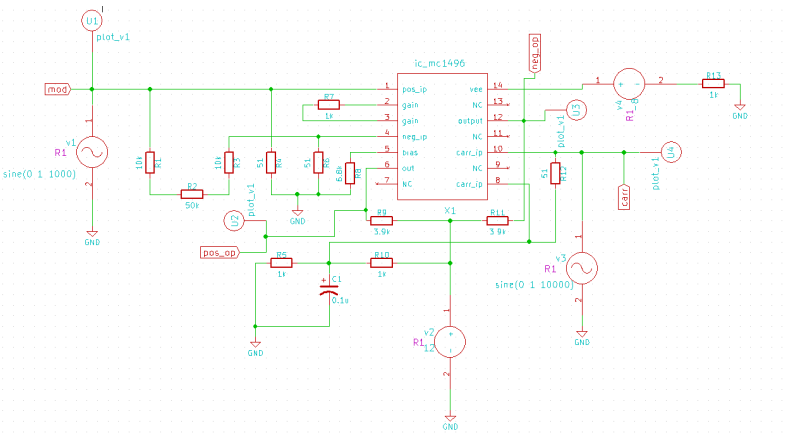
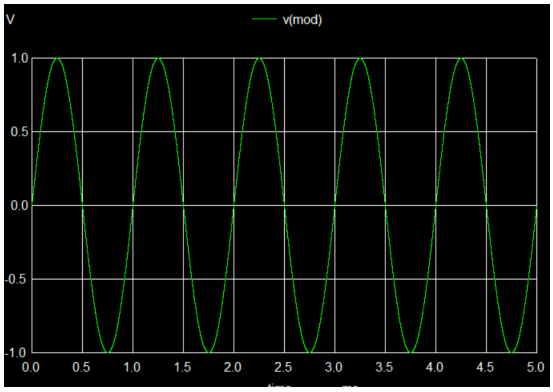
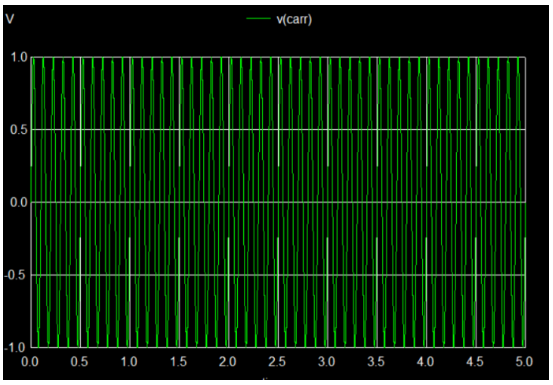


Figure 3.33: Test circuit of IC MC1496

3.7.4 Input Plot



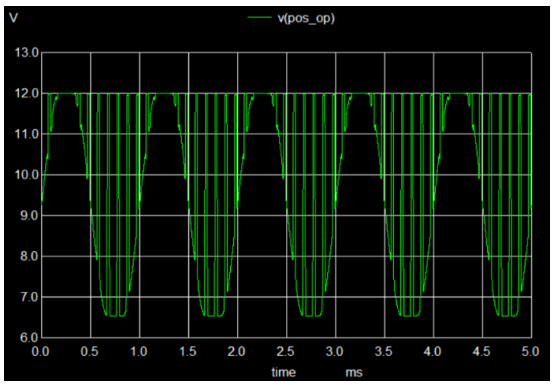
(a) Input plot (mod)



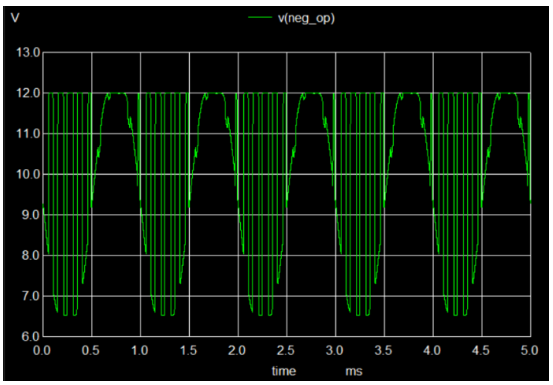
(b) Input plot (carr)

Figure 3.34: Input plots of IC MC1496

3.7.5 Output Plot



(a) Output plot (positive output)



(b) Output plot (negative output)

Figure 3.35: Output plots of IC MC1496

3.8 DM74S182 Look-ahead Carry Generators

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each DM74S182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data. Carry input and output of the ALUs are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU.

Reinterpretations of carry functions, as explained on the 181 datasheet, are also applicable to and compatible with the look-ahead generator. Positive logic equations for the DM74S182 are given below:

$$C_{n+x} = \overline{G}0 + \overline{P}0\, C_n$$

$$C_{n+y} = \overline{G}1 + \overline{P}1\,\overline{G}0 + \overline{P}1\,\overline{P}0\, C_n$$

$$C_{n+z} = \overline{G}2 + \overline{P}2\,\overline{G}1 + \overline{P}2\,\overline{P}1\,\overline{G}0 + \overline{P}2\,\overline{P}1\,\overline{P}0\, C_n$$

$$\overline{G} = \overline{G}3\,(\overline{P}3 + \overline{G}2)\,(\overline{P}3 + \overline{P}2 + \overline{G}1)\,(\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$$

$$\overline{P} = \overline{P}3\,\overline{P}2\,\overline{P}1\,\overline{P}0$$

Figure 3.36: Positive logic equations of DM74S182

3.8.1 Pin Diagram

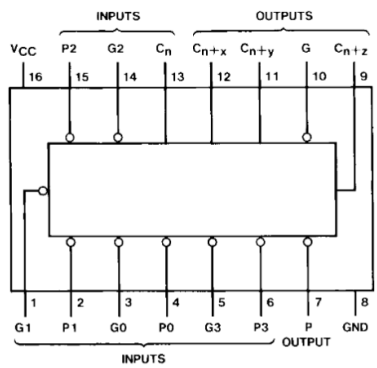


Figure 3.37: Pin configuration of IC DM74S182

3.8.2 Subcircuit Schematic Diagram

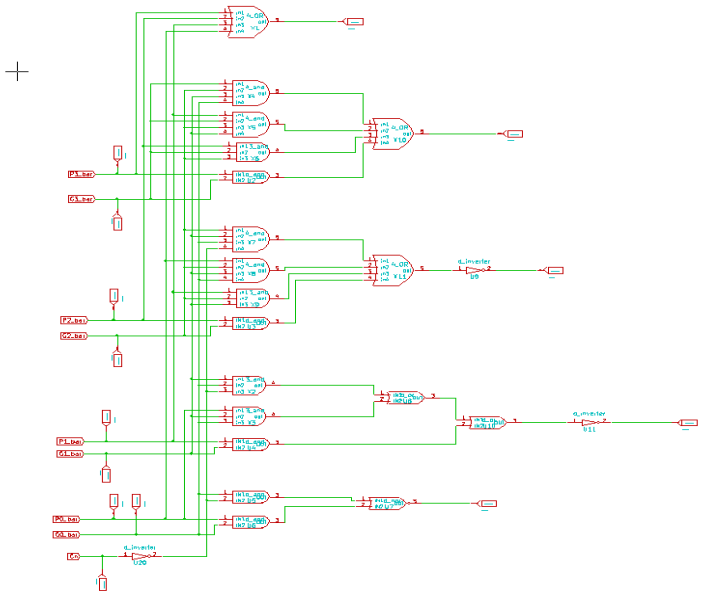


Figure 3.38: Subcircuit schematic diagram

3.8.3 Test Circuit

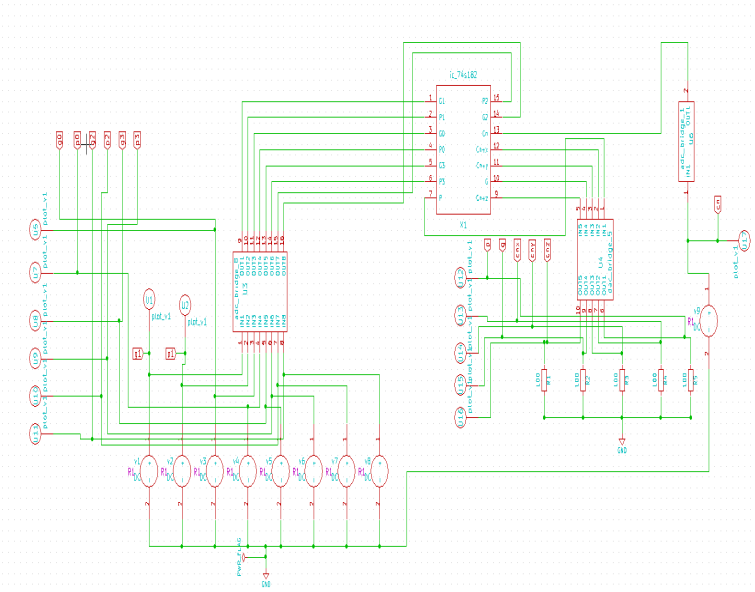
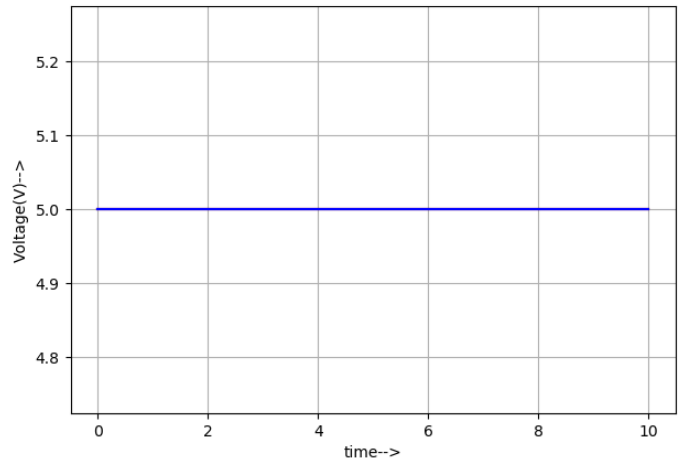
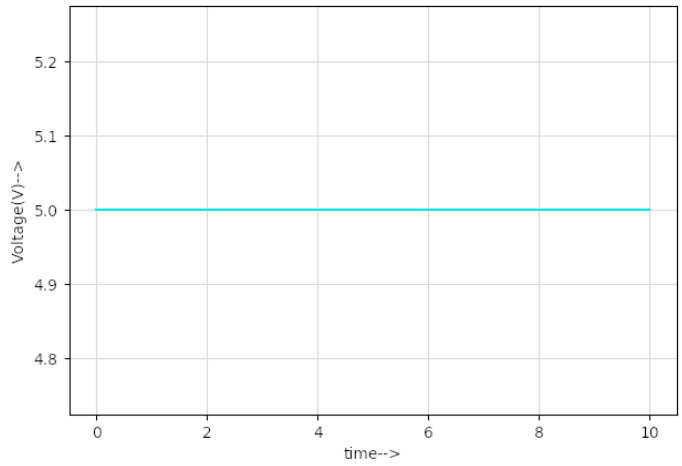


Figure 3.39: IC DM74S182 test circuit

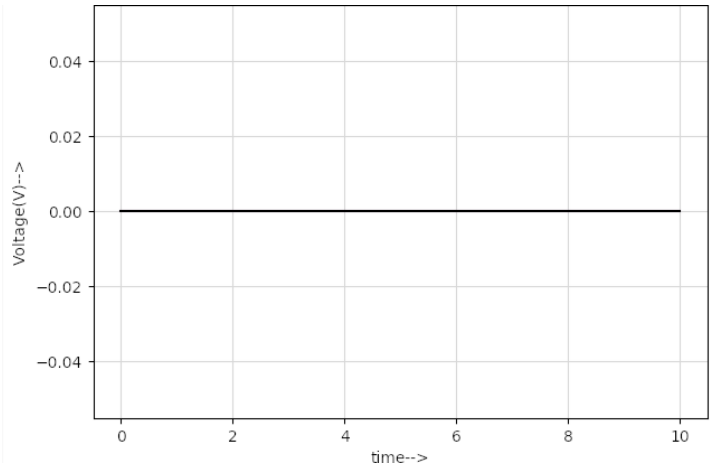
3.8.4 Input Plot



(a) Input plot (g0, g1, g2)



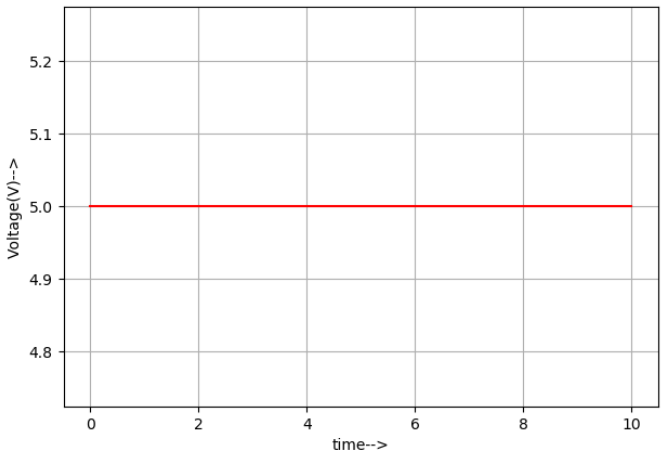
(b) Input plot (p0, p1)



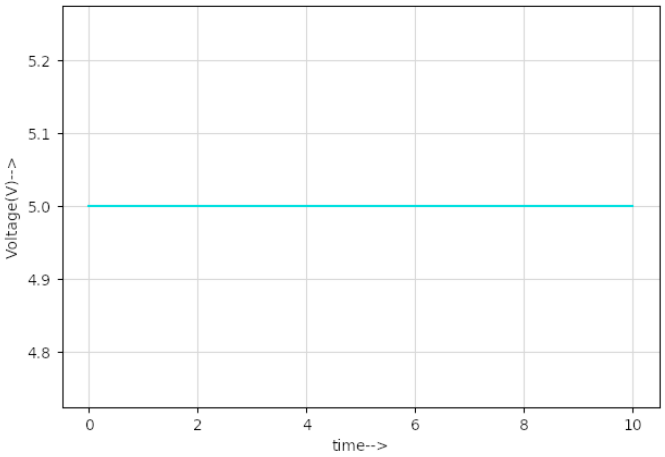
(c) Input plot (p2, p3)

Figure 3.40: Input plots of IC DM74S182

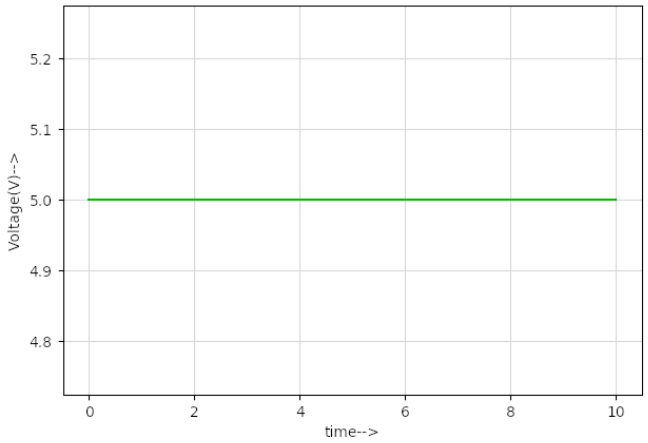
3.8.5 Output Plot



(a) Output plot (Cn)



(b) Output plot (G)



(c) Output plot (P)

Figure 3.41: Output plots of IC DM74S182

3.9 TC4008BP Parallel Processing Full Adder

The TC4008BP is a 4-bit full adder of parallel processing type equipped with a high-speed parallel carry circuit. The sum of binary inputs applied to four augend data input lines (A1A4), four addend data input lines (B1B4), and a carry input (CIN) from the lower order is obtained in binary code from added data outputs (S1S4) and a carry output (COUT) to the higher order. Adders of 4 n bits with cascade connections and add/subtract circuits with simple external circuitry can be easily implemented.

3.9.1 Pin Diagram

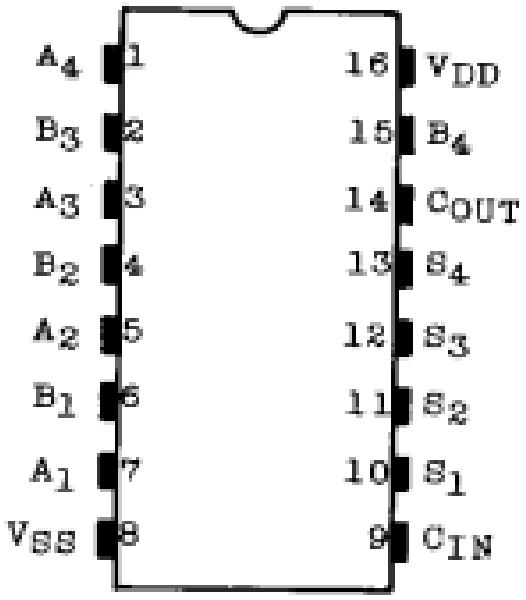


Figure 3.42: Pin configuration of IC TC4008BP

3.9.2 Subcircuit Schematic Diagram

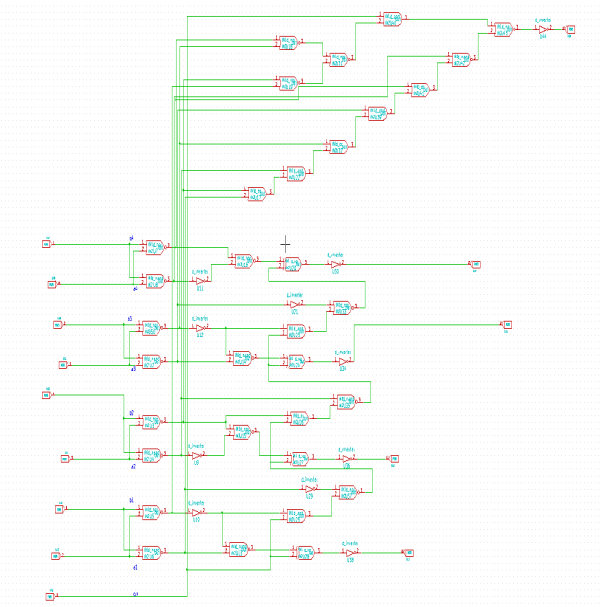


Figure 3.43: Subcircuit schematic diagram

3.9.3 Test Circuit

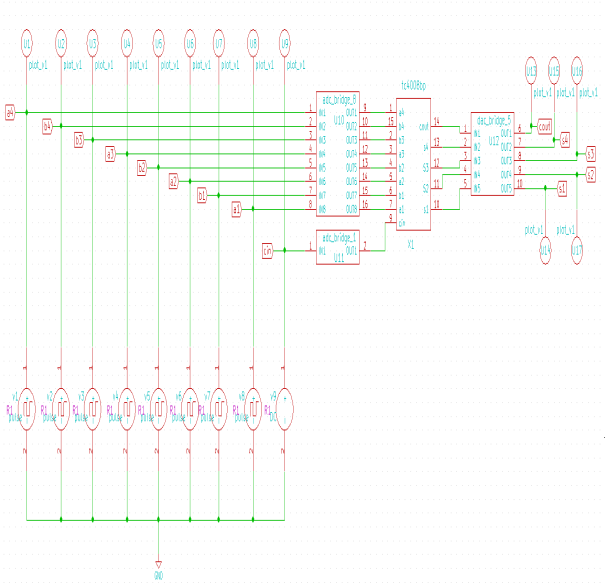
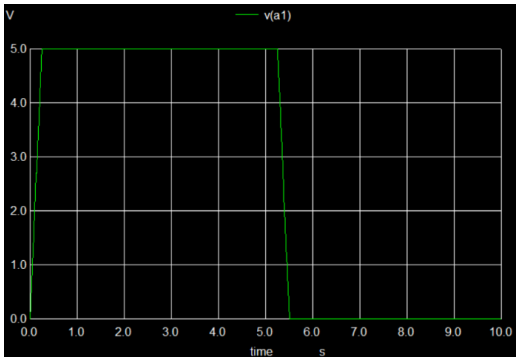
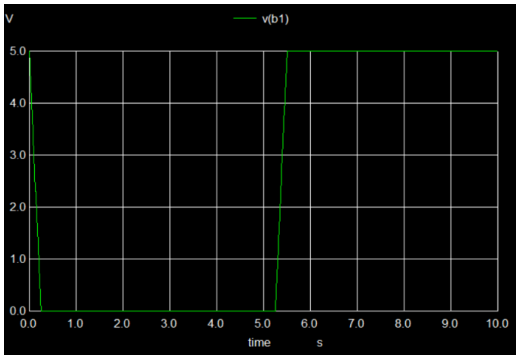


Figure 3.44: IC TC4008BP test circuit

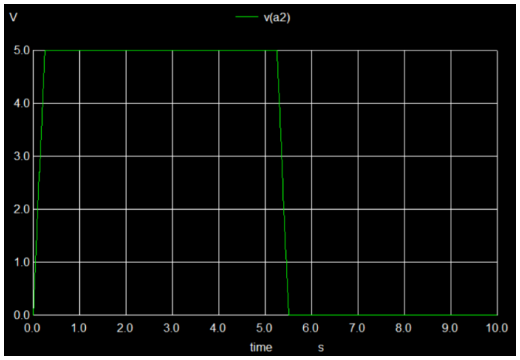
3.9.4 Input Plots



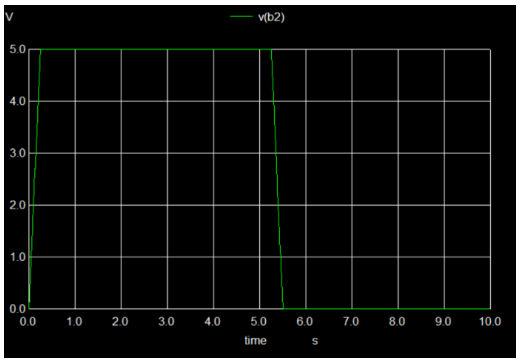
(a) Input plot (a1)



(b) Input plot (b1)

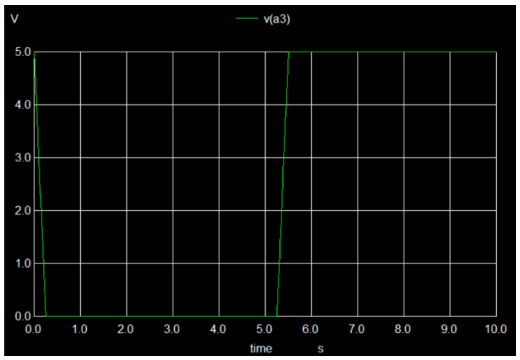


(c) Input plot (a2)

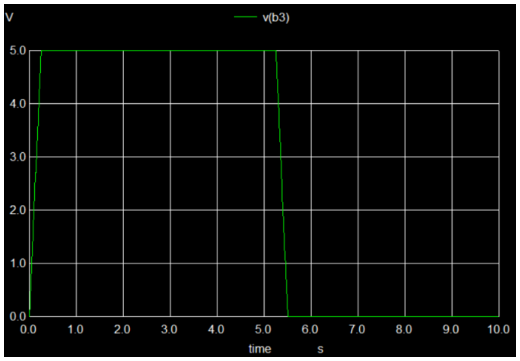


(d) Input plot (b2)

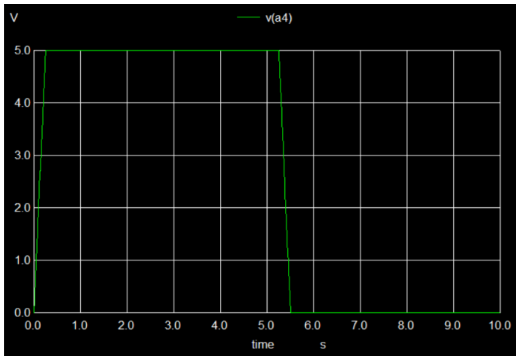
Figure 3.45: Input plots of IC TC4008BP (Part 1)



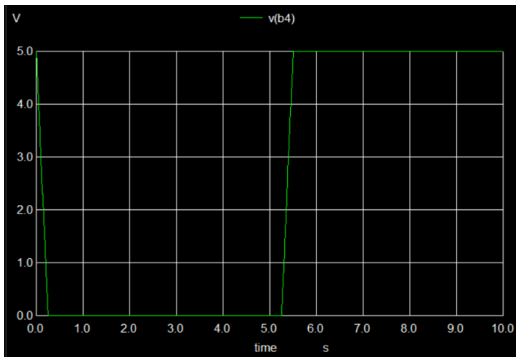
(a) Input plot (a3)



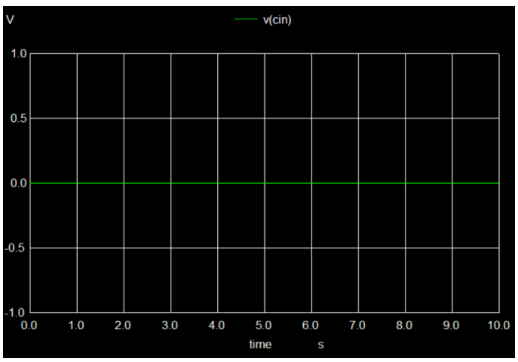
(b) Input plot (b3)



(c) Input plot (a4)



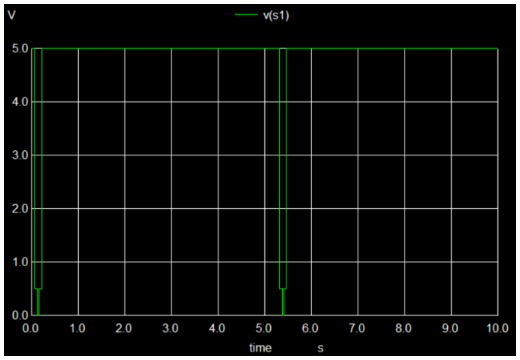
(d) Input plot (b4)



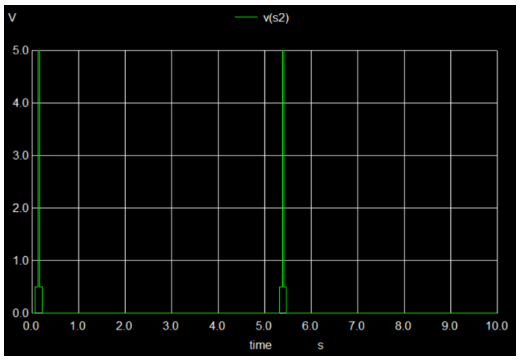
(e) Input plot (cin)

Figure 3.46: Input plots of IC TC4008BP (Part 2)

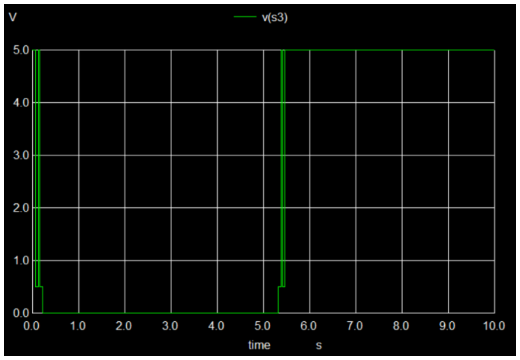
3.9.5 Output Plots



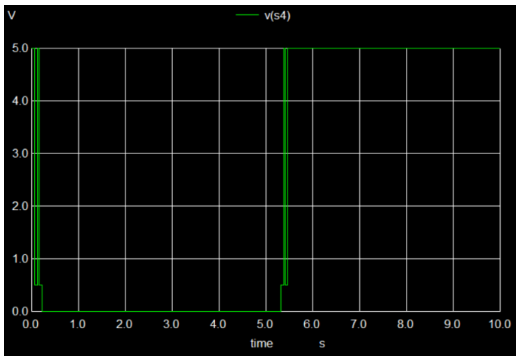
(a) Output plot (s1)



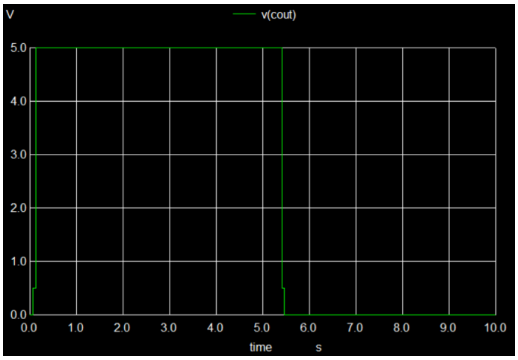
(b) Output plot (s2)



(c) Output plot (s3)



(d) Output plot (s4)



(e) Output plot (cout)

Figure 3.47: Output plots of IC TC4008BP

3.10 100117 Triple 1-2-2 Input OR-AND / OR-AND-INVERT Gate

The 100117 is a digital logic IC comprising three independent logic gates, each implementing a 1-2-2 input OR-AND or OR-AND-INVERT (OAI) function. These gates perform high-speed logic operations suitable for complex combinational logic applications. Each gate accepts five inputs grouped as one, two, and two inputs, which are first ORed and then ANDed (with optional inversion at the output). This IC is ideal for arithmetic logic circuits, programmable logic arrays, and custom logic design implementations.

3.10.1 Pin Diagram

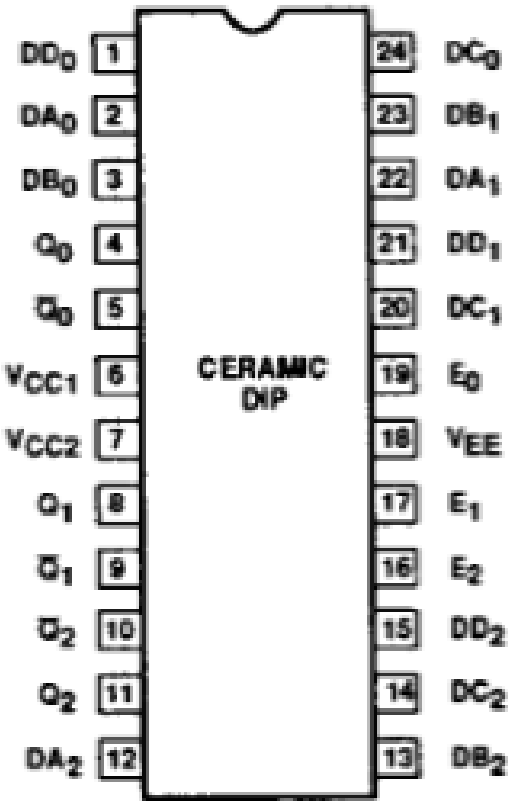


Figure 3.48: Pin configuration of IC 100117

3.10.2 Subcircuit Schematic Diagram

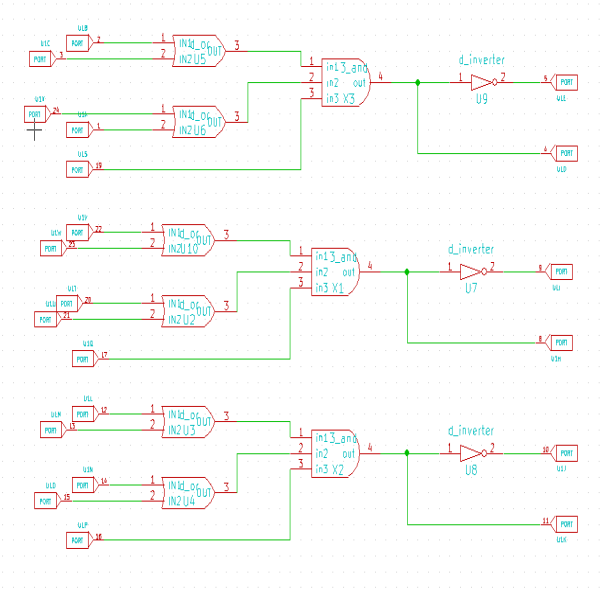


Figure 3.49: Subcircuit schematic diagram

3.10.3 Test Circuit

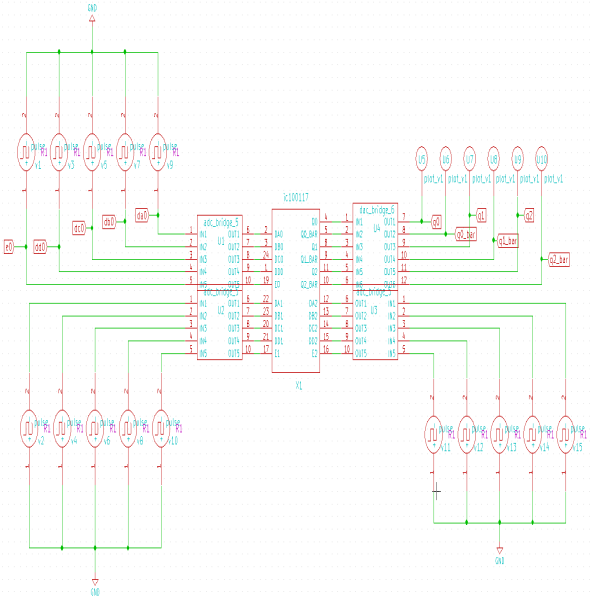
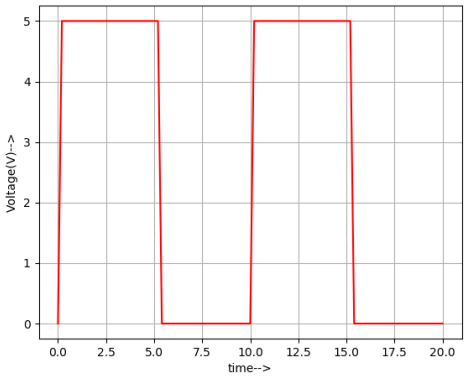
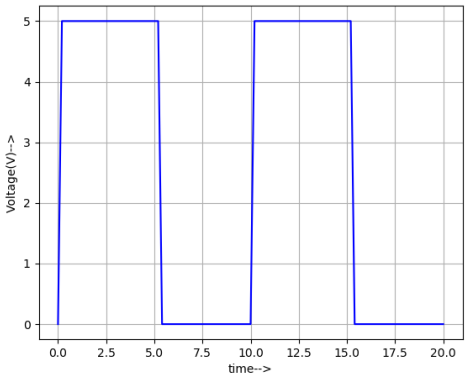


Figure 3.50: IC 100117 test circuit

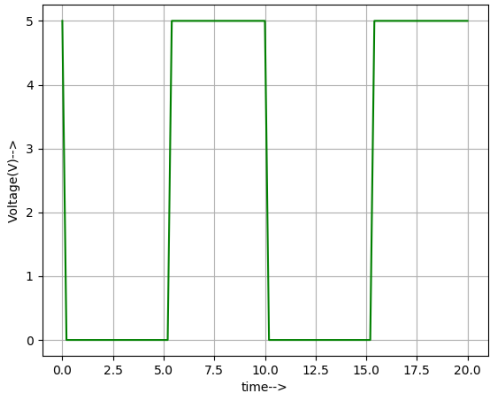
3.10.4 Input Plots



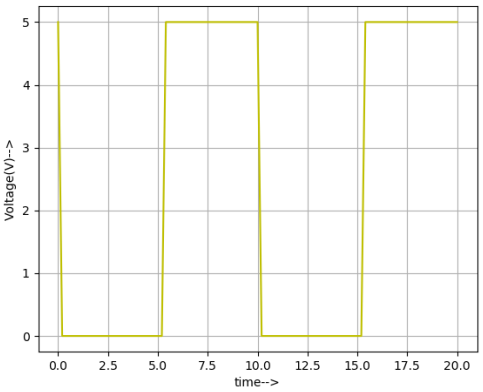
(a) Input plot (da0)



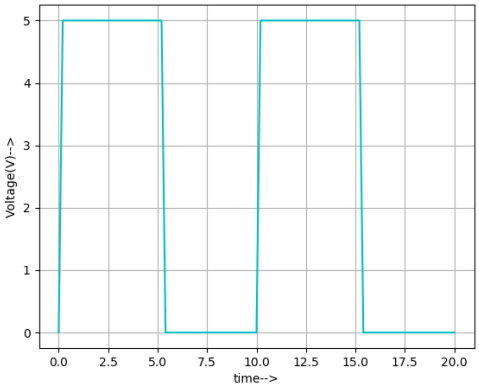
(b) Input plot (db0)



(c) Input plot (dc0)



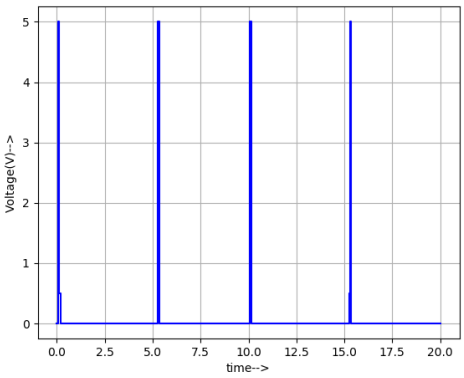
(d) Input plot (dd0)



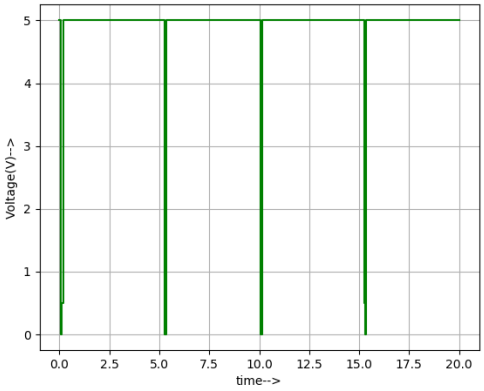
(e) fig:Input plot (de0)

Figure 3.51: Input plots of IC 100117

3.10.5 Output Plots



(a) Output plot (q0)



(b) Output plot (q0_bar)

Figure 3.52: Output plots of IC 100117

3.11 54F64 4-2-3-2-input AND-OR-INVERT (AOI) IC

The 54F/74F64 is a high-speed TTL logic IC that implements a 4-2-3-2-input AND-OR-INVERT (AOI) function. It contains gates arranged to perform a specific combination of logic: multiple AND gates receive 4, 2, 3, and 2 inputs respectively, whose outputs are then OR ed together and the result is inverted. This compact configuration allows the implementation of complex logic expressions with fewer components. The IC is typically used in arithmetic units, control logic, and signal decoding where efficient multi-input logic processing is required.

3.11.1 Pin Diagram

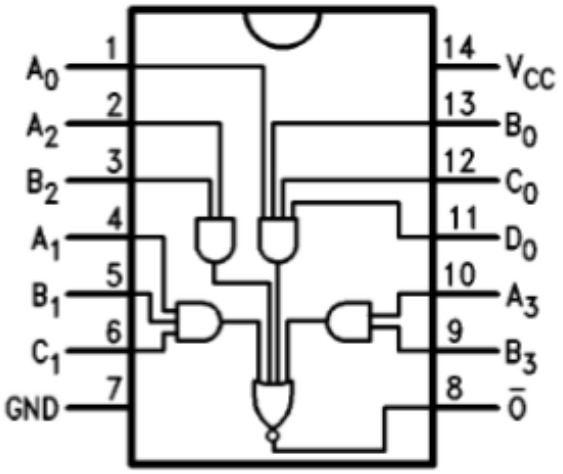


Figure 3.53: Pin configuration of IC 54F64

3.11.2 Subcircuit Schematic Diagram

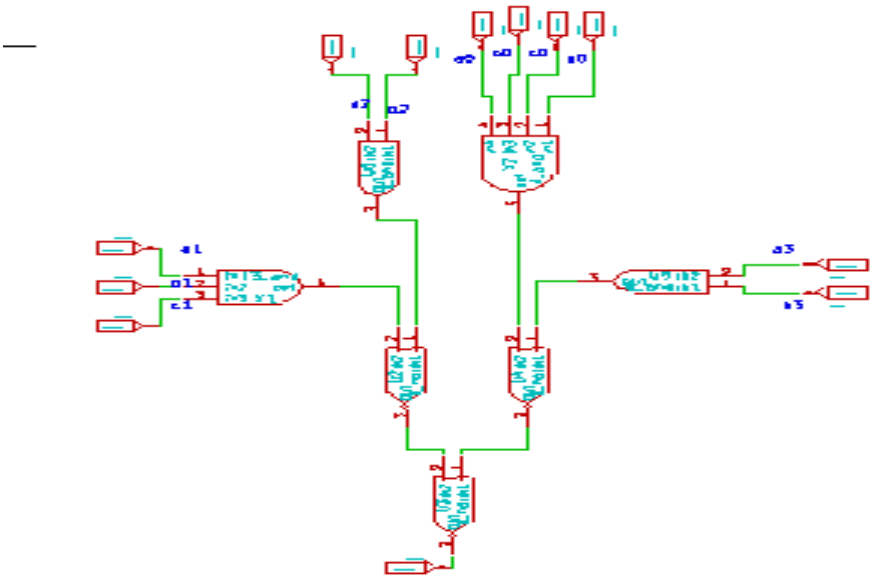


Figure 3.54: Subcircuit schematic diagram

3.11.3 Test Circuit

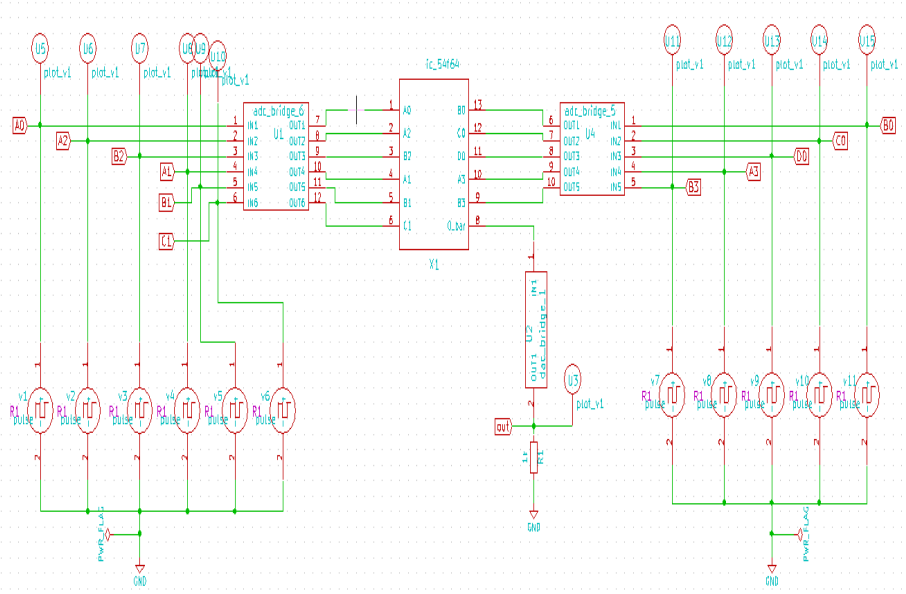
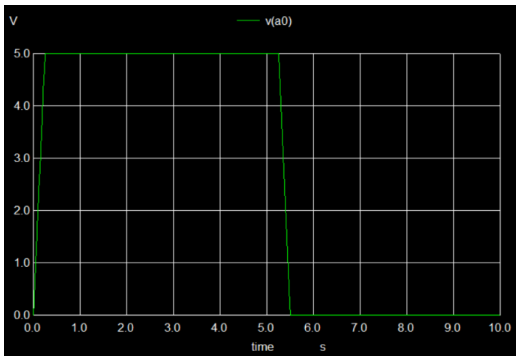
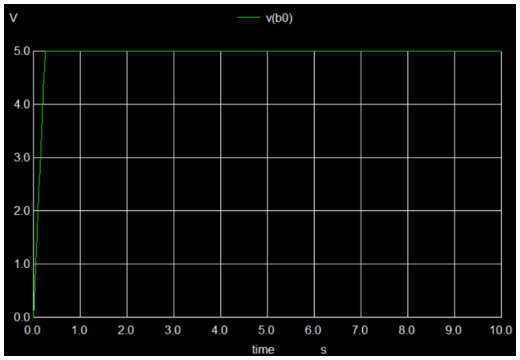


Figure 3.55: IC 54F64 test circuit

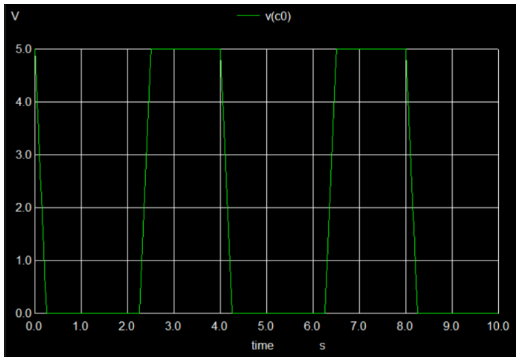
3.11.4 Input Plot



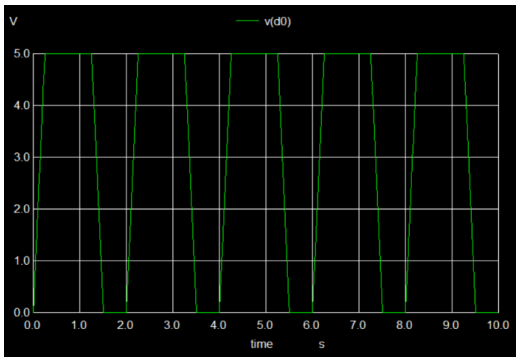
(a) 8a0



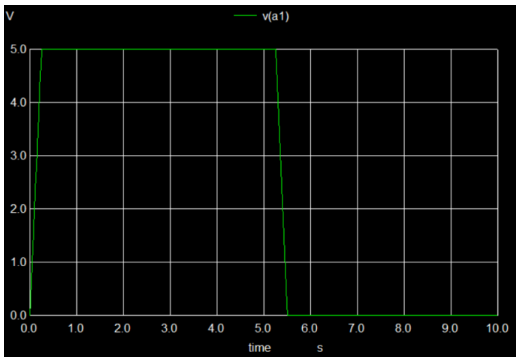
(b) 8b0



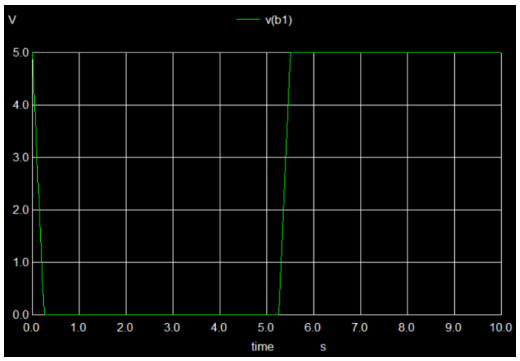
(c) 8c0



(d) 8d0

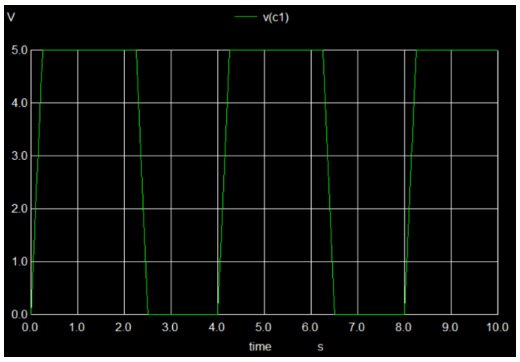


(e) 8a1

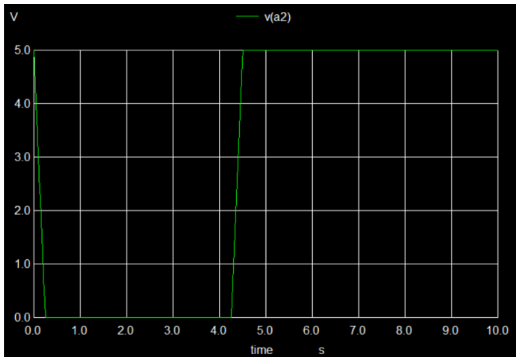


(f) 8b1

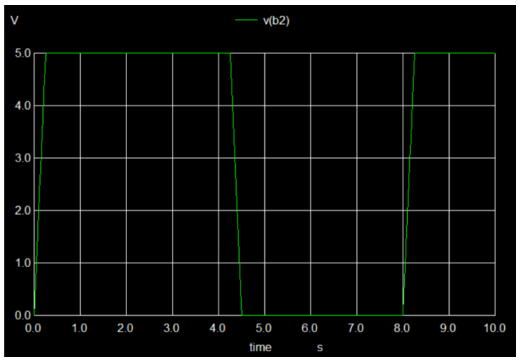
Figure 3.56: Input plots of IC 54F64 (Set 1)



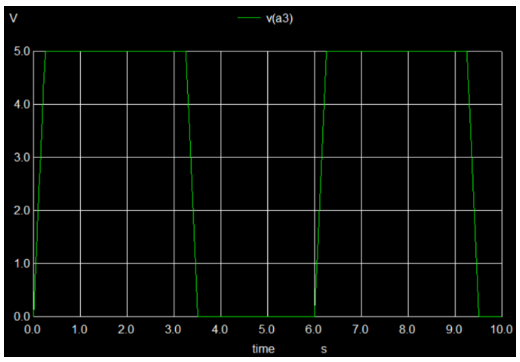
(a) 8c1



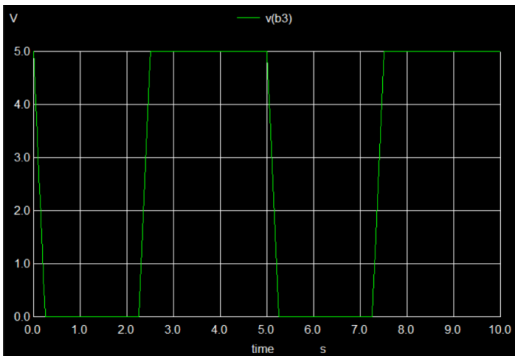
(b) 8a2



(c) 8b2



(d) 8a3



(e) 8b3

Figure 3.57: Input plots of IC 54F64 (Set 2)

3.11.5 Output Plot

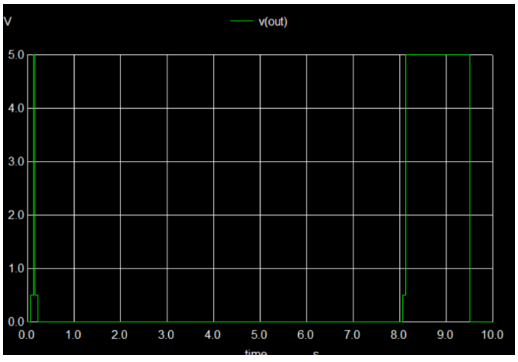


Figure 3.58: Output plot (8out)

Chapter 4

Conclusion and Future Scope

During this fellowship, I explored and modelled a variety of digital and analog IC subcircuits, closely adhering to their datasheet specifications. The project involved building and verifying functional blocks such as Carry Look-Ahead Adders, NBCD Arithmetic Units, CMOS XOR/XNOR gates, Product Modulators, AOI (AND-OR-Invert) logic, and configurable logic modules like OR/NOR and expandable gate arrays. Each design was thoroughly tested using *eSim*, with validation carried out through realistic simulation setups to ensure reliability and correctness.

These verified modules are now prepared for integration into the official `esim_subckt` library, where they can serve as reusable, drop-in components for academic projects, electronic design training, and open-source circuit development. This contribution helps broaden the reach of *eSim* as a practical tool for learning and prototyping in digital and mixed-signal domains.

Moving ahead, there is great potential to extend this work by introducing more complex building blockssuch as programmable ALUs, combinational decoders, priority encoders, memory cells, or DSP elements. Such enhancements can transform *eSim* into a go-to platform for system-level design, encouraging deeper experimentation and innovation in electronics education and research.

Chapter 5

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6. https://www.nxp.com/design/documentation:DOCUMENTATION#/
7. https://www.datasheet4u.com/Manufacture/National%20Semiconductor.php?c=7

IC Datasheets

1. SN74AUP1G58 https://www.alldatasheet.com/datasheetpdf/view/107169/TI/SN74AUP1G58.html
2. DM74LS51 https://www.alldatasheet.com/view.jsp?Searchword=DM74LS51
3. F100102 https://www.alldatasheet.com/datasheetpdf/view/121482/NSC/F100102.html
4. MC14560B https://www.alldatasheet.com/datasheetpdf/view/894428/MOTOROLA/MC14560B.html
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6. CD4077B https://www.alldatasheet.com/datasheetpdf/view/26886/TI/CD4070B.html

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