Single-Inductor Boost Converter With Ultrahigh Step-Up Gain, Lower Switches Voltage Stress, Continuous Input Current, and Common Grounded Structure

Shan Miao, *Member, IEEE*, Wei Liu, and Jinfeng Gao

***Abstract*—DC–DC boost converters with better performances, including improved voltage gain, efficiency, power density, and reliability, are urgently needed for wide conversion range applications. In this article, a single-inductor boost converter (SLBC) with ultrahigh voltage boosting capability is proposed and analyzed. For the SLBC, low-voltage-rating MOSFET with small on-resistance can be chosen and losses of switches can be reduced owing to the lower switches voltage stress and intrinsic small duty cycle, which are conducive to enhance the system efficiency. The single inductor of the SLBC is in series with its input source, therefore, continuous input current and high power density are attainable. Moreover, the SLBC has common grounded input and output terminals, which is benefit to avoid the d*u*/d*t* issues and achieve reliable output. The operational principles of steady-state mode and small-signal mode are presented to analyses the SLBC in detail. Based on these, performance comparisons with other typical converters and 250-W experiment prototype are implemented to validate the feasibility and effectiveness of the SLBC.**

***Index Terms*—DC–DC boost converter, lower voltage stress, single inductor, ultrahigh voltage gain.**

I. Introduction

AS AN important part of the future intelligent power distribution system, dc microgrid can efficiently and reliably integrate distributed renewable energy generation system, energy storage unit, electric vehicle, and other electric loads. Dc–dc converters, which are the key link to realize energy transfer between the units of dc microgrid [1]–[3], are widely researched and applied recently.

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With the proper turn ratio of transformers, isolated converters can realize electrical isolation and high voltage gain. Applying the energy regenerative snubber and bipolar voltage multiplier structure, an isolated boost converter which possesses soft switching and flexible gain extension is presented in [4]. In [5], a three-switch isolated boost converter with continuous input current, reduced one active switch, added passive components, and no snubber circuit is analyzed. However, for the nonisolated applications, the adopted transformer will increase the system volume, cost, and weight.

Coupled inductor converters are one of the typical dc–dc converter topology types. Combining with interleaved strategy, two kinds of transformerless boost converters with lower ripples are presented in [6] and [7]. The former converter has better dynamic response and reduced efficiency while the latter converter possesses small duty cycle range and zero current switching. With two hybrid voltage multiplier cells, a three-winding coupled inductor converter is presented in [8]. A boost converter is analyzed in [9] by merging different switched-capacitor techniques and coupled inductor. In [10], deriving by the association of coupled inductor, boost cells, voltage multiplier, switched capacitors and *LC* filter cells, a series of hybrid boost converters are studied and analyzed. The abovementioned converters in [8]–[10] all are single switch structures, but, more passive components are needed to construct these topologies.

Adopting the switched-network cells, many dc–dc converters with improved features are analyzed. Combining diode-capacitor circuit with boost and single ended primary inductor converter (SEPIC) converter, a boost converter which has small input ripple, common grounded terminals and limited step-up gain is analyzed in [11]. In [12], by utilizing switched-capacitor multiplier and an integrated LC^2D network, a single-switch boost converter with floating output terminal is presented. With switched-capacitor cells, two kinds of dual-switch boost converters are analyzed. The dual-switch boost converter in [13] has single-inductor structure and high step-up gain while its output voltage is floating. The dual-switch boost converter in [14] realizes high voltage gain while its topological structure is complex. Comprising the interleaved structure and modified Dickson voltage multipliers, two kinds of boost converters with high voltage gains and small input ripples are analyzed in [15] and

[16]. But, the input and output terminals of these two topologies both have no common node. Based on two types of active-passive inductor cells, [17], [18] construct boost converters with extendable structures. Adopting an active switched capacitor network and an active switched inductor network, a boost converter is analyzed in [19]. Combining switched-capacitor/switched-inductor cells with traditional switched-boost network, a family of boost converters is presented in [20]. Based on a passive switched-capacitor network and an active switched-inductor network, a boost converter is analyzed in [21]. However, the input currents of converters in [17]–[21] are discontinuous and the input terminals of these converters have no common ground with their output terminals. In [22], a passive switched-network cell is adopted to construct and extend a negative output boost converter. In [23], a boost converter which combines two charge pump cells with a switched inductor is presented. This converter adopts six switches and operates in three different working modes while its input current is discontinuous.

Z-source and quasi-Z-source structures are also effective methods to construct converters with improved characteristics. In [24] and [25], two kinds of Z-source boost converters, which possess common grounded input and output terminals are presented. The shortages of these two converters are limited voltage gain and discontinuous input current. In [26], a family of hybrid Z-source boost converters is presented by mingling traditional Z-source networks differently. These converters can realize wide conversion ratios in lower duty cycle ranges while their topological structures are complex. With a switched-capacitor and the quasi-Z-source structure, a boost converter is presented in [27]. Integrating the Z-network with switched-capacitor technique, two kinds of boost converters are presented in [28]. Converters in [27] and [28] possess common ground terminals while their voltage gains are not high enough. Using a hybrid switched-capacitors switched-inductor method, [29] analysis a quasi-Z-source boost converter which has improved step-up gain while its input and output terminals share no common node. Utilizing the switched inductor, [30] presents an enhanced quasi-Z-source converter. This boost converter has common grounded structure and high step-up gain while its duty cycle range is restricted.

In this article, a single-inductor boost converter (SLBC), which is integrated by the Sheppard–Taylor structure [31] and the switched-capacitor technique, is presented and analyzed in detail. The major contributions of the SLBC are: ultrahigh voltage boosting capability, lower voltage stress of switches and intrinsic small duty cycle to enhance the system efficiency, single-inductor structure to realize continuous input current and high power density, common grounded terminals to avoid the du/dt issues and achieve reliable output. The outlines for this article are: Sections II and III are steady-state analyses in continuous conduction mode (CCM) and discontinuous conduction mode (DCM), respectively. Section IV presents performance comparisons and Section V is small-signal modeling. Section VI is the parameters design and Section VII is related experimental results. Finally, Section VIII concludes the article.

II. CCM Analyses

The SLBC is a fifth-order topology, which consists of one input inductor L_1, three mid-capacitors C_1 to C_3 and one output capacitor C_0, as shown in Fig. 1. Semiconductors of the SLBC including two synchronously controlled switches S_1 and S_2, four mid-diodes D_1 to D_4 and one output diode D_0. The SLBC has two states in CCM basing on the ON-OFF control actions of switches, corresponding equivalent circuits and time-domain waveforms are displayed in Figs. 2 and 3, respectively.

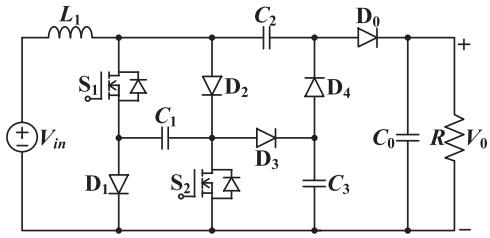

Fig. 1. Topological structure of the SLBC.

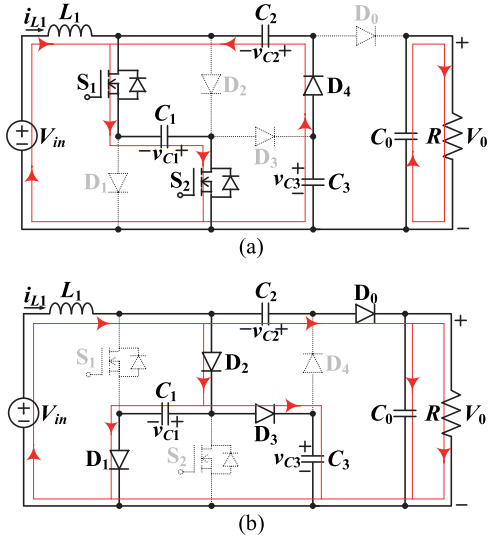

Fig. 2. Equivalent circuits of the SLBC. (a) State 1. (b) State 2.

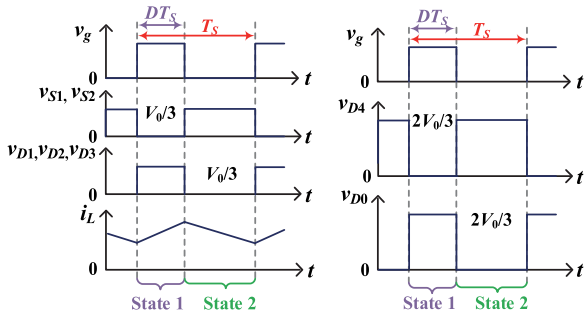

Fig. 3. Typical waveforms of the SLBC in CCM.

A. Operational Principles

State 1: As shown in Fig. 2(a), two synchronously controlled switches S_1 and S_2 together with mid-diode D_4 are ON, the other diodes are OFF in this time interval. There are three circuit loops for the SLBC operating in state 1: L_1 is magnetized by V_{in} and

C_1 via S_1 and S_2; mid-capacitors C_1 and C_3 release energy for C_2 via S_1, S_2 and D_4; C_0 releases energy for the resistive load R.

State 2: Within this period, the mid-diodes D_1 to D_3 and the output diode D_0 are ON while other switches and diode are OFF, as shown in Fig. 2(b). Three circuit loops for the SLBC in state 2 are: V_{in} and L_1 supply energy for C_1 via D_1 and D_2; V_{in} and L_1 supply energy for C_3 via D_2 and D_3; V_{in} together with L_1, C_2 supply energy for C_0 and R via D_0.

B. Calculations of Voltages

Based on the aforementioned operational analyses in state 1, corresponding voltage expressions of the SLBC are listed as follows:

$$\begin{cases} V_{L1} = V_{in} + V_{C1} \\ V_{C2} = V_{C1} + V_{C3}. \end{cases} \tag{1}$$

Similarly, the obtained voltage equations in state 2 are as follows:

$$\begin{cases} V_{L1} = V_{in} + V_{C2} - V_0 \\ V_{C1} = V_{C3} = V_0 - V_{C2}. \end{cases} \tag{2}$$

For L_1, adopting the volt-second balance and integrating related capacitor voltages in (1) and (2), the derived mid-capacitor voltages and voltage gain of the SLBC are as follows:

$$V_{C1} = V_{C3} = \frac{1}{1-2D} V_{in} \tag{3}$$

$$V_{C2} = \frac{2}{1-2D} V_{in} \tag{4}$$

$$M_{\mathrm{CCM}} = \frac{V_0}{V_{in}} = \frac{3}{1-2D}. \tag{5}$$

From (3) to (5), it is clear that the operational duty cycle range of the SLBC is $0 < D < 0.5$. Within this range, the SLBC realize low mid-capacitor voltages and ultrahigh voltage gain.

When the switches or the diodes are OFF, the voltage stress across them can be obtained as follows:

$$V_{S1} = V_{S2} = V_{D1} = V_{D2} = V_{D3} = \frac{1}{1-2D} V_{in} \tag{6}$$

$$V_{D4} = V_{D0} = \frac{2}{1-2D} V_{in}. \tag{7}$$

C. Calculations of Currents

Combining with the operational analyses of the SLBC, the expressions of capacitor currents in state 1 are derived as follows:

$$\begin{cases} I_{C1(\mathrm{on})} = -I_{L1} - I_{C2(\mathrm{on})} \\ I_{C2(\mathrm{on})} = -I_{L1} - I_{C1(\mathrm{on})} \\ I_{C3(\mathrm{on})} = I_{L1} + I_{C1(\mathrm{on})} \\ I_{C0(\mathrm{on})} = -I_0. \end{cases} \tag{8}$$

Likewise, the obtained capacitor current equations of the SLBC in state 2 are as follows:

$$\begin{cases} I_{C1(\mathrm{off})} = I_{L1} + I_{C2(\mathrm{off})} - I_{C3(\mathrm{off})} \\ I_{C2(\mathrm{off})} = -I_{L1} + I_{C1(\mathrm{off})} + I_{C3(\mathrm{off})} \\ I_{C3(\mathrm{off})} = I_{L1} - I_{C1(\mathrm{off})} + I_{C2(\mathrm{off})} \\ I_{C0(\mathrm{off})} = -I_0 - I_{C2(\mathrm{off})}. \end{cases} \tag{9}$$

The inductor L_1 of the SLBC is in series with its input voltage; so, using the power balance principle and the derived I_{L1} is as follows:

$$I_{L1} = \frac{3}{1-2D} I_0. \tag{10}$$

Combining (8) to (10), the capacitor currents in states 1 and 2 are, respectively, obtained as follows:

$$\begin{cases} I_{C1(\mathrm{on})} = \frac{-(1+D)I_0}{D(1-2D)} \\ I_{C2(\mathrm{on})} = \frac{I_0}{D} \\ I_{C3(\mathrm{on})} = \frac{-I_0}{D} \\ I_{C0(\mathrm{on})} = -I_0 \end{cases} \text{and} \begin{cases} I_{C1(\mathrm{off})} = \frac{(1+D)I_0}{(1-D)(1-2D)} \\ I_{C2(\mathrm{off})} = \frac{-I_0}{(1-D)} \\ I_{C3(\mathrm{off})} = \frac{I_0}{(1-D)} \\ I_{C0(\mathrm{off})} = \frac{DI_0}{(1-D)}. \end{cases} \tag{11}$$

Based on the aforementioned analyses, the derived current stress through switches and diodes are shown below:

$$I_{S1} = I_{S2} = I_{D1} = \frac{1+D}{1-2D} I_0 \tag{12}$$

$$I_{D2} = \frac{2-D}{1-2D} I_0 \tag{13}$$

$$I_{D3} = I_{D4} = I_{D0} = I_0. \tag{14}$$

Moreover, the rms current values of the semiconductor components are calculated as follows:

$$\begin{cases} I_{S1(\mathrm{rms})} = I_{S2(\mathrm{rms})} = \frac{\sqrt{D}(1+D)}{D(1-2D)} I_0 \\ I_{D1(\mathrm{rms})} = \frac{\sqrt{1-D}(1+D)}{(1-D)(1-2D)} I_0 \\ I_{D2(\mathrm{rms})} = \frac{\sqrt{1-D}(2-D)}{(1-D)(1-2D)} I_0 \\ I_{D3(\mathrm{rms})} = I_{D0(\mathrm{rms})} = \frac{1}{\sqrt{1-D}} I_0 \\ I_{D4(\mathrm{rms})} = \frac{1}{\sqrt{D}} I_0. \end{cases} \tag{15}$$

The rms current value for L_1 is the same with its average value in (10) and the rms current values for capacitors are as follows:

$$\begin{cases} I_{C1(\mathrm{rms})} = \sqrt{\frac{1}{D(1-D)}} \frac{(1+D)}{(1-2D)} I_0 \\ I_{C2(\mathrm{rms})} = I_{C3(\mathrm{rms})} = \sqrt{\frac{1}{D(1-D)}} I_0 \\ I_{C0(\mathrm{rms})} = \sqrt{\frac{D}{1-D}} I_0. \end{cases} \tag{16}$$

D. Ripples and Selections of Inductor and Capacitors

Integrating the obtained voltage and current expressions with aforementioned analyses, the ripples of inductor current and capacitor voltages of the SLBC, namely, Δi_{L1}, Δv_{C1}, Δv_{C2}, Δv_{C3} and Δv_{C0}, can be derived as follows:

$$\begin{cases} \Delta i_{L1} = \frac{2D(1-D)V_0 T_S}{3L_1} \\ \Delta v_{C1} = \frac{(1+D)V_0 T_S}{(1-2D)C_1 R} \\ \Delta v_{C2} = \frac{V_0 T_S}{C_2 R} \\ \Delta v_{C3} = \frac{V_0 T_S}{C_3 R} \\ \Delta v_{C0} = \frac{DV_0 T_S}{C_0 R}. \end{cases} \tag{17}$$

From (17), one can see that the inductor current ripple is related to D, V_0, T_S and the inductance value while the capacitor voltage ripples are interrelated with D, V_0, T_S, R and the capacitance values. Therefore, appropriate L_1, C_1, C_2, C_3, and C_0 can be calculated according to (17).

E. Losses and Efficiency

For the SLBC, the switch losses including conduction losses and switching losses:

$$P_S = \sum_{i=1}^{2} {I_{Si(\mathrm{rms})}}^2 r_{dsi} + \sum_{i=1}^{2} \frac{1}{2} V_{Si}(V_{Si}C_{ossi} + I_{Si}(t_{ri} + t_{fi}))f_S. \quad (18)$$

where r_{ds}, C_{oss}, $t_{r,}$ and t_f are the on-state resistance, output capacitance, rise and fall times of switch, respectively.

The losses of diodes comprise forward voltage losses and forward resistance losses, where V_F and r_D are diode's forward voltage and resistance, respectively

$$P_D = \sum_{i=1}^{4} V_{Fi}I_{Di} + V_{F0}I_{D0} + \sum_{i=1}^{4} {I_{Di(\mathrm{rms})}}^2 r_{Di} + {I_{D0(\mathrm{rms})}}^2 r_{D0}. \quad (19)$$

Inductor loss contains the copper loss and core loss, shown as follows:

$$P_L = {I_{L1(\mathrm{rms})}}^2 r_{L1} + A_c l_m a B^b f_S^c. \quad (20)$$

where r_{L1} is the equivalent series resistance (ESR) of L_1. Sendust core is adopted for L_1 and A_c is the cross section area of the core, l_m is the magnetic path length, B is the half of the ac flux swing while a, b, and c are given by the magnetic core data sheet.

The losses of capacitors can be derived as follows:

$$P_C = \sum_{i=1}^{3} {I_{Ci(\mathrm{rms})}}^2 r_{Ci} + {I_{C0(\mathrm{rms})}}^2 r_{C0}. \quad (21)$$

where r_C represents the ESR of capacitor.

With the obtained component losses from (18) to (21), the efficiency of the SLBC can be calculated as follows:

$$\begin{aligned}\eta &= \frac{P_0}{P_0 + P_S + P_D + P_L + P_C} \\ &= \frac{P_0}{[P_0 + \frac{\alpha^2 P_0(r_{ds1}+r_{ds2})}{DR} + \frac{\alpha P_0(t_{r1}+t_{f1}+t_{r2}+t_{f2})f_S}{6} + \frac{9P_0 r_{L1}}{\gamma^2 R}} \\ &\quad + \frac{{V_0}^2(C_{oss1}+C_{oss2})f_S}{18} + \frac{\alpha^2 P_0 r_{D1}}{(1-D)R} + \frac{\beta^2 P_0 r_{D2}}{(1-D)R} \\ &\quad + \frac{P_0 r_{D4}}{DR} + \frac{P_0(r_{D3}+r_{D0})}{(1-D)R} + \frac{\alpha^2 P_0 r_{C1}}{\delta R} \\ &\quad + \frac{P_0(r_{C2}+r_{C3})}{\delta R} + \frac{D^2 P_0 r_{C0}}{\delta R} \\ &\quad + \alpha V_{F1}I_0 + \beta V_{F2}I_0 + (V_{F3}+V_{F4}+V_{F0})I_0 \\ &\quad + A_c l_m a B^b f_S^c] \end{aligned} \quad (22)$$

where $\alpha = (1+D)/(1-2D)$, $\beta = (2-D)/(1-2D)$, $\gamma = 1-2D$, and $\delta = D(1-D)$.

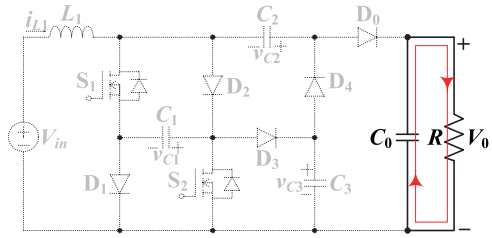

Fig. 4. Equivalent circuit of the state 3 in DCM.

III. DCM Analyses

In DCM, the SLBC possesses three states while the first two states are similar as the CCM analyses. When the SLBC operates in the third state of the DCM, the semiconductor currents reduce to zero and only C_0 releases energy for R, as shown in Fig. 4.

A. Calculations in DCM

When the SLBC working in DCM, the following equations are tenable:

$$\begin{cases} (V_{in}+V_{C1})D + (V_{in}-V_{C1})D_1 = 0 \\ V_{C1} = V_{C3} \\ V_{C2} = V_{C1} + V_{C3} \\ V_0 = V_{C1} + V_{C2} \end{cases} \quad (23)$$

where D_1 is the time ratio of state 2.

Then, the DCM step-up gain is derived as follows:

$$M_{\mathrm{DCM}} = \frac{3D + 3D_1}{-D + D_1}. \quad (24)$$

The current ripple and average current of inductor L_1 in DCM, namely, $\Delta i_{L1(\mathrm{DCM})}$ and $I_{L1(\mathrm{DCM})}$, can be calculated, respectively, as follows:

$$\Delta i_{L1(\mathrm{DCM})} = \frac{(V_{in}+V_{C1})}{L_1} DT_S = \frac{2DD_1 V_{in} T_S}{(-D+D_1)L_1}. \quad (25)$$

$$I_{L1(\mathrm{DCM})} = \frac{1}{2}\Delta i_{L1(\mathrm{DCM})}(D+D_1) = \frac{(D+D_1)DD_1 V_{in} T_S}{(-D+D_1)L_1}. \quad (26)$$

Combining the aforementioned analyses and adopting the power balance principle, the time ratio D_1 is expressed as follows:

$$D_1 = \frac{D^2 RT_S + 9L_1 + \sqrt{(D^2 RT_S + 9L_1)^2 + 36D^2 RL_1 T_S}}{2DRT_S}. \quad (27)$$

Substituting (27) into (24), the calculated DCM voltage gain for the SLBC is as follows:

$$M_{\mathrm{DCM}} = \frac{9D^2 RT_S + 27L_1 + 3\sqrt{(D^2 RT_S + 9L_1)^2 + 36D^2 RL_1 T_S}}{-D^2 RT_S + 9L_1 + \sqrt{(D^2 RT_S + 9L_1)^2 + 36D^2 RL_1 T_S}}. \quad (28)$$

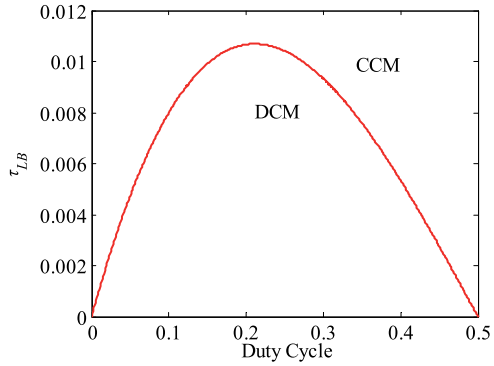

Fig. 5. Boundary condition of the SLBC.

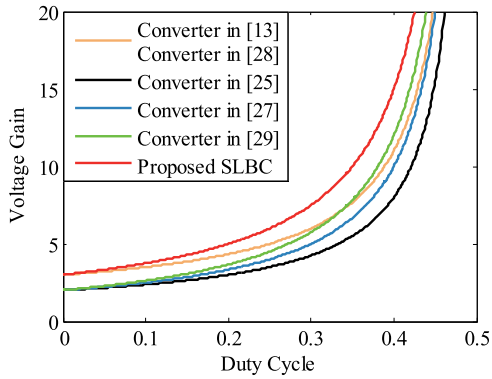

Fig. 6. Voltage gains versus duty cycle among converters.

B. Boundary Condition

In boundary conduction mode (BCM), the currents of semiconductors just reduce to zero in the end of every switching period. Therefore, in BCM, the CCM and DCM voltage gains of the SLBC are equal to each other. Combing (5) and (28), defining the normalized time constant as follows:

$$\tau_L = \frac{L}{RT_S} = \frac{Lf_S}{R}. \tag{29}$$

The boundary condition of the SLBC can be derived as follows:

$$\tau_{LB} = \frac{D(1-D)(1-2D)}{9}. \tag{30}$$

On the basis of (30), the boundary condition versus duty cycle for the SLBC is drawn in Fig. 5. It is clear that the SLBC possesses large CCM operational range and works in CCM when $\tau_L > \tau_{LB}$. Otherwise, the SLBC works in DCM.

IV. Performance Comparisons

For validating the performances, five kinds of typical boost converters are selected to make comparisons with the SLBC. Here, the converter in [28] is the presented Type-2 converter. The comparisons, including component number, voltage gain and range, voltage and current stress, total component stress factor (CSF), input current continuity and common ground feature, are presented in Table I and analyzed as follows.

A. Comparisons on Voltage Gain and Range

On the basis of Table I, Fig. 6 draws the voltage gain curves verses duty cycle among these converters. One can see that the voltage gain of the SLBC is always the highest within the duty cycle range. Moreover, for the SLBC, the obtained voltage gain ranges from 10 to 15 when D varies from 0.35 to 0.4. These duty cycle scopes are far away from the extreme duty cycle and easy to implement on the one hand and small enough to enhance the system efficiency on the other hand.

B. Comparisons on Voltage and Current Stress

The detailed voltage and current stress on switches and diodes and the corresponding total stress are presented in Table I to make comparisons among these converters.

According to Table I, the maximum voltage and current stress of these converters can be obtained and corresponding stress curves versus voltage gain are drawn in Fig. 7(a)–(d), respectively. Form Fig. 7(a), one can see that the maximum voltage stress of switches for the SLBC are only one third of the output voltage and the smallest one within the voltage gain range $M > 3$, as the red curve displays. Fig. 7(b) shows the maximum diode voltage stress curves among converters and it can be found that $V_{D(\max)}/V_0 = 2/3$ for the SLBC is the second highest one when $M > 3$ and far less than the output voltage. Fig. 7(c) and (d) compares the curves of the maximum current stress of switches and diodes among converters, respectively. It is clear that $I_{S(\max)}/I_0 = (M-1)/2$ and $I_{D(\max)}/I_0 = (M+1)/2$ for the converter in [13] and the SLBC are both the smallest values when $M > 3$.

The total voltage stress of switches are the sum of the voltage stress across each switches while the total current stress of switches are the sum of the current stress through each switches. Similarly, the total voltage and current stress for diodes can be obtained. According to Table I, the total voltage stress of switches are compared in Fig. 7(e) and it can be seen that within the voltage gain range $M > 3$, $V_{S(\text{total})}/V_0$ for the SLBC is the second highest one and far less than the output voltage. Fig. 7(f) draws the total voltage stress of diodes among converter, one can see that $V_{D(\text{total})}/V_0$ for the SLBC is the highest when $3 < M < 15$ while $V_{D(\text{total})}/V_0$ for the converters in [13] and [28] are the highest when $M > 15$. Also, from Table I, it is clear that the total current stress of switches for these converters are the same and the total current stress of diodes for the SLBC is in-between when compared with other typical boost converters.

The abovementioned comparisons demonstrate that the SLBC possesses small semiconductor voltage and current stress. Therefore, switches and diodes with low rated voltages can be selected and converter efficiency can be improved.

C. Comparisons on CSF

CSF is an analysis method, which enables direct numerical comparison of power conversion topologies, generating numerical scores for each component type in each topology for a specific set of operating conditions [32], [33]. CSF can be classified for switches (S_SCSF), diodes (S_DCSF), inductive windings (WCSF), and capacitors (CCSF). After calculating a

TABLE I
PERFORMANCE COMPARISONS AMONG CONVERTERS

Topologies	Converter in [13]	Converter in [25]	Converter in [27]	Converter in [28]	Converter in [29]	Proposed SLBC
No. of *L*/*C*/S/D	1/3/2/4	2/4/1/3	2/5/1/4	2/6/1/5	3/7/1/5	1/4/2/5
Voltage gain in CCM (M)	$\frac{3-2D}{1-2D}$	$\frac{2-D}{1-2D}$	$\frac{2}{1-2D}$	$\frac{3-2D}{1-2D}$	$\frac{2+D}{1-2D}$	$\frac{3}{1-2D}$
Voltage gain range in CCM (D=0.1→0.4)	3.5→11	2.375→8	2.5→10	3.5→11	2.625→12	3.75→15
Voltage stress of switches	$V_{S1}/V_0=\frac{M-1}{2M}$ $V_{S2}/V_0=\frac{M-1}{2M}$	$V_S/V_0=\frac{2M-1}{3M}$	$V_Q/V_0=\frac{1}{2}$	$V_S/V_0=\frac{M-1}{2M}$	$V_S/V_0=\frac{2M+1}{5M}$	$V_{S1}/V_0=\frac{1}{3}$ $V_{S2}/V_0=\frac{1}{3}$
Voltage stress of diodes	$V_{D1}/V_0=\frac{M-1}{2M}$ $V_{D2}/V_0=\frac{M-1}{2M}$ $V_{D3}/V_0=\frac{M-1}{2M}$ $V_{D0}/V_0=\frac{M-1}{M}$	$V_{D1}/V_0=\frac{2M-1}{3M}$ $V_{D2}/V_0=\frac{2M-1}{3M}$ $V_{D3}/V_0=\frac{2M-1}{3M}$	$V_{D2}/V_0=\frac{1}{2}$ $V_{D3}/V_0=\frac{1}{2}$ $V_{D4}/V_0=\frac{1}{2}$ $V_{D5}/V_0=\frac{1}{2}$	$V_{D1}/V_0=\frac{M-1}{2M}$ $V_{D2}/V_0=\frac{M-1}{2M}$ $V_{D3}/V_0=\frac{M-1}{2M}$ $V_{D4}/V_0=\frac{M-1}{2M}$ $V_{D5}/V_0=\frac{M-1}{2M}$	$V_{D1}/V_0=\frac{2M+1}{5M}$ $V_{D2}/V_0=\frac{2M+1}{5M}$ $V_{D3}/V_0=\frac{2M+1}{5M}$ $V_{D4}/V_0=\frac{2M+1}{5M}$ $V_{D5}/V_0=\frac{2M+1}{5M}$	$V_{D1}/V_0=\frac{1}{3}$ $V_{D2}/V_0=\frac{1}{3}$ $V_{D3}/V_0=\frac{1}{3}$ $V_{D4}/V_0=\frac{2}{3}$ $V_{D0}/V_0=\frac{2}{3}$
Current stress of switches	$I_{S1}/I_0=\frac{M-1}{2}$ $I_{S2}/I_0=\frac{M-1}{2}$	$I_S/I_0=M-1$	$I_Q/I_0=M-1$	$I_S/I_0=M-1$	$I_S/I_0=M-1$	$I_{S1}/I_0=\frac{M-1}{2}$ $I_{S2}/I_0=\frac{M-1}{2}$
Current stress of diodes	$I_{D1}/I_0=\frac{M-1}{2}$ $I_{D2}/I_0=\frac{M+1}{2}$ $I_{D3}/I_0=1$ $I_{D0}/I_0=1$	$I_{D1}/I_0=M$ $I_{D2}/I_0=1$ $I_{D3}/I_0=1$	$I_{D2}/I_0=M$ $I_{D3}/I_0=1$ $I_{D4}/I_0=1$ $I_{D5}/I_0=1$	$I_{D1}/I_0=M-1$ $I_{D2}/I_0=1$ $I_{D3}/I_0=1$ $I_{D4}/I_0=1$ $I_{D5}/I_0=1$	$I_{D1}/I_0=M$ $I_{D2}/I_0=1$ $I_{D3}/I_0=1$ $I_{D4}/I_0=1$ $I_{D5}/I_0=1$	$I_{D1}/I_0=\frac{M-1}{2}$ $I_{D2}/I_0=\frac{M+1}{2}$ $I_{D3}/I_0=1$ $I_{D4}/I_0=1$ $I_{D0}/I_0=1$
Total voltage stress of switches ($V_{S(\text{total})}/V_0$)	$\frac{M-1}{M}$	$\frac{2M-1}{3M}$	$\frac{1}{2}$	$\frac{M-1}{2M}$	$\frac{2M+1}{5M}$	$\frac{2}{3}$
Total voltage stress of diodes ($V_{D(\text{total})}/V_0$)	$\frac{5M-5}{2M}$	$\frac{2M-1}{M}$	2	$\frac{5M-5}{2M}$	$\frac{2M+1}{M}$	$\frac{7}{3}$
Total current stress of switches ($I_{S(\text{total})}/I_0$)	$M-1$	$M-1$	$M-1$	$M-1$	$M-1$	$M-1$
Total current stress of diodes ($I_{D(\text{total})}/I_0$)	$M+2$	$M+2$	$M+3$	$M+3$	$M+4$	$M+3$
Total CSF (Duty cycle)	193 (0.389)	426 (0.421)	306 (0.4)	259 (0.389)	271 (0.38)	140 (0.35)
Continuous input current	No	No	Yes	No	No	Yes
Common ground	No	Yes	Yes	Yes	No	Yes

CSF for each component and summing component factors of the same type, the following equation for the total CSF can be obtained:

$$\text{Total CSF} = \sum_{\text{Switches}} \text{S}_\text{S}\text{CSF}_i + \sum_{\text{Diodes}} \text{S}_\text{D}\text{CSF}_i + \sum_{\text{Windings}} \text{WCSF}_i + \sum_{\text{Capacitors}} \text{CCSF}_i. \quad (31)$$

Setting specifications as input voltage $V_{in} = 30$ V, output voltage $V_0 = 300$ V, output power $P_0 = 250$ W and adopting equal component weights, the calculated total CSF of converters with corresponding duty cycle are compared in Table I and the total CSF curves versus duty cycle are drawn in Fig. 8. From Fig. 8, one can see that the trends of these curves are the same and the small total CSF occurs in the middle of the duty cycle ranges. To meet the specifications and obtain voltage gain $M = 10$, the required duty cycle for the SLBC is the smallest and corresponding voltages and currents are small, so that the total CSF of the SLBC is the smallest, as demonstrated in Table I and Fig. 8.

Moreover, the volume of inductors and capacitors take a large proportion of the total volumes. So, with fifth-order topology implemented and only one inductor adopted, the SLBC can realize high power density.

The abovementioned analyses demonstrate that the SLBC realizes highest step-up gain, reduced topological order, low voltage and current stress, small total CSF, continuous input current, common grounded input and output terminals simultaneously. Therefore, the SLBC possesses better topology performances.

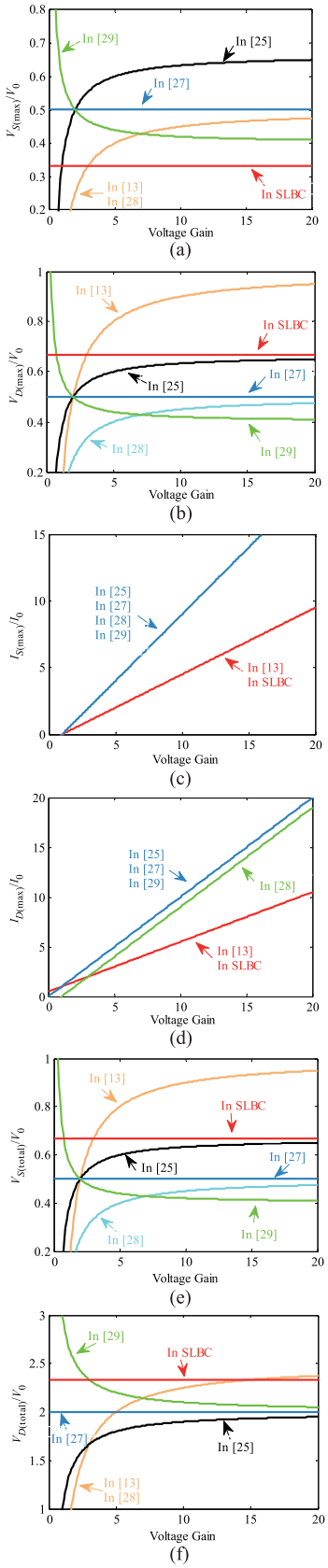

Fig. 7. Comparisons on voltage and current stress versus voltage gain among converters. (a) Maximum voltage stress of switches. (b) Maximum voltage stress of diodes. (c) Maximum current stress of switches. (d) Maximum current stress of diodes. (e) Total voltage stress of switches. (f) Total voltage stress of diodes.

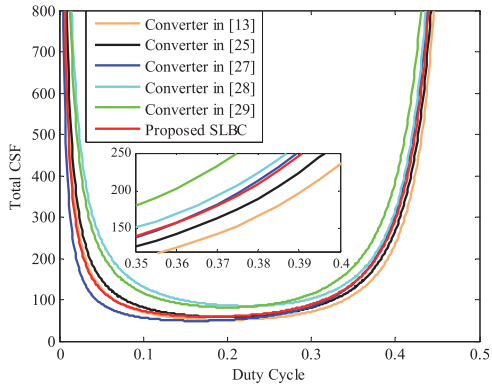

Fig. 8. Total CSF curves versus duty cycle among converters.

V. Small-Signal Analyses

Here, the CCM small-signal model is obtained by applying the state space average method. $v_{in}(t)$ is the input variable, $d(t)$ is the control variable, and $v_0(t)$ is the output variable. The state variables are named as $i_{L1}(t)$, $v_{C1}(t)$, $v_{C2}(t)$, $v_{C3}(t)$, and $v_{C0}(t)$, respectively. For analyzing the small-signal characteristic of SLBC in-depth, the ESRs of inductor and capacitors are considered fully in this section. Specially, $r_{L1} = r_L$ and $r_{C1} = r_{C2} = r_{C3} = r_{C0} = r_C$ are set to simplify calculations.

Based on the operational principle analyses in state 1, the state space average model in this state can be established as follows:

$$\begin{bmatrix} \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} \frac{-(3r_L+2r_C)}{3L_1} & \frac{2}{3L_1} & \frac{1}{3L_1} & \frac{-1}{3L_1} & 0 \\ \frac{-2}{3C_1} & \frac{-1}{3C_1r_C} & \frac{1}{3C_1r_C} & \frac{-1}{3C_1r_C} & 0 \\ \frac{-1}{3C_2} & \frac{1}{3C_2r_C} & \frac{-1}{3C_2r_C} & \frac{1}{3C_2r_C} & 0 \\ \frac{1}{3C_3} & \frac{-1}{3C_3r_C} & \frac{1}{3C_3r_C} & \frac{-1}{3C_3r_C} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_0R} \end{bmatrix} \times \begin{bmatrix} i_{L1}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ v_{C3}(t) \\ v_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t). \tag{32}$$

Similarly, according to the second principle which is mentioned in Section II, the established state space average model in state 2 is as follows:

$$\begin{bmatrix} \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} \frac{-3r_L-r_C}{3L_1} & \frac{-1}{3L_1} & \frac{1}{3L_1} & \frac{-1}{3L_1} & \frac{-1}{3L_1} \\ \frac{1}{3C_1} & \frac{-2}{3C_1r_C} & \frac{-1}{3C_1r_C} & \frac{1}{3C_1r_C} & \frac{1}{3C_1r_C} \\ \frac{-1}{3C_2} & \frac{-1}{3C_2r_C} & \frac{-2}{3C_2r_C} & \frac{-1}{3C_2r_C} & \frac{2}{3C_2r_C} \\ \frac{1}{3C_3} & \frac{1}{3C_3r_C} & \frac{-1}{3C_3r_C} & \frac{-2}{3C_3r_C} & \frac{1}{3C_3r_C} \\ \frac{1}{3C_0} & \frac{1}{3C_0r_C} & \frac{2}{3C_0r_C} & \frac{1}{3C_0r_C} & \frac{-2}{3C_0r_C} + \frac{-1}{C_0R} \end{bmatrix} \times \begin{bmatrix} i_{L1}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ v_{C3}(t) \\ v_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t). \tag{33}$$

Disturbances are added as (34), where V_{in}, D, I_{L1}, V_{C1}, V_{C2}, V_{C3}, and V_{C0} are the dc values and $\hat{v}_{in}(t)$, $\hat{d}(t)$, $\hat{i}_{L1}(t)$, $\hat{v}_{C1}(t)$, $\hat{v}_{C2}(t)$, $\hat{v}_{C3}(t)$, and $\hat{v}_{C0}(t)$ are corresponding small-signal

disturbances. Combining (32) and (33) and substituting (34) into them, separating the disturbances out, omitting the higher order small signal terms, the small-signal model for the SLBC can be derived and are shown in (35) at the bottom of this page.

$$\begin{cases} i_{L1}(t) = I_{L1} + \hat{i}_{L1}(t) \\ v_{C1}(t) = V_{C1} + \hat{v}_{C1}(t) \\ v_{C2}(t) = V_{C2} + \hat{v}_{C2}(t) \\ v_{C3}(t) = V_{C3} + \hat{v}_{C3}(t) \\ v_{C0}(t) = V_{C0} + \hat{v}_{C0}(t) \\ v_{in}(t) = V_{in} + \hat{v}_{in}(t) \\ d(t) = D + \hat{d}(t) \end{cases} \text{ with } \begin{cases} \hat{i}_{L1}(t) \ll I_{L1} \\ \hat{v}_{C1}(t) \ll V_{C1} \\ \hat{v}_{C2}(t) \ll V_{C2} \\ \hat{v}_{C3}(t) \ll V_{C3} \\ \hat{v}_{C0}(t) \ll V_{C0} \\ \hat{v}_{in}(t) \ll V_{in} \\ \hat{d}(t) \ll D. \end{cases} \tag{34}$$

VI. Parameters Design

Parameters of the power circuit and controller circuit for the SLBC are designed as follows.

A. Power Circuit

The working conditions for the SLBC are set as follows.

1) Input voltage: $V_{in} = 30$ V.
2) Output voltage: $V_0 = 300$ V.
3) Output power: $P_0 = 250$ W
4) Switching frequency: $f_S = 30$ kHz.

Corresponding duty cycle $D = 0.35$ and resistive load $R = 360\ \Omega$. What's more, on the basis of the abovementioned calculated stress, the choices of switches and diodes are as follows.

5) S_1 and S_2: IRFP4668PbF with $V_{\rm DSS} = 200$ V and $I_D = 130$ A.
6) D_1, D_2 and D_3: MBR40250 with $V_{\rm RRM} = 250$ V and $I_F = 40$ A.
7) D_4 and D_0: MUR1560 with $V_{\rm RRM} = 600$ V and $I_F = 15$ A.

The ripple ratios for inductor L_1, midcapacitors C_1 to C_3 and output capacitor C_0 are set as 25%, 10%, and 1%, respectively.

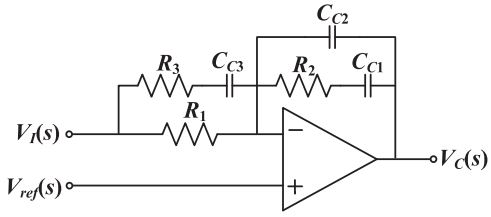

Fig. 9. Diagram of the type-III controller.

Combining the derived ripples in (17), the values of inductor and capacitors can be calculated as follows:

$$\begin{cases} L_1 \geq \frac{2D(1-D)V_0T_S}{3r_{i1}\%I_{L1}} \\ C_1 \geq \frac{(1+D)V_0T_S}{(1-2D)Rr_{c1}\%V_{C1}} \\ C_2 \geq \frac{V_0T_S}{Rr_{c2}\%V_{C2}} \\ C_3 \geq \frac{V_0T_S}{Rr_{c3}\%V_{C3}} \\ C_0 \geq \frac{DV_0T_S}{Rr_{c0}\%V_{C0}}. \end{cases} \tag{36}$$

Therefore, combining the common inductances and capacitances of energy storage elements, the adopted parameters for the SLBC are $L_1 = 1$ mH, $C_1 = 20\ \mu$F, $C_2 = 10\ \mu$F, $C_3 = 10\ \mu$F and $C_0 = 10\ \mu$F, respectively.

B. Controller Circuit

Substituting the aforementioned parameter settings and component selections into (35), using the Laplace transform, the control-to-output transfer function of the SLBC can be calculated and the expression is displayed in (37) shown at the bottom of this page.

For the SLBC, the type-III controller is adopted and the diagram is displayed in Fig. 9. Combining the aforementioned analyses, the closed-loop transfer function can be obtained as (38) shown at the bottom of this page, and its bode plot is drawn in Fig. 10. From Fig. 10, it is clear that in low frequency

$$\begin{bmatrix} \frac{\mathrm{d}\hat{i}_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{v}_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{v}_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{v}_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{v}_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} \frac{-3r_L-(D+1)r_C}{3L_1} & \frac{3D-1}{3L_1} & \frac{1}{3L_1} & \frac{-1}{3L_1} & \frac{D-1}{3L_1} \\ \frac{1-3D}{3C_1} & \frac{D-2}{3C_1r_C} & \frac{2D-1}{3C_1r_C} & \frac{1-2D}{3C_1r_C} & \frac{1-D}{3C_1r_C} \\ \frac{-1}{3C_2} & \frac{2D-1}{3C_2r_C} & \frac{D-2}{3C_2r_C} & \frac{2D-1}{3C_2r_C} & \frac{2-2D}{3C_2r_C} \\ \frac{1}{3C_3} & \frac{1-2D}{3C_3r_C} & \frac{2D-1}{3C_3r_C} & \frac{D-2}{3C_3r_C} & \frac{1-D}{3C_3r_C} \\ \frac{1-D}{3C_0} & \frac{1-D}{3C_0r_C} & \frac{2-2D}{3C_0r_C} & \frac{1-D}{3C_0r_C} & \frac{2(D-1)R+3(2D-1)r_C}{3C_0Rr_C} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C3}(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in}(t) + \begin{bmatrix} \frac{-r_C}{3L_1} & \frac{1}{L_1} & 0 & 0 & \frac{1}{3L_1} \\ \frac{-1}{C_1} & \frac{1}{3C_1r_C} & \frac{2}{3C_1r_C} & \frac{-2}{3C_1r_C} & \frac{-1}{3C_1r_C} \\ 0 & \frac{2}{3C_2r_C} & \frac{1}{3C_2r_C} & \frac{2}{3C_2r_C} & \frac{-2}{3C_2r_C} \\ 0 & \frac{-2}{3C_3r_C} & \frac{2}{3C_3r_C} & \frac{1}{3C_3r_C} & \frac{-1}{3C_3r_C} \\ \frac{-1}{3C_0} & \frac{-1}{3C_0r_C} & \frac{-2}{3C_0r_C} & \frac{-1}{3C_0r_C} & \frac{2R+6r_C}{3C_0Rr_C} \end{bmatrix} \begin{bmatrix} I_{L1} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C0} \end{bmatrix} \hat{d}(t) \tag{35}$$

$$G_{v_0d}(s) = \left.\frac{\hat{v}_0(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{-1.1\times10^5 s^4 - 3.6\times10^{12}s^3 - 2.8\times10^{19}s^2 - 5.7\times10^{25}s + 3.0\times10^{29}}{s^5 + 2.1\times10^7 s^4 + 1.3\times10^{14}s^3 + 2.5\times10^{20}s^2 + 1.7\times10^{22}s + 1.5\times10^{26}} \tag{37}$$

$$G_C = \frac{-9.6\times10^9 s^6 - 3.2\times10^{17}s^5 - 2.4\times10^{24}s^4 - 5\times10^{30}s^3 + 2.2\times10^{34}s^2 + 2\times10^{37}s + 4\times10^{39}}{s^8 + 2.2\times10^7 s^7 + 1.5\times10^{14}s^6 + 3.5\times10^{20}s^5 + 1.9\times10^{26}s^4 + 1.4\times10^{31}s^3 + 1.1\times10^{33}s^2 + 8.6\times10^{36}s} \tag{38}$$

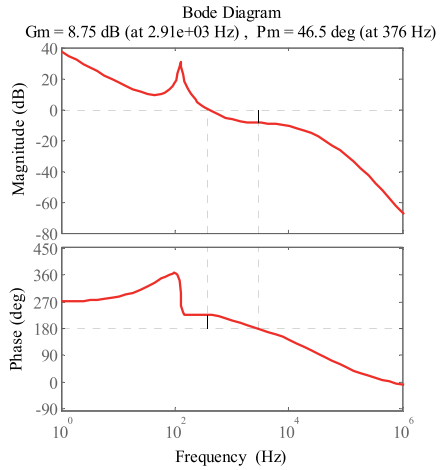

Fig. 10. Closed-loop bode plot of the SLBC.

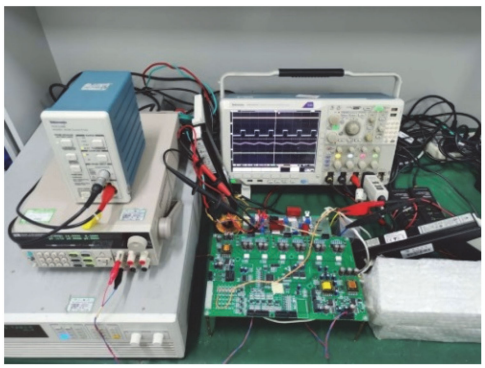

Fig. 11. Experimental setup of the SLBC under the test.

section, the slope is -20 dB/dec and the steady-state error of the system is zero. In medium frequency section, the phase margin is 46.5deg with a slope of -20 dB/dec while the gain margin is 8.75 dB, so, the system is stable and possesses fast response. In high frequency section, the slope is -40 dB/dec and the high frequency interference is well restrained.

VII. Experiment Verifications

The parameters designed in Section VI are adopted for validating the aforementioned analyses of the SLBC and the experimental setup under the test is shown in Fig. 11. Here, the Chroma 62150H-1000 and the IT6322B supply energy for the power circuit and controller circuit, respectively. Two high voltage differential probes Tektronix P5200A are used to detect the voltages. Tektronix TCP0150 and Tektronix TCPA300 are applied to detect the currents. The digital oscilloscope is Tektronix MDO4054C. Related experimental results are shown as follows.

A. Time-Domain Waveforms

The time-domain waveforms of the SLBC, including the inductor current, the switch voltages, the diode voltages, and the capacitor voltages are measured and displayed in Fig. 12. Owing to the waveforms of v_{S1} and v_{S2} are the same while v_{D1}, $v_{D2,}$ and v_{D3} are the same, only v_{S1} and v_{D1} are shown here as representative. In Fig. 12(a), the inductor current i_{L1}, switch voltage stress v_{S1} and diode voltage stress v_{D4} are shown from top to bottom, respectively. They are match with the calculations that $I_{L1} = 8.3$ A, $V_{S1} = 100$ V and $V_{D4} = 200$ V. Fig. 12(b) displays the inductor current i_{L1}, diodes voltage stress v_{D1} and v_{D0} in turn and they are consist with related calculations: I_{L1}

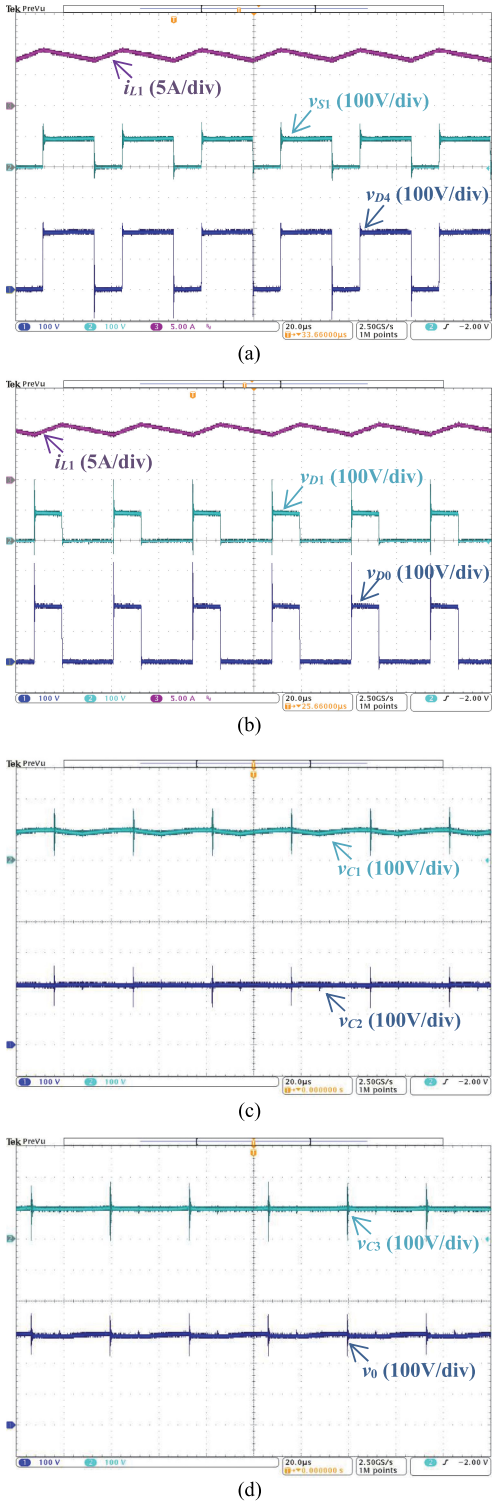

Fig. 12. Experimental waveforms of the SLBC (time: 20 μs/div). (a) i_{L1}, $v_{S1,}$ and v_{D4}. (b) i_{L1}, v_{D1} and v_{D0}. (c) v_{C1} and v_{C2}. (d) v_{C3} and v_0.

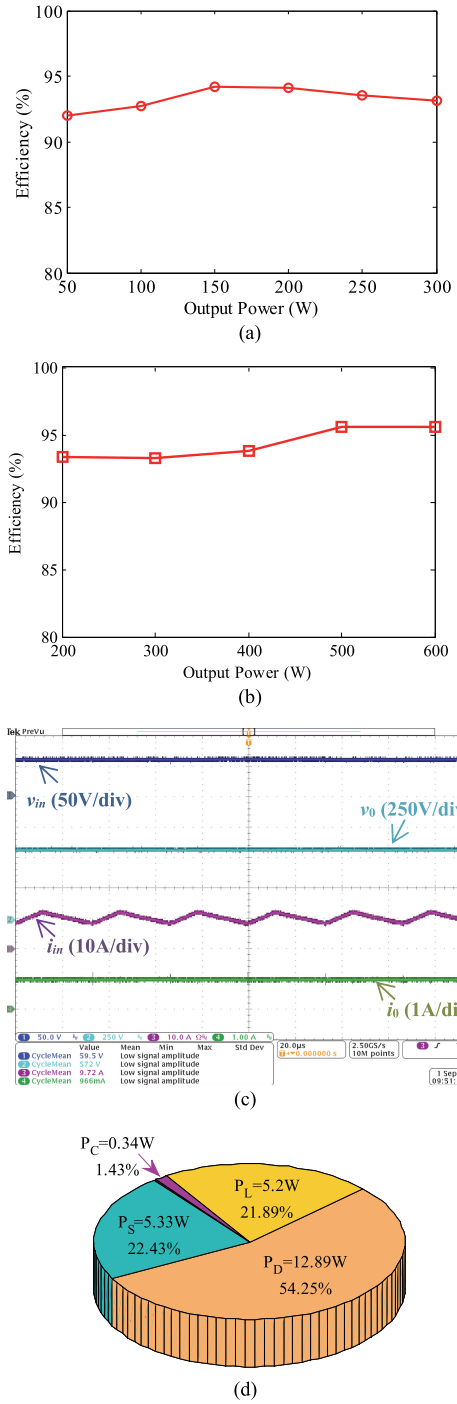

Fig. 13. Measured efficiencies versus output power and component losses of the SLBC. (a) $V_{in} = 30$ V and $V_0 = 300$ V. (b) $I_0 = 1$ A and $M = 10$. (c) Measured v_{in}, v_0, i_{in} and i_0 with $P_0 = 600$W. (d) Component losses with $P_0 = 600$ W.

$= 8.3$ A, $V_{D1} = 100$ V, and $V_{D0} = 200$ V. Fig. 12(c) presents the capacitor voltages v_{C1} and v_{C2} while Fig. 12(d) shows the capacitor voltages v_{C3} and v_0, respectively. The calculations of capacitor voltages are $V_{C1} = 100$ V, $V_{C2} = 200$ V, $V_{C3} = 100$ V, and $V_0 = 300$ V, and they are compliant with the results in Fig. 12(c) and (d). Here, voltage spikes occurred in Fig. 12 are owing to the recovery characteristics of power rectifiers.

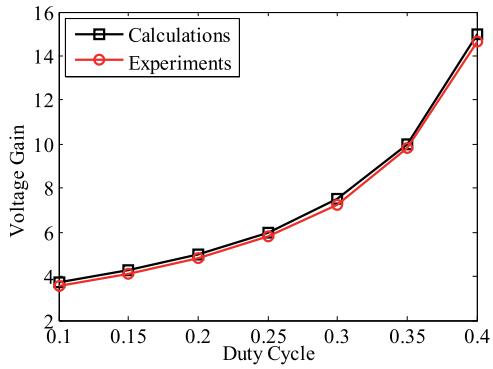

Fig. 14. Experimental and calculated voltage gains of the SLBC.

B. Efficiency

Efficiencies of the SLBC versus output power are measured under two kinds of specifications. The first condition is unchanged input voltage and output voltage, that is, $V_{in} = 30$ V and $V_0 = 300$ V, as shown in Fig. 13(a). The second condition is unchanged output current and voltage gain, namely, $I_0 = 1$ A and $M = 10$, as Fig. 13(b) displays. Here, to make the SLBC work normally in Fig. 13(b), the selections of switches and diodes are IRFP4868PbF and MUR1560, respectively.

When $P_0 = 600$ W, the measured input voltage v_{in}, output voltage v_0, input current $i_{in,}$ and output current i_0 are presented in Fig. 13(c) and the obtained efficiency is up to 95.54%. Corresponding component losses are analyzed and drawn in Fig. 13(d) and it is clear that the losses of diodes account for a large proportion in the total losses. The losses of switches and inductor are the second and third largest ones while the losses on capacitors are the smallest.

Hence, the SLBC can realize high efficiency.

C. Experimental and Calculated Voltage Gains

For verifying the achievable voltage gain of the SLBC, the obtained voltage gains in experiments versus duty cycle are compared with the calculated voltage gains, as plotted in Fig. 14. From Fig. 14, one can see that these two voltage gains have very close curves and the achievable experimental voltage gains of the SLBC are as high as the calculated values. The results in Fig. 14 also demonstrate that the SLBC can work by an effective and feasible way.

D. Dynamic Response

With the designed controller, the dynamic behaviors of the SLBC are displayed in Fig. 15. The measured waveforms from top to bottom are the output voltage v_0, the input current i_{in} and the output current i_0 in Fig. 15(a) and the output voltage v_0, the input voltage v_{in}, and the output current i_0, as shown in Fig. 15(b). From Fig. 15(a), one can see that when the resistive load varies from 360 to 300 Ω, the output voltage keep stable while the input current varies from 8.3 to 10 A and the output current varies from 0.83 to 1 A. In Fig. 15(b), when the input voltage varies from 30 to 50 V, the output voltage and current

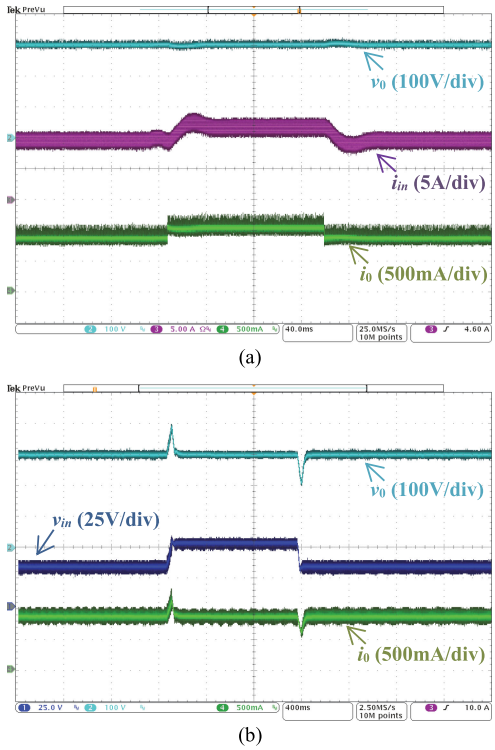

Fig. 15. Dynamic behavior for the SLBC. (a) Dynamic response when the resistive load varies from 360 to 300 Ω. (b) Dynamic response when the input voltage varies from 30 to 50 V.

have the overshoot and keep stable fast at 300 V and 0.83 A, respectively.

Fig. 15 validates that the SLBC possesses fast dynamic response.

VIII. Conclusion

This article proposes and analyses a new topology of single-inductor boost converter. Contributions of the SLBC including ultrahigh voltage boosting capability without using transformer or coupled-inductor, lower switches voltage stress, simple topological structure, continuous input current, and common grounded terminals. Steady-state analyses in CCM and DCM and small-signal analyses in CCM are presented to study the proposed SLBC in detail. Moreover, performance comparisons with other typical boost converters and 250 W experiments are conducted to validate the characteristics of the SLBC. On the basis of analyses in this article, the SLBC can be used for wide conversion range applications with high voltage gain, high efficiency, high power density, and high reliability.

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