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Implementation of a common grounded Z-source DC–DC converter with improved operation factors

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Abstract: This study proposes a common grounded Z-source DC–DC converter. In comparison with a conventional Z-source converter, it converts voltage with higher voltage gain and lower voltage stress on the switch and diodes that means an improvement in efficiency. In addition, increasing the duty cycle reduces its output voltage ripple percentage that improves its operation quality. The converter is analysed and compared with other converters. Its main equations are obtained, which show the converter advantages as lower voltage stress, smaller inductors and higher voltage gain in comparison with the reviewed converters. A prototype for the proposed converter is prepared based on analysis and theoretical parts. Experiments are done along with the analysis. Experimental results and theoretical equations are used to show the converter advantages.

1 Introduction

By developing green technologies such as photovoltaic panels, DC–DC converters have been widely used. Most of the renewable energy sources need DC–DC converters to boost low voltage in the renewable energy side to high voltage in the load side [1–5]. Traditional boost is the first choice of non-isolated DC–DC converters, which increases the voltage with infinite limitation based on its voltage gain equation. However, its boosting mode has limitations that occur due to the parasitic resistances and voltage drop on the components [6–9]. However, it has a simple and cost effective structure, it cannot be used for high-power applications and voltage stress on its components is high [6].

To solve the problems, new structures have been proposed. The structures can be selected for different applications according to their positive and negative points. The simplest method is cascading boost converters that have some disadvantages such as low efficiency, high cost, high-voltage drop and complex circuit [7]. The only positive points of cascading boost converters are high-voltage gain and reduction of voltage stress on the components. The other method is using a coupled inductor instead of the boost inductor [8, 9]. The turn ratio of the coupled inductor defines voltage gain. Thus, the converter requires a high-turn ratio to operate with high-voltage gain that imposes an extra conduction loss, leakage inductance and a big size inductor to the converter [4, 8, 9]. To overcome the problems, additional components such as inductors, capacitors, and diodes should be used as proposed in [9]. The other kind of extended converter based on boost or buck-boost is a quadratic converter, which consists of a reformed cascaded converter [10–12]. The converter voltage gain is low and can be improved by adding a coupled inductor. However, the turn ratio of the inductor matches its voltage gain with the desired value; the converter suffers from increased voltage stress on its components due to the inductor leakage inductance [10].

Other than the introduced methods and multiplier techniques, some new methods and structures have been proposed to improve operation quality and voltage gain [13–16]. The methods include switched-inductor and switched capacitor techniques to increase the voltage gain of different converters [4, 13–15]. In addition, using interleaved configuration causes high-voltage gain and reduction of voltage stress [16–19]. Although the methods have advantages, they are costly and bulky and that encourage researchers to present new converters with novel configurations.

Hence, a cost effective and efficient converter was proposed in [20], which was called Z-source DC–DC converter. By using two inductors and two capacitors the Z-source network can be implemented. The inductors and capacitors of the Z-source have connections in X-shape that makes possibility to combine the Z-source network with the other converters and techniques such as boost converter, switched-inductor, and switched capacitor [21–23]. Owing to the not common grounded structure of the basic Z-source converter, it has limit applications. In [24], switched-inductor has been combined with a Z-source network that improves voltage gain. However, the combination has drawbacks and it is complex, costly, and bulky. The other option is applying a switched-capacitor into a Z-source DC–DC converter [25]. Similar to the previous case, the combination makes a complex and costly converter that is not commonly grounded. The other proposed structures have been focused on making the converter common grounded and reduction of voltage stress [1, 26, 27]. Quasi-Z source converter is the new kind of converter retrieved from the Z-source converter [28, 29]. Using the quasi-Z source structure reduces voltage stress and makes the converter common grounded [30]. Similar to the Z-source, the quasi-Z source can be combined with the other techniques as a switched capacitor to improve the converter characteristics as voltage gain and voltage stress [29]. However, the converter needs additional components that increase its complexity and cost.

This study presents a new DC–DC converter utilising Z-source network that is common grounded and its voltage gain is higher than the similar converters. The proposed converter has important advantages such as reduced voltage stress on its components and using smaller minimum inductance for the inductors in comparison with the converters including the Z-source network. Furthermore, it operates with high efficiency for duty cycles from 0 to 0.4.

To prove the positive points of the converter, first, it has been analysed. The obtained equations are used to compare the converter with the other converters that show its advantages. Then, a prototype is built to experiment with the converter operation quality.

2 Configuration of the proposed Z-source

The proposed converter consists of a common Z-source network and two additional components (a diode and a capacitor). The additional components improve the converter properties in comparison with the similar converters, which are introduced in the

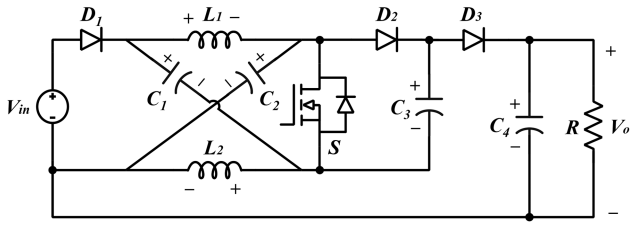


Fig. 1 *Configuration of the proposed converter*

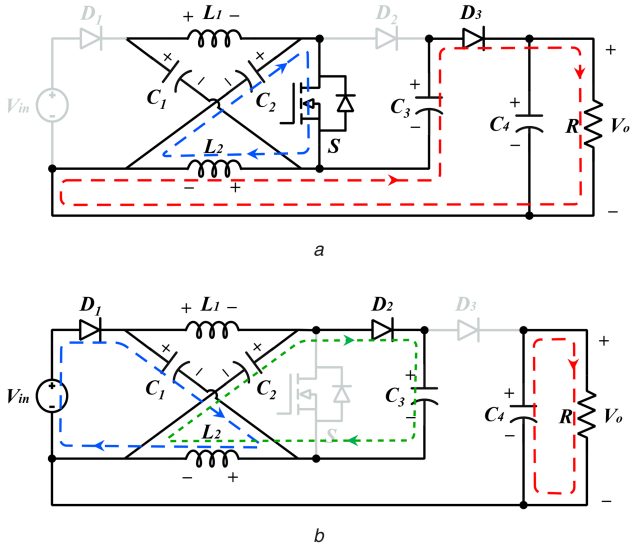


Fig. 2 *Switch on and off states for the proposed converter*
(a) First stage, the switch is on, ***(b)*** Second stage, the switch is off

next parts. Fig. 1 depicts the proposed converter structure consisting of a Z-source network (L_1, L_2, C_1 and C_2), three diodes, a switch, and two capacitors. In comparison with the conventional Z-source, the proposed one is common grounded.

3 Operation stages of the converter

This section explains the operation stages of the converter. The results of the analysis include the main equations of the converter with which its characteristics can be checked out. The components are assumed ideal and the converter operation for the switch turn on and turn off stages are shown in Fig. 2.

A pulse-width modulation (PWM) signal turns on the power switch when the signal is equal to one. The diodes D_1 and $D_2$are blocking and diode D_3 is on. According to the equivalent circuit in Fig. 2*a*, the state makes three possible loops during the operation. The first and second loops consist of L_1–C_1 and L_2–C_2, respectively. The capacitors (C_1 and C_2) discharge and energise inductors (L_1 and L_2) in the loops. The third loop includes L_2, C_3, D_3, C_4, and load (R) in which C_3 discharges energy to L_2 and load. Using the loops in Fig. 2*a*, circuit relations can be written as

$$\begin{aligned} v_{L1} = v_{L2} = v_{C1} = v_{C2} \rightarrow v_C = v_L, \\ v_o = v_{C3} + v_C. \end{aligned} \tag{1}$$

When the PWM signal is zero, the switch turns off and the equivalent circuit can be drawn as Fig. 2*b*. In this state, diode D_3 is blocking and the other diodes (D_1 and D_2) are on. The circuit is made of five loops that are highlighted in Fig. 2*b*. The first and second loops include inductors (L_1 and L_2), capacitors (C_1 and C_2), diode D_1, and voltage source. During the interval of the state, L_1 and L_2 discharge and energise C_1 and C_2, respectively. Furthermore, V_{in} takes part in the capacitor's charge during the interval of the state. The two loops have similarities in their operation that consist of L_1–C_1–D_2–C_3 and L_2–C_2–D_2–C_3. In the last loop, C_4 discharges the load and makes the load current continues. Based on the equivalent circuit, the following equations can be derived:

$$\begin{aligned} v_C + v_C - v_{C3} - v_{in} = 0 \rightarrow v_{C3} = 2v_C - v_{in}, \\ v_L = v_{in} - v_C. \end{aligned} \tag{2}$$

Steady state analysis leads to the essential equations of the converter. The inductors charge and discharge during a cycle and their average voltages are equal to zero. By assuming DC values of v_{in} and v_c as V_{in} and V_C, the inductor average voltage equation is

$$DV_C + (1-D)(V_{in} - V_C) = 0 \rightarrow V_C = \frac{1-D}{1-2D} V_{in}, \tag{3}$$

where D is the switching duty cycle. Substituting (3) into (2), V_{C3} can be described by V_{in}

$$V_{C3} = \frac{1}{1-2D} V_{in}. \tag{4}$$

Substituting (4) into (1), the voltage gain of the converter is as below

$$M = \frac{V_o}{V_{in}} = \frac{2-D}{(1-2D)}, \tag{5}$$

where the range of the duty cycle is $0 < D < 0.5$. From (5), the voltage gain of the converter is >2 (in $D = 0$, $M = 2$). When the duty cycle gets close to 0.5, voltage gain increases (for $D = 0.4$, the voltage gain is 8).

The other quality factors of the converter such as voltage stress on the components, output voltage ripple, the inductors current ripple, and minimum inductance of the inductors are analysed in the following.

3.1 Voltage stress on components

During the stages, the converter's components should withstand reverse voltage and not be affected. The voltage stress on the components is investigated in this part. The converter includes four capacitors and their voltage stress i obtained by the following equations. The voltages of C_1 and C_2 are equal and by substituting (5) into (3), their voltage stress is

$$V_C = \frac{1-D}{(2-D)} V_o. \tag{6}$$

During switch on the state, the voltage of C_3 is equal to V_o–V_C. So, substituting (5) into the relation gives its voltage stress as below. In addition, for the parallel capacitor with load, voltage stress is $V_{C4} = V_o$

$$V_{C3} = \frac{1}{(2-D)} V_o. \tag{7}$$

Semiconductors are the other components, which have to resist inverse voltage. When the switch is turned off, its voltage is equal to V_{C3} (Fig. 2*b*). Therefore, its voltage stress is

$$V_{Switch} = \frac{1}{(2-D)} V_o. \tag{8}$$

D_1 and D_2 are blocking during the switch operation (Fig. 2*a*). Therefore, their reverse voltage is obtained with the following equations:

$$V_{D1} = 2V_C - V_{in} \text{ and } V_{D2} = V_{C3}. \tag{9}$$

Substituting (5)–(7) into (9), voltage stress across the diodes is similar to the switch voltage stress

$$V_{D1} = V_{D2} = \frac{1}{(2-D)} V_o . \tag{10}$$

D_3 is blocking during turn off interval. Using Fig. 2*b*, the diode inverse voltage is obtainable

$$V_{D3} = V_o - V_{C2} = \frac{1}{(2-D)} V_o . \tag{11}$$

3.2 Minimum inductance of the inductors

To achieve output voltage ripple and size of the inductors, current equations for some of the components should be analysed. In this part, the converter operation is assumed in continuous current mode (CCM). Figs. 2*a* and *b* consider current relations are in on and off states. In the following equations, on and off suffixes define the power switch state, which means current relations are based on Fig. 2*a* for the on suffix and Fig. 2*b* for the off suffix. The inductors average current determines their inductances. Thus, they have to be obtained by using Fig. 2 and the current balance equation of the inductors as follows:

$$DI_{C1on} + (1-D) I_{C1off} = 0 , \tag{12}$$

$$I_{C1on} = I_{L1} \quad \text{and} \quad I_{C1off} = I_{L1} - I_{inoff} . \tag{13}$$

Substituting (13) into (12), the average current of L_1 is equal to the source average current

$$I_{L1} = (1-D) I_{inoff} \rightarrow I_{L1} = I_{inave} . \tag{14}$$

In this regard, the average current of L_2 is determined by using the following equations:

$$DI_{C2on} + (1-D) I_{C2off} = 0, \tag{15}$$

$$I_{C2on} = I_{L2} - I_{C4on} + I_o \;\&\; I_{C2off} = I_{L2} - I_{inoff} . \tag{16}$$

To complete the analysis, I_{C4on} is derived from its current balance equation

$$DI_{C4on} + (1-D) I_{C4off} = 0 \;\&\; I_{C4off} = I_o, \tag{17}$$

$$I_{C4on} = -\frac{(1-D)}{D} I_o . \tag{18}$$

Substituting (16) and (18) into (15) gives an average current of L_2

$$I_{L2} = (1-D) I_{inoff} - I_o \rightarrow I_{L2} = I_{inave} - I_o . \tag{19}$$

By the above equations, analysis of the inductors current ripple and size of their inductance is possible. During turn on state, the following equations can be written:

$$\begin{cases} L \mathrm{d}i_{L1}/\mathrm{d}t = V_{L1}, \\ \mathrm{d}t = DT_S \text{ and } \mathrm{d}i_{L1} = \Delta I_{L1} . \end{cases} \tag{20}$$

Substituting (5) and (6) into (1), the inductor voltage is

$$V_L = V_C = \frac{1-D}{(1-2D)} V_{in} . \tag{21}$$

Using (20) and (21), inductance and current ripple of L_1 are equal to

$$L_1 = \frac{D(1-D)}{(1-2D)\Delta I_{L1} f_s} V_{in}, \tag{22}$$

$$\Delta I_{L1} = \frac{D(1-D)}{(1-2D) L_1 f_s} V_{in} . \tag{23}$$

In DC–DC converters, the inductors charge and discharge with triangular waveform current. The waveform average is equal to $\Delta I_L/2$ on the boundary of current continuous and discontinuous modes ($I_{Lmin} = 0 \rightarrow I_L = \Delta I_L/2$). If we assume the converter is ideal, the average current of the source is $I_{inave} = ((2-D)/(1-2D)) I_o$. Substituting the inductor and source average currents into (23), minimum required inductance can be calculated as

$$L_{1min} = \frac{D(1-D)(1-2D)}{2(2-D)^2 f_s} R_{out} . \tag{24}$$

To achieve the minimum size of L_2, a similar analysis should be done. The only difference is in their average current equations ((14) and (19)). Thus, the equation of L_2 min is

$$L_{2min} = \frac{D(1-D)(1-2D)}{2(2-D)(1+D) f_s} R_{out} . \tag{25}$$

Design of the inductors based on current ripple or minimum inductance is possible by (22), (24) and (25). Using them depends on the design method and consideration of operation quality.

3.3 Output voltage ripple

Output voltage ripple can be found by studying the discharge of the parallel capacitor (C_4). Thus, the following relations are written:

$$\begin{cases} \Delta V_o = \Delta V_{C4}, \\ C_4 \mathrm{d}v_{C4}/\mathrm{d}t = i_{C4off}, \\ \mathrm{d}t = (1-D) T_S \text{ and } \mathrm{d}v_{C4} = \Delta V_{C4}, \\ \Delta V_o = \dfrac{i_{C4off}(1-D)}{C_4 f_S} . \end{cases} \tag{26}$$

From Fig. 2*b*, it can be concluded $i_o = i_{C4off}$, so the voltage ripple equation is

$$\Delta V_o = \frac{i_o(1-D)}{C_4 f_S} \rightarrow \frac{\Delta V_o}{V_o} = \frac{(1-D)}{R_o C_4 f_S} . \tag{27}$$

According to (27), increasing the duty cycle reduces the percentage of the voltage ripple that can be mentioned as an advantage.

3.4 Power loss of components

The main parts of DC–DC converters losses can be classified into conduction loss and switching loss. Switching loss has to be analysed in diode and power switch. Since the flowing current in components causes noticeable conduction loss in most of them. Thus, conduction loss of power switch, diodes, inductors, and capacitors is investigated for the converter.

Power switch losses: Conduction loss of a switch has a general equation similar to (29). According to (14), (16) and (18), the switch on state current (I_{Son}) is as follows:

$$I_{Son} = \frac{1+D}{D(1-2D)} I_o . \tag{28}$$

Conduction loss of the power switch is equal to

$$P_{SC} = r_{DS} I_{Srsm}^2 . \tag{29}$$

where I_{sms} and r_{DS} are switch current and switch resistance.

Using (28) and (29), the final equation for the switch conduction loss can be written as

$$P_{SC} = \frac{r_{DS}}{R_o} \left(\frac{(1+D)^2}{D(1-2D)^2} \right) P_o, \tag{30}$$

where P_o is the output power of the converter.

Turn-on and turn-off losses of a power switch have a common equation such as (31) which is obtained for the proposed converter's switch in (32)

$$P_{SS} = V_{switch} I_{switch_{ave}} (t_r + t_f) \frac{f_s}{2}, \tag{31}$$

$$P_{SS} = \frac{(1+D)(t_r + t_f) f_s}{2(2-D)(1-2D)} P_o, \tag{32}$$

where P_{SS}, t_r,t_f, V_{switch}, $I_{switch_{ave}}$ and f_s are switching loss, turn-on delay time, turn off delay time, the voltage of switch, the average current of a switch, and switching frequency, respectively.

Diode power losses: Diode power loss is classified into conduction loss, forward voltage drop loss, and switching loss. Equation (33) illustrates forward voltage drop loss of diode (P_{Df}). Using the equation, the loss is obtained for the converter's diodes. Equation (34) contains the sum of the diodes forward voltage drop loss

$$P_{Df} = V_F I_{Dave}. \tag{33}$$

where V_F and I_{Dave} are a forward voltage drop of the diode and an average current of diode, respectively

$$P_{Df} = \left(\frac{V_{F1}}{V_{in}} + \frac{V_{F2}(1-2D)}{(2-D)V_{in}} + \frac{V_{F3}(1-2D)}{(2-D)V_{in}} \right) P_o. \tag{34}$$

The second calculated loss for the diodes is conduction loss (P_{DC}). The sum of the diodes conduction loss for the converter is

$$P_{DC} = \left(\frac{r_{D1}(2-D)^2}{(1-D)(1-2D)^2 R_o} + \frac{r_{D2}}{(1-D)R_o} + \frac{r_{D3}}{DR_o} \right) P_o, \tag{35}$$

where r_{D1}, r_{D2} and r_{D3} are resistances of converter's diodes. The last equation of diode losses is switching loss (P_{DS}) that has a common equation such as (36). Equation (37) is extracted for switching loss of the converter's diodes

$$P_{DS} = V_D I_{D_{ave}} t_{rr} \frac{f_s}{2}, \tag{36}$$

$$P_{DS} = \left(\frac{t_{rr1}}{2(1-2D)} + \frac{t_{rr2}}{2(2-D)} + \frac{t_{rr3}}{2(2-D)} \right) f_s P_o, \tag{37}$$

where t_{rr}, V_D, and $I_{D_{ave}}$ are reverse recovery time of diode, diode voltage, and diode average current, respectively.

- *Inductors conduction loss*: Conduction loss of the inductors (P_{LCU}) is derived using (38) and written as (39).

$$P_{LCU} = r_{L1} I_{L1rms}^2 + r_{L2} I_{L2rms}^2, \tag{38}$$

$$P_{LCU} = \frac{r_{L1}(2-D)^2 + r_{L2}(1+D)^2}{(1-2D)^2 R_o} P_o. \tag{39}$$

Capacitors conduction loss: Capacitor resistance causes conduction loss. The proposed converter has four capacitors and the sum of their conduction loss is

$$\begin{aligned} P_{CC} &= \left(r_{C1} \left(\frac{\sqrt{D}(1-D)(2-D) + D\sqrt{1-D}(2-D)}{(1-D)(1-2D)} \right)^2 \right. \\ &+ r_{C2} \left(\frac{(D^2 - D + 1)(\sqrt{1-D} + \sqrt{D})}{(1-2D)\sqrt{D(1-D)}} \right)^2 \\ &+ r_{C3} \left(\frac{\sqrt{1-D} + \sqrt{D}}{\sqrt{D(1-D)}} \right)^2 \\ &\left. + r_{C4} \left(\frac{\sqrt{D}(1-D) + \sqrt{D(1-D)}}{\sqrt{D}} \right)^2 \right) \frac{P_o}{R_o}, \end{aligned} \tag{40}$$

where P_{CC} and r_C are conduction loss of the four capacitors and the capacitor's resistance, respectively.

The introduced loss equations are used in efficiency calculations for comparing the calculations with the experiments in Section 5 (Figs. 3*a* and 4*a*). The loss calculations are possible with the values in Table 1.

4 Comparison with other converters

The converter quality factors are compared with similar converters in Figs. 5–7 and Table 2. Fig. 5 depicts a comparison between voltage gains of the converters as the first compared factor. The voltage gain curves are drawn (based on the equations in Table 2) for the boost converter, two-level boost converter, quadratic boost converter, Z-source DC-C converter, converter in [1], and the proposed converter.

As shown in Fig. 5, the voltage gain to duty cycle (M–D) curves from top to bottom are the proposed converter, the converter in [1], Z-source DC–DC converter, quadratic boost converter, two levels boost converter and boost converter, respectively. Fig. 5 demonstrates that the proposed converter has a higher voltage gain than the compared converters for the same duty cycles. This excellence can be seen in the whole duty cycles. Furthermore, the proposed converter, two level boost converter and converter in [1], the start boosting voltage from $D = 0$ and $M = 2$. However, the quadratic boost converter and Z-source DC–DC converter have $M = 2$ in $D = 0.29$ and 0.25, respectively. In addition, the proposed

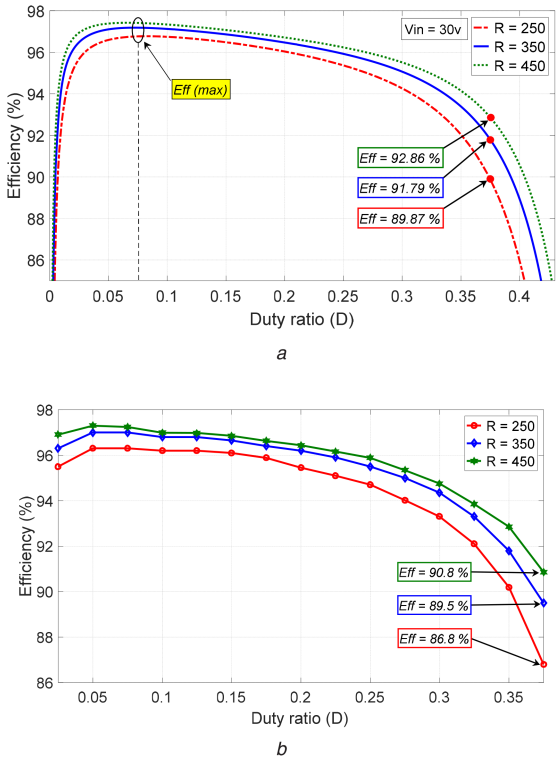
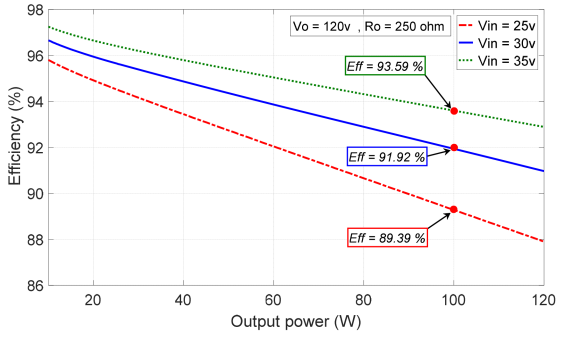
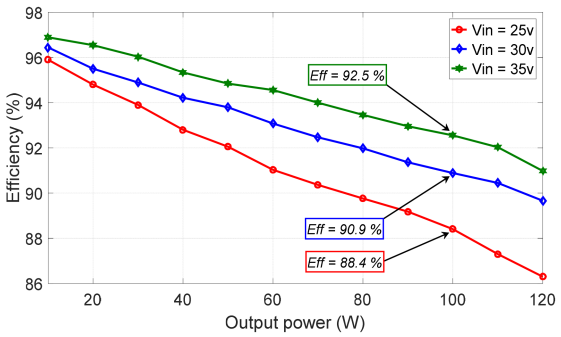


Fig. 3 *Efficiency for different duty cycles – $V_{in} = 30$ V, $R = 250$, 350 and 450 Ω*

(a) Theoretical results, **(b)** Experimental results



a



b

Fig. 4 *Efficiency of the converter during load variation with different input voltage–output voltage is 120 V (it is controlled)*
(a) Theoretical results, ***(b)*** Experimental results

Table 1 Specifications of the laboratory prototype of the proposed converter

Parameter	Value
input voltage	30 V
inductors (L_1 and L_2)	1 mH
inductors resistances (r_1 and r_2)	0.1 Ω
capacitors (C_1, C_2, and C_3)	680 μF
output capacitor (C_4)	680 μF
capacitors' resistance	0.025 Ω
switching frequency	25 kHz
switch on resistance (R_{on})	0.04 Ω
turn-on + turn-off delay times of the switch ($t_r + t_f$)	108 ns
diode forward voltage (V_{DF})	0.2–0.8
diodes' resistance	0.04 Ω
reverse recovery time of diodes	100 ns
resistive load (R)	250 Ω

converter raises its output voltage with the highest slope and it arrives at maximum voltage gain in the lowest duty cycle in comparison with the others.

For the proposed converter, voltage stress across the switch and diodes depends on the duty cycle. In the duty cycle equal to zero, the voltage stresses of the two-level converter, the converter in [1] and the proposed converter are $V_o/2$. Increasing the duty cycle influences the voltage stresses of the proposed converter and converter in [1]. The two converters operate until $D = 0.4$ in which the voltage stresses have their maximum values. For $D = 0.4$, voltage stress across semiconductors has values equal to $V_o/1.6$ and $V_o/1.2$ for the proposed converter and the converter in [1], respectively. Fig. 6 depicts a comparison between voltage stress on the components of the conventional Z-source converter, the converter in [1], and the proposed converter. The converters are based on a Z-source network that can be good choices for the comparison. The results show that voltage stress on the switch, diodes, and capacitors in the proposed converter is lower.

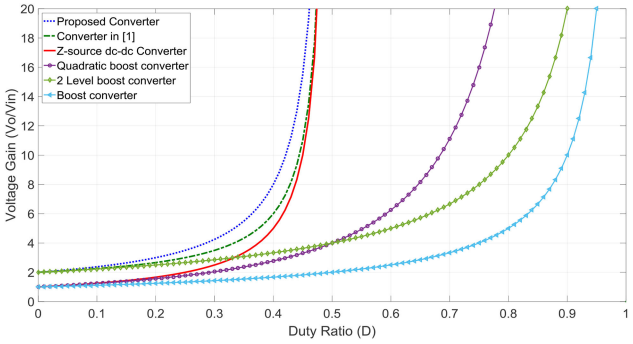


Fig. 5 *Voltage gain variations for different duty cycles for the compared converters*

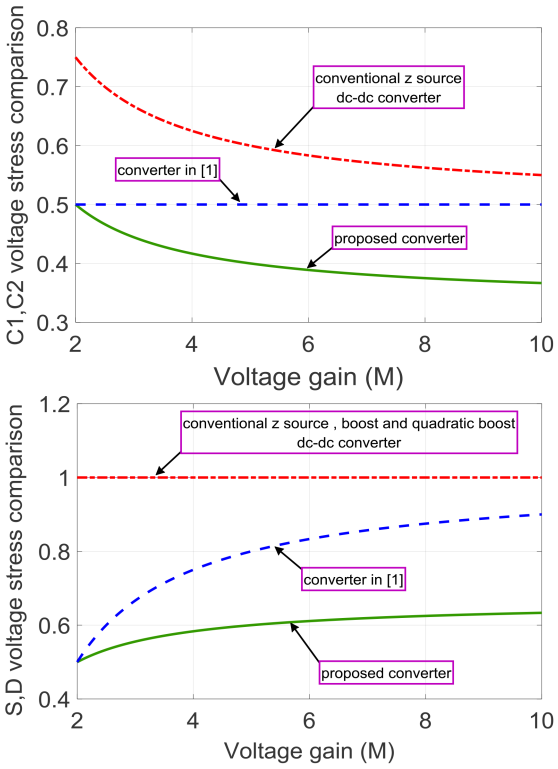


Fig. 6 *Voltage stress on the components of the converters*

The last discussion of the quality factors is about minimum inductance of the inductors. Fig. 7 illustrates the L_{min} of the converters based on the Z-source network. In the proposed converters L_{min1} and L_{min2} have different equations (24) and (25), so two curves are drawn for the converter. However, the converter in [1] and conventional Z-source have similar equations for their inductors. The inductances depend on the duty cycle, load, and frequency. Hence, the load and frequency are assumed 350 Ω and 25 kHz, respectively, and the inductance curves are drawn for different duty cycles. For the worst case, the proposed converter needs two inductors with minimum inductances equal to 211 and 314 μH (Fig. 7). The converter in [1] should have two inductors with minimum inductance equal to 500 μH and the values increase in the conventional Z-source until 680 μH (Fig. 7). According to the negative effects of parasitic components on DC–DC converters operation, smaller inductors in the proposed converter is an important positive point.

4.1 Cost comparison

The proposed converter has additional components (A diode and a capacitor) in comparison with the converter in [1]. This may cause to choose the converter in [1] instead of it. Hence, this study compares the quality factors of the proposed converter with similar converters as in [1]. It has positive points (higher voltage gain, the

lower voltage stress on its components and needs smaller inductors) in comparison with the converter in [1] and the others. However, it has two additional components in comparison with the main reference [1]; the positive quality factors may reduce its cost. Lower cost makes the converter as a good choice, which has higher quality. Hence, the cost of the components is compared for the proposed converter and the converter in [1].

Inductors cost: Both converters have two inductors. According to the explanations, the proposed converter needs smaller inductors. A comparison of the inductors is possible after designing their cores. To design the cores, it is assumed output power is 150 W and the cores are magnetics molypermalloy powder (MPP) as a good choice. MPP core is a kind of powder core that has appropriate characteristics to be used in the compared converters. Table 3 covers essential results of the converters analysis for designing their inductors. In Table 3, I_L, J, I_{pk} and E are DC current, current density, current peak and energy handling capability of a core, respectively. It is assumed, similar twisted wires are used in the inductors with cross section (A_{CU}) equal to 0.0078 cm2. During core calculations, maximum flux density (B_m) and maximum window utilisation factor (K_u) are 0.3 and 0.4, respectively.

In the first step, inductor's core proposed in [1] is designed. Equation (41) determines the area product for inductor core (A_P). Calculation of A_P helps to determine the cores part number and their characteristics from the datasheet

$$A_P = \frac{2 \times 10^4}{B_m J K_u}, \tag{41}$$

Using the values in Table 3, assumptions and (41), $A_P = 0.99$. Among MPP cores, core with part number: 55,894 has a suitable A_P value to be utilised for [1] inductors. The core parameters such as window area (W_a), magnetic path length (MPL), mH for 1000 turns (A_L) and relative permeability (μ) are equal to 1.517 cm^2, 6.35 cm, 75 mH and 60, respectively.

Equation (42) shows the relation between the extracted values from the datasheet and the desired relative permeability (μ_Δ).

$$\mu_\Delta = \frac{B_m \cdot \mathrm{MPL}10^4}{0.4\,\pi W_a J K_u}. \tag{42}$$

According to the core parameters and current density of the inductors (700 A/cm^2), its desired relative permeability is 35.7. The MPP core has relative permeability equal to 60, which guaranties inductor's operation in higher output powers without saturation. This happens because of the higher value of the core relative permeability (60) in comparison with the desired value (35.7).

A number of coil turns equation is

$$N = 1000\sqrt{\frac{L(\mathrm{mH})}{A_L}}. \tag{43}$$

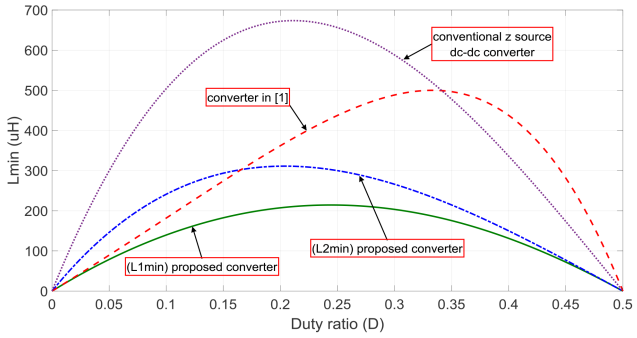


Fig. 7 *Minimum inductance of the two inductors for the proposed converter, conventional Z-source, and converter in [1]*

Table 2 Comparisons between the proposed converter and other high-voltage-gain converters

Converters	Voltage-gain	Amount of inductors	Amount of capacitors	Amount of diodes	Amount of power switches	Maximum voltage stress across diodes	Maximum voltage stress across power switches	Common ground
boost converter	$1/(1-d)$	1	1	1	1	V_o	V_o	yes
2-Level boost converter	$2/(1-d)$	1	3	3	1	$V_o/2$	$V_o/2$	yes
quadratic boost converter	$1/(1-d)^2$	2	2	3	1	V_o &$(1-d)V_o$	V_o	yes
z-source converter	$1/(1-2d)$	2	3	2	1	V_o	V_o	no
converter in [1]	$2(1-d)/(1-2d)$	2	3	2	1	$V_o/(2-2d)$	$V_o/(2-2d)$	yes
proposed converter	$(2-d)/(1-2d)$	2	4	3	1	$V_o/(2-d)$	$V_o/(2-d)$	yes

Table 3 Essential parameters of the converters for designing their inductors (output power is 150 W)

Essential parameters	Values for ref. [1] inductors ($L_1 = L_2$)	Values for the proposed converter inductor (L_1)	Values for the proposed converter inductor (L_2)
inductance, μH	374	165	139.5
I_L, A	2.64	4.998	4.22
I_{rms}, A	4.98	9.4	7.95
j, (A/cm^2)	700	1200	1000
I_{pk}, A	4.74	9	7.6
e, watt-seconds	0.0042	0.00668	0.004

Table 4 Comparison of MOSFET price for the proposed converter and the converter in [1]

	MOSFET model	Manufacture	V_{DS}	Price
case study 1: V_{in} = 50 V, V_o = 300 V				
proposed converter	IRFP260Npbf (R_{DSon} = 40 mΩ, I_d = 50 A, P_d = 300 W)	Infineon	200 V	$3.13
converter in [1]	IRFP300P227 (R_{DSon} = 40 mΩ, I_d = 50 A, P_d = 300 W)	Infineon	300 V	$5.94
case study 2: V_{in} = 25 V, V_o = 150 V				
proposed converter	IRF540Npbf (R_{DSon} = 44 mΩ, I_d = 33 A, P_d = 140 W)	Infineon	100 V	$1.05
converter in [1]	IRFU4615 (R_{DSon} = 42 mΩ, I_d = 33 A, P_d = 144 W)	Infineon	150 V	$1.57

Table 5 Comparison of diodes price for the proposed converter and the converter in [1]

	Diodes model	Manufacture	V_{KA}	Price
case study 1: V_{in} = 50 V, V_o = 300 V				
proposed converter	SBR20A200CT(V_F = 0.96 V, I_F = 20 A)	Diodes Incorporated	200 V	$1.16
converter in [1]	SBR20A300CT (V_F = 1.06 V, I_F = 20 A)	Diodes Incorporated	300 V	$2.36
case study 2: V_{in} = 25 V, V_o = 150 V				
proposed converter	SBR10100CT (V_F = 0.8 V, I_F = 10 A)	Diodes Incorporated	100 V	$0.73
converter in [1]	SBR101SOCT (V_F = 0.92 V, I_F = 10 A)	Diodes Incorporated	150 V	$1.15

The calculated number of turns is 70 and it is used in (44) to determine the window utilisation factor of the inductors

$$K_{uL} = \frac{NA_{CU}}{W_a} \tag{44}$$

Using the core parameters and N, the window utilisation factor (K_{uL}) is 0.36 which is lower than the maximum value ($K_u = 0.4$). The results demonstrate that the core window has enough space for inductors with more turns. Based on the results, it seems the core with part number: 55,894 is suitable for the inductors of [1].

A similar method is used to select the inductor's core of the proposed converter. However, MPP- 55,894 can be utilised in the converter, the converter's inductors have too lower desired relative permeability (it is about 20 for both of them) and the inductors window utilisation factor is 0.2. In addition, the inductors need core with a lower area product. Hence, a smaller MPP core with part number: 55,059 is chosen. The core (MPP-55059) parameters such as window area (W_a), MPL, mH for 1000 turns (A_L) and relative permeability (μ) are equal to 1.356 cm^2, 5.67 cm, 43 mH, and 60, respectively. Using the values and (42), (43) and (44), the proposed converter's inductors are analysed as below

$$\mu_{\Delta 1} = \frac{0.3 \times 5.67 \times 10^4}{0.4\,\pi \times 1.356 \times 1200 \times 0.4} = 20.79,$$

$$\mu_{\Delta 2} = \frac{0.3 \times 5.67 \times 10^4}{0.4\,\pi \times 1.356 \times 1000 \times 0.4} = 24.96,$$

$$N_1 = 1000\sqrt{\frac{0.165}{43}} = 62,$$

$$N_2 = 1000\sqrt{\frac{0.139}{43}} = 57,$$

$$K_{uL1} = \frac{62 \times 0.0078}{1.356} = 0.36,$$

$$K_{uL2} = \frac{57 \times 0.0078}{1.356} = 0.33,$$

where $\mu_{\Delta 1}$, $\mu_{\Delta 2}$, N_1, N_2, K_{uL1} and K_{uL2} are the desired relative permeability of L_1 and L_2, number of turns for L_1 and L_2 and window utilisation factor of L_1 and $L2$, respectively. The desired relative permeability of L_1 and $L2$ is lower than the core relative permeability. Furthermore, the inductors window utilisation is lower than the maximum value (0.4). Thus, the results prove that the core is suitable for L_1 and L_2.

Price of cores with part numbers 55059 and 55894 are 2.4 and 3.6$, respectively. Therefore, the price of the core for the proposed converter is lower than the chosen core for the converter in [1].

- *Power switch cost*: According to the analysis in Fig. 6, the converter's power switch has lower voltage stress for different voltage gains. The equations in Table 2 help to calculate maximum voltage stress across the power switch that is an important parameter in metal oxide semiconductor field effect transistor (MOSFET) price definition. To compare the converters, two case studies are introduced and MOSFET prices are found for them (Table 4). Voltage stress of MOSFET in case study 1 is 183.26 and 250 V for the proposed converter and converter in [1], respectively. The basis of choosing the MOSFETs in Table 4 is the calculated values using equations in Table 2. In addition, the voltage stress in case study 2 is 91 and 125 V for the proposed converter and the converter in [1], respectively.
- *Diodes cost:* The proposed converter and converter in [1] contain three and two diodes in their structures, respectively. Similar to the previous part, the voltage stress on the diodes is computed using Table 2. Table 5 shows the details of the chosen diodes. Maximum voltage stress across the diodes has an equation that is extracted from the theory part (Table 2). The voltage stress in case study 1 is 183.26 and 250 V for the proposed converter and converter in [1], respectively. Furthermore, the value in case study 2 is 91 and 125 V for the proposed converter and converter in [1], respectively.
- *Capacitors cost*: The proposed converter has four capacitors that have lower voltage stress in comparison with capacitors in [1]. Calculations of voltage stress on the diodes are done using (6) and (7). In addition, the voltage stress of C_4 is equal to V_o. The voltage stresses for the converter in [1] are calculated based on the analysis in the study. The voltage stresses for the proposed converter in case study 1 are

$$V_{C1} = V_{C2} = 116.74\,\text{V}, V_{C3} = 183.26\,\text{V} \text{ and } V_{C4} = 300\,\text{V}.$$

The values for the converter in [1] are (case study 1)

$$V_{C1} = V_{C2} = 150\,\text{V} \text{ and } V_{C3} = 300\,\text{V}.$$

The voltage stresses for the proposed converter in case study 2 are

$$V_{C1} = V_{C2} = 58.37\,\text{V}, V_{C3} = 91\,\text{V} \text{ and} V_{C4} = 150\,\text{V}.$$

The values for the converter in [1] are

$$V_{C1} = V_{C2} = 75\,\text{V} \text{ and } V_{C3} = 150\,\text{V}.$$

According to the voltage stress values, the capacitors are chosen for the converters (see Table 6).

Total cost: Using Tables 3–6, the converter's components cost can be calculated. Thus, the total cost of the proposed converter for case study 1 and case study 2 is 28.76 and 14.9$, respectively. The

values for the converter in [1] are 31.18 and 17.91$. The proposed converter has a lower cost in comparison with the converter in [1].

Therefore, the proposed converter seems a better candidate for industry and research applications (its positive points in comparison with the converter in [1] consist of lower voltage stress on the components, higher voltage gain, inductors with smaller size and lower cost).

5 Experimental results

To analyse the proposed converter, a prototype is built as shown in Fig. 8. Design and implementation of the converter are done according to the analysis and available power electronic components, which are listed in Table 1.

The inductor core is ferrite with an ETD39 identification number. To reduce skin effect and coil resistance, four string wires are twisted. MOSFET is IRFP260N which has turn on resistance equal to $r_{DS} = 0.04\ \Omega$. MBR150CT is the used diode that operates in a good way during switching with 25 kHz frequency. The inductors are chosen with higher values to limit current ripple in the worse cases ($L_{min}$is not selection criteria here).

Fig. 9 depicts experimental results for the proposed Z-source converter. The results consist of operation quality factors of the converter as output voltage, the voltage stress on the components and the inductors current ripple.

The converter operates in $0 \ll D \ll 0.4$ in accordance with (5). According to the voltage gain equation, output voltage for duty cycle equal to 0.3 should be 127.5 V. The value in the experiment is 123.7 V (Fig. 9*a*), which has 3% difference with the theoretical value. The difference occurs due to the influence of equivalent series resistance (ESR) in the voltage conversion ratio and voltage drop on semiconductors. To illustrate output voltage quality, a zoomed part is shown in Fig. 9*a*, which does not include spikes. Using (7)–(11), voltage stress on the diodes and the switch for output voltage equal to 127.5 V for $D = 0.3$ is 75 V. In the experiment, voltage stress on D_1, D_2, D_3 and the switch is 70, 71.2, 73.14 and 72.22 V, respectively (Fig. 9*c*–*e*). Voltage stress on capacitors C_1, C_2, C_3, and C_4 is 51, 50.4, 73.6 and 123.7 V, respectively (Figs. 9*b* and *c*). The values have to be 52.5 V for C_1 and C_2, 75 V for C_3 and 127.5 V for C_4. It can be seen, experimental results are in a good accordance with the calculated ones. Fig. 9*f* depicts inductors current that are continuous with appropriate ripples. The inductors current continuous mode proves the suitable design method for the inductors. The converter operates near maximum duty cycles and for higher duties, the inductor's current is continues too.

Fig. 3 and 10 illustrate efficiency and voltage gain for different duty cycles. According to the results, the converter boosts input until six times with efficiency >87% for $R \geq 250\ \Omega$ (Figs. 3 and 10). It converts input voltage with voltage gain equal to 5.5 and efficiency >90% (for $R = 250$, 350 and 450 Ω). The converter voltage gain reaches 7.45 for $R = 450\ \Omega$ with efficiency >90% (Fig. 11 and Fig. 3*a*). Achieving voltage gain equal to 7.5 with efficiency >90% for higher output power is possible by using redesigned components and prototypes that are more qualified.

The calculations and experiments are comparable to the results that are depicted in Figs. 3 and 10. There is 2–3% difference between experimental and theoretical results in Fig. 3. The difference is visible by comparing the written values for $D = 0.375$ in Fig. 3*a* and *b*. The difference occurs because of not considering core loss calculation in theory (section 3.4). For the lower duty cycles, the difference is <2%. Thus, the calculations and experiments are in accordance with each other.

According to the results in Fig. 3*a*, the converter has maximum efficiency for $D = 0.075$. In $0 \leq D \leq 0.02$ efficiency is <90%. It happens because a significant percentage of input power is spent on core loss and switching loss. When output power increases, the losses percentage decreases that cause higher efficiency (in $D =$ 0.075 the converter has the highest efficiency). After the point, efficiency drops because of increasing conduction losses of inductors, capacitors and other components (Figs. 3*a* and *b*).

Table 6 Comparison of capacitors price for the proposed converter and the converter in [1]

	Capacitor number	Manufacture	Voltage rating	Price
case study 1: $V_{in} = 50$ V, $V_o = 300$ V				
proposed converter	C_1 (470 μF)	United Chemi-Con (UCC)	160 V	$3.18
	C_2 (470 μF)	UCC	160 V	$3.18
	C_3 (470 μF)	UCC	200 V	$3.99
	C_4 (330 μF)	Nichicon	400 V	$6.96
	C_1 (470 μF)	United Chemi-Con (UCC)	160 V	$3.18
	C_2 (470 μF)	UCC	160 V	$3.18
	C_3 (330 μF)	Nichicon	400 V	$6.96
case study 2: $V_{in} = 25$ V, $V_o = 150$ V				
proposed converter	C_1 (470 μF)	United Chemi-Con (UCC)	63 V	$0.93
	C_2 (470 μF)	UCC	63 V	$0.93
	C_3 (470 μF)	UCC	100 V	$1.83
	C_4 (470 μF)	UCC	160 V	$3.18
converter in [1]	C_1 (470 μF)	United Chemi-Con (UCC)	100 V	$1.83
	C_2 (470 μF)	UCC	100 V	$1.83
	C_3 (470 μF)	UCC	160 V	$3.18

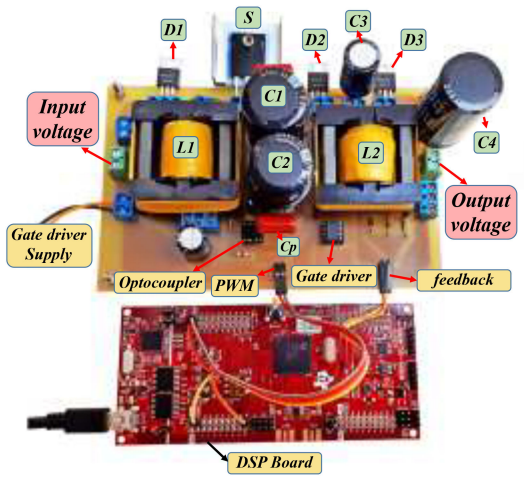


Fig. 8 *Prototypes of the proposed converter – digital signal processing board is Texas instruments TMS320F28379D*

In the next step, a proportional–integral controller is used to regulate output voltage during load variation. The controller is designed based on a small signal model that is not considered in the study. Output voltage (V_o) regulation for changes illustrates the controller operation quality. The results prove that it is designed properly (Fig. 12). The controller has a very fast response to load variation and input voltage variation under transient conditions. In Fig. 12, the input voltage is varied during a short time from 15 to 32.4 V and the controller tracks the changes very fast with regulating the output voltage. In the next step, the input voltage is decreased from 32.4 to 16 V and the controller regulates output voltage similar to the previous step. Fig. 4 illustrates the efficiency of the converter during load variation with controlled output voltage. The theoretical and experimental results are obtained for output voltage equal to 120 V for different input voltages (25, 30 and 35 V). The converter transfers power ≤ 100 W with efficiency >90% for $V_{in} \geq 30$ V (in $V_{in} = 25$ V efficiency for 100 W is 88%). Furthermore, theoretical and experimental efficiencies in 120 W with $V_{in} = 30$ V are 91 and 89.6%, respectively (Figs. 4*a* and *b*). The converter prototype is designed and prepared for output power, input voltage and output voltage equal to 100 W, 30 and 120 V,

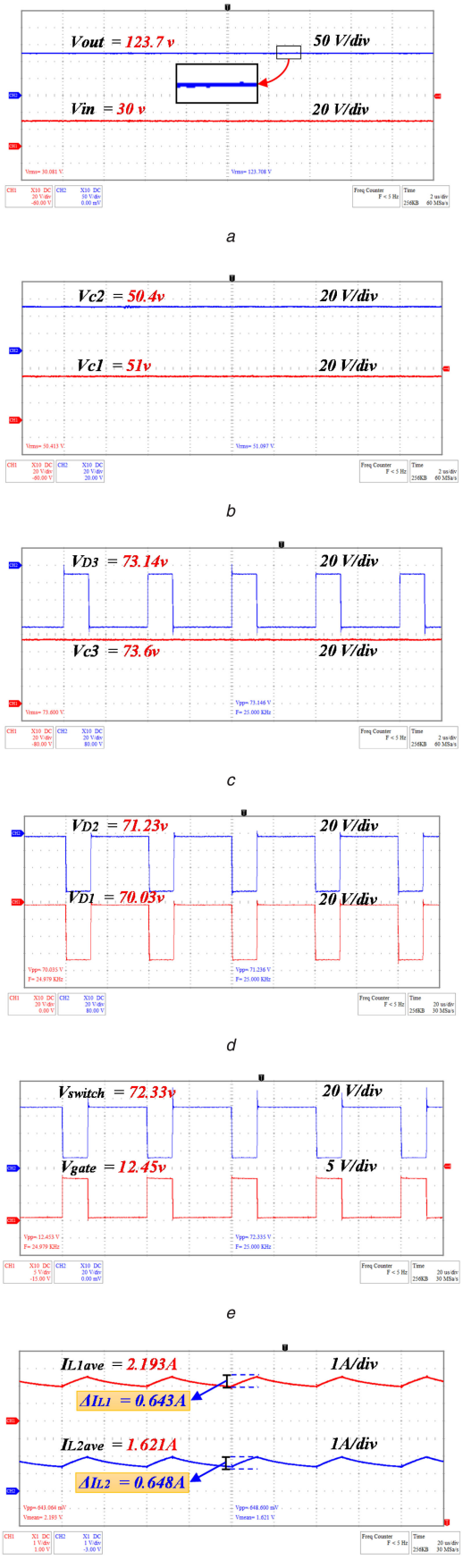


Fig. 9 *Experimental results of the proposed converter – for duty cycle equal to 0.3*
(a) Input and output voltages, ***(b)*** voltage of capacitors C_1 and C_2, ***(c)*** voltage of D_3 and capacitor C_3, ***(d)*** the diodes voltage (D_1 and D_2), ***(e)*** the switch voltage and gate voltage, ***(f)*** the inductors (L_1 and L_2) current and their current ripples

respectively. Thus, to prove the converter operation quality, most of the results in the range of the designed values are discussed.

The theoretical curves are drawn based on all mentioned power losses in Section 3 and they have 1–2% differences with

experimental curves. According to the values shown in the curves (Figs. 4*a* and *b*), the differences are ≤1% for output power ≤100 W. Thus, the calculations and experiments are in accordance with each other.

6 Conclusion

A DC–DC converter with high-voltage gain is proposed based on the Z-source network. The converter is commonly grounded and its voltage gain is higher than the compared converters for the whole duty cycles. The converter boosts input until six times with efficiency >87% for $R \geq 250\ \Omega$. It converts input voltage with voltage gain equal to 5.5 and efficiency >90% (for $R = 250$, 350 and 450 Ω). The converter voltage gain reaches 7.45 for $R = 450\ \Omega$ with efficiency >90%. Achieving voltage gain equal to 7.5 with efficiency >90% for higher output power is possible using redesigned components and prototypes that are more qualified. Comparing with the converter in [1] and the conventional Z-source converter, lower voltage stress appears on the switch and diodes of the proposed converter. According to the analysis, voltage stress on C_1 and C_2 is <0.4 V_o. Furthermore, voltage stress on the switch and diodes is <0.65 V_o. The other advantage of the converter is its smaller inductors in comparison with the two-compared converters. In order to investigate minimum inductance of the inductors, inductance equations are obtained for the converters. For a definite condition, the proposed converter needs two inductors with minimum inductances equal to 211 and 314 μH. The converter proposed in [1] should have two inductors with minimum inductances equal to 500 μH and the values increase in the conventional Z-source until 680 μH (for the two inductors). Smaller inductors reduce parasitic effects and increase the converter efficiency.

Output voltage does not contain spikes and increasing duty cycle reduces its voltage ripple. The converter includes one extra diode and one extra capacitor in comparison with the main reference, but it has some advantages as higher voltage gain in lower duty cycles, the lower voltage stress on its components and smaller inductors, which justify the extra components. In addition, the total cost of the proposed converter for case study 1 and case study 2 is 28.76 and 14.9$, respectively. The values for the converter in [1] are 31.18 and 17.91$. Thus, the proposed converter has a lower cost in comparison with the converter in [1]. Therefore, it is a better choice for industry and research applications.

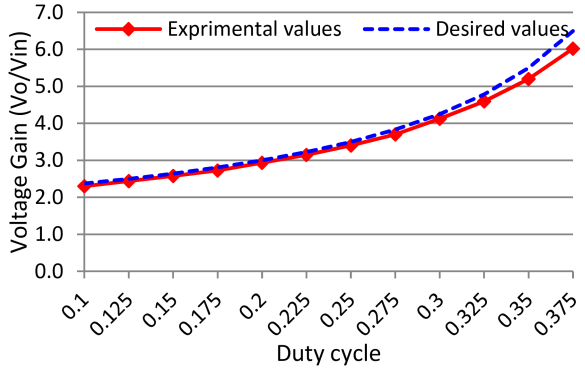


Fig. 10 *Voltage gain for different duty cycles – V_{in} = 30 V, R = 250 Ω*

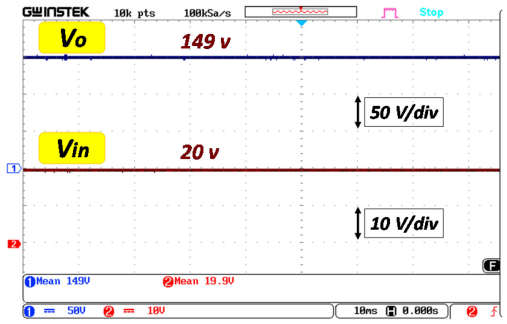


Fig. 11 *Output voltage for D = 0.4, R = 450 Ω*

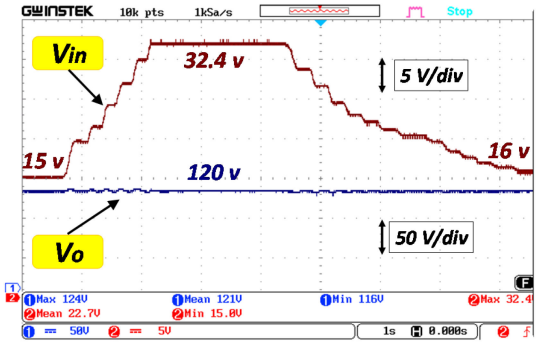


Fig. 12 *Controller operation during input voltage variations – R = 250 Ω*

7 References

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