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High Step-Up Quasi-Z Source DC-DC Converter

Mohammad Mehdi Haji-Esmaeili, Ebrahim Babaei, *Senior Member, IEEE,* and Mehran Sabahi

***Abstract*—In this paper, a high step-up Quasi-Z Source (QZS) DC-DC converter is proposed. This converter uses a hybrid switched-capacitors switched-inductor method in order to achieve high voltage gains. The proposed converter have resolved the voltage gain limitation of the basic QZS DC-DC converter while keeping its main advantages such as continuous input current and low voltage stress on capacitors. Compared to the basic converter, the duty cycle is not limited, and the voltage stress on the diodes and switch isn't increased. In addition to these features, the proposed converter has a flexible structure, and extra stages could be added to it in order to achieve even higher voltage gains without increasing the voltage stress on devices or limiting the duty cycle. The operation principle of the converter and related relationships and waveforms are presented in the paper. Also, a comprehensive comparison between the proposed and other QZS based DC-DC converters is provided which confirms the superiority of the proposed converter. Simulations are done in PSCAD/EMTDC in order to investigate the MPPT capability of the converter. In addition, the valid performance and practicality of the converter are studied through the results obtained from the laboratory built prototype.**

Index Terms—DC-DC converter, High step-up, Impedance network, Quasi-Z source

I. Introduction

Nowadays, power electronic converters play an important role as renewable energy interface devices [1]-[3]. Also, they are widely used in other applications such as distributed generation resources, power factor correction equipment, hybrid electrical vehicles, air-space industries, and HVDC [4]-[7]. Power electronic converters are generally classified as DC-DC, AC-DC, DC-AC and AC-AC. In some applications, multi-stage power conversion is required, and simultaneous use of several different types of converters is needed. This increases the number of elements which will result in lower efficiency, higher power loss, higher possibility of failure and lower reliability of the whole system. Impedance network based converters as an emerging technology in energy conversion are invented to overcome these disadvantages [8], [9]. They have capability of single-stage power conversion, and they could overcome the limitations of classical converters. Single-stage power conversion will result in important advantages such as fewer components, lower power loss, higher efficiency, higher reliability and lower cost compared to multi-stage conversion. Various impedance network based converters were proposed in the recent years. A comprehensive review of these structures is given in [10], [11]. Impedance networks proposed in recent years can generally be classified as: 1-Transformer/coupled inductor based (TCIB), and, 2-non-transformer/coupled inductor based (n-TCIB). Comparing these two structures, TCIB structures have two main advantages as higher voltage gain and electrical isolation between input and output. On the other hand, n-TCIB converters have advantages such as lower volume, lower weight, lower cost, lower voltage and current stress on their elements, lower power loss, and higher efficiency. These advantages have made them more popular. However, their main weakness is their lower voltage gain which can limit their use in high gain applications. Generally, there are four different methods which have been proposed in order to increase the voltage gain of n-TCIB converters using: 1-diode-capacitor-inductor units [12], 2-switched-inductor units [13], 3-switched-capacitor units [14], and, 4-hybrid switched-capacitors switched-inductors units [15].

Among different types of n-TCIB network based converters, quasi-Z source (QZS) network has some key advantages such as continuous input current, low voltage stress on capacitors, and, common ground between input and output of the circuit. These advantages make this impedance network suitable for a variety of applications. However, similar to other n-TCIB converters, it suffers from low voltage gain which this issue can limit its use in high gain applications. Therefore, in recent years, different structures have been proposed in order to increase its voltage gain while keeping the main features of it unchanged. Basic QZS DC-DC converter structure is shown in Fig. 1.

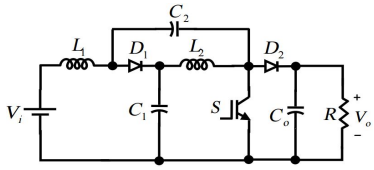

Fig. 1. Quasi-Z source DC-DC converter [16]

High-frequency transformer has been used in [17] and [18], and coupled inductors have been used in [19] and [20], in order to increase the voltage gain of QZS impedance network. But the fact is that using transformers or coupled inductors results in some disadvantages which are listed below:

1- Peak of voltage/current stress on diodes and switches will be increased. 2- Even a small value of a DC voltage will cause the magnetic core to be saturated. This will disrupt the operation of the converter. 3- Saturation of magnetic core will result in a drastic decrease in the inductance value of transformer or coupled inductors, which this will cause a severe stress on the switch. 4- Higher weight, higher volume, higher power loss, and lower efficiency of the converter.

Considering the above-mentioned drawbacks, using transformer or coupled inductors is not a proper method to improve the voltage gain of QZS network.

Another method which has been presented in [21]-[24] is cascading several modules of QZS network to increase the total voltage gain. But, in this method, the number of components is notably increased. This results in high power loss, low efficiency, high possibility of failure, and low

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reliability of the whole system. Therefore, this method also cannot be counted as a suitable and optimized solution.

In [25], a two-stage and a general multi-stage structure for QZS converter have been proposed. This converter has improved the basic QZS converter by increasing its stages. The only advantage of this converter is that it can attain same voltage gains in lower duty cycles. However, this advantage is at the cost of extra elements.

In [26], switched capacitors have been added to the basic QZS converter. The voltage gain has been improved while the voltage stress on elements has been kept unchanged and the duty cycle of the switch hasn't been limited. But, the voltage gain improvement is not significant, and this converter also cannot reach high voltage gains in practice.

In [27], switched inductors have been used to improve the basic QZS converter. The voltage gain has been improved. However, the duty cycle has been limited. Voltage stress on the switch and diodes has also been increased. Considering the mentioned limitations, this topology doesn't have the ability to reach high voltage gains in practice.

In [28], a combined switched-inductors switched-capacitor method has been employed to improve the QZS converter. The voltage gain relationship has been improved. But, the drawbacks mentioned for [27] also exist for this converter.

In [29], a voltage-lift cell has been added to the QZS converter. This converter has better voltage gain compared to the before-mentioned structures. However, duty cycle limitation and increased voltage stress on diodes and switch still exist in this converter. Therefore, despite the voltage gain improvement, this converter also can't reach high voltage gains in practice, considering the mentioned limitations.

In this paper, a novel QZS DC-DC converter with high step-up capability is proposed. In addition to the QZS network, this converter uses switched-capacitors and an extra inductor in order to achieve high voltage gains. The proposed converter keeps the main advantages of the basic converter. Also, the voltage stress on the diodes and switch will be kept unchanged, and the duty cycle of the switch won't be limited, compared to the main QZS converter. In addition to theoretical improvement, the topology of the proposed converter, allows it to reach high voltage gains practically. Also, the proposed converter has a flexible structure, and extra stages can be added to achieve even higher voltage.

In section II, structure of the proposed converter and circuit operation principles will be presented and the related relationships will be obtained. In section III, a comprehensive comparison between the proposed converter and other structures will be provided. Designing calculations will be presented in section IV. Then, in section V, the simulation results in PSCAD/EMTDC will be presented. In section VI, experimental results will be provided to examine the practicality of the converter. Finally, section V will provide a conclusion.

II. The Proposed Converter

The structure of the proposed high step-up QZS DC-DC converter is shown in Fig. 2. In addition to the QZS network, this converter uses C_3, C_4, C_5, and C_6 as switched capacitors. The switching of the capacitors is done in offline mode using D_2, D_3, and D_4. The Inductor L_3 is also used as the switched inductor in order to increase the voltage boost capability. It should be mentioned that, in order to convert the proposed converter to an inverter, an H-bridge (including 4 switches and 4 diodes) should be connected in parallel with the output capacitor.

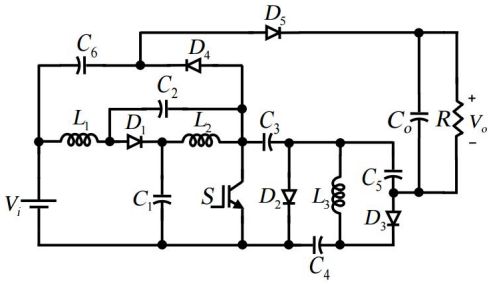

Fig. 2. Proposed high step-up quasi-Z source DC-DC converter

The proposed converter consists of three operation modes. Circuit operation explanations and necessary relationships will be provided. In the following relationships, D represents the duty cycle of the switch. It is obtained by dividing the on-time period of the switch by the total period as:

$$D = \frac{t_{on}}{T} = \frac{t_1 - t_0}{T} \tag{1}$$

It's obvious that if the on-time of the switch equals to DT, then, the off-time of the switch will be (1-D)T.

D'T represents the time range of second operation mode of the converter ($t_1 \le t < t_2$). D' is calculated as:

$$D' = \frac{t_2 - t_1}{T} \tag{2}$$

A. Mode I ($t_0 \le t < t_1$)

The equivalent circuit of the proposed converter in its first operation mode is shown in Fig. 3. This mode begins as the switch turns on. In this mode, L_1 and L_2 are charged by C_1 and C_2 through the path provided by the switch. Capacitor C_3 charges L_3, C_4, and the load. Also, considering the conduction of D_5, the energy of the load will be provided by the input voltage source, and C_3, C_5, and C_6. Therefore, the current passing through L_1, L_2 and L_3, and the voltage across C_4 increase and they get charged. While, the voltages across C_1, C_2, C_3, C_5 and C_6 decrease and they get discharged. This mode will end as the switch turns off.

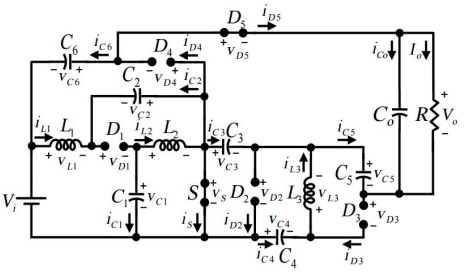

Fig. 3. Equivalent circuit of the proposed converter for mode I

Considering the on/off situations of the switching devices, by applying KVL to the main circuit, the following relationships can be written for the first operation mode:

$$v_{L1} = V_i + v_{C2} \tag{3}$$

$$v_{L1} = V_o + v_{C2} - v_{C3} - v_{C5} - v_{C6} \tag{4}$$

$$v_{L2} = v_{C1} \tag{5}$$

$$v_{L3} = v_{C3} - v_{C4} \tag{6}$$

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B. Mode II ($t_1 \le t < t_2$)

As the switch turns off, the 2nd mode of operation begins. In this mode, D_1, D_3 and D_4 are forward biased, while, D_2 and D_5 are reverse biased. The equivalent circuit of the converter in this mode can be achieved by applying the mentioned on/off states of the switch and diodes to Fig.3. In this mode, Inductors L_1 and L_2 charge the capacitors C_1, C_2, and C_3 and also charge C_6 through the path provided by D_4. The capacitor C_5 is also charged by L_3 and C_4. Therefore, the voltages across C_1, C_2, C_3, C_5 and C_6 increase and they get charged, while, the voltage across C_4 and the currents passing through L_1, L_2, and L_3 decrease and they get discharged.

Considering the on/off situations of the switching devices, by applying KVL to the main circuit, the following relationships can be written for the second operation mode:

$$v_{L1} = V_i - v_{C1} \quad (7)$$

$$v_{L1} = v_{C2} - v_{C6} \quad (8)$$

$$v_{L2} = v_{C1} - v_{C3} + v_{C4} - v_{C5} \quad (9)$$

$$v_{L2} = -v_{C2} \quad (10)$$

$$v_{L3} = -V_i + v_{C3} - v_{C4} - v_{C6} \quad (11)$$

C. Mode III ($t_2 \le t < T$)

As it was mentioned, in mode II, the voltage across C_4 decreases while the voltage across C_5 increases. As v_{c4} reaches v_{c5}, the voltage across D_2 gets positive, and therefore, D_2 gets forward biased and ready to conduct. As D_2 conducts, the 3rd operation mode begins. Therefore, in this mode, the switch is still off, D_1, D_3 and D_4 are forward biased, and D_2 and D_5 are reverse biased. The equivalent circuit of the converter in this mode can be achieved by applying the mentioned on/off states of the switch and diodes to Fig.3. In this mode, L_1 and L_2 charge C_3 and C_5 and also C_6 through the path provided by D_4. Meanwhile, considering the conduction of D_2, the capacitors C_4 and C_5 are connected in parallel and get charged through L_3. Therefore, the voltages across C_1, C_2, C_3, C_4, C_5 and C_6 decrease and they get discharged, while, the currents passing through L_1, L_2 and L_3 increase and they get charged.

Considering the on/off situations of the switching devices, by applying KVL to the main circuit, it is concluded that the relationships obtained for mode II (relationships (7) to (11)) are also valid for mode III. Also, the following relationship can be written for this mode:

$$v_{L3} = -v_{C4} \quad (12)$$

D. Theoretical waveforms

Before presenting the steady state analysis, the obtained theoretical waveforms will be presented in this sub-section. The waveforms of the proposed converter are shown in Fig. 4. They have been illustrated through the calculated voltage and current relationships of components in each of the operation modes. The waveforms, respectively from top to bottom, are related to gate pulse of the switch, currents of L_1, L_2 and L_3, and voltages of C_1, … , C_6.

E. Steady state analysis

By applying voltage balance law in a period for L_1 using (3) and (7), the following relationship is obtained:

$$V_i - (1-D)v_{C1} + Dv_{C2} = 0 \quad (13)$$

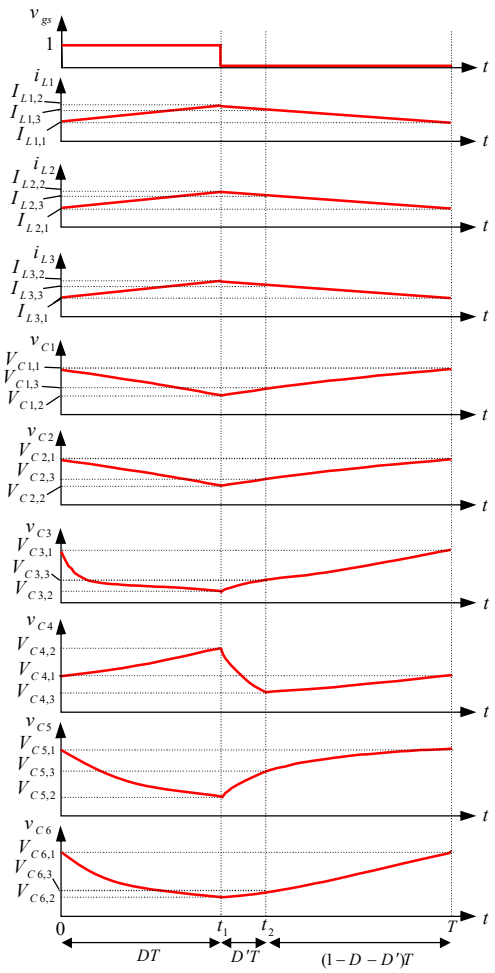

Fig. 4. Theoretical waveforms of the proposed converter

By applying voltage balance law for L_2 using (5) and (10), the following expression can be written as:

$$v_{C2} = \frac{D}{(1-D)} v_{C1} \quad (14)$$

By replacing v_{C2} from (14) into (13), V_{C1} and V_{C2} in the steady state are obtained as follows:

$$V_{C1} = \left(\frac{1-D}{1-2D}\right) V_i \quad (15)$$

$$V_{C2} = \left(\frac{D}{1-2D}\right) V_i \quad (16)$$

By applying voltage balance law for L_1 using (3) and (8), the following expression is obtained as:

$$D(V_i + v_{C2}) + (1-D)(v_{C2} - v_{C6}) = 0 \quad (17)$$

Replacing V_{C2} from (16) in (17), V_{C6} will be obtained as:

$$V_{C6} = \left(\frac{2D}{1-2D}\right) V_i \quad (18)$$

Applying voltage balance law for L_3 using (6) and (11), the following expression is obtained as:

$$D(v_{C3} - v_{C4}) + (1-D)(-V_i + v_{C3} - v_{C4} - v_{C6}) = 0 \quad (19)$$

By replacing V_{C6} from (18) into (19), (V_{C3}-V_{C4}) will be obtained as:

$$v_{C3} - v_{C4} = \left(\frac{1-D}{1-2D}\right) V_i \quad (20)$$

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Applying voltage balance law for L_2 using (5) and (9), the following expression is obtained as:

$$Dv_{C1}+(1-D)(v_{C1}-v_{C3}+v_{C4}-v_{C5})=0 \quad (21)$$

Applying V_{C1} and (V_{C3}-V_{C4}) using (15) and (20) into the above relationship, V_{C5} will be obtained as follows:

$$V_{C5}=\left(\frac{D}{1-2D}\right)V_i \quad (22)$$

Applying voltage balance law for L_3 using (6), (11) and (12), the following expression is obtained as:

$$-v_{C4}+(D+D')v_{C3}-D'(V_i+v_{C6})=0 \quad (23)$$

Applying the relationships (18) and (20) into the above relationships will give V_{C3} and V_{C4} as follows:

$$V_{C3}=\left(\frac{1}{1-2D}\right)V_i \quad (24)$$

$$V_{C4}=\left(\frac{D}{1-2D}\right)V_i \quad (25)$$

Applying voltage balance law for L_1 using (4) and (7), the following expression will be obtained as:

$$D(V_o+v_{C2}-v_{C3}-v_{C5}-v_{C6})+(1-D)(V_i-v_{C1})=0 \quad (26)$$

Finally, replacing V_{C1}, V_{C2}, V_{C3}, V_{C5} and V_{C6} from (15), (16), (24), (22) and (18) into the above expression, the voltage gain relationship will be obtained as:

$$G=\frac{V_o}{V_i}=\frac{2+D}{1-2D} \quad (27)$$

By applying KVL to the main circuit (shown in Fig. 2), and using the above-calculated voltage relationships of capacitors in steady-state, the voltage stress on the switch and diodes can be calculated. The following relationships show the voltage stresses on the diodes (anode to cathode) and switch (drain to source) in the steady state:

$$v_S=\left(\frac{1}{1-2D}\right)V_i \quad (28)$$

$$v_{D1}=v_{D2}=v_{D3}=v_{D4}=v_{D5}=v_{D6}=-\left(\frac{1}{1-2D}\right)V_i \quad (29)$$

III. Comparison

In order to give a comprehensive comparison between the proposed and other QZS network based converters, Table I is provided. In this table, circuit structures, voltage gain relationships, maximum duty cycles of the switches, and voltage stresses on diodes and switches are presented.

In comparison for voltage gain relationships, it can be seen that the proposed converter can reach higher voltage gains compared to other structures. Also, no limitation is created for the duty cycle of the switch compared to the basic converter. Therefore, the duty cycle can be adjusted up to the maximum value of %50. In order to give a graphical comparison about the voltage gains of the converters, Fig. 5 is illustrated. The slope of the curves should also be noticed. The curves related to converters presented in [25]-[29] have steep slopes near D_{max}. It means that, although these converters can reach high voltage gains in theory, reaching such high voltage gains in practice is impossible for them. But, as it can be seen in the figure, the curve related to the proposed converter has a mild slope, and it can generate higher voltage gains than other structures, with a safe distance from D_{max} margin. To give a numerical example, as it can be seen in Fig. 5, for reaching the voltage gain of 16, the curve related to the proposed converter the voltage gain of 16 with the duty cycle of 0.425 with a mild slope, while, the curves related to other converters reach their saturation zone with steep slopes for the voltage gain of 16.

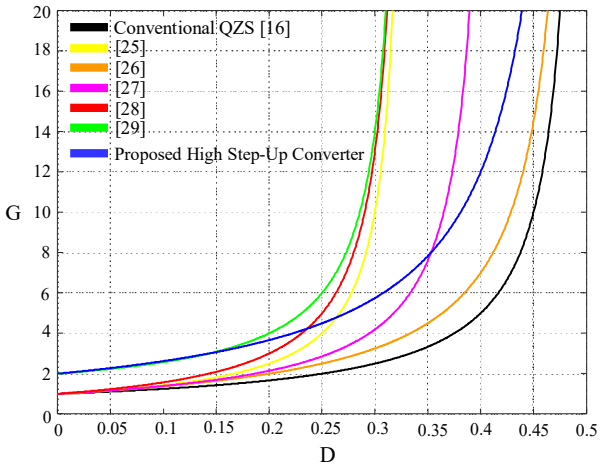

Fig. 5. Voltage gain comparison between the proposed and other QZS based DC-DC converters

Back to Table I, in comparison for voltage stress on devices, despite the improvements in voltage gain relationships for the converters presented in [25], [27], [28] and [29], the voltage stresses on the switches are increased, and they're equal to the output voltage.

Another issue is the voltage stresses on the diodes. Voltage stresses of all diodes in [25] and [28] and D_1 in [27] are equal to the output voltage. Also, voltage stress of D_1 in [29] is more than the output voltage. In another meaning, despite the voltage gain improvement in these converters, the voltage stresses on diodes and switches are significantly increased. These high voltage stresses will increase the defection possibility of these elements which leads to low reliability of the whole system. Also in high gain application, these converters need switches and diodes with high power rates (several times bigger than the nominal power rate of the load). It leads to higher cost, higher power loss and lower efficiency of the converters. These issues also can limit the voltage gains of converters in practical uses. But, as it can be seen, the proposed converter has kept the voltage stress on diodes and switch unchanged, compared to the basic structure. Comparing the proposed and other QZS based converters, improving the voltage gain while not changing the duty cycle limitation and voltage stress on the switch and diodes can be counted as the main advantages of the proposed converter.

The proposed converter also has the capability of reaching higher voltage gains through adding extra stages. The stages can be increased by repeating the part including C_3, C_4, D_2, and L_3. Relationships for 2-stage, 3-stage and K-stage structures in steady state are provided in Table II, which include the relationships for voltage gain and voltage stress on diodes and switches. As it can be seen in the table, higher voltage gains will be available in multi-stage structures. The interesting feature which should be noted is that the duty cycle of the switch is not limited, and, the voltage stress on diodes and switches are unchanged in all of the multi-stage structures.

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TABLE I.
COMPARISON BETWEEN THE PROPOSED AND OTHER QZS BASED DC-DC CONVERTERS

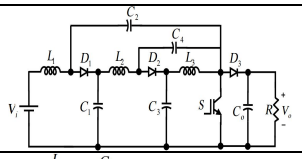
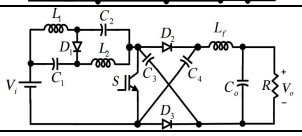
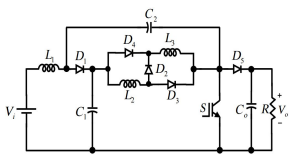
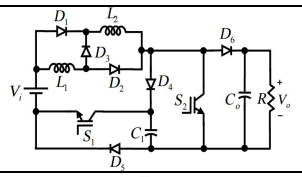
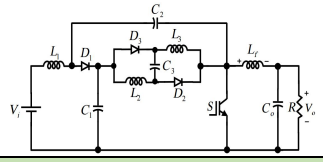
Refs.	Structures	Components	Voltage gain	D_{max}	Voltage stress on diodes and switches	Main features and drawbacks
[16]	Fig. 1	2 Diodes 1 Switch 2 Inductors 3 Capacitors	$G=\frac{1}{1-2D}$	0.5	$V_{D1,D2}=-V_S=\frac{-1}{1-2D}V_i$	Basic Conventional Quasi-Z source DC-DC Converter
[25]		3 Diodes 1 Switch 3 Inductors 5 Capacitors	$G=\frac{1}{1-3D}$	0.33	$V_{D1,D2,D3}=-V_S=\frac{-1}{1-3D}V_i$	✓Improved voltage gain ✓Capability of adding extra stages to the converter for reaching higher voltage gains ×Not a significant voltage gain improvement ×The duty cycle is limited ×Still can't reach high voltage gains
[26]		3 Diodes 1 Switch 3 Inductors 5 Capacitors	$G=\frac{1+D}{1-2D}$	0.5	$V_{D1}=-V_S=\frac{-1}{1-2D}V_i$ $V_{D2}=\frac{-D}{1-2D}V_i$	✓Improved voltage gain ✓Unchanged voltage stress on devices ×Not a significant voltage gain improvement ×Still can't reach high voltage gains
[27]		5 Diodes 1 Switch 3 Inductors 3 Capacitors	$G=\frac{1+D}{1-2D-D^2}$	0.41	$V_{D1,D5}=-V_S=-\left(\frac{1+D}{1-2D-D^2}\right)V_i$ $V_{D2}=-\left(\frac{1-D}{1-2D-D^2}\right)V_i$ $V_{D3,D4}=-\left(\frac{D}{1-2D-D^2}\right)V_i$	✓Improved voltage gain ×The duty cycle is limited ×Increased voltage stress on devices ×Still can't reach high voltage gains
[28]		6 Diodes 2 Switches 2 Inductors 2 Capacitors	$G=\frac{1+D}{1-3D}$	0.33	$V_{D1,D2}=\frac{-2D}{1-3D}V_i$ $V_{D3}=-2\left(\frac{1-D}{1-3D}\right)$ $V_{D4,D5,D6}=-V_{S1,S2}=-\left(\frac{1+D}{1-3D}\right)V_i$	✓Improved voltage gain ×The duty cycle is limited ×Increased voltage stress on devices ×Extra switch ×Still can't reach high voltage gains
[29]		3 Diodes 1 Switch 4 Inductors 4 Capacitors	$G=\frac{2(1-D)}{1-3D}$	0.33	$V_{D1}=-\frac{2}{1-3D}V_i$ $V_{D2,D3}=-\frac{1-D}{1-3D}V_i$ $V_S=\frac{2(1-D)}{1-3D}V_i$	✓Improved voltage gain ×The duty cycle is limited ×Increased voltage stress on devices ×Still can't reach high voltage gains
Proposed	Fig. 2	5 Diodes 1 Switch 3 Inductors 7 Capacitors	$G=\frac{2+D}{1-2D}$	0.5	$V_{D1,D2,D3,D4,D5}=\frac{-1}{1-2D}V_i$ $V_S=\frac{1}{1-2D}V_i$	✓High step-up capability ✓Capability of adding extra stages for reaching higher voltage gains ✓Unchanged voltage stress on devices × Lack of common ground between the input and output of the converter × Initial inrush current for D5 (for a few μS)

TABLE II
RELATIONSHIPS FOR 2,3 AND K-STAGE STRUCTURES

Number of stages	Voltage gain (G)	D_{max}	Voltage stress on devices
2	$G=\frac{2+2D}{1-2D}$	0.5	$v_{D1}=\ldots=v_{D6}=-v_S=\left(\frac{-1}{1-2D}\right)V_i$
3	$G=\frac{2+3D}{1-2D}$	0.5	$v_{D1}=\ldots=v_{D7}=-v_S=\left(\frac{-1}{1-2D}\right)V_i$
K	$G=\frac{2+KD}{1-2D}$	0.5	$v_{D1}=\ldots=v_{Dn+2}=-v_S=\left(\frac{-1}{1-2D}\right)V_i$

After mentioning the advantages of the proposed converter, it should be mentioned that a disadvantage of it compared to the other structures, is lack of common ground between the input and output. This issue should be considered if common ground between the input and output was necessary. Another issue is that considering the connection between C_6 and the input source, an initial inrush current will exist for diode D_5. However, due to the simulations done for the converter, this initial inrush current only lasts about a few micro seconds and it isn't long enough to make any damage to the diode. Also, in the experimental tests and without any soft-starting circuit for D_5, no problems were observed.

IV. PARAMETERS DESIGN

A. Inductors L_1, L_2 and L_3

Generally, the following relationship is valid for an inductor on a switching period:

$$L=\frac{V_L.D}{f_s\Delta I_L} \tag{30}$$

Replacing V_{C1}, V_{C2}, V_{C3}, and V_{C4}, from (15), (16), (24) and (25) into (3), (5) and (6), respectively, gives the following relationships for V_{L1}, V_{L2}, and V_{L3} in the switching period $(0\le t<DT)$:

$$V_{L1}=V_{L2}=\left(\frac{1-D}{1-2D}\right)V_i \tag{31}$$

$$V_{L3}=\left(\frac{1-D}{1-2D}\right)V_i \tag{32}$$

Applying V_{L1}, V_{L2} and V_{L3} from the above relationships into (30) gives the following relationship for L_1, L_2, and L_3 as:

$$L_1=L_2=\left(\frac{1-D}{1-2D}\right)\frac{DV_i}{\Delta I_L f_s} \tag{33}$$

$$L_3=\left(\frac{1-D}{1-2D}\right)\frac{DV_i}{\Delta I_L f_s} \tag{34}$$

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ΔI_L represents the ripple of the current passing through the inductor. The average current passing through inductors L_1 and L_2 is equal to the input current, while for L_3, it is equal to the output current. Therefore, considering the current ripple as %10 of the input current for L_1 and L_2, and %50 of the output current for L_3, the following relationships are obtained as:

$$L_1 = L_2 = \left(\frac{1-D}{1-2D}\right)\frac{DV_i^{\,2}}{(0.1)P_i f_s} \tag{35}$$

$$L_3 = \left[\frac{D(1-D)(2+D)}{(1-2D)^2}\right]\frac{V_i^{\,2}}{(0.5)P_i f_s} \tag{36}$$

B. Capacitors C_1, C_2, C_3, C_4, C_5, C_6 and C_o

Generally, the following relationship is valid for a capacitor on a switching period:

$$C = \frac{D.I_C}{f_s \Delta V_C} \tag{37}$$

ΔV_C is the voltage ripple of the capacitor which in the calculations, it is considered as %2 of the voltage across capacitors. The voltages across capacitors C_1, C_2, C_3, C_4, C_5, and C_6 are given in relations (15), (16), (24), (25), (22) and (18), respectively, and, the voltage across C_o is equal to V_o.

Considering the average current passing through each of capacitors in a switching period ($0 \le t < DT$), the following relationships are obtained for capacitors C_1, … , C_6 and C_o:

$$C_1 = \left[\frac{D(1-2D)}{1-D}\right]\frac{P_n}{(0.02)V_i^{\,2} f_s} \tag{38}$$

$$C_2 = (1-2D)\frac{P_n}{(0.02)V_i^{\,2} f_s} \tag{39}$$

$$C_3 = \left[\frac{D(1-2D)^2}{2+D}\right]\frac{P_n}{(0.02)V_i^{\,2} f_s} \tag{40}$$

$$C_4 = C_5 = C_6 = \left[\frac{(1-2D)^2}{2+D}\right]\frac{P_n}{(0.02)V_i^{\,2} f_s} \tag{41}$$

$$C_o = (1-D)\left(\frac{1-2D}{2+D}\right)^2 \frac{P_n}{(0.01)V_i^{\,2} f_s} \tag{42}$$

V. Simulation Results

In order to investigate the MPPT capability of the proposed converter, simulations are done in PSCAD/EMTDC. In the simulation, a photovoltaic panel is connected to the converter. The parameters used in the simulation are shown in Table III. T_r, T, $V_{oc,r}$, $I_{SC,r}$, G_r, G, N, and R_S are related to the PV panel and they respectively represent reference temperature, ambient temperature, open circuit voltage of PV, short circuit current of PV, reference sun radiation, solar radiation on the PV panel surface, number of serried PV cells, and series resistance of the PV panel. A PI controller is used for controlling the duty cycle of the switch in order to track the maximum power point. Fig. 6(a) shows the simulation result for output power versus output voltage of PV panel. As it can be seen, the P-V curve is being increased from zero, and, finally, it stopped by reaching the maximum power point. In Fig. 6(b), the duty cycle of the switch, output voltage and output power of PV panel, and the output voltage of converter are shown. As it can be seen, the duty cycle is constantly adjusted by PI controller. The output power of PV panel fluctuates around 150.128W which due to Fig. 6(a), it is the maximum power point. Also, the output voltage of the converter is 270V with an acceptable ripple. Therefore, considering the simulation results, MPPT capability of the proposed converter is confirmed.

TABLE III.
PARAMETERS USED IN THE SIMULATIONS

L_1,L_2,L_3	C_1, C_2	C_3,…,C_6,C_o	f_S	R_L	r_{diodes}
3 mH	330 µF	100 µF	40 kHz	500 Ω	0.03 Ω
$r_{Inductors}$	$r_{Capacitors}$	r_{Switch}	T_r (°K)	T (°K)	G_r (W/m²)
0.1 Ω	0.003 Ω	0.05 Ω	298	293	1000
G (W/m²)	$V_{OC,r}$	$I_{SC,r}$	N	R_S	
800	180 V	5 A	360	36 Ω	

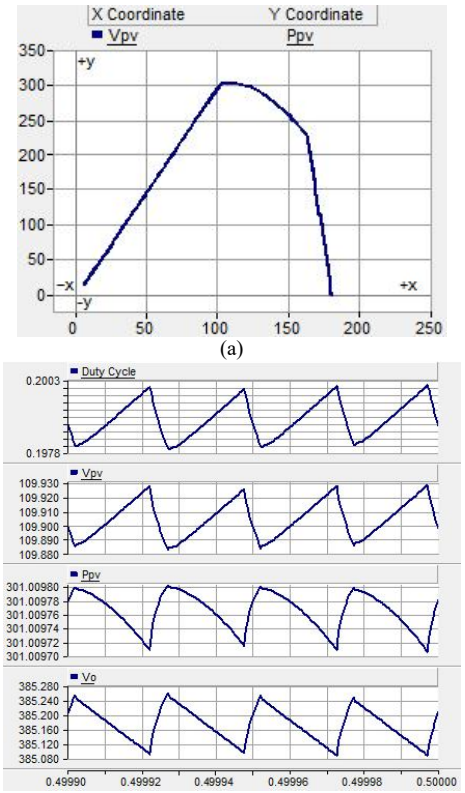

Fig. 6. Simulation results (a) Power versus voltage diagram of the PV panel (b) waveforms including duty cycle, V_{PV}, P_{PV} and V_o.

VI. Experimental Results

In order to prove the feasibility of the proposed high step-up DC-DC converter, a 150W prototype has been synthesized in the laboratory. The specifications of the prototype are listed in Table IV.

The switching pulse applied to the gate of the switch is shown in Fig. 7(a). The duty cycle is considered as 0.43.

Experimental results of the output voltage are shown in Fig. 7(b). As it can be seen, the output voltage has the value of 365V, which means that the prototype has successfully generated the voltage gain of 15.2. It is worth mentioning that, considering the duty cycle of 0.43, the expected theoretical voltage gain obtained from relation (27) is 17.35. The difference between the theoretical and practical voltage gains is normal, and it is because of the internal resistance of the components. In order to give a better comparison between theoretical and practical voltage gains for different duty cycles, experiments are done in the laboratory and the results are summarized in Table V.

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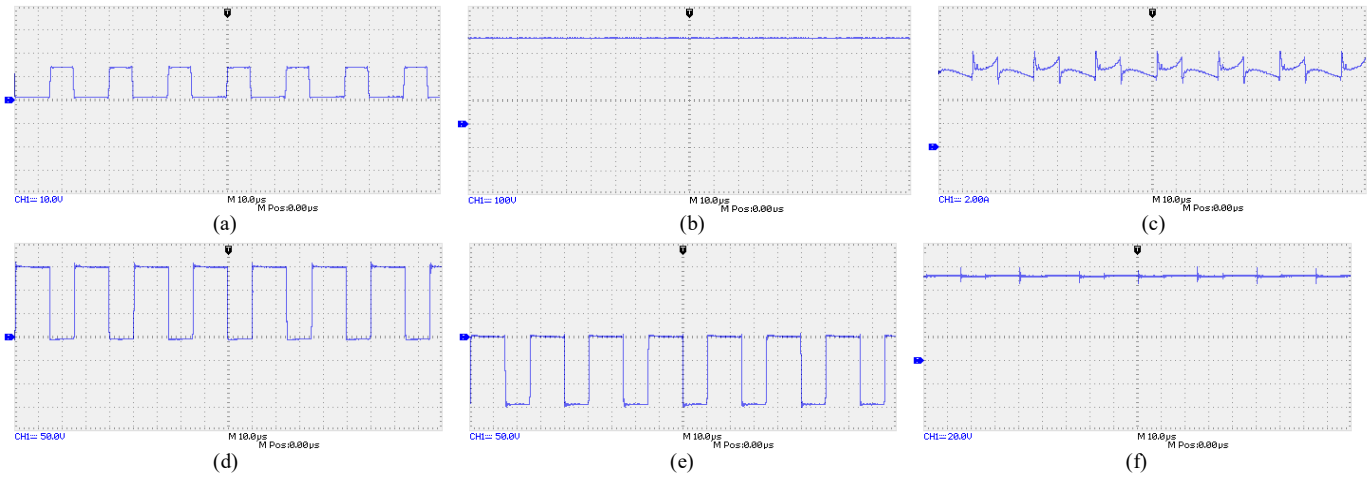

Fig. 7. Experimental results (a) Gate pulse of the switch (V_{GS}) (b) Output voltage (V_o) (c) Input current (I_i) (d) Voltage stress of the switch (V_{DS}) (e) Voltage stress of D_1 (V_{D1}) (f) Voltage across C_1 (V_{C1})

TABLE IV.
SPECIFICATIONS OF THE PROTOTYPE

V_i and V_o	f_S	C_1 and C_2	C_3,…,C_6 and C_o
24V and 365V	40 kHz	330 µF	100 µF
Duty Cycle	L_1 and L_2	L_3	R_L
%42	2 mH	2.8 mH	885 Ω
Microprocessor	MOSFET	Diode	Optocoupler
ATMEGA 32A	IRFP260N	MUR1560	TLP250

TABLE V.
THEORETICAL VERSUS PRACTICAL VOLTAGE GAINS

Duty cycle	0.2	0.25	0.3	0.35	0.4	0.42	0.44	0.46
G_{Theory}	3.66	4.5	5.75	7.83	12	15.125	20.33	30.75
$G_{Practical}$	3.54	4.31	5.48	7.44	11.03	13.56	17.22	24.81

The input current waveform is shown in Fig. 7(c). It is continuous, as it was expected. The waveforms of voltage stress on the switch (drain to source) and diode D_1 are shown in Fig. 7(d) and (e), respectively. Voltage stress peaks of other diodes are similar to diode D_1. As it can be seen in the waveforms, the voltage stresses have the peak of 150V. Therefore, this proves that the proposed converter has highly improved the voltage gain of the basic converter without changing the voltage stress on the switch and diodes.

The results for the voltage across the capacitor C_1 is also shown in Fig. 7(f).

In order to investigate the efficiency of the proposed converter, the experiments were done at four different power levels as 50W, 100W, 150W, and 200W. The experiments were done for different duty cycles from 0.2 to 0.48. The input voltage for all the experiments was considered as 24V. Also, a variable resistance was used in the output to adjust the output power to the desired value in all situations. The input and output voltages and currents were measured in each scenario using the oscilloscope, to calculate the efficiency. The efficiency results are shown in Fig. 8. As it can be seen, the converter has its best efficiency response for the duty cycles between 0.3 to 0.46. For very low and very high duty cycles, the power loss increases and the efficiency of the converter decreases which this issue is rational and inevitable for all step-up DC-DC converters. As it can be seen in Fig. 8, the proposed converter has a desirable efficiency. Experimental efficiency analysis is also done for the conventional and proposed QZS converters. Considering that the conventional converter couldn't reach voltage gains higher than 6, the comparison is done for voltage gains between 2 and 6. The obtained results are shown in Table. VI. As it can be seen in the table, as the voltage gain increases, the efficiency of the conventional converter decreases, while, the efficiency of the proposed converter increases. That is because increasing the voltage gain causes the conventional converter to reach its saturation zone soon, and the parasitic power losses will decrease the efficiency. It is worth mentioning that, as it can be seen in Fig. 8, the efficiency of the proposed converter will also decrease by reaching the saturation zone. Anyway, for this range of voltage gains, the proposed converter has better efficiency in higher gains.

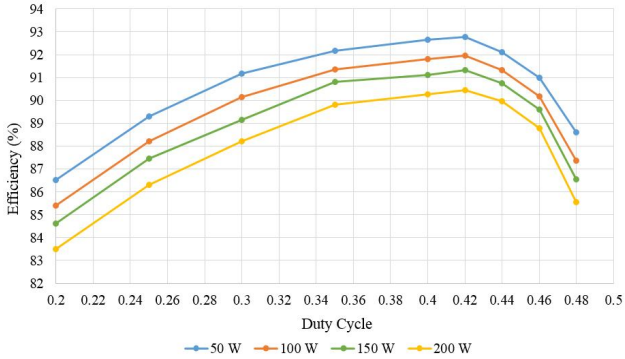

Fig. 8. Experimental efficiency analysis results of the proposed converter

TABLE VI.
EFFICIENCY OF THE PROPOSED AND CONVENTIONAL CONVERTERS

Voltage Gain	2	3	4	5	6
%Eff. (conventional)	94.9	92.3	89.6	86.6	83.2
%Eff. (proposed)	83.3	84.1	87.3	88.4	90.1

VII. CONCLUSION

An improved QZS based DC-DC converter with high step-up capability was proposed. In addition to the QZS network, the proposed converter has used a combined method of switching-capacitors and switching-inductor. It could resolve the voltage gain limitation of the basic converter while keeping its main advantages such as continuous input current and low voltage stress on capacitors. The maximum duty cycle and voltage stress on the switch and diodes are remained unchanged. Therefore, they will not affect the voltage gain of the converter in practice. Extra stages can also be added to the converter to achieve even higher voltage gains. It was seen

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that the voltage stress on diodes and switch stays unchanged after increasing the stages.

Circuit operation principles, analysis, and necessary relationships were presented. A comparison between the proposed and other QZS based converters was also provided. Considering the results, the superiority of the proposed converter to other structures was confirmed.

The simulations were done in PSCAD/EMTDC using a photovoltaic panel input. The results have confirmed the MPPT capability of the converter.

A 150W prototype of the proposed converter was also synthesized in the laboratory. The experimental results have confirmed the theoretical analysis, and, the practicality of the converter and its proper efficiency have been assured.

Considering the approved advantages of the converter such as continuous input current, high voltage gain, low voltage stress on elements, and MPPT capability, it could be a suitable choice in a variety of industrial applications such as photovoltaic systems, fuel cells, PMSG based wind turbines, and, power systems based on battery banks and super capacitors. Also, in applications such as uninterruptable power supply (UPS), and LED lamps, low and varying voltage of the battery and fuel cell should be converted to the standard DC bus voltage (380-400V), which the proposed converter can be a suitable choice for them. The point which also should be mentioned is that, considering the non-isolated structure of the proposed converter, in applications which an isolation between the input and output side is required, an isolating transformer could be used in series with the converter.

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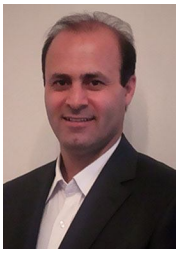

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