Two-switch High Gain Boost Converter

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***Abstract*- A two-switch based high gain boost converter (TSHBC) exhibiting improved voltage gain is proposed in this paper. Its operating duty ratio range is 0 to 0.5 and is able to establish high-voltage transformation ratio. To achieve this, two charge-pump capacitors along with an inductance is utilized in the topological development. A capacitor is also connected across the load to suppress the ripples and thus the converter forms a fourth-order system. Principle of operation is explained for the continuous inductor current mode of operation. Steady-state analysis is performed and the converter elements design equations are formulated. Later on state-space models are formulated to quantify the TSHBC dynamic behavior and then to design suitable controller. In addition, a brief tabular form of features of the proposed converter and other dual-switch based converters is brought out for ready reference. A 15 V to 48/60 V, 40 W prototype TSHBC is constructed for experimental verification. Measurement results are supported with simulation results to demonstrate the proposed high gain boost converter salient features.**

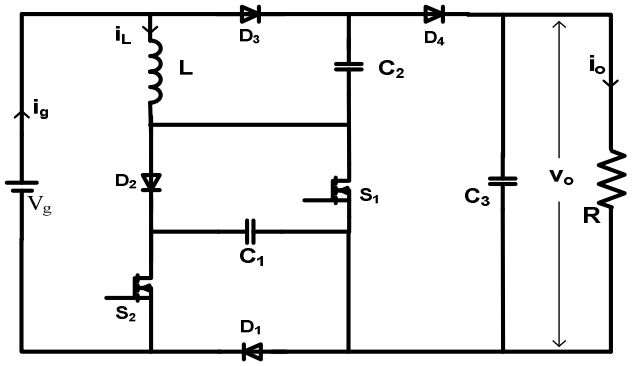
Keywords- High gain DC-DC converter, Boost converter, Charge-pump cell, Switching inductor cell. Z-source DC-DC converter.

I. INTRODUCTION

For the past many years energy requirement is increasing with fast rate and there is a huge impact of energy. So, there is a need to switch towards the clean energy sources. Due to this the clean energy resources such as fuel cell, wind and solar photovoltaics have gained popularity in the recent years. The photovoltaic sources are intermittent and can produce low dc voltage which depends on the size of the panel. Here, it is necessary to design suitable dc-dc conversion topologies which are boosting this low dc voltage so that it can be used at the supply side of inverters and such topologies are popularly known as Z-source boost topologies. They primarily produce high voltage gain at low duty ratios. Also, their design should be cost effective and have high efficiency. The traditional boost converter (TBC) will operate for duty ratio's in the range (0 to 1) and the ideal voltage gain is very high at duty ratio close to 1.0. However, voltage drop due to parasitic resistance of inductor and capacitor limits the voltage gain.

A family of dc-c conversion topologies exhibiting high gain and containing (1-2D) in the denominator were evolved [1]. The basis for these topological evolution is that the Z-network or its restructured configuration. It also used two switches. The Z-network is inserted in between switching devices and the power source so that it exhibits high voltage gain. Other configurations gives high voltage gain but it can be either positive output or negative output voltage. In these topologies, the duty ratio range is same as the conventional boost converters, i.e. range is (0 to 1). The Z-source based DC-DC converters exhibits high voltage gain at low duty ratios as their voltage transformation ratio's denominator terms involve (1-2D), (1-3D), (1-4D), etc,. These voltage gains are realized in the literature by using the Z-network along with switched-inductor, switched capacitor and their hybrid combinations.

Realizing a higher gain is possible by reducing the denominator term which is possible by restricting the duty ratio range. In this direction many topologies were reported in literature [1]-[8]. Many of these evolutions are based on single-switch but the number of L-C component are more. Some of them also used multiple switches but with less passive components. Amongst these, the high gain topologies essentially used more number of L-C components to boost-up the voltage through multiple-stages. Although such solutions provide better gains but their feasibility is determined by the key factors like efficiency, ripple content and controllability. From control point of view, the single switch topologies enforce limitations. Multiple-switch based topologies give more degree of freedom in terms of controllability as well as in restructuring of the L-C elements such that better voltage gain tuning is possible while realizing ripple requirements. This paper proposes a two-switch high gain boost converter (TSHBC). The proposed dual-switch converter uses two charge-pump capacitor cells for improving boosting factor.



(a)

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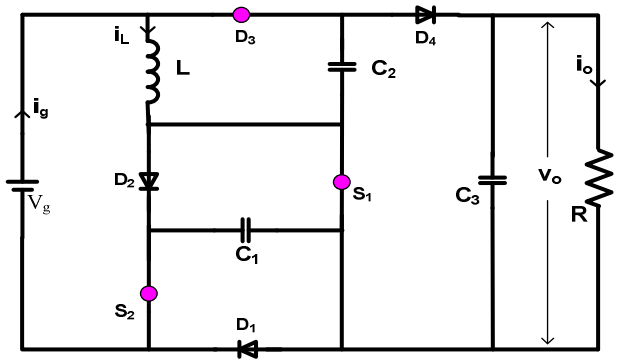

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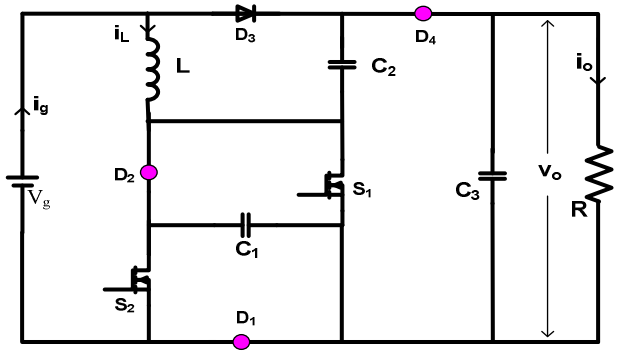


(c)

Fig.1. (a) Proposed Converter (b) Equivalent circuit of Mode-1, (c) Equivalent circuit of Mode-2.

II. Proposed Converter And Its Modelling

The two-switch high boost converter (TSHBC) circuit diagram along with all possible modes are shown in Fig. 1. The converter introduced in this paper consists of two switches (S_1, S_2), one inductor (L), three capacitors (C_1, C_2, C_3), and four diodes (D_1, D_2, D_3, and D_4). It is assumed that the inductor currents is continuous i.e. the switching devices and some of the diodes operate in complementary operation leading two modes of operation in one switching cycle. The corresponding equivalent circuits are shown in Fig. 1. Table I shows the sequence of the conduction devices of the TSHBC converter. The steady-state analysis and state-space based linearized analysis is given below.

TABLE I. SEQUENCE OF DEVICES CONDUCTION

	S_1	S_2	D_1	D_2	D_3	D_4
Mode-1	ON	ON	OFF	OFF	ON	OFF
Mode-2	OFF	OFF	ON	ON	OFF	ON

A. Steady-State Analysis

Switch-ON period: Fig. 1b is the resulting circuit for two switches ON-state condition. This mode persists for duty ratio time duration DT_s. The notation used here is: voltage across capacitors are v_{C1}, v_{C2} and $v_{C3.}$ while the inductor current is i_L. Depending on the location of L-C elements their currents/voltage starts increasing/decreasing leading to establishing current/voltages in various branches of TSHBC. To begin with the Kirchhoff's voltage law (KVL) equations are given below.

$$v_L = v_{C2} \tag{1}$$

Diodes ON period: Fig. 1c is the resulting circuit when the diodes D_1, D_2 and D_4 are in ON-state while two switches and diode D_3 will be in OFF-state. In this mode, the current in inductance i_L is decreasing. For this equivalent circuit, the KVL expressions are given as:

$$v_L = (V_g + v_{c2} - v_o) \tag{2a}$$

$$v_o = (v_{c1} + v_{c2}) \tag{2b}$$

Now by applying volt-sec balance to the inductance L the voltage of the capacitor -C_2 is obtained as:

$$v_{c2} = (1-D)v_o - (1-D)V_g \tag{3}$$

From mode-1 circuit, the following relationship is obtained as:

$$V_g = (v_{c2} - v_{c1}) \tag{4}$$

Now using eqns. 1, 2, and 3 the equation relating the load voltage and capacitor C_2 voltage is obtained as:

$$v_o = \frac{(3-2D)}{(1-2D)} v_{c2} \tag{5}$$

Using equation (2b) and (4) the capacitor C_2 voltage is obtained as given below.

$$v_{c2} = \frac{(V_g + v_o)}{2} \tag{6}$$

Simplification of eqn. 5 together with eqn. 6 results in the voltage gain of the proposed TSHBC as given below.

$$\frac{v_o}{V_g} = \frac{(3-2D)}{(1-2D)} \tag{7}$$

The voltage gain variation of the proposed TSHBC and SC-SBC [9] is compared in Fig. 2. It is clear that the proposed topology gives high gain than the SC-SBC.

TABLE II. COMPONENT COUNT IN VARIOUS TOPOLOGIES

	Converter in [9]	Converter in [10] (SC-SBC)	Proposed TSHBC
Voltage Gain	$(3-2D)/(1-2D)$	$(2-2D)/(1-2D)$	$(3-2D)/(1-2D)$
Inductors	2	1	1
Capacitors	5	3	3
Switches	1	2	2
Diodes	4	4	4

B. Small-signal Analysis

For analyzing the characteristic features offered during dynamics the state-space modeling which is well established in linear control theory is used. In CCM, the designed topology shown above is having three modes of operation as discussed above. Here, the state-space averaging technique is

applied to the converter and the detailed models are described below.

$$[\dot{x}] = [A_k][x] + [B_k][u] \quad (8a)$$

$$[y] = [E_k][x] + [F_k][u] \quad (8b)$$

$$[x] = \begin{bmatrix} i_1 & i_2 & v_{c1} & v_{c2} & v_{c3} \end{bmatrix}, [u] = [V_g] \text{ and } [y] = [V_0].$$

$$[A] = \sum_{k=1,2} A_k D_k; [B] = \sum_{k=1,2} B_k D_k; [E] = \sum_{k=1,2} E_k D_k; [F] = \sum_{k=1,2} F_k D_k$$

where k = 1, 2 defines the circuit shown in Figs. 1b, 1c and 1d, respectively. The matrices [A], [B], [E] and [F] are defined as state matrix, input matrix, output matrix and feed forward matrix respectively. [x] is the state vector, [y] is the output vector and [u] is the forcing function vector. In state-space modeling the non-idealities of inductor and capacitor are also considered. Using the state-space model defined in equation (8), the output to input voltage and duty ratio-to-load voltage transfer function can easily be found from the equations listed in (9).

TABLE III. COMPARISON BASED ON STRESS ON COMPONENTS

	Ref [9] Converter	Ref Converter [10]	Proposed TSHBC
Voltage Gain	$(3-2D)/(1-2D)$	$(2-2D)/(1-2D)$	$(3-2D)/(1-2D)$
V_{C1}	$\left(\frac{(1-D)}{(3-2D)}\right)V_o$	$\frac{DV_g}{(1-2D)}$	$\left(\frac{1}{(3-2D)}\right)V_o$
V_{C2}	$\left(\frac{(1-D)}{(3-2D)}\right)V_o$	$\left(\frac{1-D}{1-2D}\right)V_g$	$\left(\frac{(2-2D)}{(3-2D)}\right)V_o$
V_{C3}	$\left(\frac{1}{(3-2D)}\right)V_o$	$\left(\frac{2-2D}{1-2D}\right)V_g$	V_o
V_S	$\left(\frac{1}{(3-2D)}\right)V_o$	$\frac{DV_g}{(1-2D)}$	$\left(\frac{1}{(3-2D)}\right)V_o$
V_D	$\left(\frac{1}{(3-2D)}\right)V_o$	$\frac{DV_g}{(1-2D)}$	$\left(\frac{1}{(3-2D)}\right)V_o$
Com. Ground	Yes	No	No

$$[A_1] = \begin{bmatrix} \frac{-k_2}{L} & \frac{k_1}{L} & \frac{k_3}{L} & 0 \\ \frac{-k_1}{C_1} & \frac{-k_1}{C_1 r_{c2}} & \frac{-k_1}{C_1 r_{c2}} & 0 \\ \frac{(k_1-1)}{C_2} & \frac{k_1}{C_2 r_{c2}} & \frac{-k_1}{C_2 r_{c2}} & 0 \\ 0 & 0 & 0 & \frac{b}{RC_3} \end{bmatrix};$$

$$[B_1] = \begin{bmatrix} \frac{k_1}{L_1} & \frac{k_1}{C_1 r_{c2}} & \frac{-k_1}{C_1 r_{c2}} & 0 \end{bmatrix} [E_1] = [0 \quad 0 \quad 0 \quad b]; [F_1] = [0]$$

$$[B_2] = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \end{bmatrix}; [E_2] = [p_9 \quad p_{10} \quad p_{10} \quad p_{11}]; [F_2] = [0]$$

$$[A_2] = \begin{bmatrix} \frac{-p_7}{L} & \frac{-p_8}{L} & \frac{r_{c1}p_5}{L} & \frac{-r_{c1}p_6}{L} \\ \frac{p_4}{C_1} & \frac{-p_5}{C_1} & \frac{-p_5}{C_1} & \frac{p_6}{C_1} \\ \frac{-p_2 r_{c1}}{C_2} & \frac{-p_2}{C_2 b} & \frac{-p_2}{C_2 b} & \frac{p_3}{C_2 b} \\ \frac{p_2 r_{c1}}{C_3} & \frac{p_2}{C_3} & \frac{p_2}{C_3} & \frac{-p_1 p_2}{C_3} \end{bmatrix};$$

$$G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \left[E(sI - A)^{-1} B + F \right] \quad (9a)$$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \left[E(sI - A)^{-1} T \right] \quad (9b)$$

where the different matrices for the proposed converter are given above.

TABLE IV. CONVERTER COMPONENT VOLTAGE EQUATIONS

	Mode-1	Mode-2
V_{C1}	$\left(\frac{V_g}{(1-2D)}\right)$	$\left(\frac{V_g}{(1-2D)}\right)$
V_{C2}	$\left(\frac{2(1-D)V_g}{(1-2D)}\right)$	$\left(\frac{2(1-D)V_g}{(1-2D)}\right)$
V_{C3}	$\left(\frac{(3-2D)V_g}{(1-2D)}\right)$	$\left(\frac{(3-2D)V_g}{(1-2D)}\right)$
V_L	$\left(\frac{2(1-D)V_g}{(1-2D)}\right)$	$\left(\frac{-2DV_g}{(1-2D)}\right)$

TABLE V
PARAMETERS AND SPECIFICATIONS OF TSHBC

Parameter	Value
V_g	15 V
V_0	48/60 V
C_1	47 µF
C_2	47 µF
C_3	100 µF
L	1.0 mH
f_s	50 kHz
R	150-60 Ω

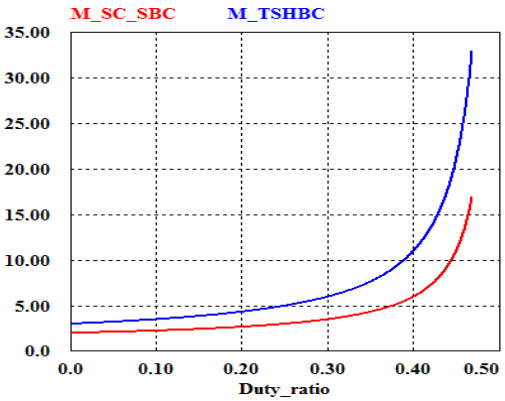


Fig. 2. Voltage gain variation with duty ratio.

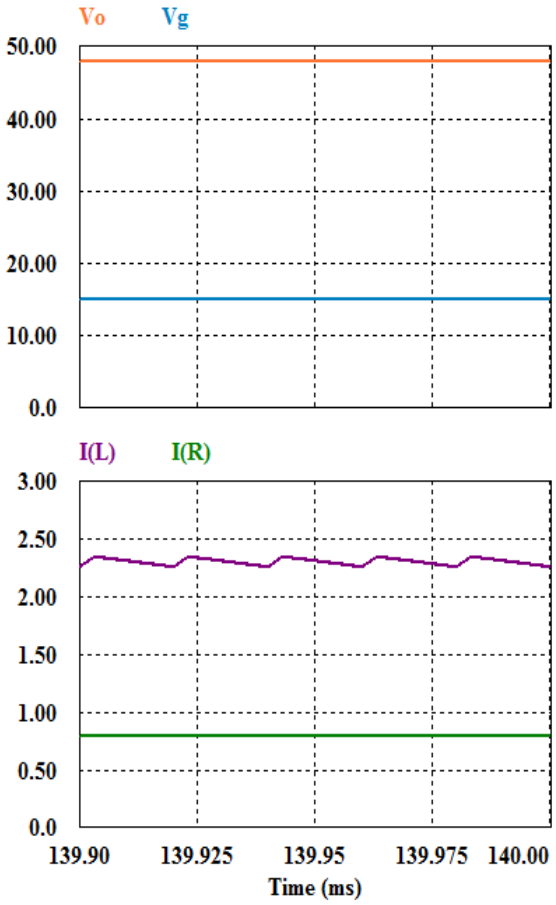


Fig. 3. Steady-state waveforms depicting load voltage, supply voltage and inductor current waveforms (simulation).

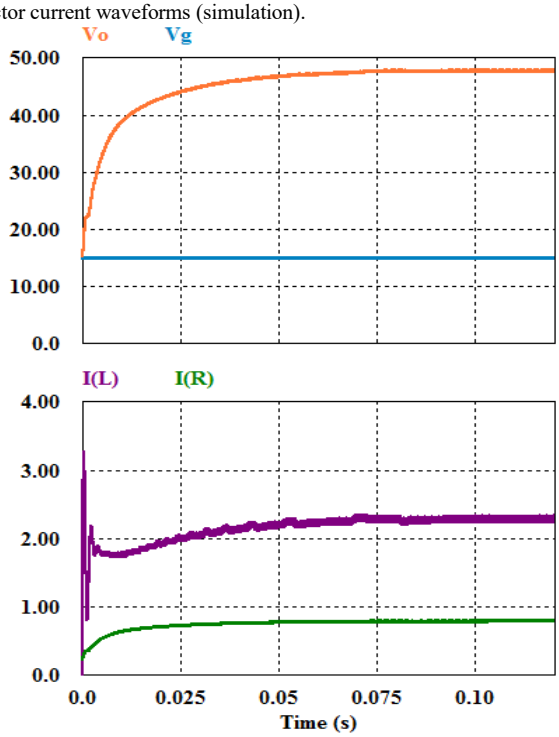


Fig. 4. Transient response of load voltage (Light load to full load, simulation).

III. L-C Component Design

The following equations are used to design the L-C elements of the TSHBC topology as discussed above. The voltage and current of each component can easily be obtained using Table IV and VI . Based on the design equations (10a)-(10d), the design parameters are computed as listed in Table V.

$$L > \left[2D(1-D)V_g\right] / \left[\Delta i_L f_s (1-2D)\right] \quad (10a)$$

$$C_1 > \left[D(3-2D)I_o\right] / \left[\Delta v_{C1} f_s (1-2D)\right] \quad (10b)$$

$$C_2 > \left[D(3-2D)I_o\right] / \left[\Delta v_{C2} f_s (1-2D)\right] \quad (10c)$$

$$C_3 > \left[V_o D\right] / \left[\Delta v_{C3} R f_s\right] \quad (10d)$$

IV. Results And Discussions

The state-space model for the proposed converter obtained in eqn. (8) can easily be used to obtain various transfer functions. It is a fourth-order system having four poles and four zeros. All the poles are in left half of s-plane. It shows that the proposed converter show no right-half-plane-poles at any frequency which indicates that stabilizing the converter is not a difficult task. Generally, the dc-dc converters which are evolved by ensuring energy conservation principles along with feasible power conversion will have no right half of s-plane poles. Further, there is a possibility that the transfer function may have right-half-plane zeros which will not be problematic from stability point of view but only limits the speed of response as it contribute time-delay within the system.

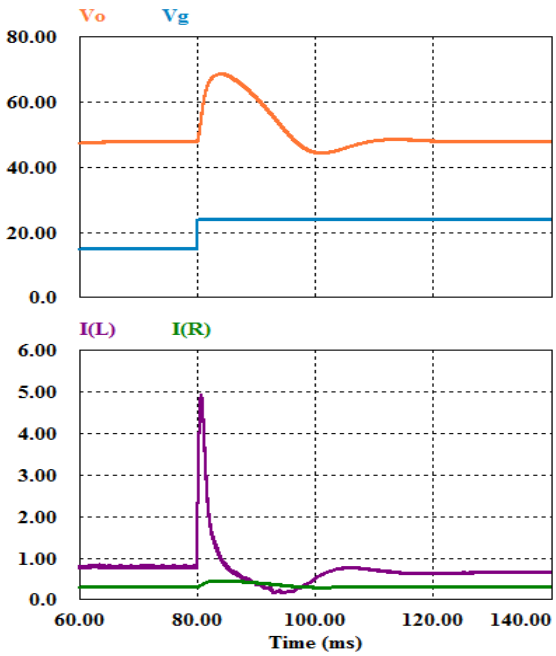


Fig. 5. Dynamic response of load voltage (V_g: 15 to 24 V, simulation).

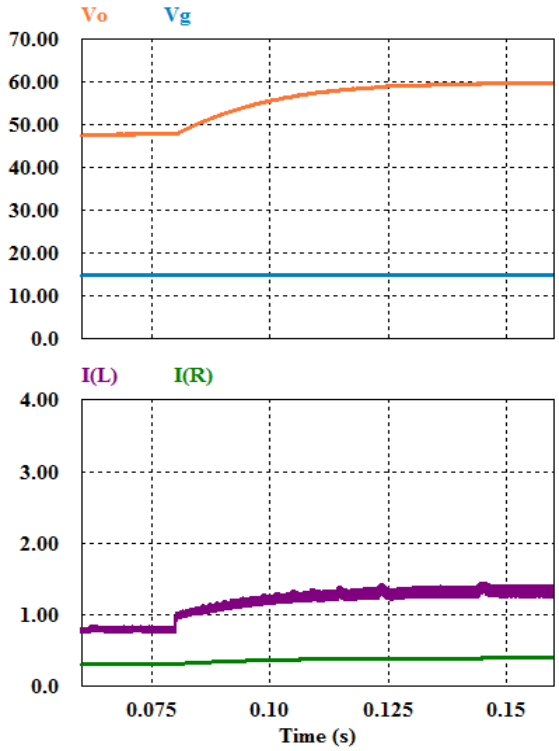


Fig. 6. Load voltage reference tracking(V_g: 15 V, V_o: 48 to 60 V).

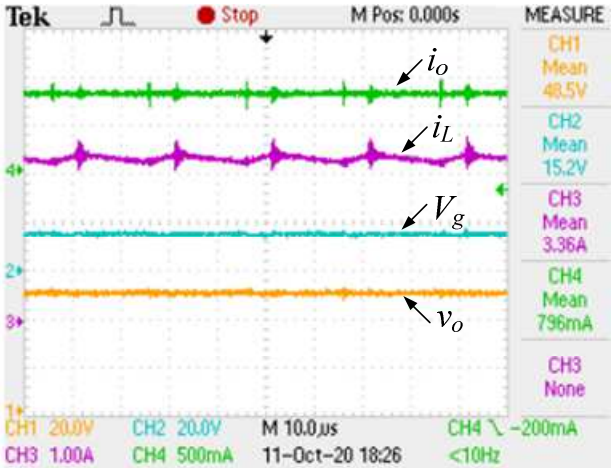
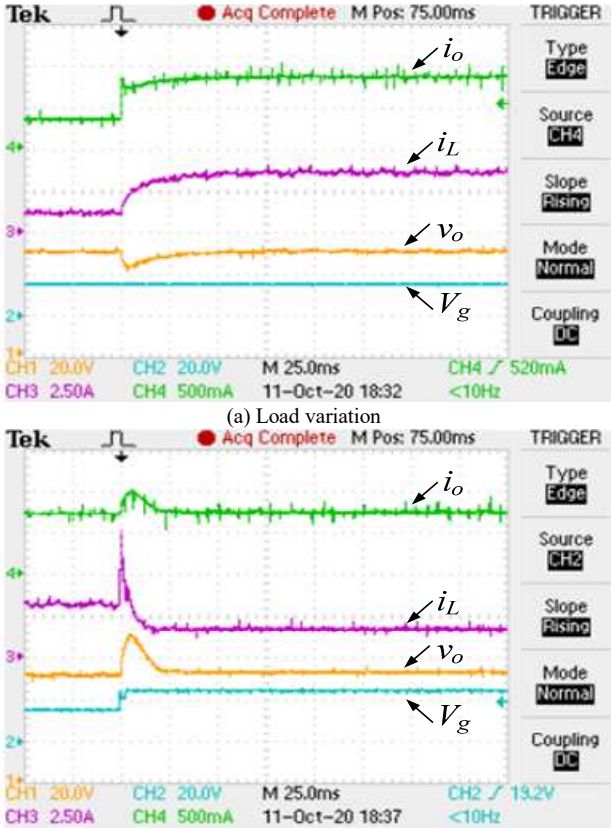


Fig. 7. Steady-state waveforms.

The mathematical analysis given in the preceding sections is useful to predetermine the proposed converter performance. The presence of an inductor on the input side helps in boosting as well as ensures the voltage gain is a function of duty ratio. Since the input source current is the summation of the inductor and capacitor current, the ripple content is slightly higher. However, the achievable voltage gain with less number of L-C elements is high. There are three capacitors (two intermediate and one on load side) in this proposed converter of which C_3 is connected across the load which essentially useful to maintain constant load voltage and hence its voltage stress is equal to load voltage. While the remaining two capacitors (C_1 and C_2) are located in between load and source and they will charge to voltages as listed in Table III. Since the proposed TSHBC is boosting type, both the capacitors (C_1 and C_2) voltage vary as function of duty ratio like in conventional boost converter. However, their magnitude is decided by the location within the converter. The capacitors voltage and device stress of the reported topologies and the proposed TSHBC is compared in Table III.



(a) Load variation

(b) V_g- variation

Fig. 8. Transient response of the proposed converter.

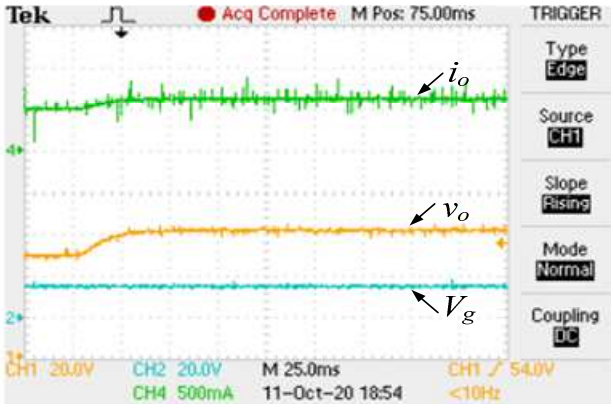


Fig. 9. Load voltage reference change.

The above given qualitative analysis is useful to understand the proposed converter operation. With this as basis an extensive simulation studies are carried out for better understanding the proposed converter operation. The simulation studies are done using the parameters presented in Table V. For both simulation and experimental studies the source voltage of 15 V is used to generate a load voltage of 48 V. The nominal load power is close to 35 W. In simulations, with 15 V as source voltage the load voltage of 48 V is obtained under steady-state conditions as shown in Fig. 3. Furthermore, the inductor L current is continuous and thus its ripple content is low. The switch duty ratio is close to 0.1. The proposed converter dynamic performance as well as closed-loop regulation capability is tested in simulation for two different cases described below. In the first case, the start-up response is measured and the load voltage is slowly established within 50 msec. Keeping constant load-R (R: 150 Ω) the source voltage is changed (V_g: 15 to 24 V) and the corresponding dynamic response is shown in Fig. 5. In the third case, the load on the converter kept constant (V_g: 15 V, R: 150 Ω) while the reference for the control-loop is changed from 48 to 60 V and the simulated dynamic response is shown in Fig. 6. Though the voltage across the load is tracking to new reference due to the presence of controlling action but its recovery is slow (tracking time about 30 msec).

The simulation results are now validated with experimental prototype measurements. Test conditions corresponding to the above simulation cases are set in the experimentation and measurements are captured with digital storage oscilloscope as shown in Figs. 7 to 9. The measured steady-state waveforms (Fig. 7) are almost identical with those obtained in simulation. The dynamic performance test results for load and supply voltage changes is given in Fig. 8 where it is seen that in either of these cases the voltage regulation ensured. The regulation time is decided by the converter as well as the controller used for closed-loop regulation. The converter capability for reference voltage changes and its tracking capability is tested experimentally and for illustration purpose one sample measurement is given in Fig. 9. The initial load voltage is 48 V and reference command change it is changed to 60 V in about 25 ms time.

V. Conclusion

A two-switch based enhanced voltage transformation ratio boosting topology was proposed in this paper. To achieve this, an inductor, two charge pump capacitors and four diodes were used. Detailed investigation of the TSHBC revealed that it gives high voltage gain together at very low duty ratios. The proposed converter operating principle was explained and its performance was analyzed for the CCM operation. Moreover, a brief comparison between the converter evolved in this paper and other dual-switch based topologies is brought out for ready reference. Simulations confirm the measurements results.

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