111- Days verification challenge

day ①: Topic :- flip flops & Latches

Skill : Digital electronics

1. Explain functioning of JK & SR-flipflop.

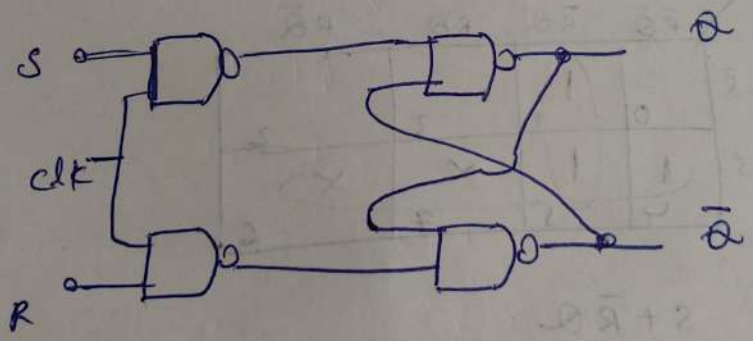
flipflop =→ Latch + clock

① Truth Table → i/p o/p

② characteristic Table → i/p ps Ns

③ Excitation Table → i/p | ps Ns ( )

SR flipflop :-



Truth Table :-

clock	S	R	Q_{n+1}	
0	x	x	Q_n	→ Memory state
1	0	0	Q_n	→ Hold state
1	0	1	0	→ reset state
1	1	0	1	→ set state
1	1	1	x	→ invalid.

2) Difference b/w FF & Latch.

Memory Elements

Latch	Flipflop
— latch : Logic gates → level triggered.	— mem ckt : stores 1 bit data → edge triggered
2 i/p : set, Reset	→ clock is present
2 o/p : Q, $\bar{Q}$	→ Latch + clock
→ o/p changes immediatly based on i/p	→ synchronous.
→ stores 1 bit data at a specified time	Appl: counters, registers, freq divider
→ No clock	eg:- SR, D JK, T FF.
→ Asynchronous operation.	
eg:- SR latch D latch.	

3) why latches are fasted than Flipflops.

→ Flipflops are sensitive to both the i/p signal and the clock signal.

→ Latches are sensitive to the i/p signal only when enabled.

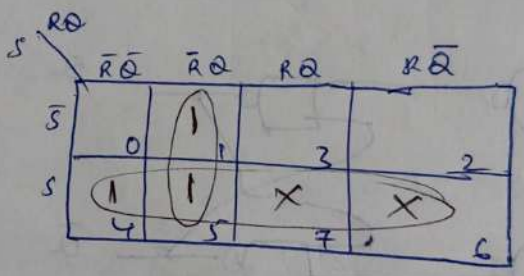
→ FF operates at slow speed

→ Latches operates at fastest speed

* Characteristic Table :-

S	R	Q_n	Q_{n+1}	
0	0	0	0	} Hold
0	0	1	1	
0	1	0	0	} Reset
0	1	1	0	
1	0	0	1	} Set
1	0	1	1	
1	1	0	X	} Invalid
1	1	1	X	

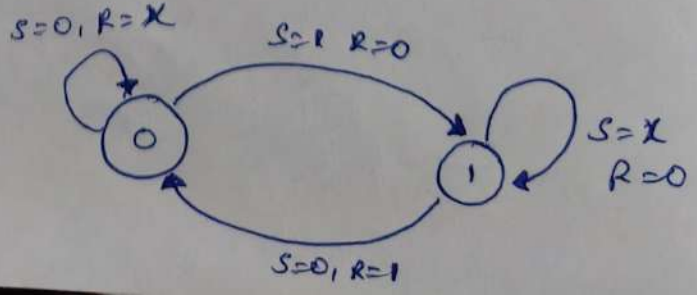
$$CE = \Sigma m(1,4,5) + \Sigma d(6,7)$$



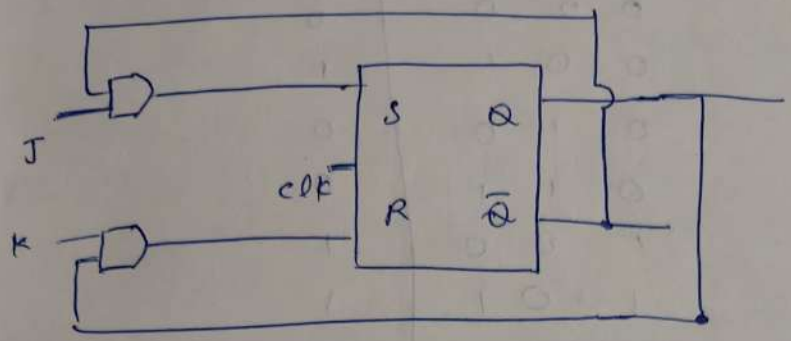
$$= S + \bar{R}Q$$

* Excitation Table :-

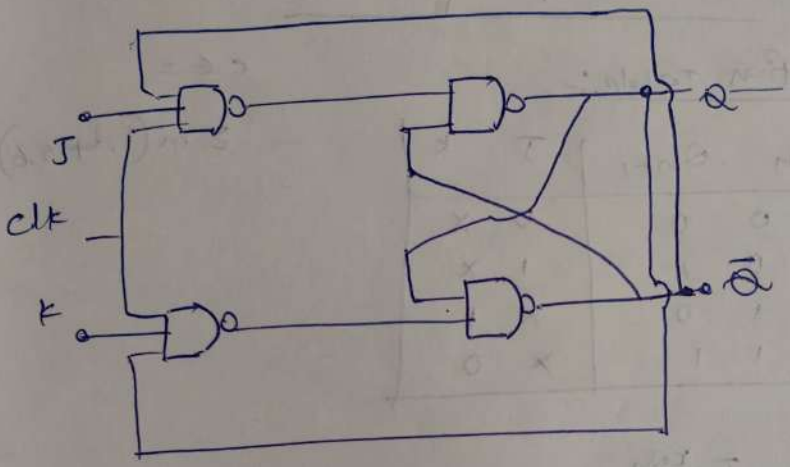
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



JK Flipflop :-



(or)



Truth Table

J	K	Q_{n+1}	
0	0	Q_n	→ Hold
0	1	0	→ Rest
1	0	1	→ set
1	1	$\bar{Q}_n$	→ Toggle

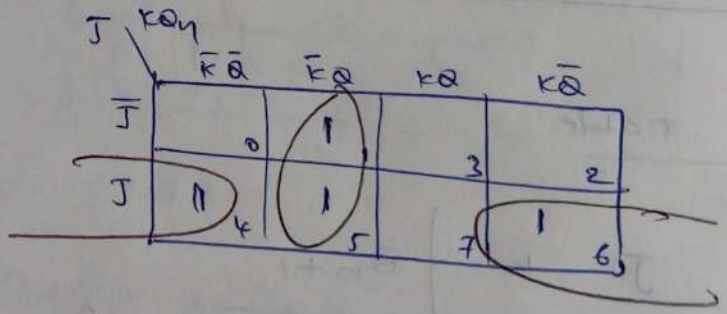
* characteristic table :-

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

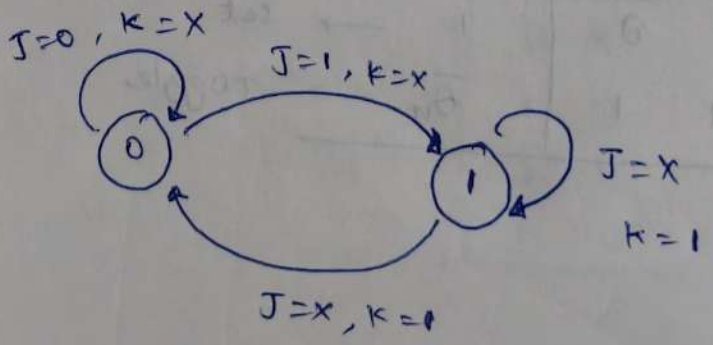
* Excitation table :-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$\Sigma m(1,4,5,6)$



$Q_{n+1} = J\bar{Q} + \bar{K}Q$



4) uses of latch and flipflop

→ Latches used for temporary data storage
→ FF used for permanent data storage until they are reset or overwritten

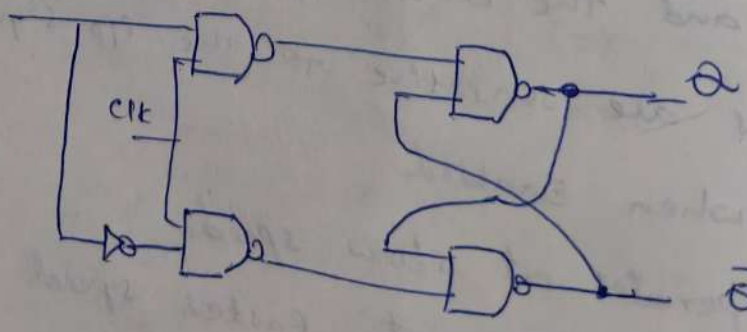
5) why gated SR FF is called as Asynchronous latch.

→ Asynchronous latch also known as a gated SR latch, is a type of FF with an Enable i/p
→ its level triggered, meaning its o/p changes instantly based on its inputs, and does not depend on a clock pulse
→ when Enable i/p is '1', the latch works and when its '0' it retains its previous state.

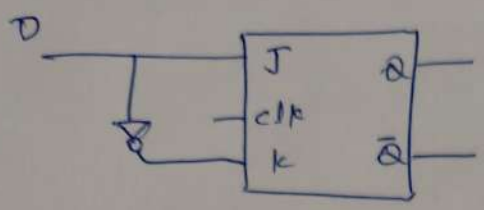
Gated i/p :- adding a gate i/p to an SR FF makes its synchronous, meaning the set and Reset inputs can only change the FF when the gate i/p is active

6) implement d-ff using nand gate :-

D



* D-flipflop → Transparent / Data / Delay D-latch



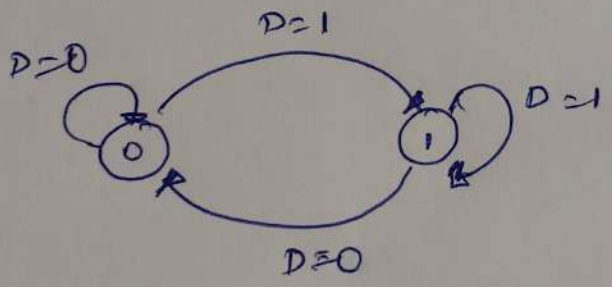
clk	D	Q_{n+1}
0	X	Q_n memory
1	0	0
1	1	1

* Characteristic Table :-

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

* Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1



7) design D-FF using 2×1 mux