University of Maryland Baltimore County
Department of Computer Science and Electrical Engineering

CMSC 411, Computer Architecture

Assignment #1 Due: Thursday 9/21/17 in class

Question 1: *(40 Points)*

Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions (A, B, C, D, and E) in the instruction set.

P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is as follows:

Class	CPI for this class on P1	CPI for this class on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	3	4

A) Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence. What are the peak performances of P1 and P2 expressed in instructions per second?

B) If the number of instructions executed in a certain program is divided equally among the classes of instructions except for class A, which occurs twice as often as each of the others, how much faster is P2 than P1? At what frequency does P2 have the same performance as P1 for this instruction mix?

Question 2: *(35 Points)*

Consider adding a new index addressing mode to MIPS. The addressing mode adds two registers and an 11-bit signed offset to get the effective address. Our compiler will be changed so that the following two code sequences will be replaced as indicated:

```
(1) ADD   R1, R1, R2          }
    LW    Rd, 100(R1)         }   LW   Rd, 100 (R1, R2)

(2) ADD   R1, R1, R2          }
    SW    Rd, 100(R1)         }   SW   Rd, 100 (R1, R2)
```

Use the instruction frequencies shown in the following table.

Instruction	load	store	add	sub	mul	compare	load imm	cond branch	jump	call	return	shift	and	or	other
Frequency	22.8%	14.3%	14.6%	0.5%	0.1%	12.4%	6.8%	11.5%	1.3%	1.1%	1.5%	6.2%	1.6%	4.2%	1.1%

A) Assume that the addressing mode can be used for 10% of the displacement loads and stores (accounting for both the frequency of this type of address calculation and the shorter offset). What is the ratio of instruction count on the enhanced MIPS compared to the original MIPS?

B) If the new addressing mode lengthens the clock cycle by 5%, which machine will be faster and by how much?

Question 3: *(25 Points)*

Your company could speed up a Java program on their new computer by adding hardware support for garbage collection. Garbage collection currently comprises 20% of the cycles of the program. You have two possible changes to the machine. The first one would be to automatically handle garbage collection in hardware. This causes an increase in cycle time by a factor of 1.2. The second would be to provide for new hardware instructions to be added to the ISA that could be used during garbage collection. This would halve the number of instructions needed for garbage collections but increase the cycle time by 1.1. Which of these two options, if either, should you chose? (You MUST explain your answer).