Question: 09
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1 Background

Now, perform a post-synthesis simulation using the module in (6). By observing the times printed using a **$monitor** call in your testbench, show that the output y and z change with some delay after the clk edge. Be sure to create a 50 MHz clock from your testbench according to a time unit convention you document. Provide your output and discuss what other change you see in the output as compared to what you saw in the presynthesis simulation. **WARNING: USE EXPLICIT PORT MAPPING IN YOUR TESTBENCH SINCE SYNTHESIS SOMETIMES REORDERS THE PORTS.**

2 Implementation

The module from Question 06 was used to go through the Post-Synthesis Simulation process. A screen capture of the successful simulation is provided below.

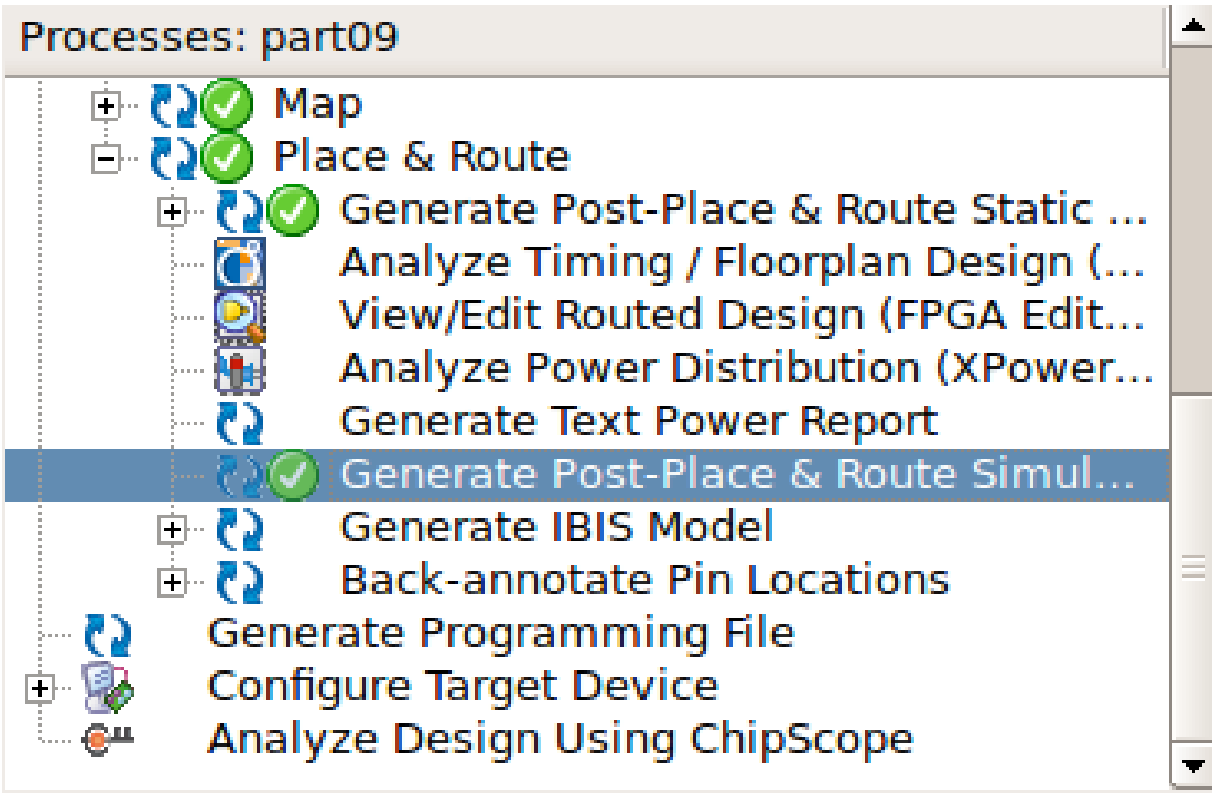

Figure 1: Successful Post-Place & Route Simulation

The module and its test bench with explicit port declarations and a 50 MHz clock were synthesized, and the waveforms were generated.

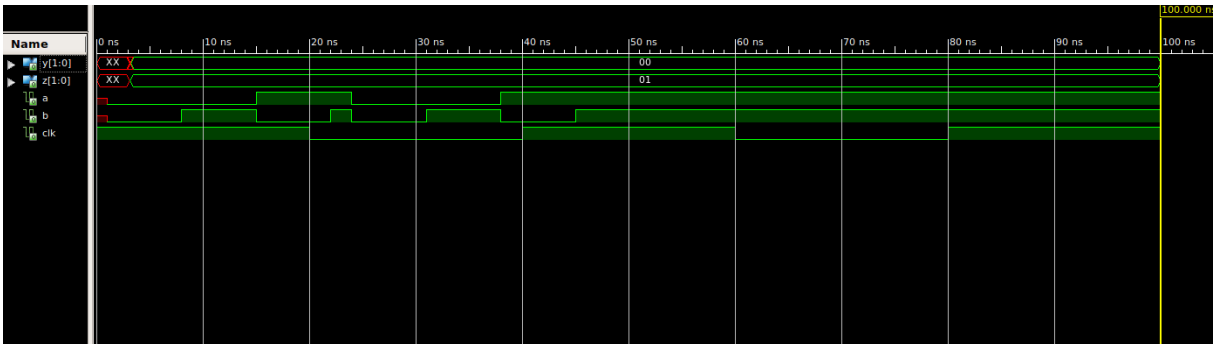

Figure 2: Waveform Generated from Part 9 Test Bench

The output from the test bench were saved in the following table:

Table 1: Inputs and Outputs of The Part 9 Test Bench

time	a	b	y	z
3000	0	0	xx	xx
3000	0	0	0x	01
3000	0	0	00	01
8000	0	1	00	01
10000	0	1	00	01
15000	1	0	00	01
17000	1	0	00	01
22000	1	1	00	01
24000	0	0	00	01
26000	0	0	00	01
31000	0	1	00	01
33000	0	1	00	01
38000	1	0	00	01
40000	1	0	00	01
45000	1	1	00	01
47000	1	1	00	01

3 Observations

The outputs do not appear to be affected after the post-synthesis. In the presynthesis simulations, the test bench would display changes on the outputs. The post-synthesis simulation appears to only affect after the initial change in the clock. The lack of expected changes in the outputs may be caused due to the improper implementation in the original module.