8086 Microprocessor Design Project

CMPE 310
Systems Design and Programming
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Contents

1 Introduction

This document provides detailed instructions to develop an 8086 microprocessor board using Cadence® OrCAD® Capture software. Included are the schematics of individual IC components and their description. Details of the ICs include decoding, programming specifications, and descriptions of IC pinouts.

1.1 Purpose

As per the project description, this document is to serve as the only documentation of the operational and functional specifications of the Intel 8086. The documentation is to be thorough and concise to provide information to design a similar board.

1.2 Scope and Organization of Document

The document will elaborate on the individual building blocks of the 8086 board. The integrated circuit (IC) chips used in designing the board will be discussed, along with brief, high-level overviews of their pinouts, their various connections and their functionalities. The connections and dependencies between the different components such as memory and IO devices will be discussed in detail.

The document is organized into sections that cover the individual components and their IC pinouts, functionalities, connections and role in the 8086 board. Schematics of the different components and their circuitry are included. Code snippets, including the VHDL (VHSIC Hardware Description Language) implementations of the decoding hardware and the Assembly implementations of the data and memory addressing, are also incorporated in the document.

2 8086 Microprocessor

The 8086 microprocessor is an enhanced version of the 8085 microprocessor developed by Intel in 1978. It is a 16-bit microprocessor, with 20 address lines and 16 data lines to provide up to 1 MB of physical memory. The 8086 microprocessor described in the project will operate in its minimum mode.

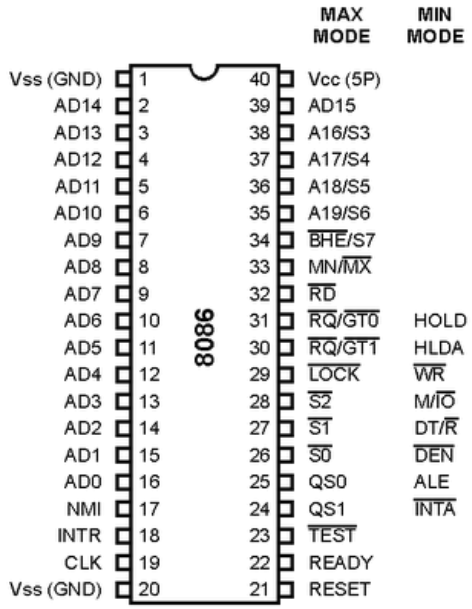

Figure 1: 8086 Microprocessor

2.1 Features

The 8086 microprocessor is known for its significant advancements since its predecessors. The most prominent features include, but are not limited to:

- 6 bytes of cache memory for faster processing
- Pipelining stages: Fetch Stage and Execute Stage
- Instruction queue
- 256 vectored interrupts
- Maximum and minimum modes of operation, suitable for multiple and single processors respectively

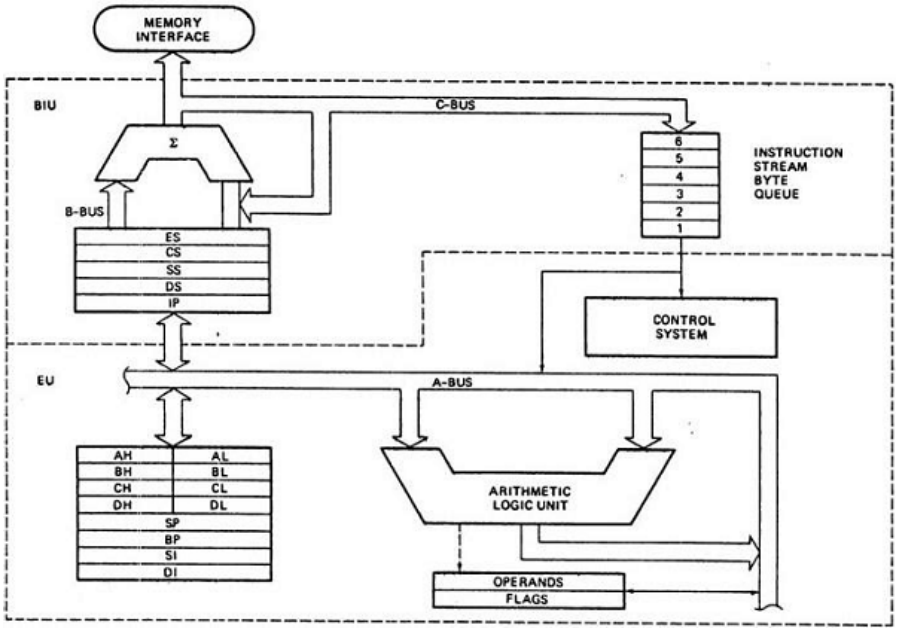

Figure 2: Architecture of 8086

2.2 Address and Data Buses

The 8086 CPU has a unidirectional address bus with 20 address lines and a bidirectional data bus with 16 data lines. [1] The address bus is used to select the desired memory or I/O device by generating a unique address which corresponds to the memory location or the location of I/O device of the system. The data bus is used to transfer data between the CPU and memory and the CPU and I/O devices.

The address bus is denoted as $A_{19} - A_0$ (20 lines) and the data bus $D_{15} - D_0$ (16 lines). The peripheral devices implemented with the 8086 in this document however consist of 8-bit data bus architectures. The data bus would therefore be multiplexed and more commonly denoted as $D_7 - D_0$ (8 lines).

2.3 Control Bus

The control bus of 8086 carries control signals which are used to specify the memory and I/O devices. [1] The bus is bidirectional and assists the CPU in synchronizing control signals to internal devices and external components. It is comprised of interrupt lines, byte enable lines, read/write signals and status lines.

2.4 Pinouts

Refer to Appendix B for the pinouts of the chip.

3 Decoding

3.1 Programming Logic Device - 16L8

3.2 Programming the PLD

3.3 Pinouts

Refer to Appendix B for the pinouts of the chip.

4 Clock Generator - 8284A

The 8184A Clock Generator is an ancillary component to the 8086. This system clock is used to synchronize both internal and external operations using an external oscillator. The device is also used for READY and RESET synchronizations and TTL-level peripheral clock signal generation.

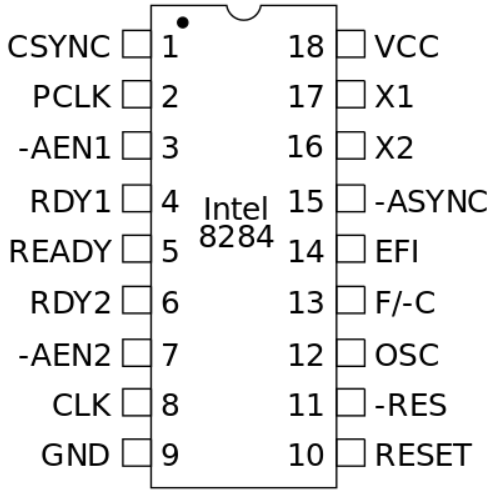

Figure 3: 8284A Clock Generator

4.1 Clock Speed

The 8086 internal clock has a frequency of 5 MHz ($\frac{1}{3}$ of CLK). The external crystal typically oscillates at 15 MHz.

4.2 RESET Operation

Correct reset timing requires that the RESET input to the 8086 becomes a logic 1 in 4 clock cycles and remain high for at least 50 μS. The reset switch is implemented in a RC circuit with typical resistance of 100 $k\Omega$ and 10 μF.

4.3 Pinouts

Refer to Appendix B for the pinouts of the chip.

5 Memory Architecture

5.1 Static Random Access Memory - CY7C199

5.2 Interfacing Memory Banks with the Microprocessor

5.3 Addressing

5.4 CMOS Flash Memory - 28F010

5.5 Flash Memory Implementation

5.6 Addressing Flash Memory

6 Programmable Keyboard/Display Interface - 8279

6.1 Description

6.2 Interfacing with a 5x5 Keyboard Matrix

6.3 Addressing

6.4 Programming the Keyboard Interface

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6.6 Assembly Implementation

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7.2 Programming

7.3 Addressing

7.4 Assembly Implementation

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8.1 Description

8.2 Interfacing 30-Pin Headers with the 8255

8.3 Addressing

8.4 Assembly Implementation and Programming of the 8255

8.5 Interfacing 14-Pin Headers with the 8254

8.6 Interfacing 14-Pin Headers with the 8259

8.7 Interfacing 60-Pin External Header to the Address, Data and Control Bus

9 Interrupt Controller - 8259

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9.2 Implementing a Master Interrupt Controller

9.3 Addressing

9.4 Assembly Implementation and Programming

10 UART

10.1 16550 UART

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12.1 Seven-Segment LEDs

12.2 Addressing

12.3 LEDs

12.4 Addressing

12.5 DIP Switches

12.6 Addressing

A Appendix A: Schematics

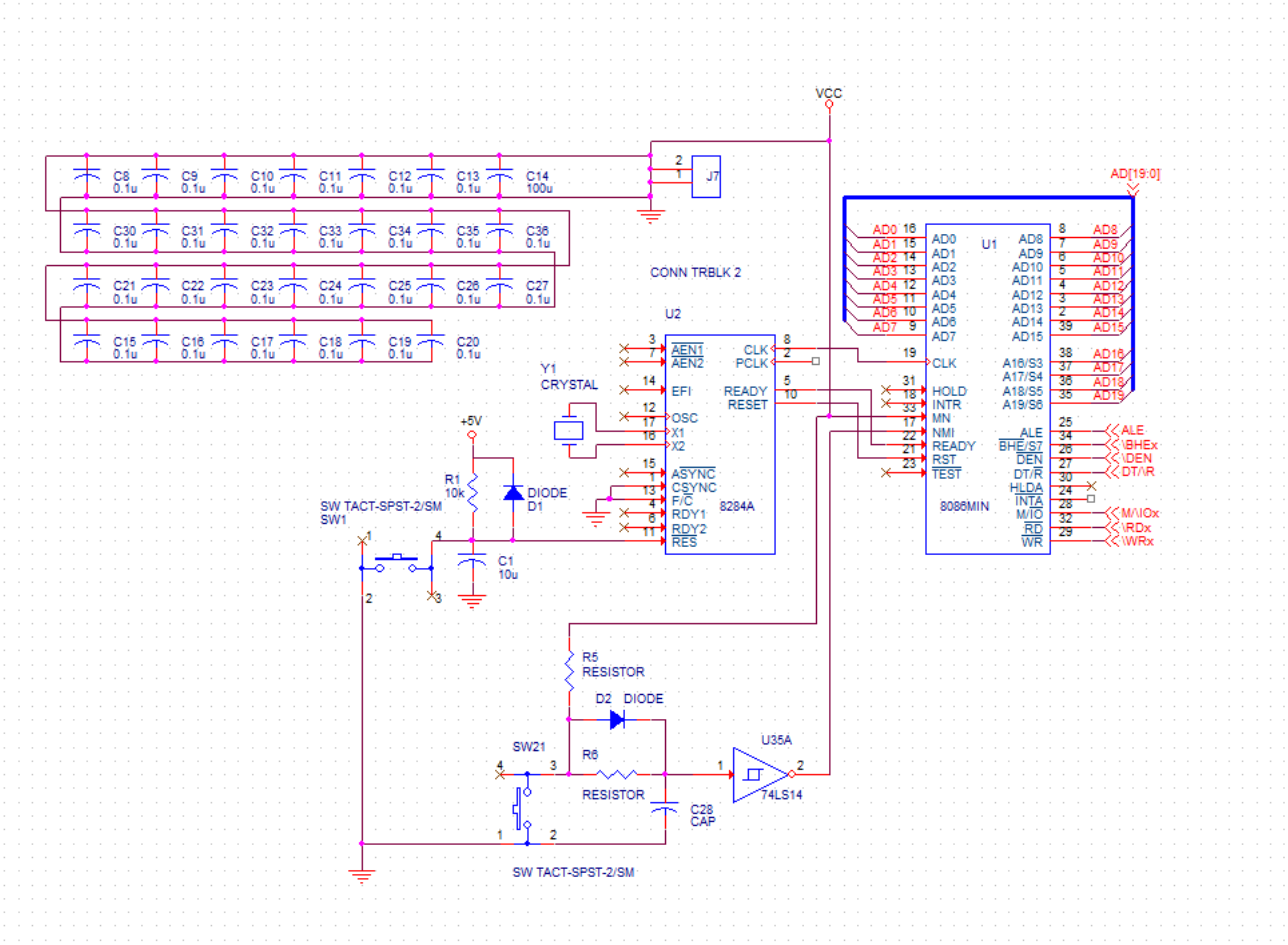

Figure 4: 8086 interfaced with the 8284A clock generator and its Reset RC Push Button Circuit, and the Power Bank of the Board

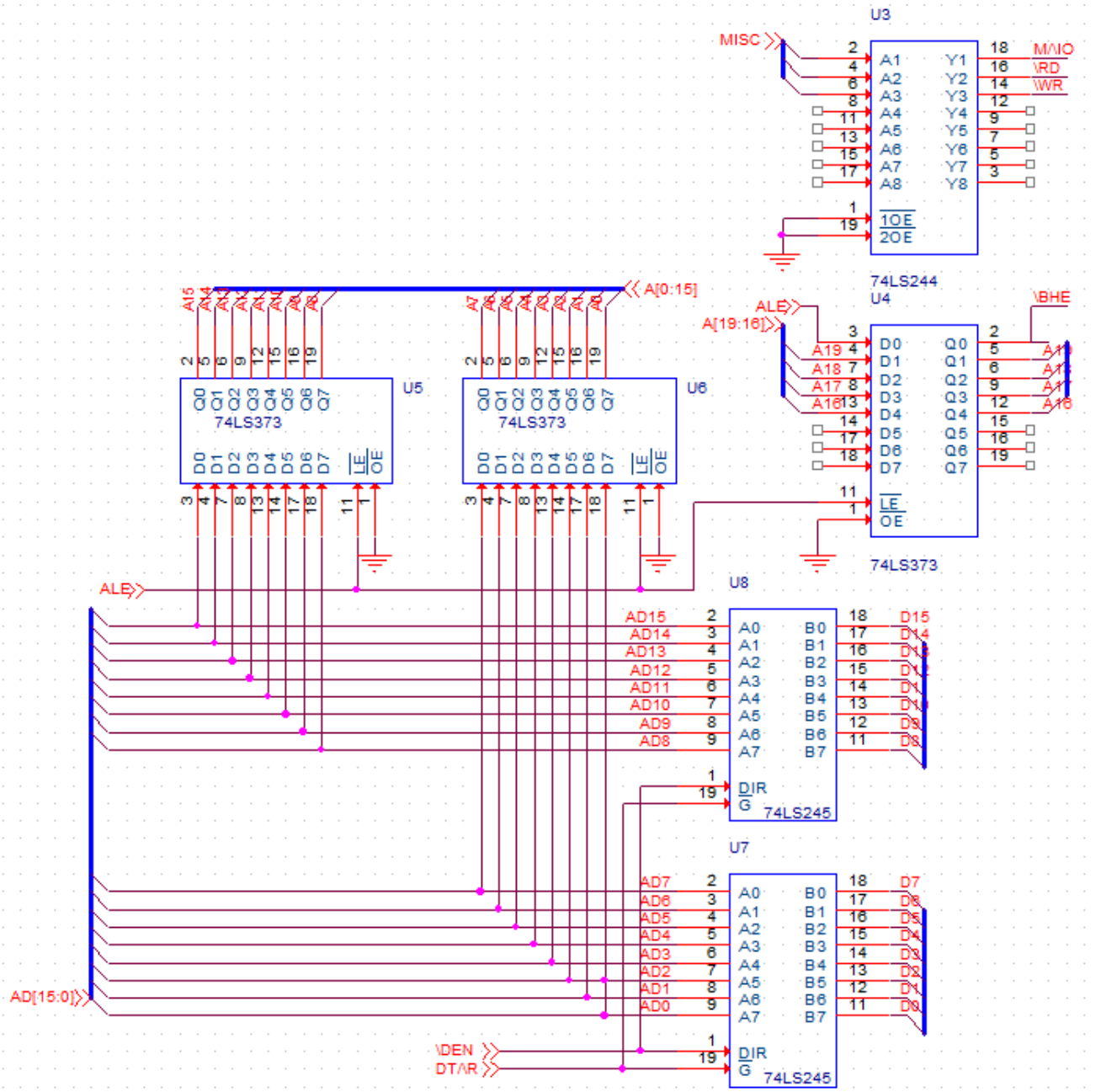

Figure 5: 8086 Demultiplexed

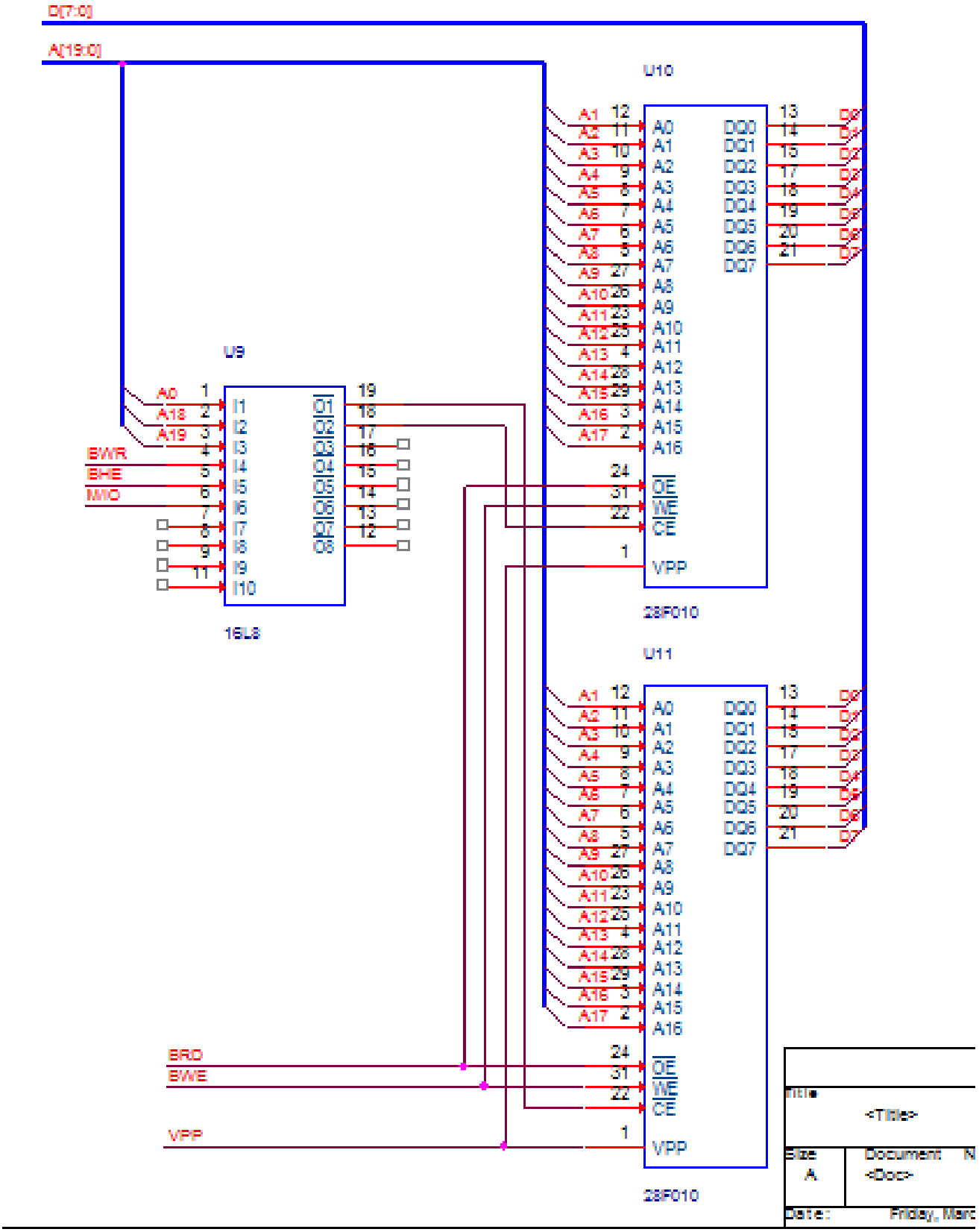

Figure 6: 256 kB of CMOS Flash Memory and 128 kB Static SRAM

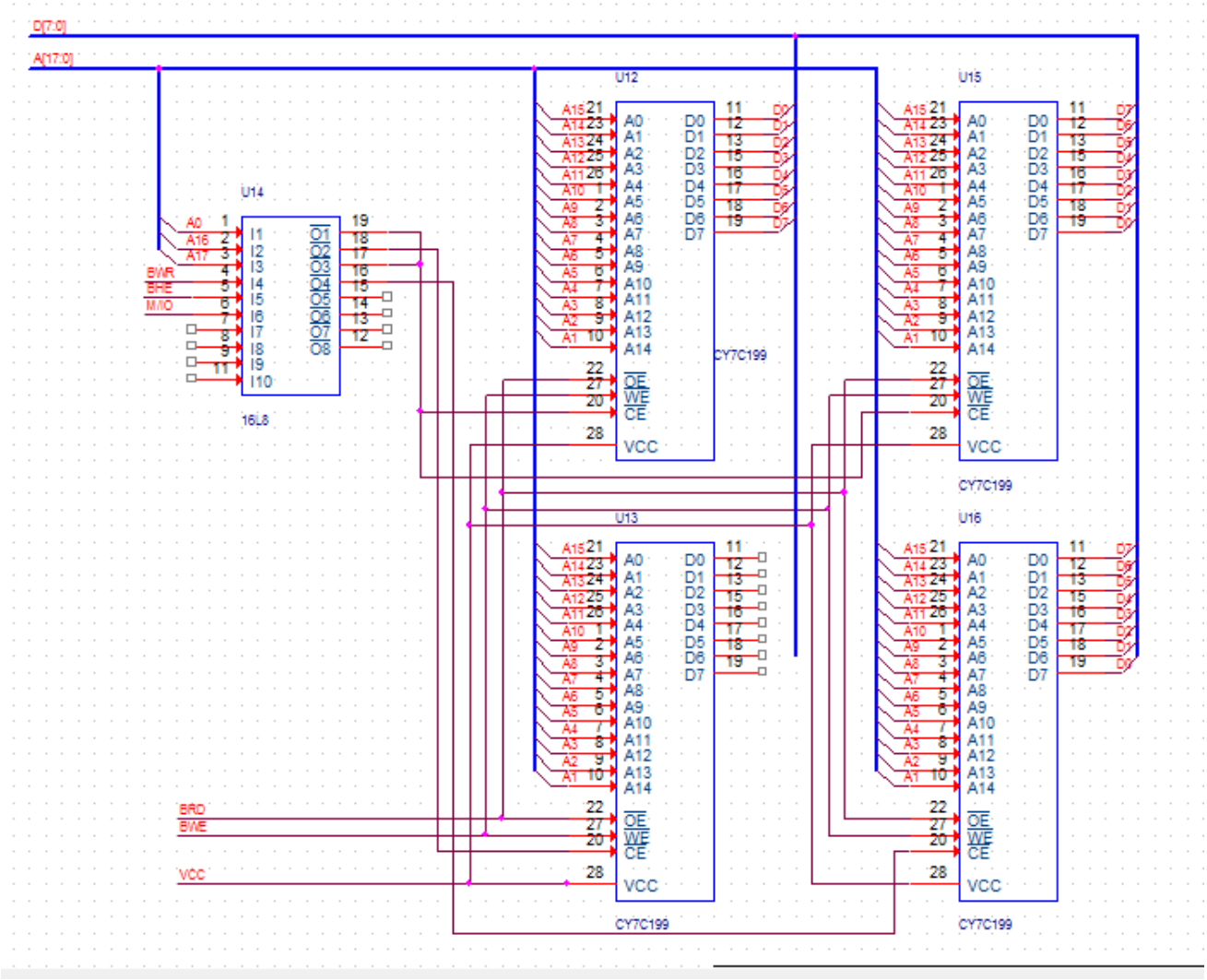

Figure 7: 8255 Programmable Peripheral Interface Chips with Port Connections Pulled into Headers

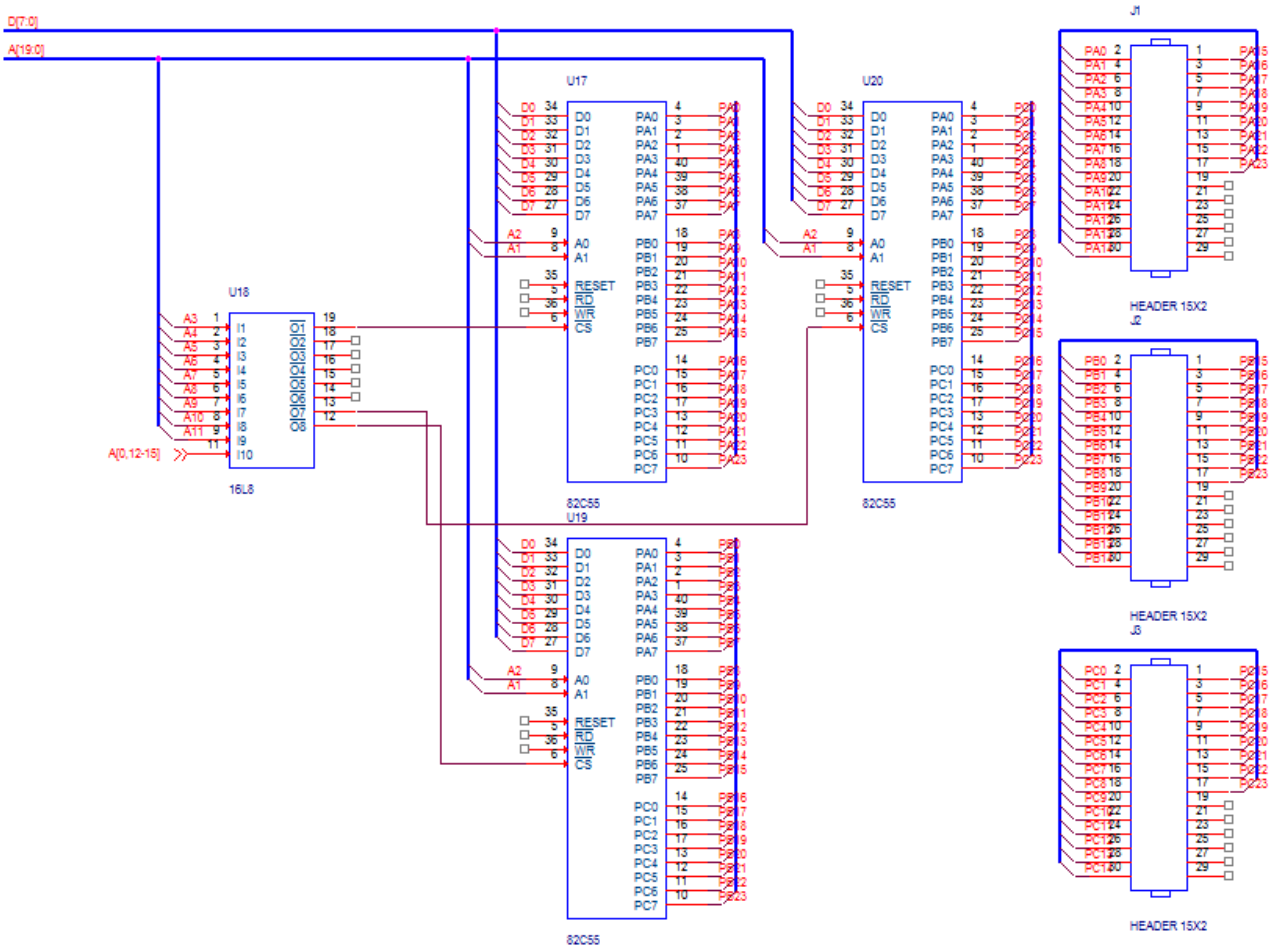

Figure 8: 8284A Interfaced with 8086 and its Reset RC Push Button Circuit

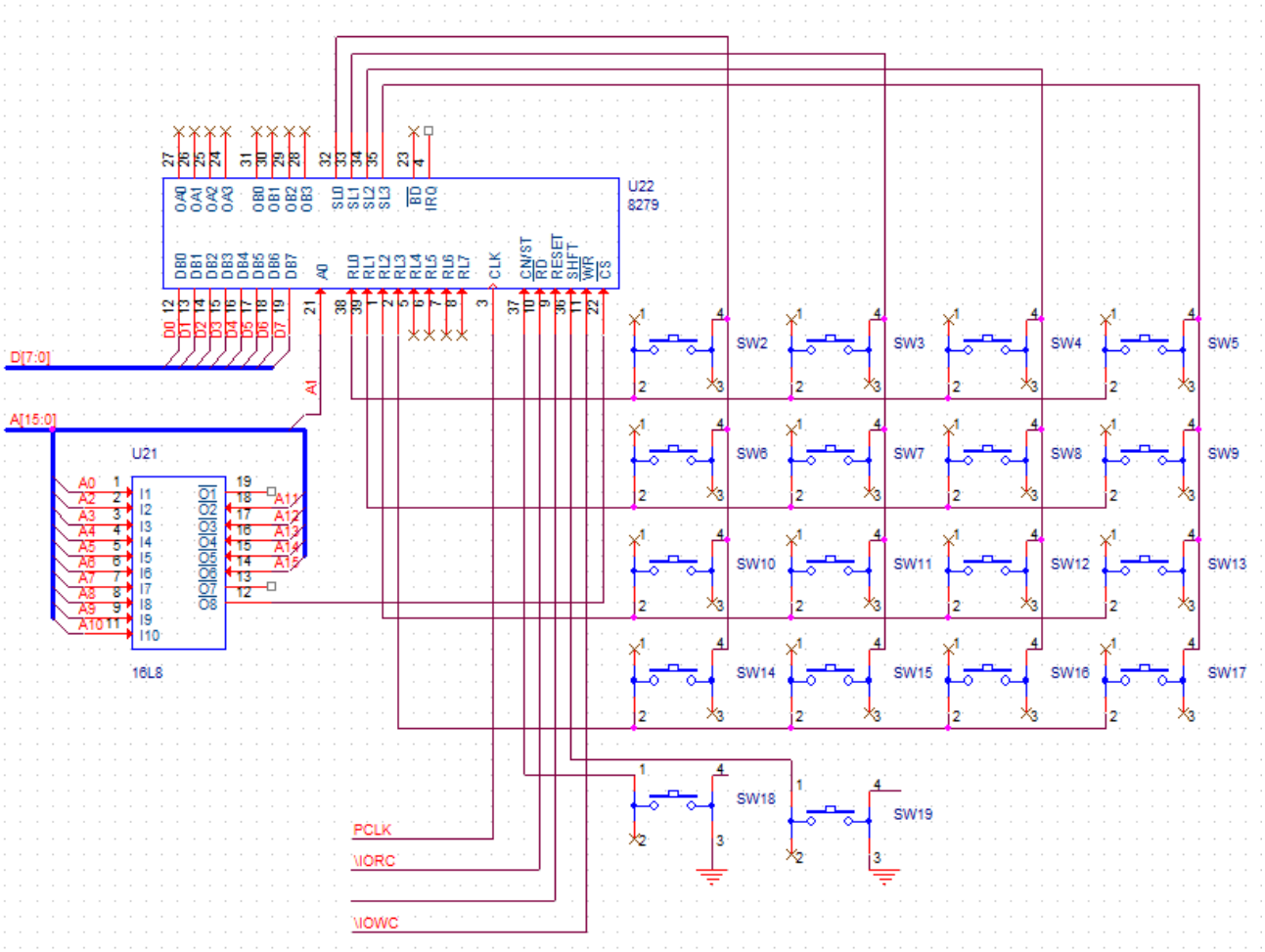

Figure 9: 8284A Interfaced with 8086 and its Reset RC Push Button Circuit

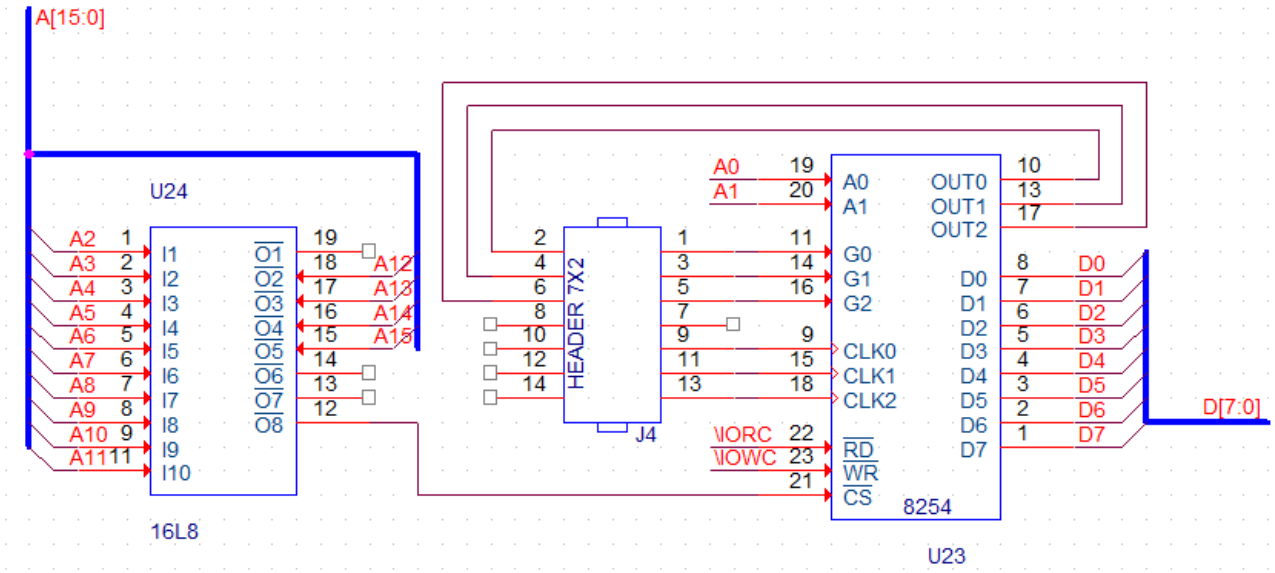

Figure 10: 8284A Interfaced with 8086 and its Reset RC Push Button Circuit

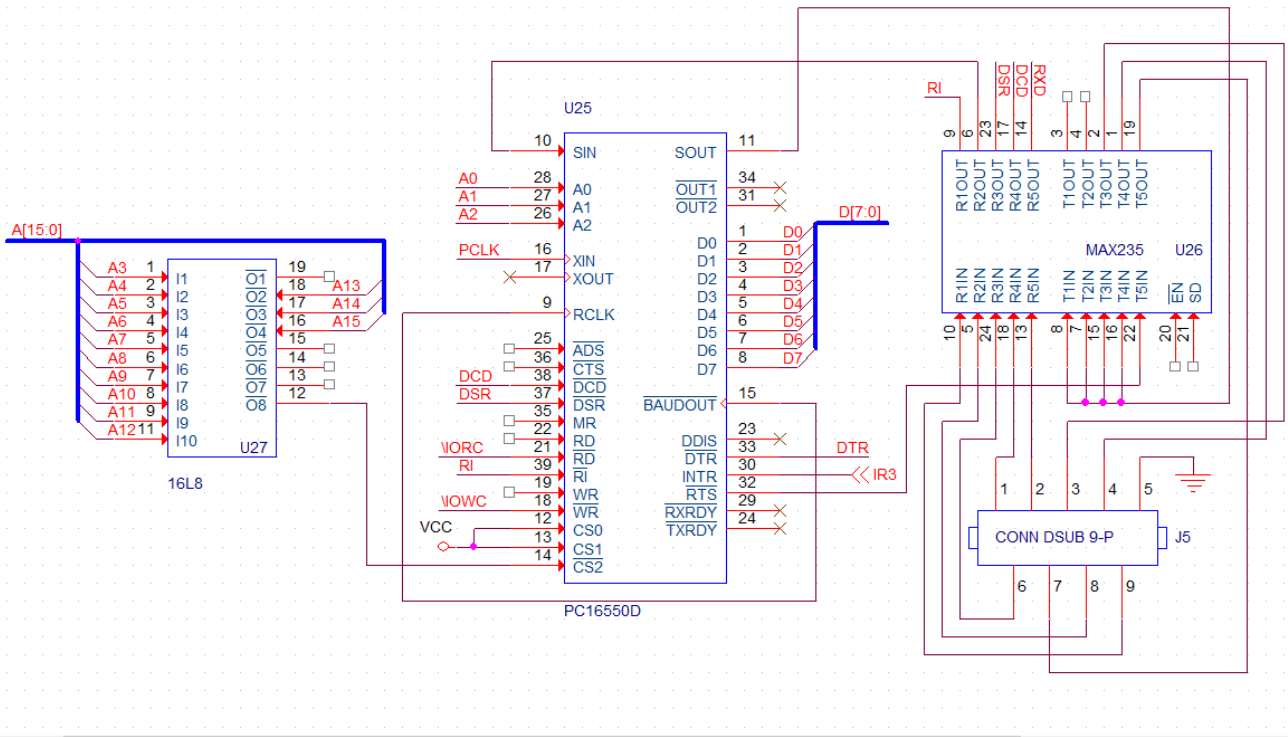

Figure 11: 8284A Interfaced with 8086 and its Reset RC Push Button Circuit

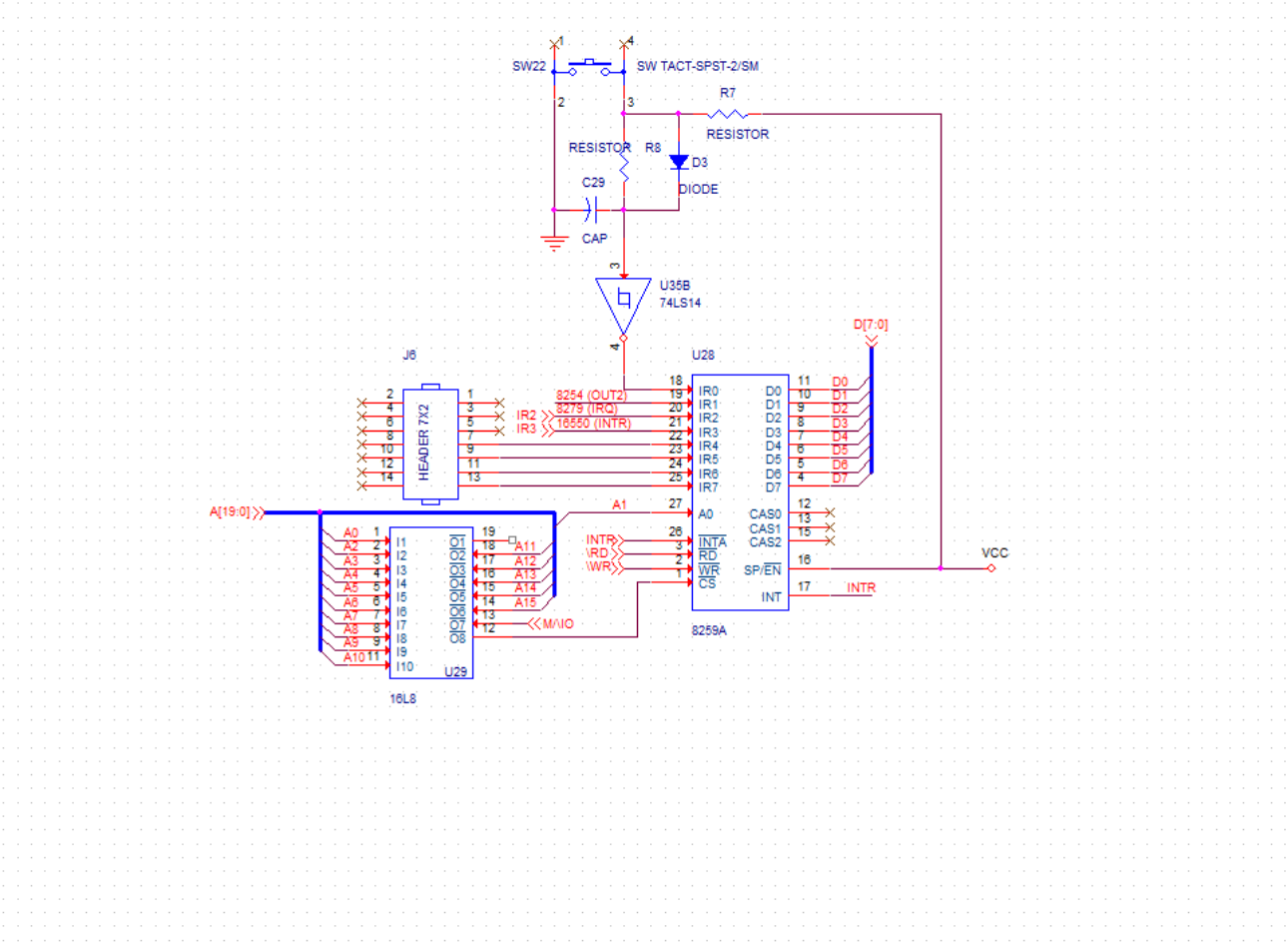

Figure 12: 8284A Interfaced with 8086 and its Reset RC Push Button Circuit

B Appendix B: Pinouts

B.1 8086 Chip

- $M/\overline{IO}$: (Memory/ I/O) indicates if the address is a memory or I/O address
- $\overline{INTA}$: (Interrupt Acknowledgment) generated in response to $INTR$ to put the interrupt vector on the data bus
- ALE: (Address Latch Enable) when 1, address data bus contains a memory or I/O address
- $\overline{DEN}$: (Data Bus Enable) activates external data bus buffers

References

[1] DBHJDS http://gradestack.com/Microprocessors-and/Architecture-of-8086-and/Address-Bus-Data-Bus-/19317-3912-38171-study-wtw