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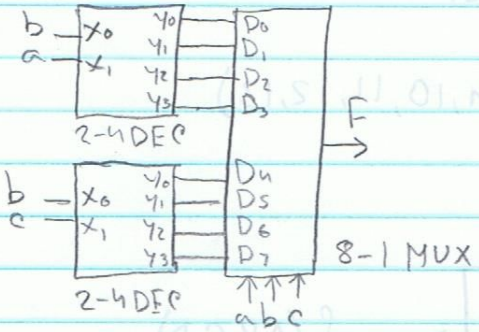
CMPE 212
HW4

① Find the canonical SOP expression of:




* 2-4 DEC:

| a | b | b | c | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

$\therefore Y_{0a} = \bar{a}\bar{b}$, $Y_{0b} = \bar{b}\bar{c}$
$Y_{1a} = \bar{a}b$, $Y_{1b} = \bar{b}c$
$Y_{2a} = a\bar{b}$, $Y_{2b} = b\bar{c}$
$Y_{3a} = ab$, $Y_{3b} = bc$

* 8-1 MUX:

| a | b | c | F |
|---|---|---|---|
| 0 | 0 | 0 | $Y_{0a}$ |
| 0 | 0 | 1 | $Y_{1a}$ |
| 0 | 1 | 0 | $Y_{2a}$ |
| 0 | 1 | 1 | $Y_{3a}$ |
| 1 | 0 | 0 | $Y_{0b}$ |
| 1 | 0 | 1 | $Y_{1b}$ |
| 1 | 1 | 0 | $Y_{2b}$ |
| 1 | 1 | 1 | $Y_{3b}$ |

$\therefore F = \bar{a}\bar{b}\bar{c}Y_{0a} + \bar{a}\bar{b}cY_{1a} + \bar{a}b\bar{c}Y_{2a} + \bar{a}bcY_{3a} + ab\bar{c}Y_{0b} + abcY_{1b} + ab\bar{c}Y_{2b} + abcY_{3b}$

$\Rightarrow \bar{a}\bar{b}\bar{c}(\bar{a}\bar{b}) + \bar{a}\bar{b}c(\bar{a}\bar{b}) + \bar{a}b\bar{c}(\bar{a}b) + \bar{a}bc(\bar{a}b) + ab\bar{c}(\bar{b}\bar{c}) + abc(\bar{b}c) + ab\bar{c}(b\bar{c}) + abc(bc)$

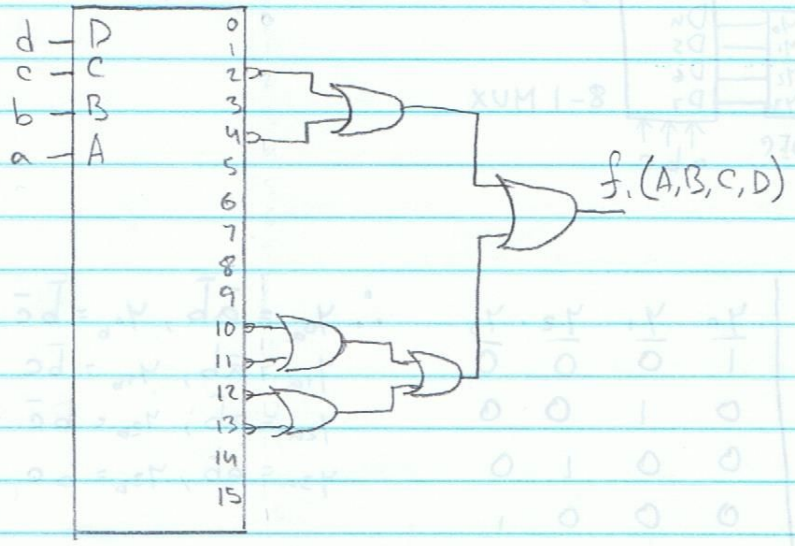
$\Rightarrow \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c} + a\bar{b}c + ab\bar{c} + abc$

$\Leftrightarrow 000 + 100 + 101 + 110 + 111$

$\Leftrightarrow \sum m(0,4,5,6,7)$ □

② Realize the following set of functions w/ only one 74154 decoder module and logic gates:

a) $f_1(A,B,C,D) = \sum_m(2,4,10,11,12,13)$




b) $f_2(A,B,C,D) = C(\bar{B}+A) + \bar{A}\bar{C}D$

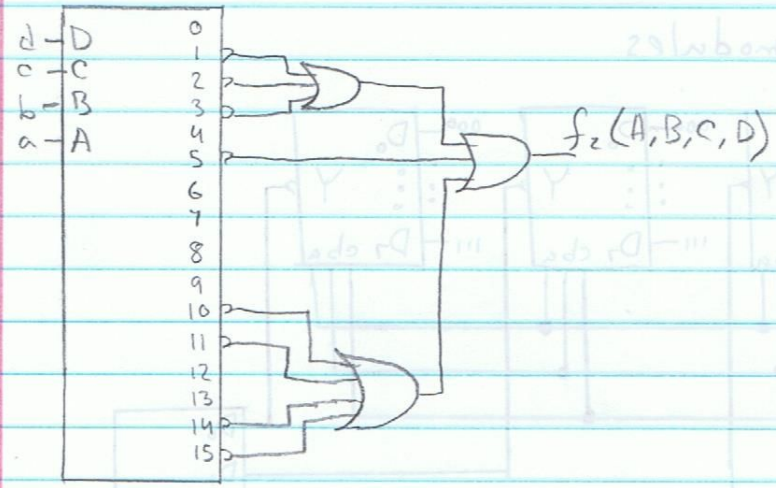
$\Rightarrow \bar{B}C + AC + \bar{A}\bar{C}D$

$\Leftrightarrow x\bar{B}Cx + AxCx + \bar{A}x\bar{C}D$, where x := don't care

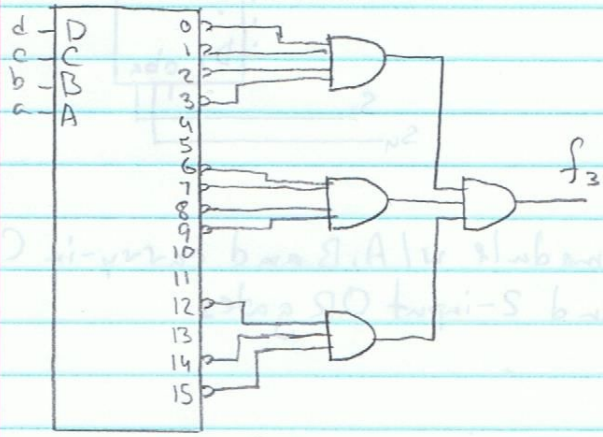
| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | 1 | 1 |
| 01 | | 1 | | |
| 11 | | | 1 | 1 |
| 10 | | | 1 | 1 |

$\Rightarrow f_2 := 0001 + 0010 + 0011 + 0101 + 1010 + 1011 + 1110 + 1111$

$\Leftrightarrow \sum_m(1,2,3,5,10,11,14,15)$

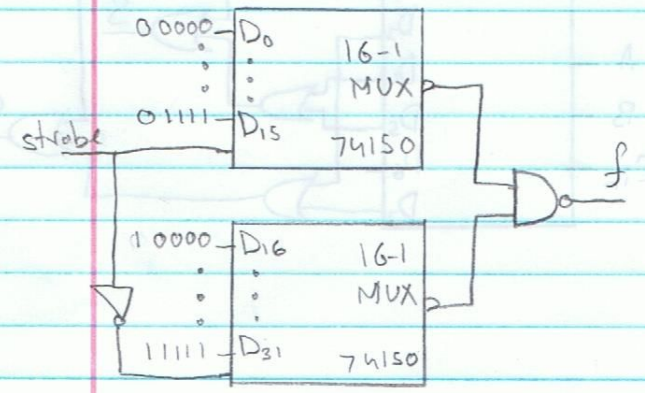



c) $f_3(A,B,C,D) = \prod M(0,1,2,3,6,7,8,9,12,14,15)$

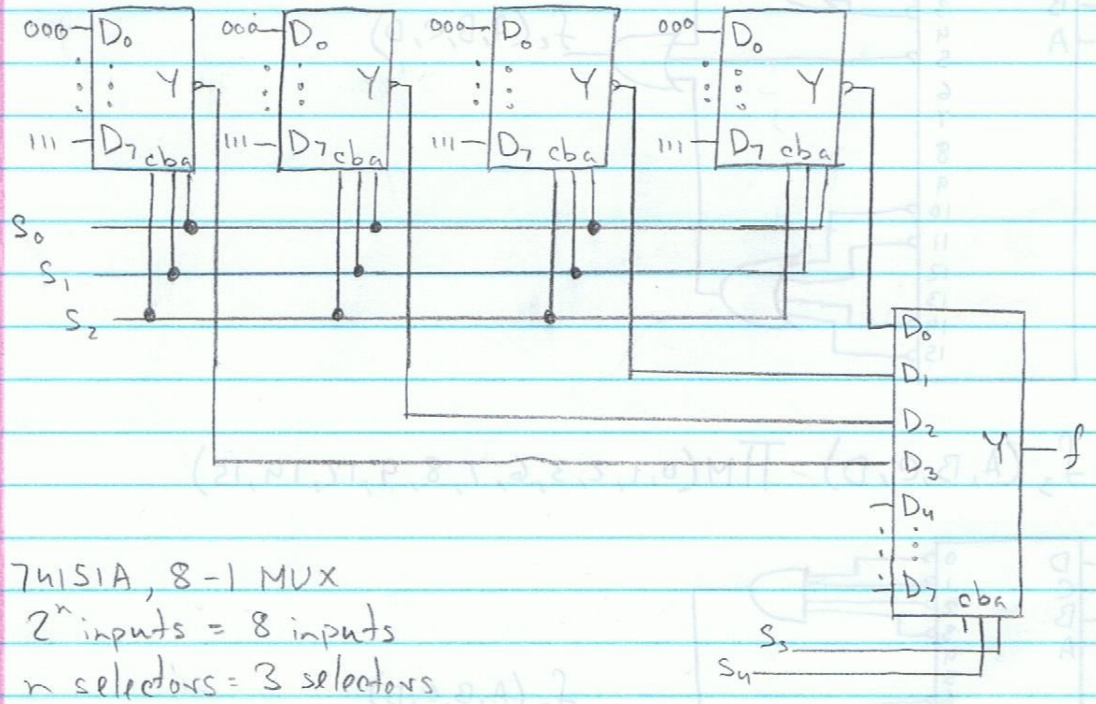



③ Design a 32-1 MUX using:

a) two 74150 modules, one inverter, and one NAND gate



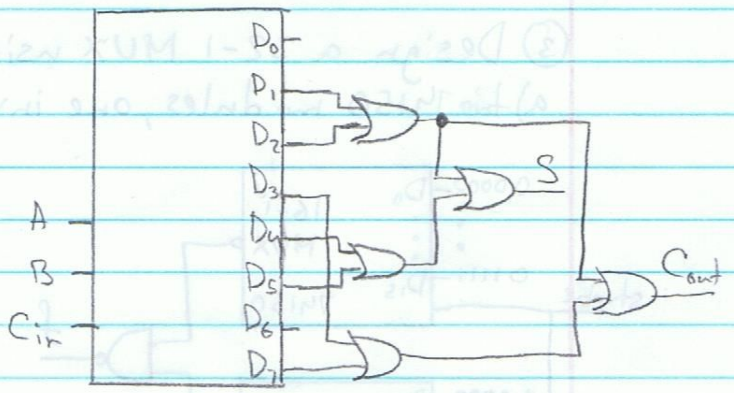
b) Only 74151A modules




74151A, 8-1 MUX
$2^n$ inputs = 8 inputs
n selectors = 3 selectors

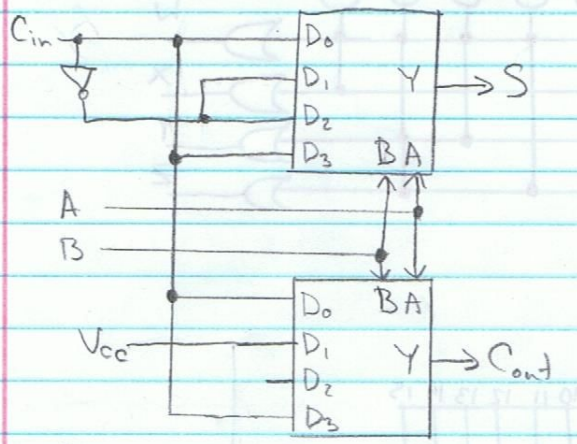
④ Design a subtraction module w/ A, B and carry-in $C_{in}$.
a) Using a 3-8 decoder and 2-input OR gates

| A | B | $C_{in}$ | S | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |



b) Using two 4-2 MUX and one inverter

| A | B | $C_{in}$ | S | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | $0 = C_{in}$ | $0 = C_{in}$ |
| 0 | 0 | 1 | $1 = C_{in}$ | $1 = C_{in}$ |
| 0 | 1 | 0 | $1 = \bar{C}_{in}$ | 1 |
| 0 | 1 | 1 | $0 = \bar{C}_{in}$ | 1 |
| 1 | 0 | 0 | $1 = \bar{C}_{in}$ | 0 |
| 1 | 0 | 1 | $0 = \bar{C}_{in}$ | 0 |
| 1 | 1 | 0 | $0 = C_{in}$ | $0 = C_{in}$ |
| 1 | 1 | 1 | $1 = C_{in}$ | $1 = C_{in}$ |




⑤ Design a BCD to excess-3 code converter:

| A | B | C | D | $M_{10}$ | $(M+3)_{10}$ | W | X | Y | Z |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 3 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 4 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 2 | 5 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 3 | 6 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 4 | 7 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 5 | 8 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 6 | 9 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 7 | 10 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 8 | 11 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 12 | 1 | 1 | 0 | 0 |

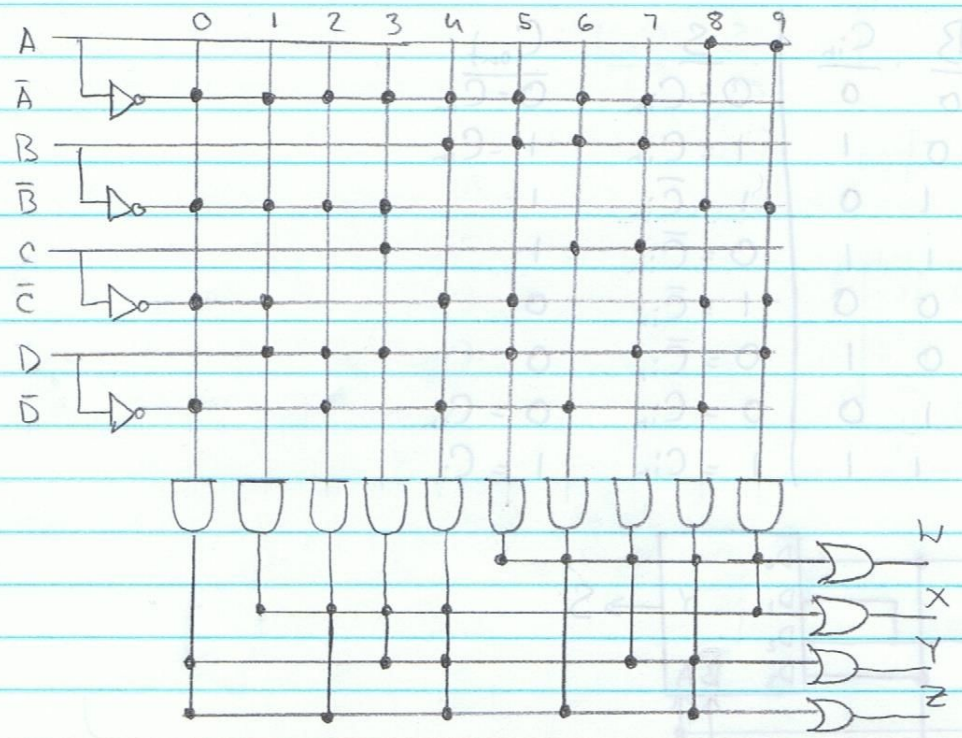
$\therefore W = \sum m(5,6,7,8,9)$

$X = \sum m(1,2,3,4,9)$

$Y = \sum m(0,3,4,7,8)$

$Z = \sum m(0,2,4,6,8)$

a) Using PLA:




Using ROM: