

CMPE 310 Systems Design and Programming

L5: Chapter 9 – 8086/8088 Hardware Specifications

UMBC

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L5 Objectives

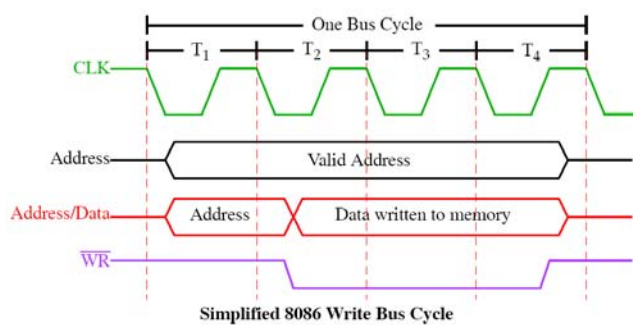
- * Timing diagrams

BUS Timing

* **Important to understand before choosing memory or I/O**

* **Writing**

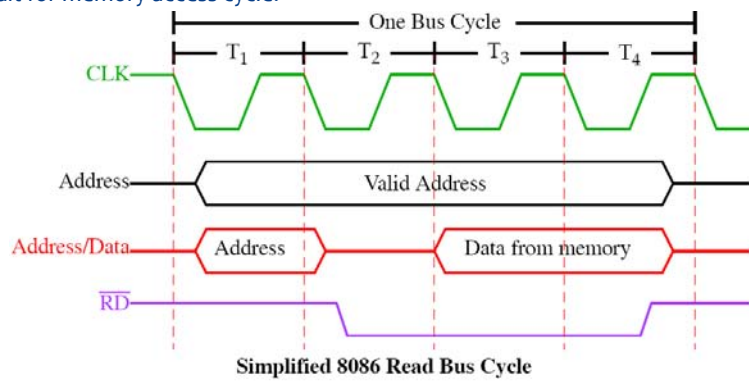
- * Dump address on address bus.
- * Dump data on data bus.
- * Issue a write (\overline{WR}) and set M/\overline{IO} to 1.



BUS Timing

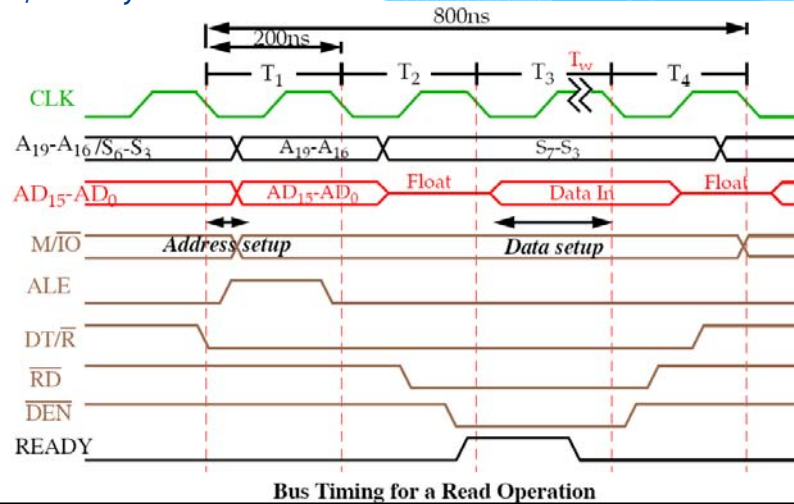
* **Reading**

- * Dump address on address bus.
- * Issue a read (\overline{RD}) and set M/\overline{IO} to 1.
- * Wait for memory access cycle.



BUS Timing

* x86/88 bus cycle



BUS Timing

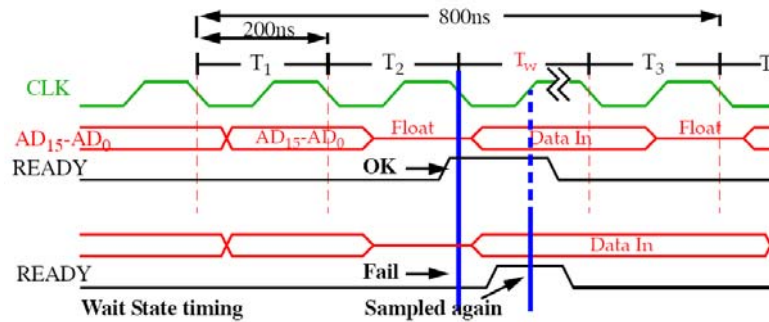
- * During T₁:
 - * The address is placed on the Address/Data bus.
 - * Control signals M/I₀, ALE and DT/R specify memory or I/O, latch the address onto the address bus & set the direction of data transfer on data bus.
- * During T₂:
 - * 8086 issues the \overline{RD} or \overline{WR} signal, \overline{DEN} , and, for a write, data appear on the data bus.
 - * \overline{DEN} enables the memory or I/O device to receive the data for writes and the 8086 to receive the data for reads.
- * During T₃:
 - * This clocking period is provided to allow memory to access data.
 - * READY is sampled at the end of T₂.
 - * If low, T₃ becomes a wait state (T_w).
 - * Otherwise, the data bus is sampled at the end of T₃.
- * During T₄:
 - * All bus signals are deactivated, in preparation for next bus cycle.
 - * Data is sampled for reads, writes occur for writes.

BUS Timing

- * Each BUS CYCLE on the 8086 equals **four system clocking periods (T states)**
- * The clock rate is **5MHz, therefore one Bus Cycle is 800ns.**
- * The transfer rate is **1.25MHz.**
- * Memory specifications (memory access time) must match constraints of system timing.
 - * For example, bus timing for a read operation shows almost **600ns are needed to read data.**
 - * However, memory must access faster due to setup times, e.g. Address setup and data setup.
 - * This subtracts off about **140ns.**
 - * Therefore, memory must access in at least **460ns minus another 40ns guard band** for buffers and decoders.
 - * **420ns DRAM required for the 8086.**

BUS Timing

- * **READY**
 - * An input to the 8086 that causes **wait states** for slower memory and I/O components.
 - * A wait state (T_w) is an extra clock period inserted between T_2 and T_3 to lengthen the bus cycle.
 - * For example, this **extends a 420 ns bus cycle (at 5MHz clock) to 620ns.**



Next Time

* Memory Devices

