Question: 05
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1 Background

Leveraging the concatenation operator, create a module that accepts a 64-bit input x, and swaps pairs of even-and odd bytes to produce a 64-bit output u. The output should be registered using a clock signal clk.

2 Implementation

The odd and even indices of 'x' were swapped in a simple while loop to create the output 'u'.

The module implementation along with its testbench can be found in the 'scripts' directory. A sample of the waveform generated is provided:

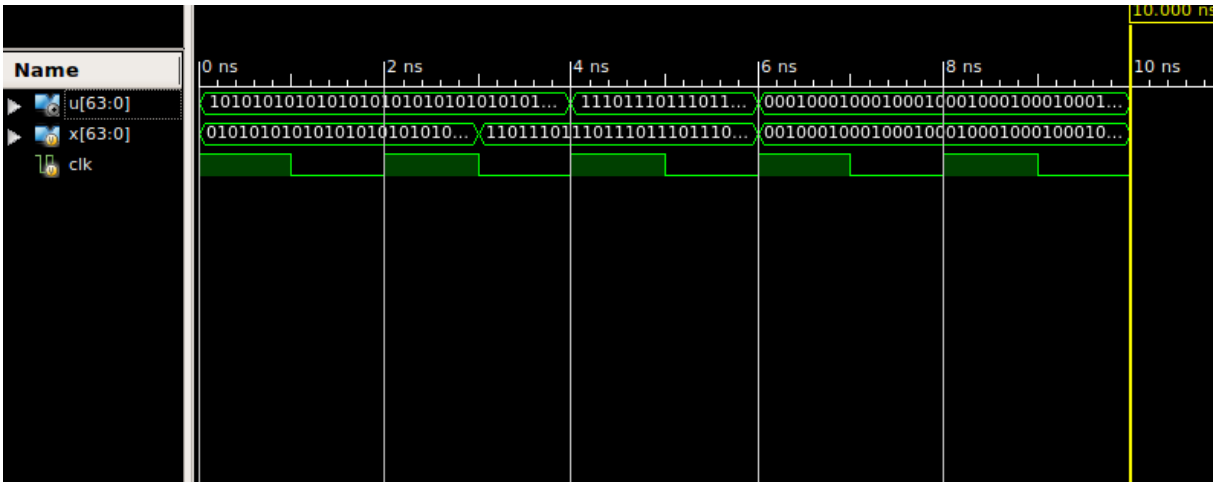

Figure 1: Waveform Generated from Part 4 Test Bench

The following output is dumped from the test bench as well, demonstrating the swapping of the bits:

```
x = 0101010101010101010101010101010101010101010101010101010101010101 when clk = 1
u = 1010101010101010101010101010101010101010101010101010101010101010 when clk = 1
x = 1101110111011101110111011101110111011101110111011101110111011101 when clk = 1
u = 1110111011101110111011101110111011101110111011101110111011101110 when clk = 1
x = 1101110111011101110111011101110111011101110111011101110111011101 when clk = 0
u = 1110111011101110111011101110111011101110111011101110111011101110 when clk = 0
x = 0010001000100010001000100010001000100010001000100010001000100010 when clk = 1
u = 0001000100010001000100010001000100010001000100010001000100010001 when clk = 1
```