

CMPE 310 Systems Design and Programming

L10: Chapter 11 – BASIC I/O Interface

UMBC

AN HONORS UNIVERSITY IN MARYLAND

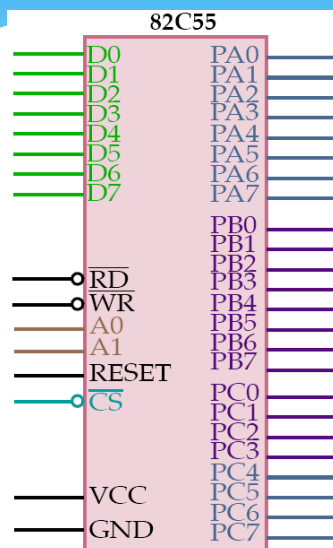
L10 Objectives

- * Describe the function of each pin of the 82C55
- * Diagram how the 82C55 is connected to the x86/88 PC
- * Program the 82C55

Programmable Peripheral Interface

- * The 82C55 is a popular interfacing component, that can interface any TTL-compatible I/O device to the microprocessor.
- * It is used to interface to the keyboard and a parallel printer port in PCs (usually as part of an integrated chipset).
- * Requires insertion of wait states if used with a microprocessor using higher than an 8 MHz clock.
- * PPI has 24 pins for I/O that are programmable in groups of 12 pins and has three distinct modes of operation.
- * In the PC, an 82C55 or its equivalent is decoded at I/O ports 60H-63H.

Pinout of 82C55 PPI



Group A

Port A (PA7-PA0) and upper half of port C (PC7 - PC4)

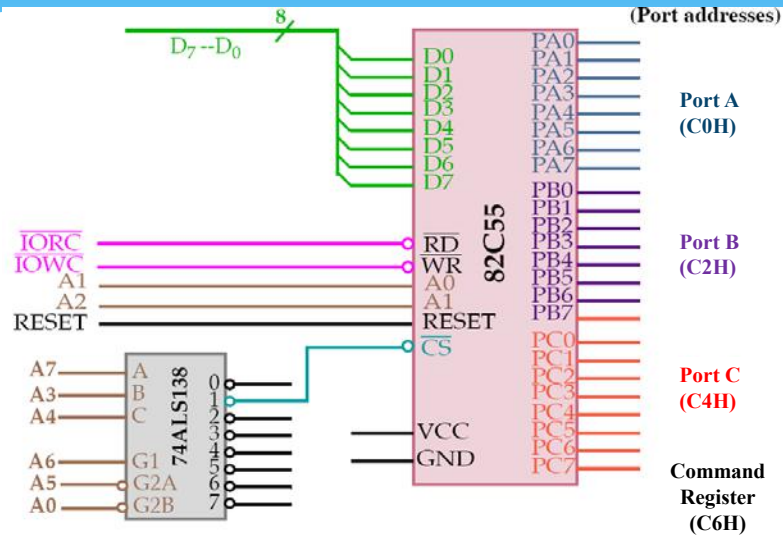
Group B

Port B (PB7-PB0) and lower half of port C (PC3 - PC0)

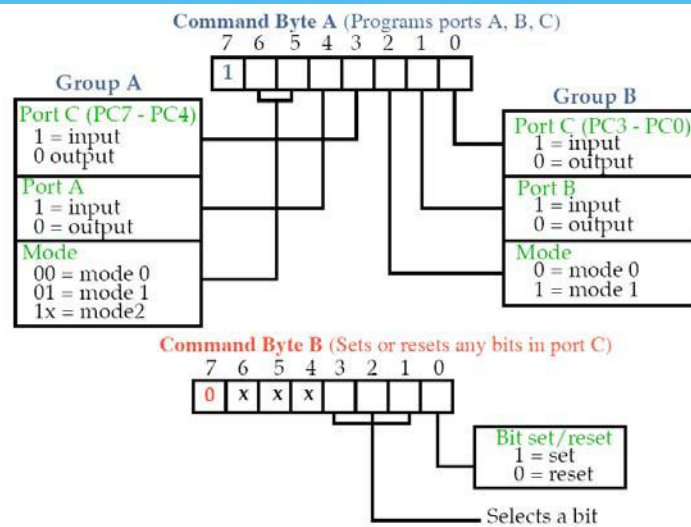
I/O Port Assignments

| A_1 | A_0 | Function |
|-------|-------|------------------|
| 0 | 0 | Port A |
| 0 | 1 | Port B |
| 1 | 0 | Port C |
| 1 | 1 | Command Register |

Interfacing the 82C55 PPI to the low bank of the 80386SX



Programming the 82C55



82C55: Mode 0 Operation

4x4 keyboard matrix interface

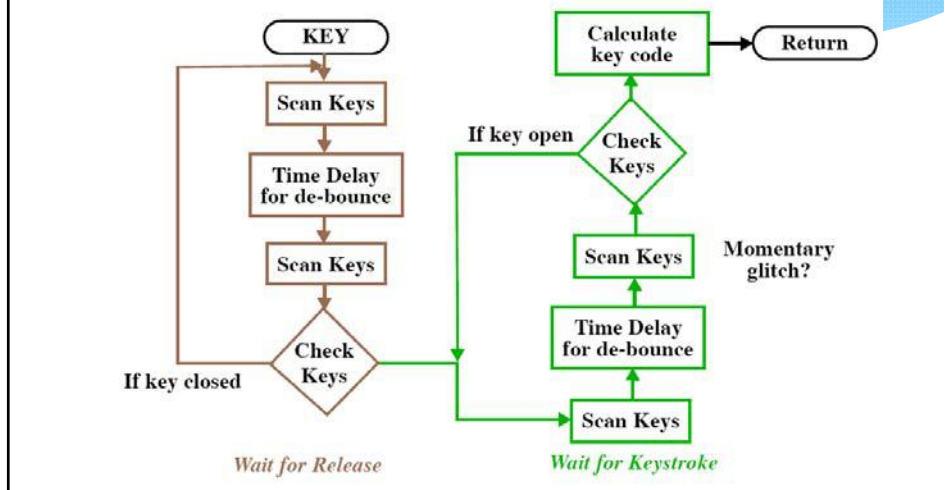
The diagram illustrates the connection of an 82C55 PPI to a 4x4 keyboard matrix. The 82C55 is configured in Mode 0, where all four ports (A, B, C, and D) are used as simple input/output lines. The keyboard matrix is a 4x4 grid of switches. The rows are connected to the 82C55 ports: Row₀ to Port A (A₀-A₃), Row₁ to Port B (B₀-B₃), Row₂ to Port C (C₀-C₃), and Row₃ to Port D (D₀-D₃). The columns are connected to the 82C55 pins: Col₀ to A₄, Col₁ to A₅, Col₂ to A₆, and Col₃ to A₇. Pull-up resistors are connected to V_{CC} for each column line. The 82C55 is also connected to a 16L8 shift register, which provides the IO/M signal to the 82C55. The 82C55 is configured with IORC and IOWC as active-low signals, and the Reset pin is connected to a Reset signal. The 82C55 is also connected to a 16L8 shift register, which provides the IO/M signal to the 82C55. The 82C55 is configured with IORC and IOWC as active-low signals, and the Reset pin is connected to a Reset signal.

Example

If Port B is programmed to output 1110; what column is selected for a read and which keys/ switches can be read by Port A?

82C55: Mode 0 Operation

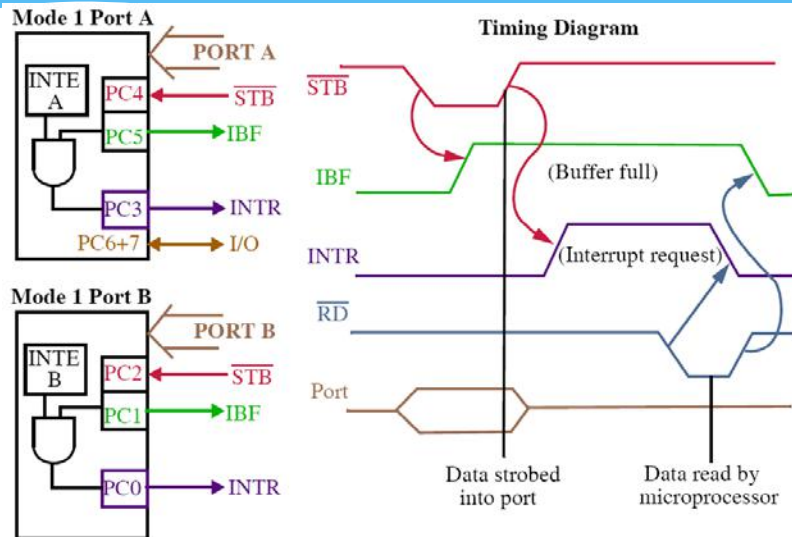
Flow chart of a keyboard-scanning procedure



82C55: Mode 1 strobed input

- * Port A and/or port B function as latching input devices. External data is stored in the ports until the microprocessor is ready.
- * Port C used for control or handshaking signals (cannot be used for data).
- * **Signal definitions for Mode 1 Strobed Input**
 - * **STB** The **strobe** input loads data into the port latch on a 0-to-1 transition
 - * **IFB** **Input buffer full** is an output indicating that the input latch contain information
 - * **INTR** **Interrupt request** is an output that requests an interrupt
 - * **INTE** The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.
 - * **PC7, PC6** The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

82C55: Mode 1 strobed input



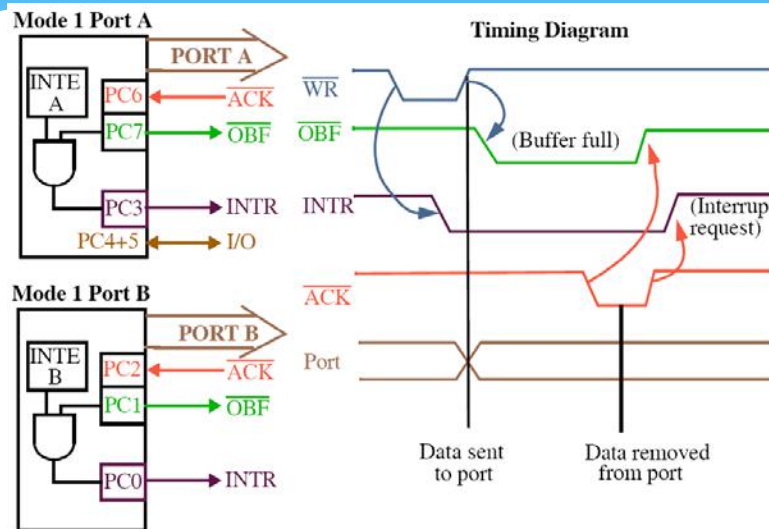
82C55: Mode 1 strobed output

- * Similar to Mode 0 output operation, except that handshaking signals are provided using port C.

- * **Signal Definitions for Mode 1 Strobed Output**

- * **OBF Output buffer full** is an output that goes low when data is latched in either port A or port B.
- * **ACK** The **acknowledge** signal causes the **OBF** pin to return to 1. This is a response from an external device.
- * **INTR Interrupt request** is an output that requests an interrupt
- * **INTE** The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.
- * **PC5, PC4** The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.

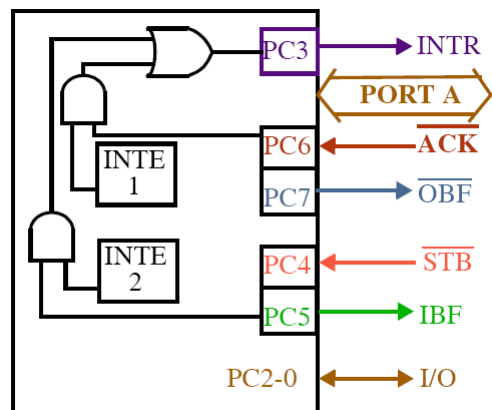
82C55: Mode 1 strobed output



82C55: Mode 2 Bi-directional operation

- * Only allowed with port A. Bi-directional based data used for interfacing two computers, GPIB interface etc.
- * **INTR Interrupt request** is an output that requests an interrupt
- * **OBF Output buffer full** is an output indicating that the output buffer contains data for the bi-directional bus
- * **ACK Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
- * **STB** The strobe input loads data into the port A latch
- * **IFB Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
- * **INTE Interrupt enable** are internal bits that enable the **INTR** pin. Bit **PC6**(**INTE1**) and **PC4**(**INTE2**)
- * **PC2, PC1 and PC0** These port C pins are general-purpose I/O pins that are available for any purpose.

82C55: Mode 2 Bi-directional Operation



- * Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.

Next Time

- * Programmable Keyboard/Display Interface

