

Distributed by:



**[www.Jameco.com](http://www.Jameco.com) ♦ 1-800-831-4242**

The content and copyrights of the attached  
material are the property of its owner.

# SN54LS245, SN74LS245

## OCTAL BUS TRANSCEIVERS

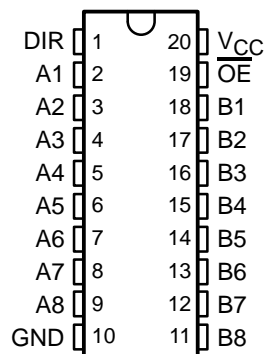
### WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce dc Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

TYPE	I <sub>OL</sub> (SINK CURRENT)	I <sub>OH</sub> (SOURCE CURRENT)
SN54LS245	12 mA	–12 mA
SN74LS245	24 mA	–15 mA

SN54LS245 . . . J OR W PACKAGE  
SN74LS245 . . . DB, DW, N, OR NS PACKAGE  
(TOP VIEW)

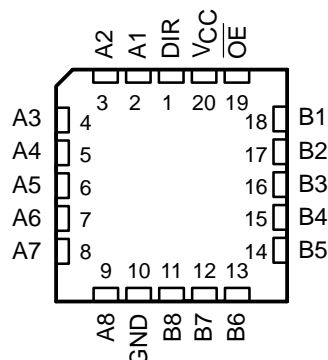


### description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{\text{OE}}$ ) input can disable the device so that the buses are effectively isolated.

SN54LS245 . . . FK PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS245N	SN74LS245N
	SOIC – DW	Tube	SN74LS245DW	LS245
		Tape and reel	SN74LS245DWR	
	SOP – NS	Tape and reel	SN74LS245NSR	74LS245
–55°C to 125°C	SSOP – DB	Tape and reel	SN74LS245DBR	LS245
	CDIP – J	Tube	SN54LS245J	SN54LS245J
		Tube	SNJ54LS245J	SNJ54LS245J
	CFP – W	Tube	SNJ54LS245W	SNJ54LS245W
	LCCC – FK	Tube	SN54LS245FK	SN54LS245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

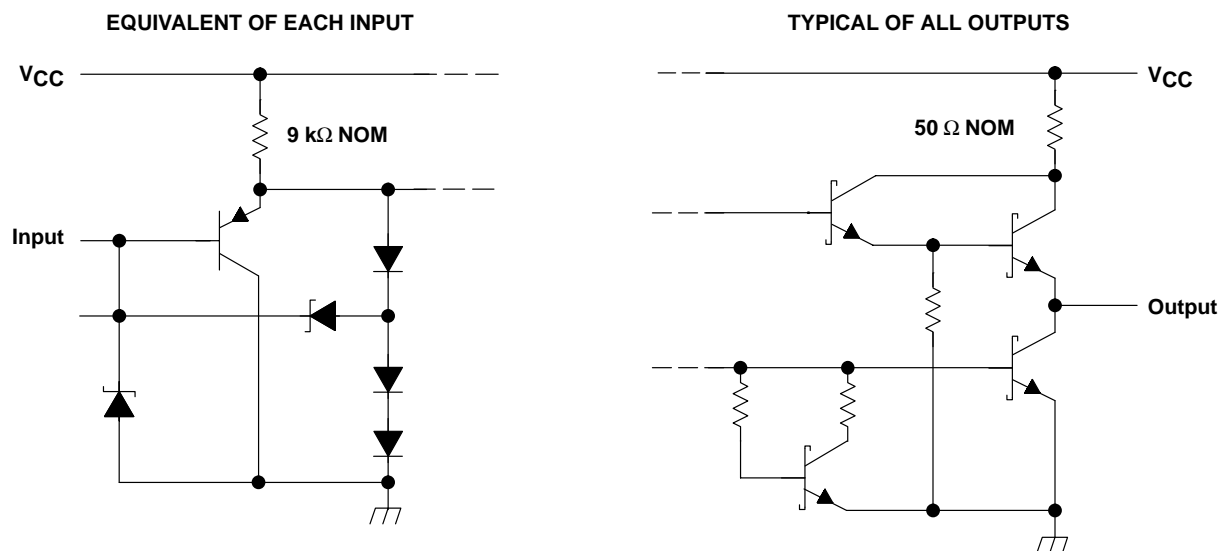
# SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

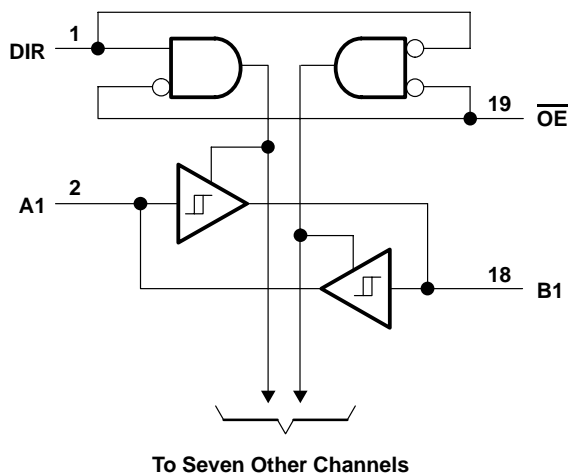
## FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## schematics of inputs and outputs



**logic diagram (positive logic)**



# SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ (see Note 1)	7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

		SN54LS245			SN74LS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C



# SN54LS245, SN74LS245

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	SN54LS245			SN74LS245			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		A or B	V <sub>CC</sub> = MIN	0.2	0.4	0.2	0.4		V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL(max)</sub>	I <sub>OH</sub> = -3 mA			2.4		3.4	V
			I <sub>OH</sub> = MAX		2	2			
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL(max)</sub>	I <sub>OL</sub> = 12 mA		0.4			0.4	V
			I <sub>OL</sub> = 24 mA					0.5	
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, OE at 2 V	V <sub>O</sub> = 2.7 V		20			20	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, OE at 2 V	V <sub>O</sub> = 0.4 V		-200			-200	μA
I <sub>I</sub>	Input current at maximum input voltage	A or B	V <sub>I</sub> = 5.5 V		0.1			0.1	mA
		DIR or $\overline{\text{OE}}$	V <sub>I</sub> = 7 V		0.1			0.1	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>IL</sub> = 0.4 V			-0.2			-0.2	mA
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX	-40		-225	40		-225	mA
I <sub>CC</sub>	Supply current	Total, outputs high			48	70	48	70	mA
		Total, outputs low			62	90	62	90	
		Outputs at high Z			64	95	64	95	

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

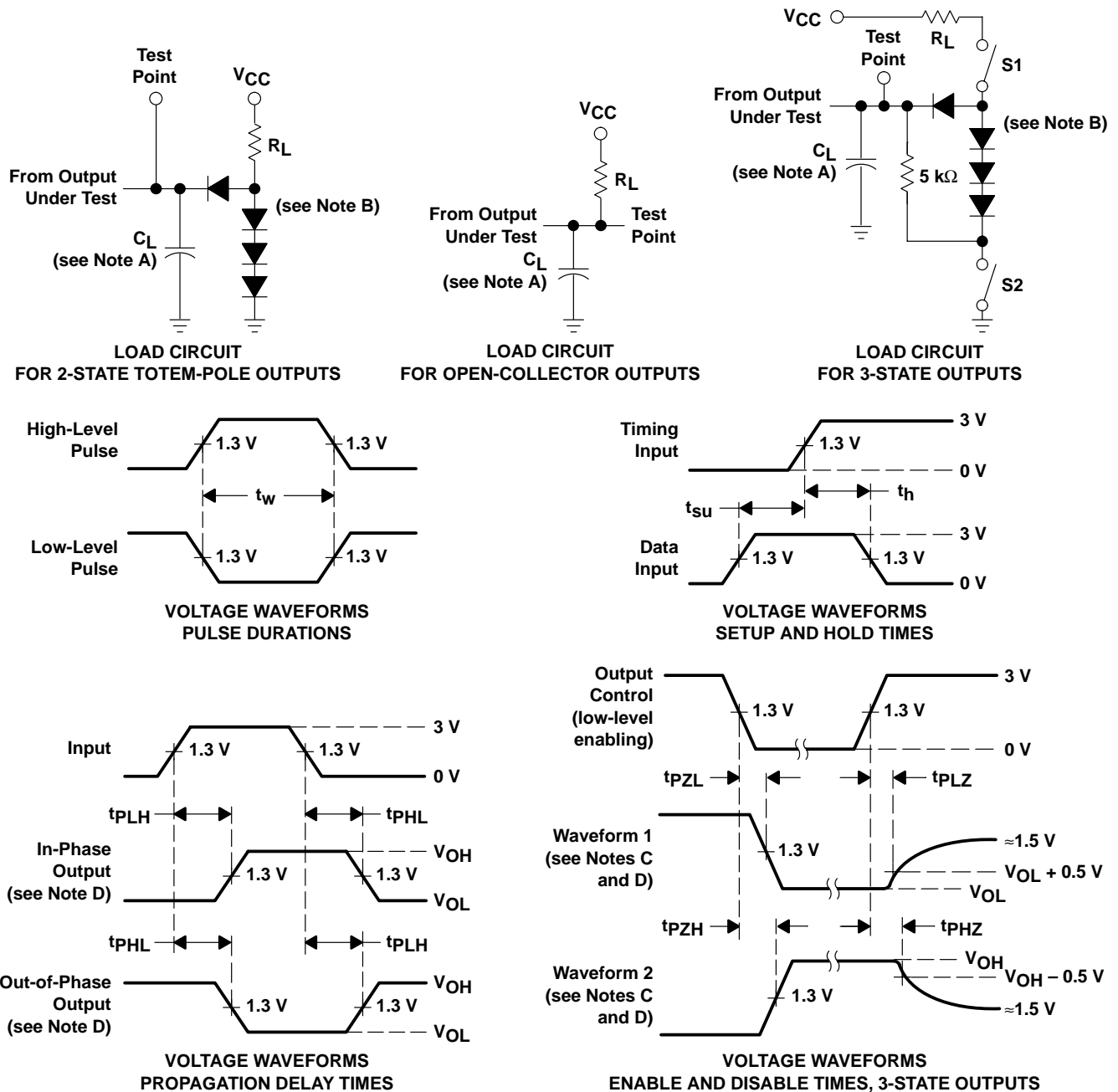
### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω			8	12	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output				8	12	
t <sub>PZL</sub>	Output enable time to low level	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω			27	40	ns
t <sub>PZH</sub>	Output enable time to high level				25	40	
t <sub>PLZ</sub>	Output disable time from low level	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 667 Ω			15	25	ns
t <sub>PHZ</sub>	Output disable time from high level				15	28	



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N3064 or equivalent.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.  
G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265