CMPE 212
Principles of Digital Design

Lecture 24

Analysis of Sequential Circuits

April 20, 2016

www.csee.umbc.edu/~younis/CMPE212/CMPE212.htm

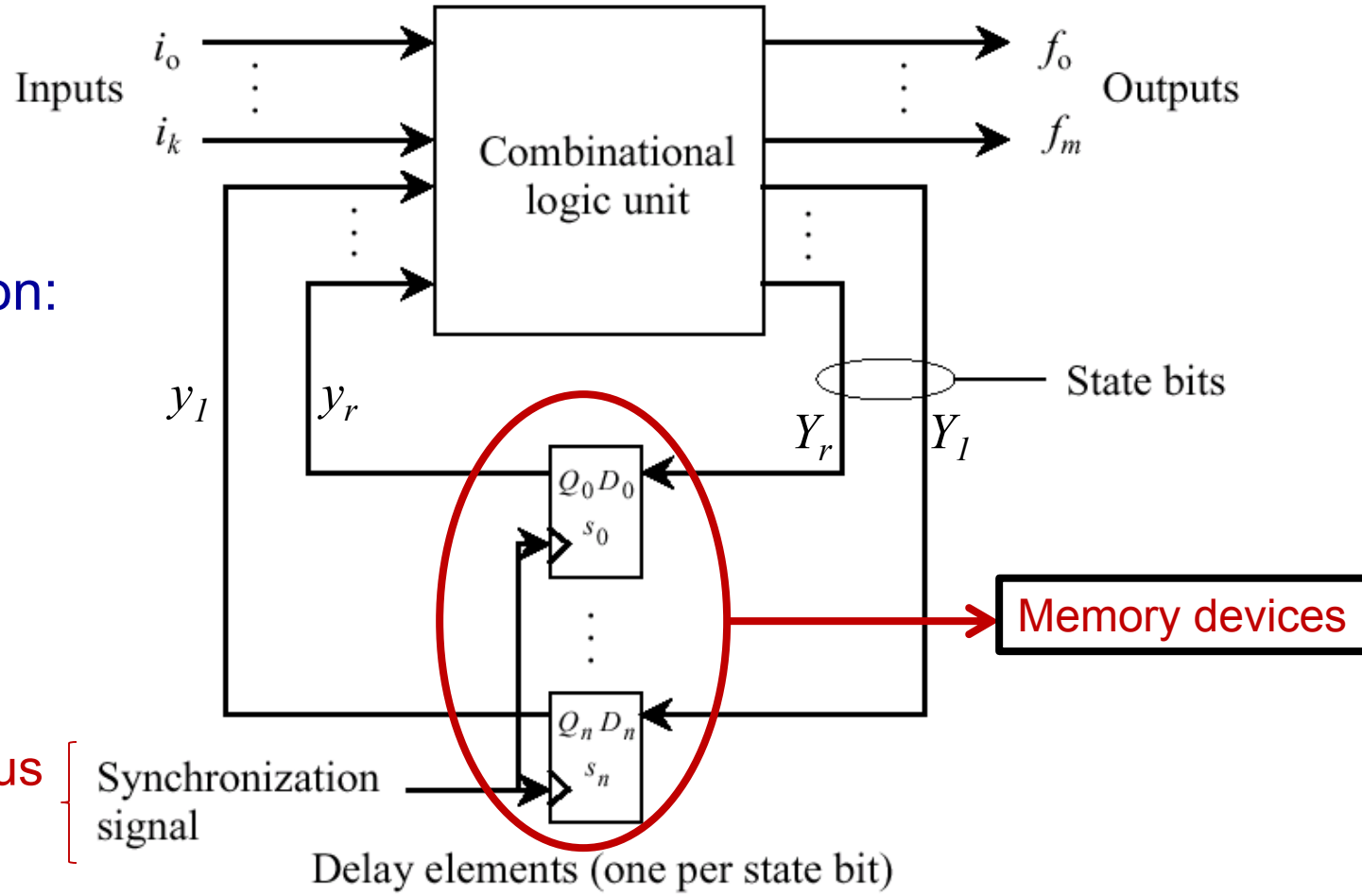
Lecture's Overview

- ***Previous Lecture***
  - ➔ Modulo-N Counters
  - ➔ Synchronous and asynchronous BCD counters
  - ➔ Counter resetting
  - ➔ Shift register as a counter
  - ➔ Multiple sequence counters
  - ➔ Fractional rate multipliers
- ***This Lecture***
  - ➔ Synchronous sequential circuits models
  - ➔ Describing the behavior of sequential circuits
  - ➔ Sequential circuits analysis

Sequential Circuit Model

Possible realization:

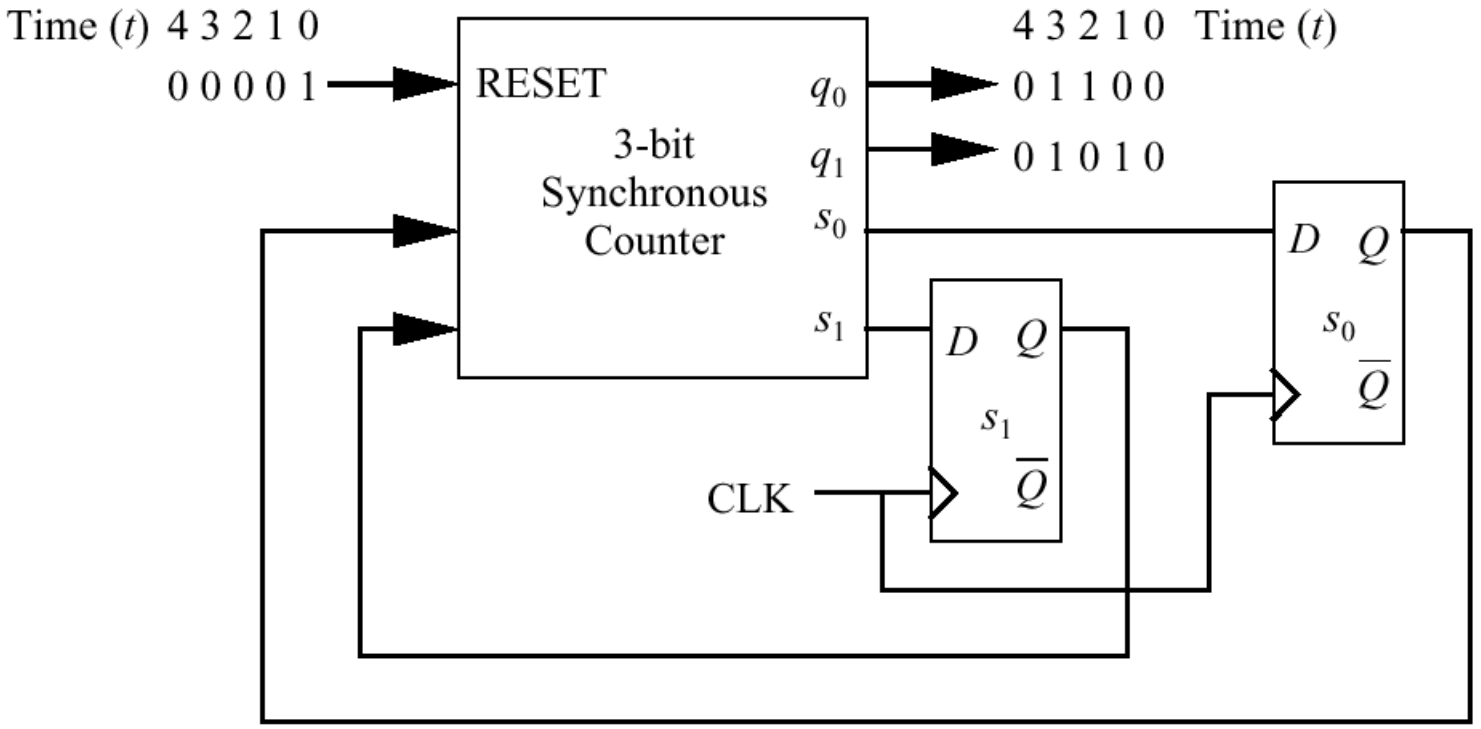
1. Mealy model
2. Moore model



- Composed of a combinational logic unit and delay elements in a feedback path, which maintains state information
- Defined by output relation to input and circuit state (values in flip-flops)

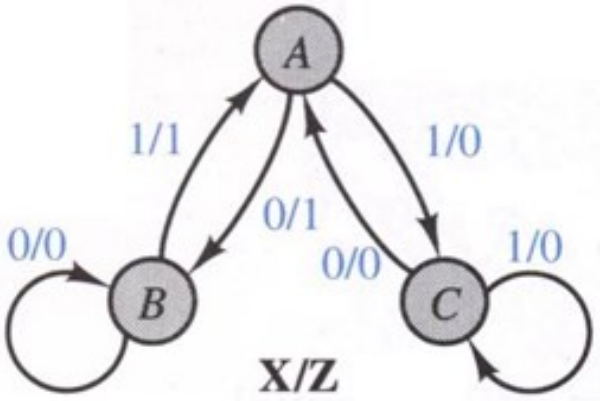
Example: FSM for Modulo-4 Counter

- Finite state machines use flip flops and combinational logic to implement the desired function
- A counter is a sequential circuit that tracks the number of ones or zeros in an input or the number of clock cycles
- A modulo-4 counter has two output lines, which take on values of 00, 01, 10, and 11 on subsequent clock cycles



* Slide is courtesy of M. Murdocca and V. Heuring

Mealy Model



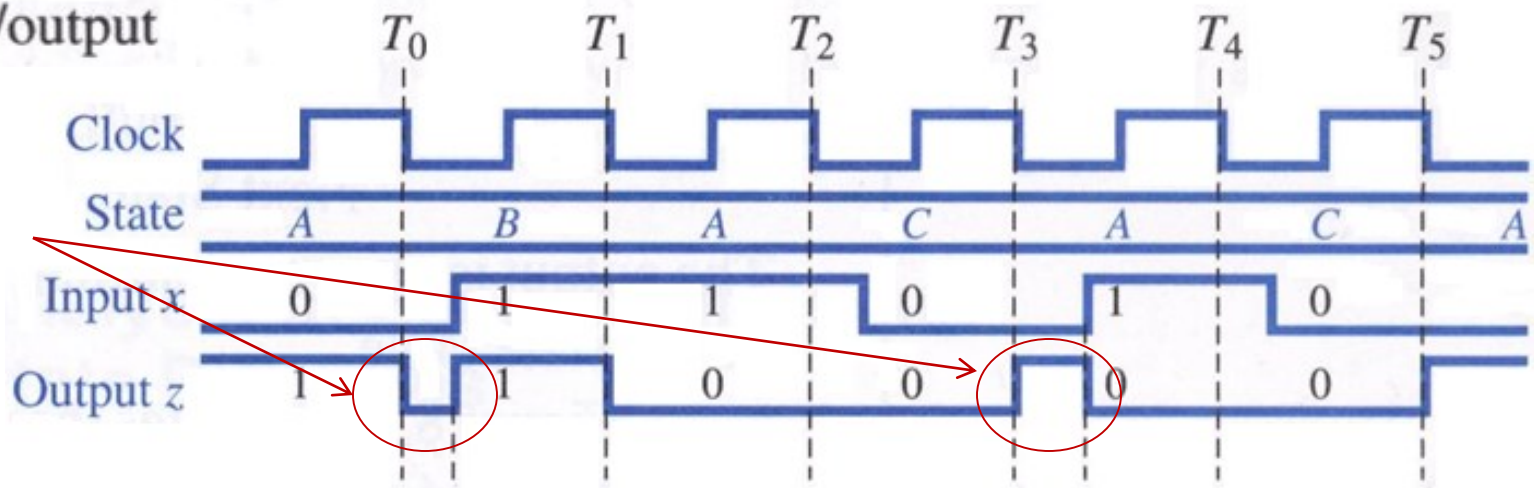
- Categorized by having the outputs to be a function of state bits and inputs

Present state	Input x = 0	Input x = 1
A	$B/1$	$C/0$
B	$B/0$	$A/1$
C	$A/0$	$C/0$

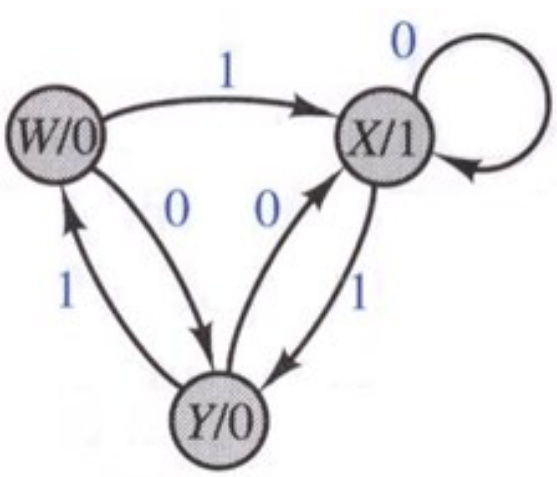
Next state/output

Time:	0	1	2	3	4	5
Present state:	A	B	A	C	A	C
Input:	0	1	1	0	1	0
Output:	1	1	0	0	0	0
Next state:	B	A	C	A	C	A

o/p depends on i/p and thus should be checked at the right time



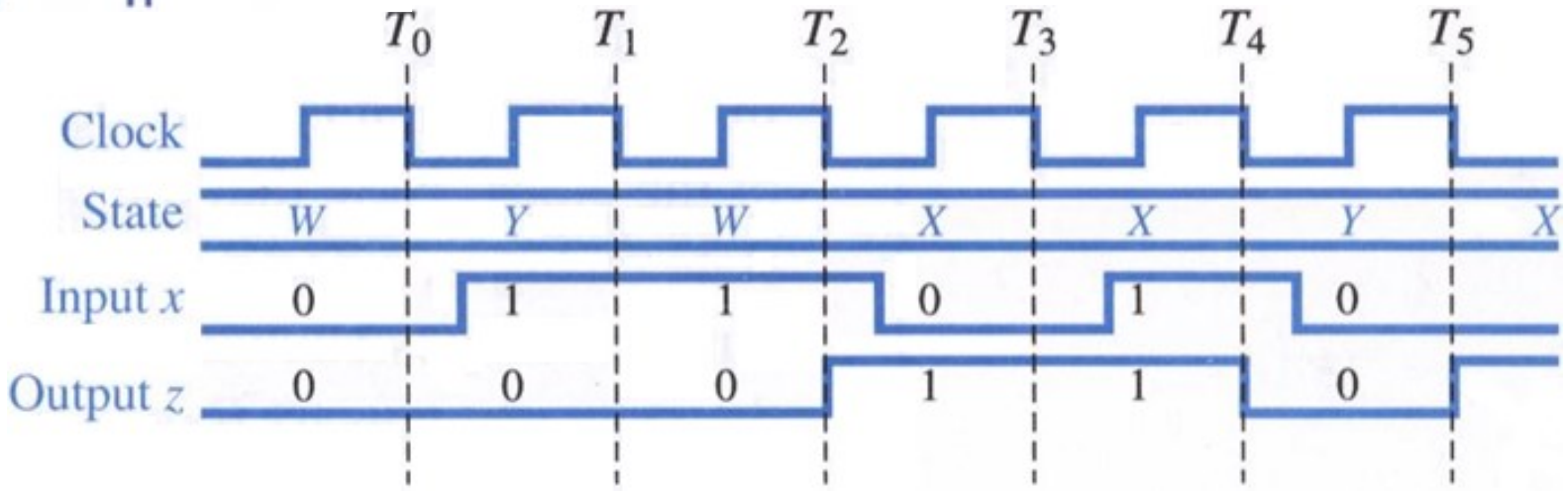
Moore Model



- Outputs is a function of ONLY the state bits
- Less design flexibility and more states (flip-flops), yet more stable output than Mealy model)

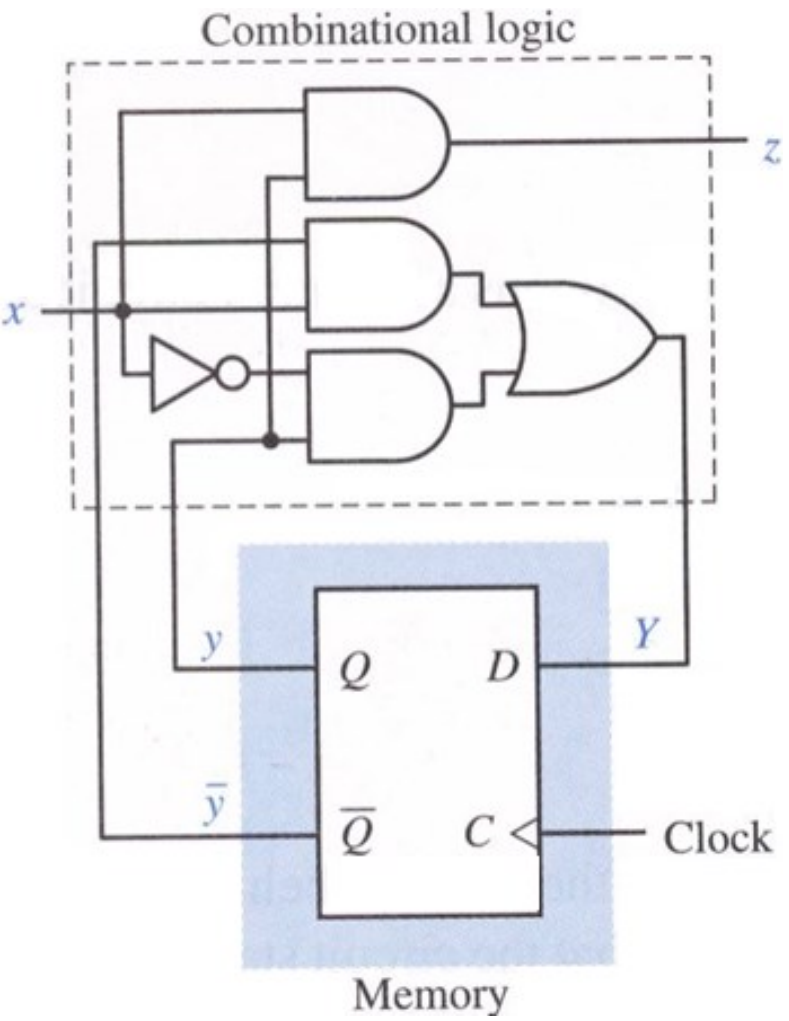
Present state	Input x = 0	Input x = 1	Outputs
W	Y	X	0
X	X	Y	1
Y	X	W	0

Time:	0	1	2	3	4	5
Present state:	W	Y	W	X	X	Y
Input:	0	1	1	0	1	0
Output:	0	0	0	1	1	0
Next State:	Y	W	X	X	Y	X

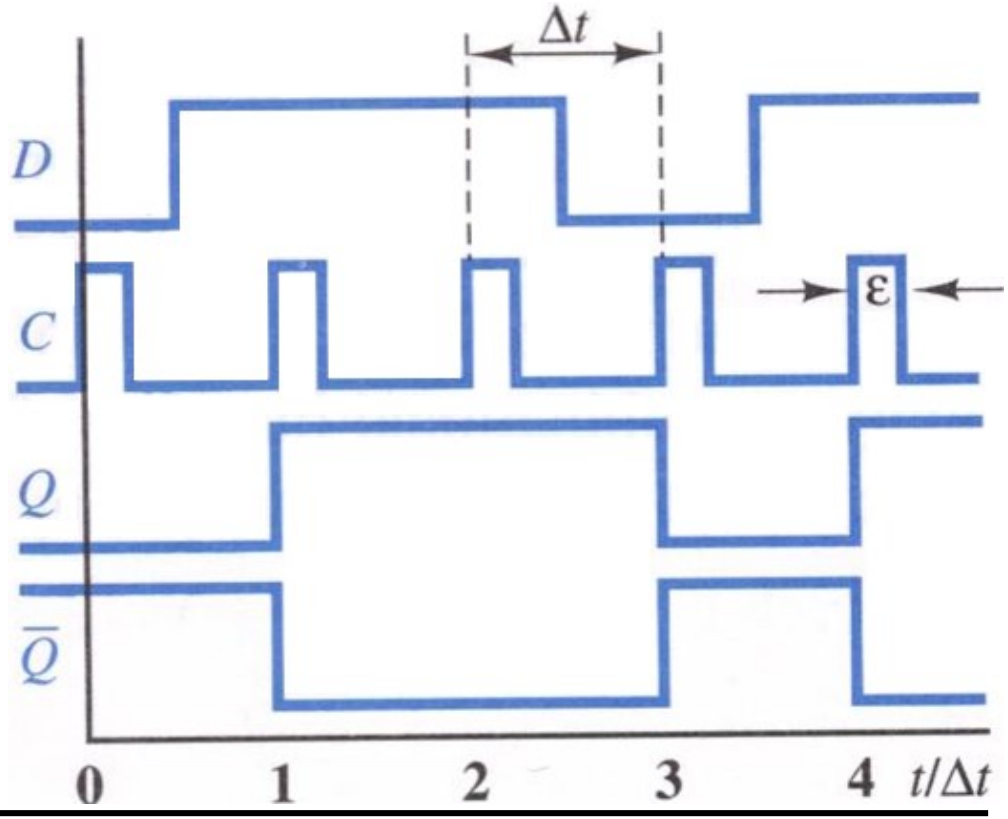


Output is synchronized with the state transition

Analyzing Sequential Circuits

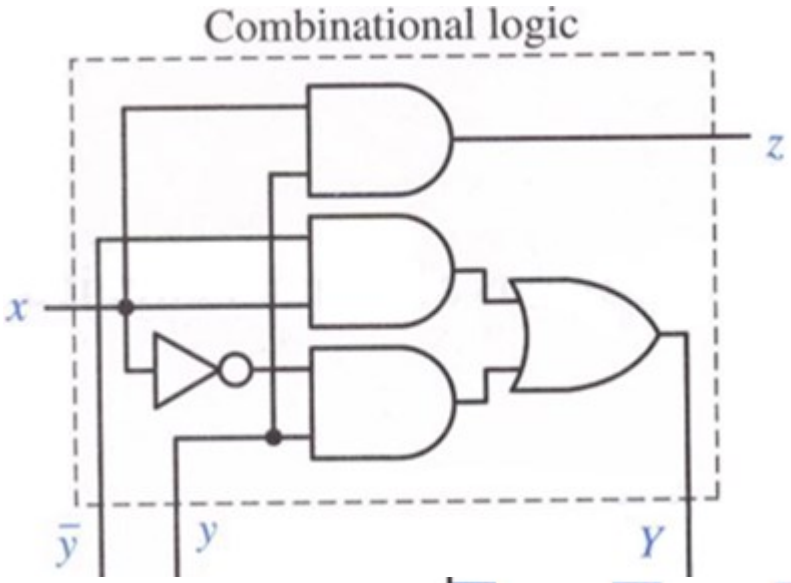


- Available: sequential circuit schematic
- Determine the circuit response to an input sequence (using relation between inputs, state variables, and outputs)
- Type: Mealy or Moore sequential circuit?



Problem: Given a circuit determine the state diagram

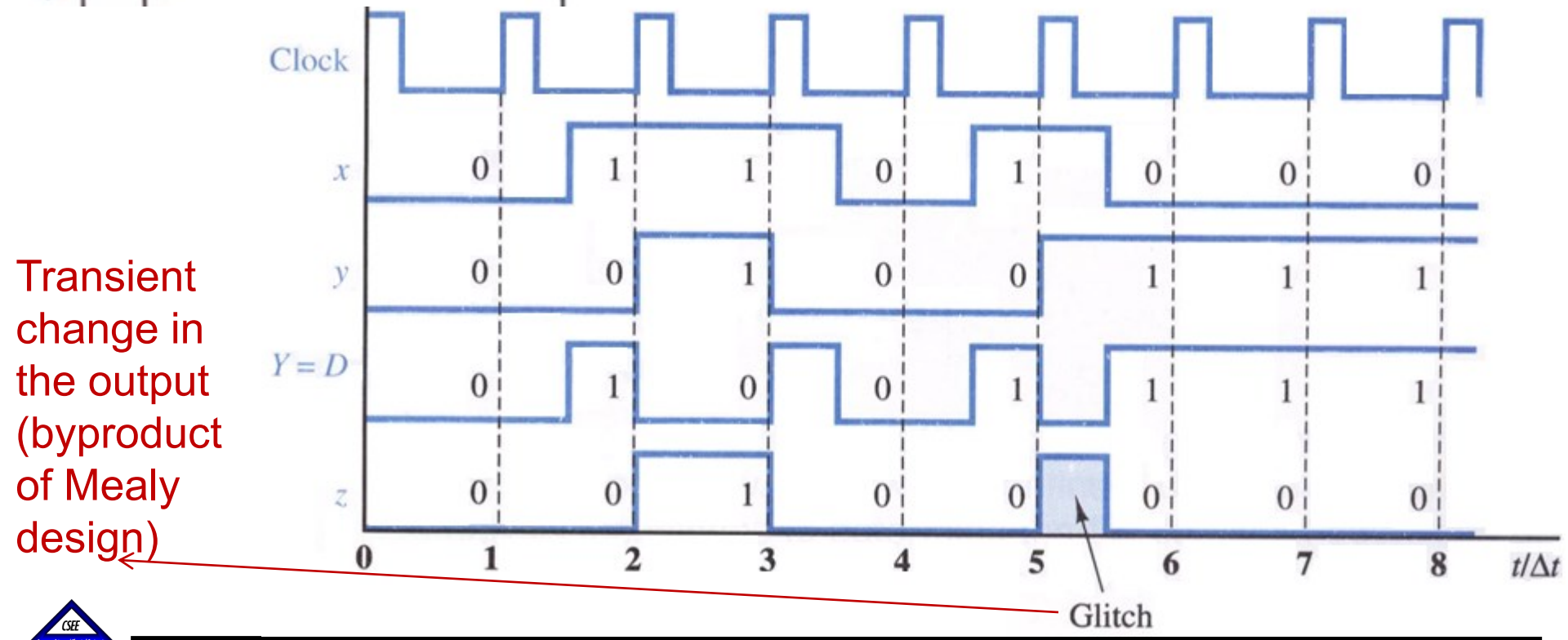
Timing Behavior Analysis



$$z = xy$$

$$Y = x\bar{y} + \bar{x}y = x \oplus y$$

x=01101000



Transient change in the output (byproduct of Mealy design)

Deriving State Diagram

- There is only 1 flip-flop ➔ there is only 2 states (0 ≡ A; 1 ≡ B)
- Notation: y^k represents $y(k\,\Delta t)$, k = integer; Δt = clock period

Present state y^k	Input x^k = 0	Input x^k = 1
0		
1		

Present state y^k	Input x^k = 0	Input x^k = 1
0	0/0	1/0
1	1/0	0/1

Next state/output

Present state	Input x^k = 0	Input x^k = 1
A	A/0	B/0
B	B/0	A/1

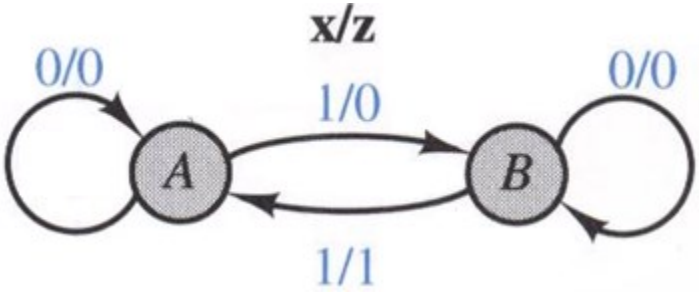
Next state/output

Reflects $Y^k = y^{k+1}$ and z^k

$$z^k = x^k y^k$$

$$Y^k = x^k \oplus y^k = y^{k+1}$$

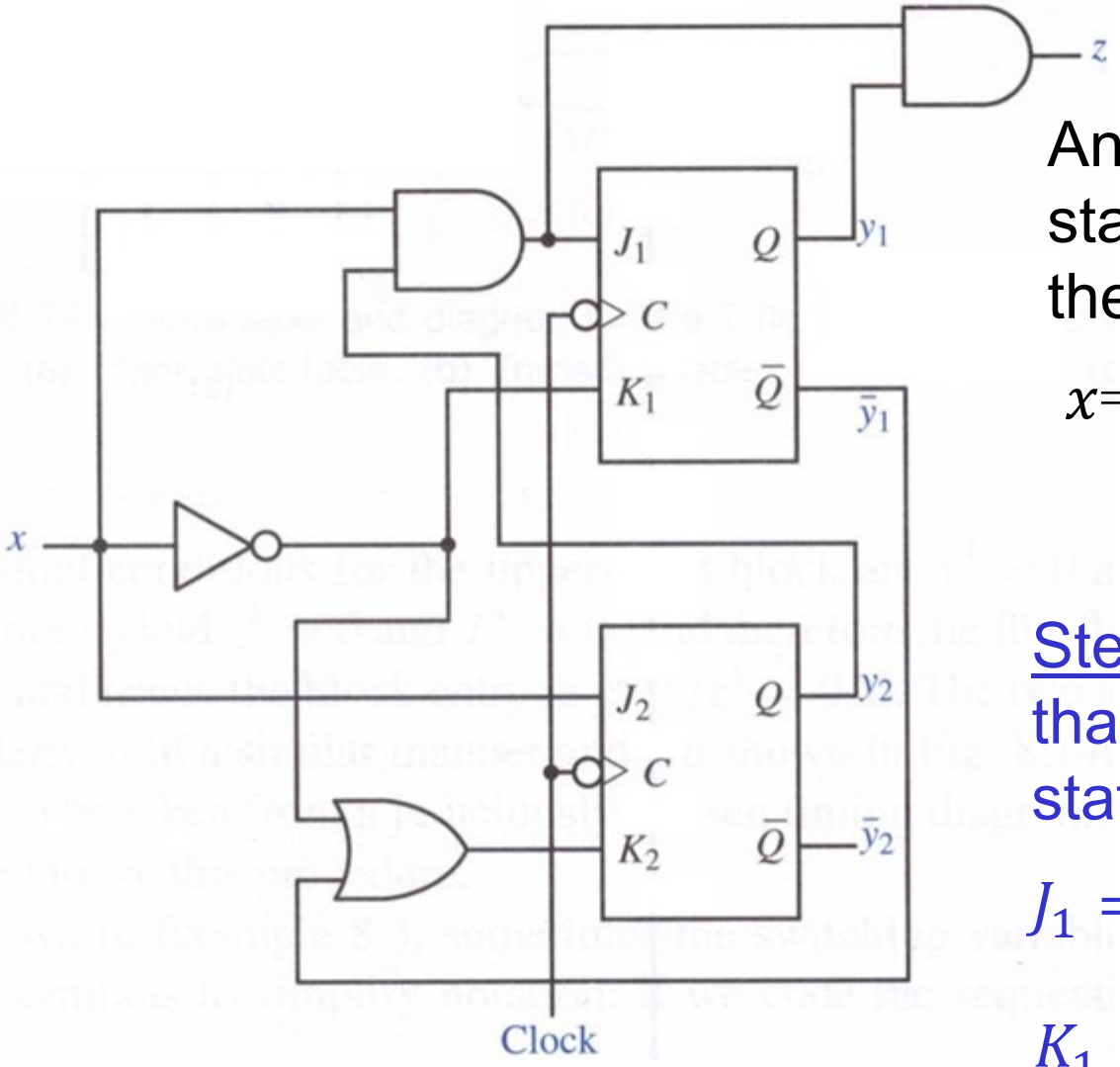
Populated using



Analysis Procedure

1) If a state table or diagram is given, proceed to steps 6 and 7, otherwise use combinational logic analysis to derive the flip-flip input and circuit output equations
2) Construct the k-maps for all logic equations from step 1
3) Combine the k-maps for all flip-flops inputs into a single map
4) Using the characteristic equations of the flip-flops, construct a next-state map
5) Combine the next-state and output maps into a single map to construct a binary state table
6) Form a binary state diagram from the binary state table, if desired.
7) Draw a timing diagram showing the clock, the given input sequence and the starting state
8) On the timing diagram, derive the waveforms for the flip-flop input(s) and state(s) for all remaining circuit input values
9) On the timing diagram derive the waveforms of the circuit output(s)

Example



Analyze the circuit (show the state and timing diagram) for the input sequence:

x=0011110, and $y_1{}^0 y_2{}^0$=10

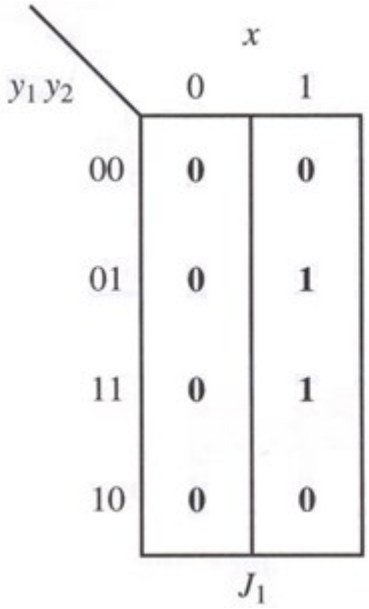
Step 1: The logic equations that describe the input and state variables are:

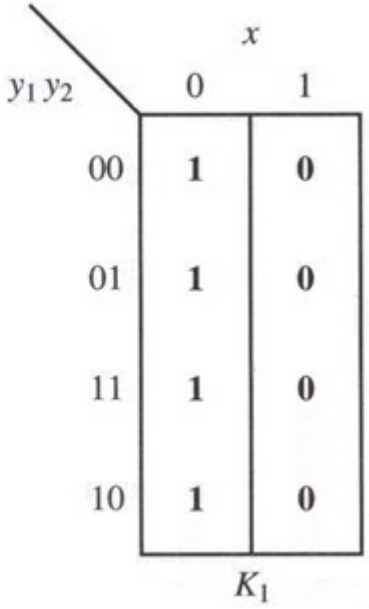
$$J_1 = xy_2, \quad J_2 = x, \quad z = xy_1y_2,$$

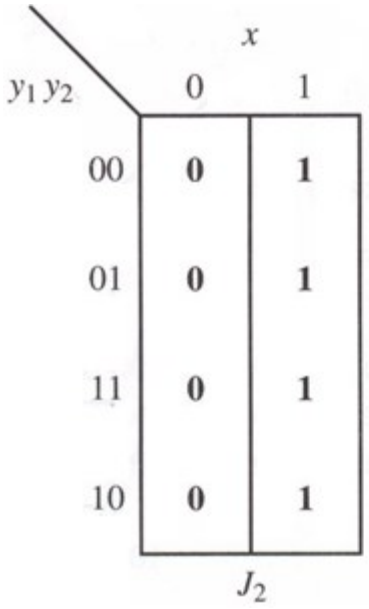
$$K_1 = \bar{x}, \quad K_2 = \bar{x} + \overline{y_1}$$

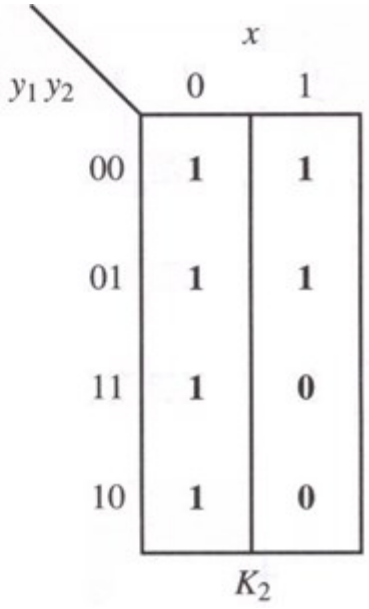
Two flip-flops ➔ 4 states sequential circuit

Step 2: k-maps for i/p & state variables



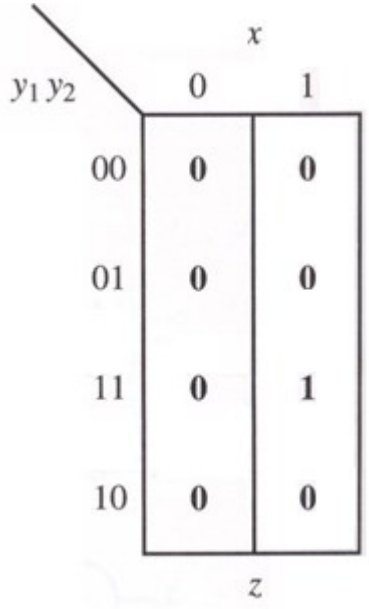






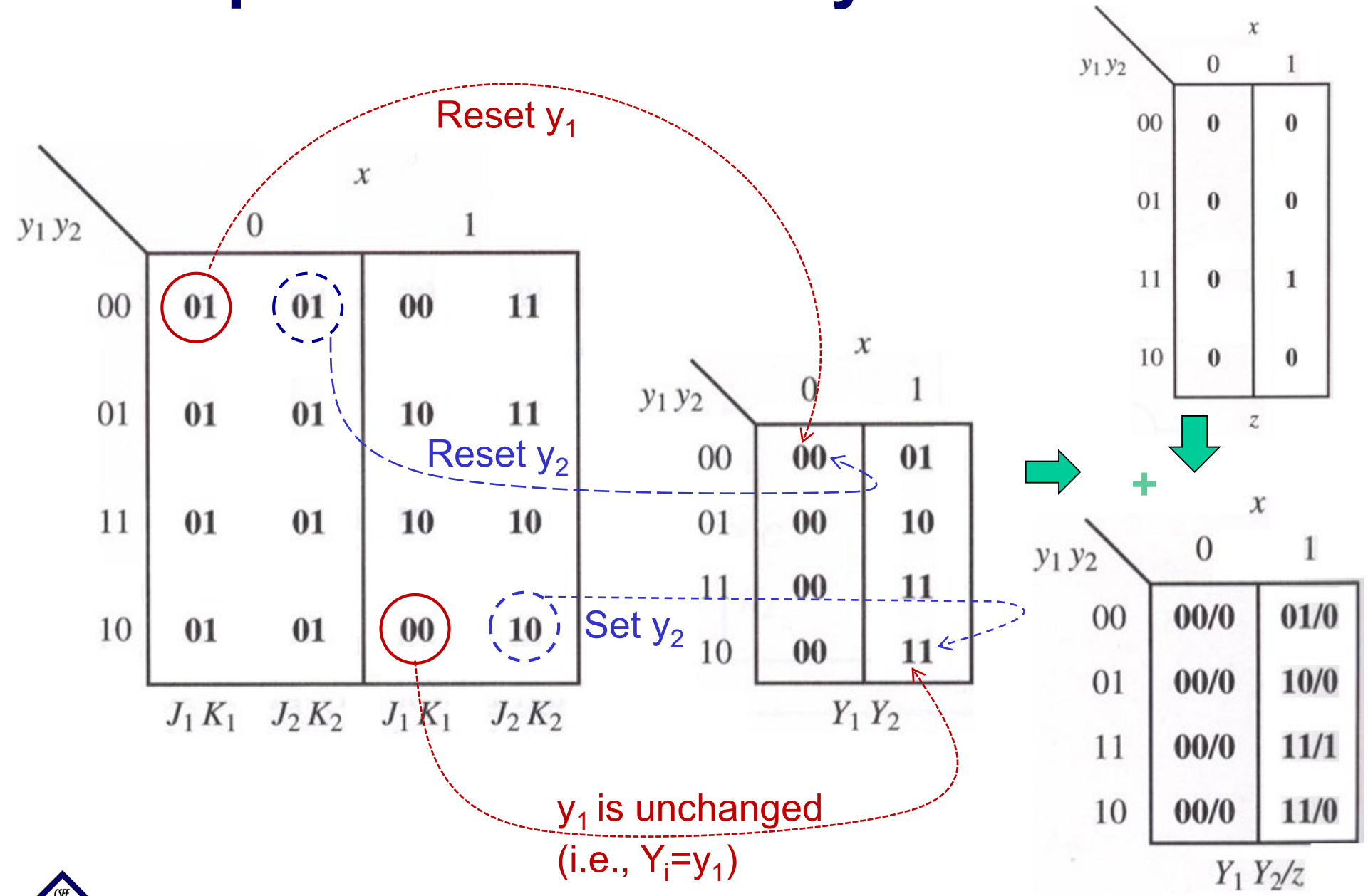
$J_1 = xy_2, \quad J_2 = x$

$K_1 = \bar{x}, \quad K_2 = \bar{x} + \overline{y_1}$

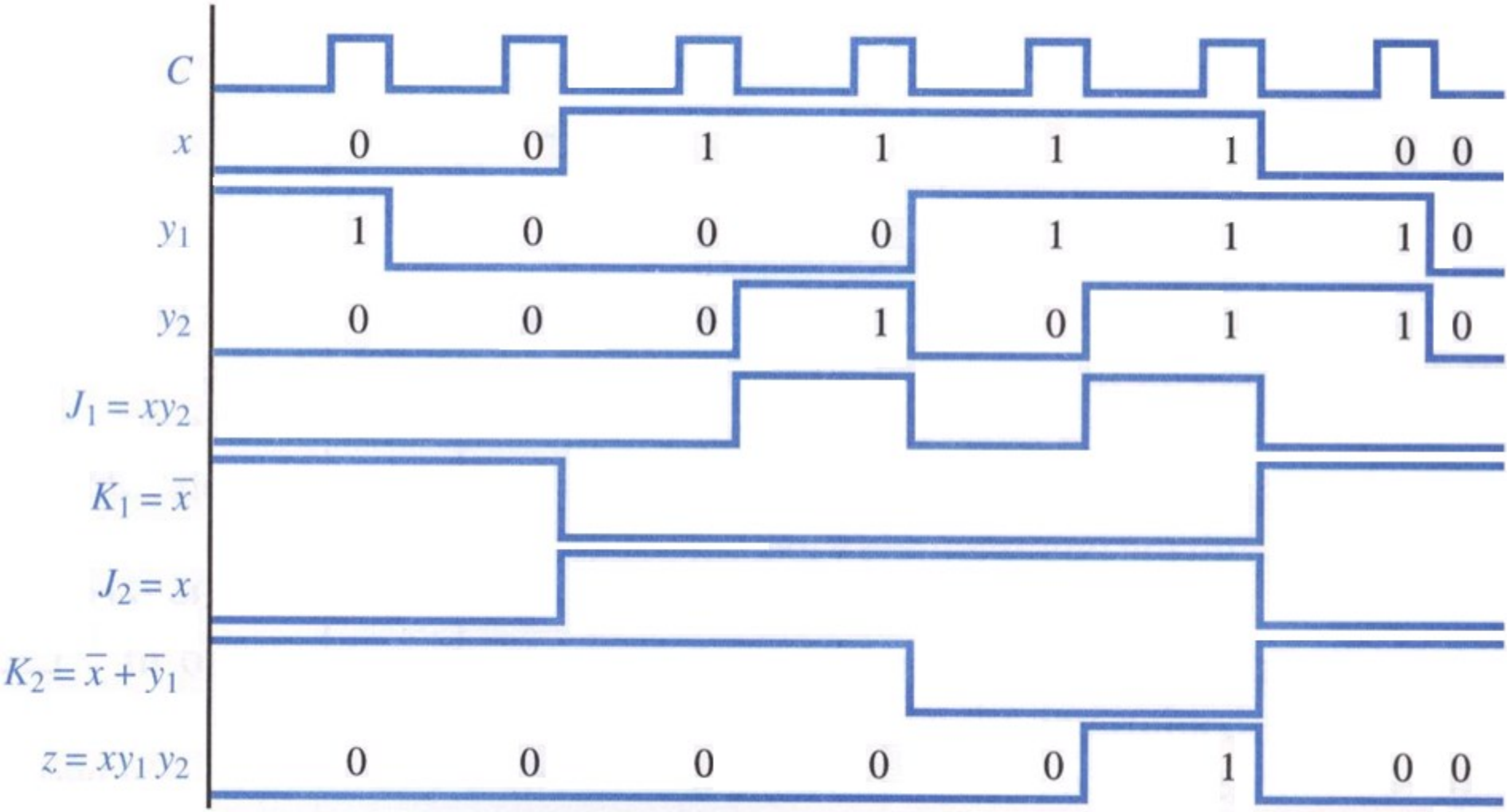


$z = xy_1y_2,$

Steps 3-5: Form Binary State Table



Steps 7-9


C
x
0 0 1 1 1 1 0 0
y1
1 0 0 0 1 1 1 0
y2
0 0 0 1 0 1 1 0
J1 = xy2
K1 = x̄
J2 = x
K2 = x̄ + ȳ1
z = xy1 y2
0 0 0 0 0 1 0 0

Conclusion

- ***Summary***
  - ➔ What does analyzing sequential circuit mean?
  - ➔ Mealy and Moore models
  - ➔ Procedure for analyzing a sequential circuit
    1. Define relation between input and state variables and output
    2. Combine the logic equations (and k-map) to define state table
    3. Draw state diagram from state table
    4. Draw timing diagram to capture behavior
- ***Next Lecture***
  - ➔Synthesis of synchronous sequential circuits

Reading assignment: Sections 8.1 – 8.2 in the textbook