CMPE 212

Spring, 2016

Project 1 Report

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1. **Project description:**

The goal of this project is to design and implement a combinational logic circuit that accepts a four-bit binary number as the input from the user and displays the decimal value up to 9, and the letter “H” for the digit beyond 9 to represent hexadecimal on the MAN74 7-segment display.

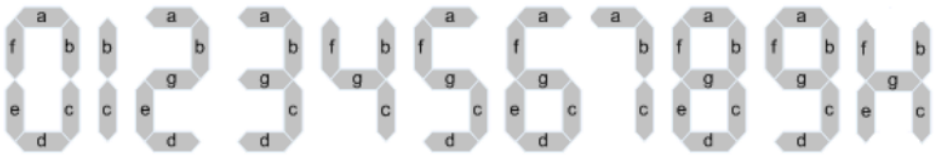
2. **Process:**

   a. **Functions:**

The truth table below had to be implemented for the seven different outputs:

Individual Segments							Display
a	b	c	d	e	f	g	
×	×	×	×	×	×		0
	×	×					1
×	×		×	×		×	2
×	×	×	×			×	3
	×	×			×	×	4
×		×	×		×	×	5
×		×	×	×	×	×	6
×	×	×					7

Individual Segments							Display
a	b	c	d	e	f	g	
×	×	×	×	×	×	×	8
×	×	×	×		×	×	9
	×	×		×	×	×	H



7-Segment Display Elements for all Numbers.

Truth Table for a 7-segment display, source: CMPE 212, Spring, 2016 Lab 6 Discussion

Using the 4 inputs, the only way to compute the logic gates required for the functions efficiently was to construct Karnaugh maps for each one of those functions.

i. Function a:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	0	1	1	1
AB	0	0	0	0
$A\bar{B}$	1	1	0	0

a = $\bar{A}C + \bar{A}\bar{B}\bar{D} + \bar{A}BD + A\bar{B}\bar{C}$

ii. Function b:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	0	1	0
AB	1	1	1	1
$A\bar{B}$	1	1	1	1

b = $A + \bar{B} + \bar{C}\bar{D} + CD$

iii. Function c:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	0
$\bar{A}B$	1	1	1	1
AB	1	1	1	1
$A\bar{B}$	1	1	1	1

c = $A + B + \bar{C} + D$

iv. Function d:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	0	1	0	1
AB	0	0	0	0
$A\bar{B}$	1	1	0	0

d = $\bar{A}\bar{B}\bar{D} + \bar{A}\bar{B}C + \bar{A}C\bar{D} + A\bar{B}\bar{C}D$

v. Function e:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	1
$\bar{A}B$	0	0	0	1
AB	1	1	1	1
$A\bar{B}$	1	0	1	1

e = $AB + AC + \bar{B}\bar{D} + C\bar{D}$

vi. Function f:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	0
$\bar{A}B$	1	1	0	1
AB	1	1	1	1
$A\bar{B}$	1	1	1	1

f = $A + B\bar{C} + B\bar{D} + \bar{C}\bar{D}$

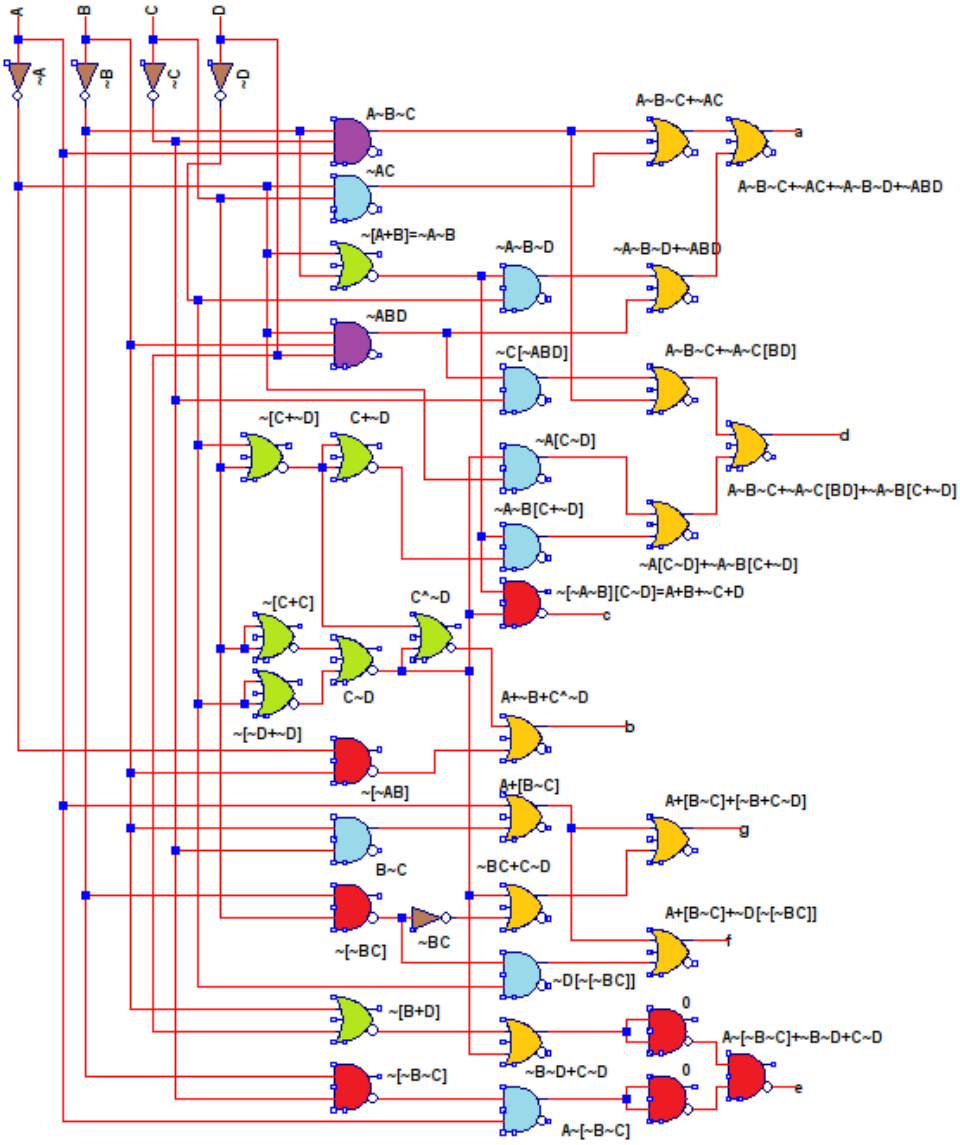
vii. Function g:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	1	1
$\bar{A}B$	1	1	0	1
AB	1	1	1	1
$A\bar{B}$	1	1	1	1

g = $A + B\bar{C} + \bar{B}C + C\bar{D}$

b. Design:

After several Boolean function manipulation, the following designed was finalized as the working blueprint for implementation:



Circuit design of a 7-segment decoder (Colors distinguish different logic gates)

The circuit was designed on LTSpice to minimize clutter and its total number of gates and IC chips was optimized through using single gates for multiple outputs. Outlier gates were replaced with extra gates left on other chips, i.e. instead of using one XOR-gate, NOR-gates were reused from other chips.

c. Verification:

The logic of the entire circuit was verified using Verilog:

```
→ proj1 git:(master) ✗ ./a.out
switches = ABCD, a, b, c, d, e, f, g

0000:  0: a=1, b=1, c=1, d=1, e=1, f=1, g=0
0001:  1: a=0, b=1, c=1, d=0, e=0, f=0, g=0
0010:  2: a=1, b=1, c=0, d=1, e=1, f=0, g=1
0011:  3: a=1, b=1, c=1, d=1, e=0, f=0, g=1
0100:  4: a=0, b=1, c=1, d=0, e=0, f=1, g=1
0101:  5: a=1, b=0, c=1, d=1, e=0, f=1, g=1
0110:  6: a=1, b=0, c=1, d=1, e=1, f=1, g=1
0111:  7: a=1, b=1, c=1, d=0, e=0, f=0, g=0
1000:  8: a=1, b=1, c=1, d=1, e=1, f=1, g=1
1001:  9: a=1, b=1, c=1, d=1, e=0, f=1, g=1
1010: 10: a=0, b=1, c=1, d=0, e=1, f=1, g=1
1011: 11: a=0, b=1, c=1, d=0, e=1, f=1, g=1
1100: 12: a=0, b=1, c=1, d=0, e=1, f=1, g=1
1101: 13: a=0, b=1, c=1, d=0, e=1, f=1, g=1
1110: 14: a=0, b=1, c=1, d=0, e=1, f=1, g=1
1111: 15: a=0, b=1, c=1, d=0, e=1, f=1, g=1
```

3. Conclusion:

After the designing processes were completed, the circuit was constructed on a breadboard, and the logic above was verified again. Due to time restrictions, not all functions were implemented and the outputs of the 7-segment LED was incomplete.