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CMSC 411 - HW 05

DATE: November 25, 2017

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1. The table below lists parameters for different direct-mapped cache designs.

	Cache Data Size	Cache Block Size
i)	64 KB	1 word
ii)	64 KB	2 words

   (a) **Question** Calculate the total number of bits required for the cache listed in the table, assuming a 32-bit address.

   Answer

   (b) **Question** What is the total number of bits if the cache is organized as a 4-way associative with one word blocks?

   Answer

2. For a pipeline with a perfect CPI=1 if no memory-access related stall, consider the following program and cache behaviors.

Data Reads Per 1000 Instructions	Data Writes Per 1000 Instructions	Instruction Cache Miss Rate	Data Cache Miss Rate	Block Size (Byte)
200	160	0.20%	2%	8

   (a) **Question** For a write-through, write-allocate cache with sufficiently large write buffer (i.e., no buffer caused stalls), what's the minimum read and write bandwidths (measured by byte-per- cycle) needed to achieve a CPI of 2?

   Answer

   (b) **Question** For a write-back, write-allocate cache, assuming 30% of replaced data cache blocks are dirty, what's the minimal read and write bandwidths needed for a CPI of 2?

   Answer

3. Using the sequences of 32-bit memory read references, given as word addresses in the following table:

6	214	175	214	6	84	65	174	64	105	85	215

For each of these read accesses, identify the binary address, the tag, the index, and whether it experiences a hit or a miss, for each of the following cache configurations. Assume the cache is initially empty.

(a) **Question** A direct-mapped cache with 16 one-word blocks.

Answer

(b) **Question** A direct-mapped cache with two-word blocks and a total size of eight blocks.

Answer

(c) **Question** A fully associative cache with two-word blocks and a total size of eight words. Use LRU replacement.

Answer

(d) **Question** A 2-way set associative cache with one-word block size and total size of 8 words, while applying LRU replacement policy.

Answer