CMPE 310
Systems Design and Programming

L6: Chapter 10 – Memory Interface

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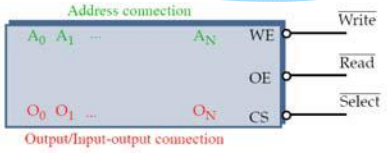
L6 Objectives

* Explore Semiconductor memories
* Three main characteristics of memory devices
* Memory address decoding

Semiconductor memories

- Almost all systems contain two basic types:
  - ***ROM:* Read-only memory**
  - ***RAM:* Read-Write memory**
- Three Memory Characteristics:
  - ***IC Memory/ Chip Capacity***
    - ***No. of bits that a chip can store***
  - ***Memory Organization***
    - 2^x locations, x = no. of address pins
    - Each location contains y bits; y = no. of data pins
    - Chip contain 2^x x y bits
  - ***Speed***
    - Access time varies → IC technology used



Example

- If you have a memory chip with 12 address pins and 8 data pins:
  - Memory organization
  - Chip capacity

- If you have a 512K chip with 8 data pins:
  - Memory organization
  - Number of address pins

Memory Interface

Memory Chips

- The number of address pins is related to the number of ***memory locations.***
  - Common sizes today are **1K to 1G locations.**
  - Therefore, between 10 and 30 address pins are present.
- The data pins are typically ***bi-directional in read-write memories.***
  - The number of data pins is related to the ***size of the memory location.***
  - For example, an 8-bit wide (byte-wide) memory device has ***8 data pins.***
  - Catalog listing of ***1K X 8 indicate a byte addressable 8K bit memory with 10 address*** pins.

Memory chips

Memory Chips

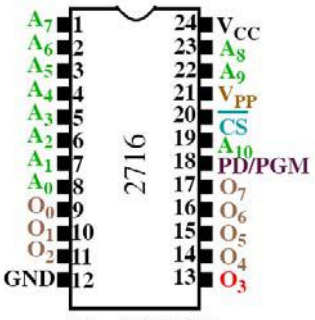
- Each memory device has at least one ***chip select*** ($\overline{CS}$) ***or chip enable*** ($\overline{CE}$) ***or select*** ($\overline{S}$) ***pin*** that enables or select the memory device.
  - This enables read and/or write operations.
  - If more than one are present, then all must be 0 in order to perform a read or write.
- Each memory device has at least one control pin.
  - ROMs: an ***output enable*** ($\overline{OE}$) ***or gate*** ($\overline{G}$) ***connection is present.***
    - The OE pin enables and disables a set of tristate buffers located in the device and must be active to read data.
  - RAMs: a ***read-write*** ($R/\overline{W}$) ***or write enable*** ($\overline{WE}$) ***and read enable*** ($\overline{OE}$) ***are*** present.
    - For dual control pin devices, it must be hold true that both are not 0 at the same time to read or write data.

Memory Interface

Memory Chips

- ***ROM:***
  - Non-volatile memory: Maintains its state when powered down.
  - There are several forms:
  - ROM: Factory programmed, cannot be changed. Older style.
  - PROM: Programmable Read-Only Memory.
    - Field programmable but only once. Older style.
  - EPROM: Erasable Programmable Read-Only Memory.
    - Reprogramming requires up to 20 minutes of high-intensity UV light exposure.
- **Flash (EEPROM): Electrically Erasable Programmable ROM.**
  - Also called **EAROM (Electrically Alterable ROM) and NOVRAM (NOn-Volatile** RAM).
  - Writing is much slower than a normal RAM.
  - Used to store setup information, e.g. video card on computer systems.
  - Can be used to replace EPROM for BIOS ROM memory.

Intel 2716 EPROM

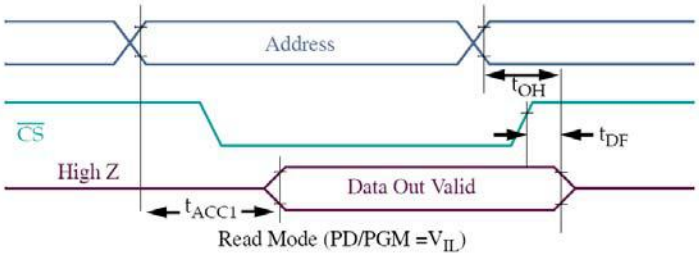


2K x 8 EPROM

V_{pp} is used to program the device by applying 25V and pulsing PGM while holding $\overline{CS}$ high

Pin(s)	Function
A_0-A_{10}	Address
PD/PGM	Power down/Program
$\overline{CS}$	Chip Select
O_0-O_7	Outputs

2716 Timing diagram



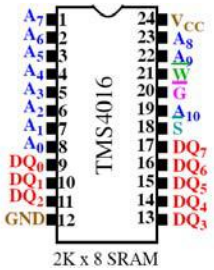
Sample of the data sheet for the 2716 A.C. Characteristics.

Symbol	Parameter	Limits			Unit	Test Condition
		Min	Typ.	Max		
t_{ACC1}	Addr. to Output Delay		250	450	ns	PD/PGM= $\overline{CS}$ =V_{IL}
t_{OH}	Addr. to Output Hold	0			ns	PD/PGM= $\overline{CS}$ =V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM=V_{IL}
...	...	...	...	...	...	...

Memory Interface

SRAMs

- Data is available as long as power supplied
  - Volatile Memory: as data is lost at power down
  - ***TI TMS 4016 SRAM (2K X 8):***



2K x 8 SRAM

Pin(s)	Function
A_0-A_{10}	Address
DQ_0-DQ_7	Data In/Data Out
$\overline{S}$ ($\overline{CS}$)	Chip Select
$\overline{G}$ ($\overline{OE}$)	Read Enable
$\overline{W}$ ($\overline{WE}$)	Write Enable

- Virtually identical to the EPROM with respect to the pinout.
- However, access time is faster (250ns).
- See the timing diagrams and data sheets in text.
- Modern SRAMs used for *caches have access times as low as 10ns.*

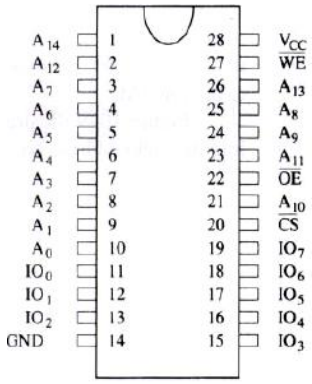
Memory Interface

SRAMs

* **62256 (32K X 8) RAM**
  * Access Time: 120-150 ns

PIN FUNCTION

A_0 - A_{14}	Addresses
IO_0 - IO_7	Data connections
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V Supply
GND	Ground

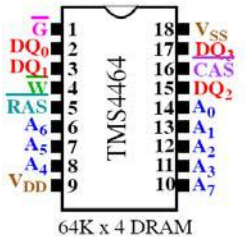


* Other sizes
  * 8K X 8
  * 128K X 8
  * 256K X 8

DRAM

* SRAMs are limited in size (up to 1M X 8).
* DRAMs are available in much larger sizes (up to 4G; 256 x 8, 4G x 1).
* Requires as little as 70 ns to access data
  * DRAMs MUST be refreshed (rewritten) every **2 to 4 ms**
* This refresh is performed by a special circuit in the DRAM which refreshes the entire memory.
  * Refresh also occurs on a normal read or write.
* The large storage capacity of DRAMs make it impractical to add the required number of address pins.
  * Instead, the address pins are *multiplexed.*

TI TMS4464 DRAM



64K x 4 DRAM

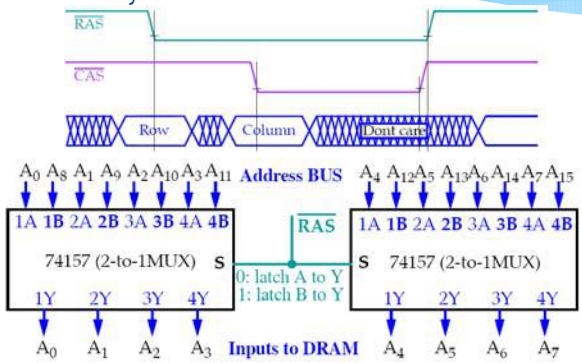
Pin(s)	Function
A_0-A_7	Address
DQ_0-DQ_3	Data In/Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

$\overline{CS}$

* Total chip capacity ➔ **256K bits** of data.
* It has **64K** addressable locations which means it needs 16 address inputs, but **it has only 8.**
  * 16 address bits can be forced into eight address pins in two 8-bit increments
  * The **row address** (A_0 - A_7) are placed on the address pins and strobed into a set of internal latches by **RAS**
  * The **column address** (A_8 - A_{15}) is then strobed in using **CAS**

TI TMS4464 DRAM timing diagram

* 16-bit address in the internal latches, which addresses the contents of one of the 4-bit memory locations.

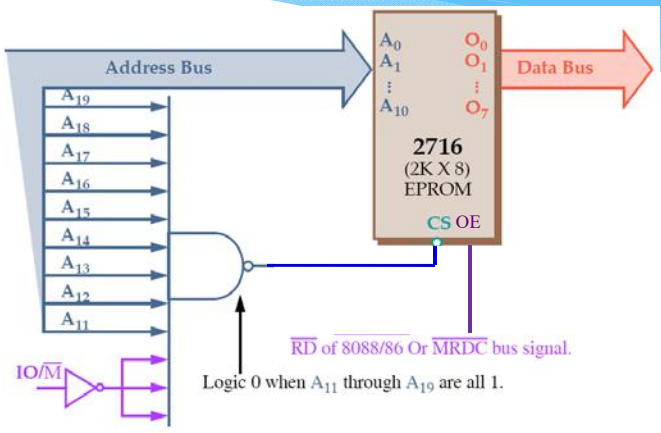


* Multiplexers used to strobe col and row addresses into the 8 address pins
* $\overline{RAS}$ signal strobes the row address into the DRAM and selects which part of the address is applied to the address inputs.

Memory address decoding

* The processor can usually address a memory space that is *much larger than the memory* space covered by an individual memory chip.
* In order to splice a memory device into the address space of the processor, decoding is necessary.
* For example, the 8088 issues ***20-bit addresses for a total of 1MB of memory address space.***
* However, the BIOS on a 2716 EPROM has only 2KB of memory and *11 address pins.*
* A decoder can be used to decode the additional 9 *address pins and allow the EPROM to be* placed in any 2KB section of the 1MB address space.

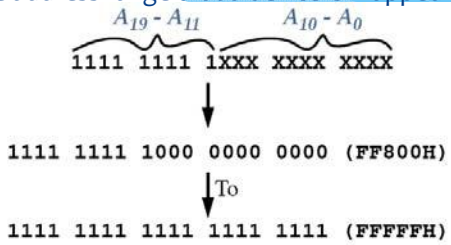
NAND gate decoder



OE connection for RD (PD/ PGM pin on chip)

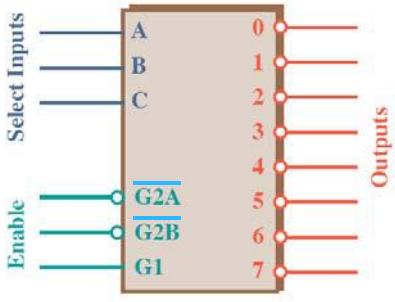
20-bit address decoding

* To determine the address range that a device is mapped into:



* This 2KB memory segment maps into the ***reset location*** of the 8086/8088 (FFFF0H).
* NAND gate decoders are not often used
  * Large fan-in NAND gates are not efficient
  * Multiple NAND gate IC's might be required to perform such decoding
  * Rather the 3-to-8 Line Decoder (74LS138) is more common.

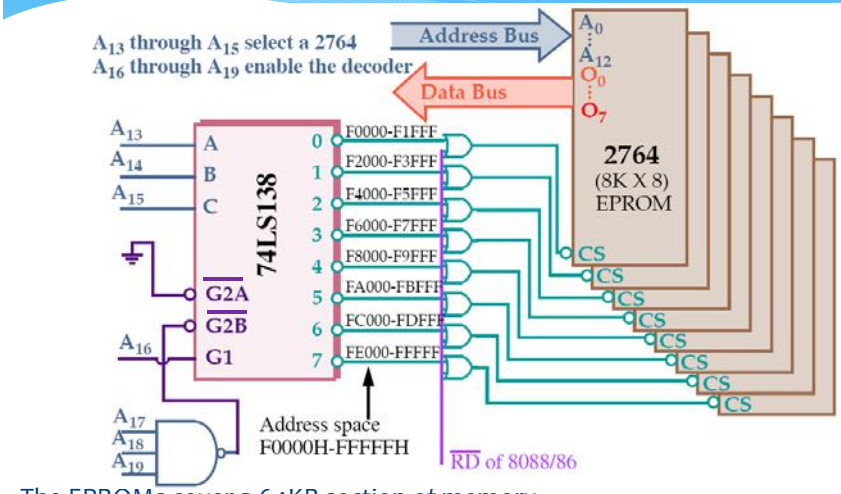
3-to-8 line decoder (74LS138)



Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

* Note that all *three Enables ($\overline{G2A}$, $\overline{G2B}$, and G1) must be active, e.g. low, low and high*, respectively.
* Each output of the decoder can be attached to an 2764 EPROM (*8K X 8*).

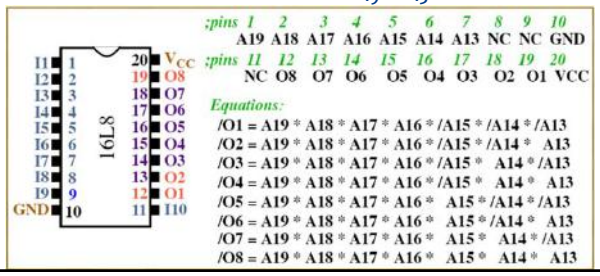
Memory address decoding



The EPROMs cover a 64KB section of memory.

Memory address decoding

- ***AMD 16L8 PAL decoder***
  - Commonly used to decode the memory address, particularly for 32-bit addresses generated by the 80386DX and above.
  - It has 10 fixed inputs (Pins 1-9, 11), two fixed outputs (Pins 12 and 19) and 6 pins that can be **either** (Pins 13-18).
- AND/NOR device with logic expressions (outputs) with up to 16 ANDed inputs and 7 ORed product terms.
  - ***Programmed to decode address lines A_{19} - A_{13} onto 8 outputs.***



Next Time

* Memory Interfacing
  * 8-bit memory interface