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## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B - OCTOBER 1975 - REVISED AUGUST 2002

- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Clock-Enable Input Has Hysteresis to** Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

## description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive relatively low-impedance loads. high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

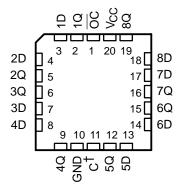
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

SN54LS373, SN54LS374, SN54S373, SN54S374...J OR W PACKAGE SN74LS373, SN74S374 . . . DW, N, OR NS PACKAGE SN74LS374 . . . DB, DW, N, OR NS PACKAGE SN74S373 . . . DW OR N PACKAGE (TOP VIEW)

				1
OC [	1	U	20	] v <sub>cc</sub>
1Q [	2		19	[] 8Q
1D [	3		18	] 8D
2D [	4		17	] 7D
2Q [	5		16	] 7Q
3Q [	6		15	] 6Q
3D [	7		14	] 6D
4D [	8		13	] 5D
4Q [	9		12	] 5Q
GND [	10		11	] C†

† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE (TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control  $(\overline{OC})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OC does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.



testing of all parameters.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

TA	PACI	KAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
		Tube	SN74LS373N	SN74LS373N
	PDIP – N	Tube	SN74LS374N	SN74LS374N
	PDIP = N	Tube	SN74S373N	SN74S373N
		Tube	SN74S374N	SN74S374N
		Tube	SN74LS373DW	LS373
		Tape and reel	SN74LS373DWR	L33/3
		Tube	SN74LS374DW	1.0074
000 to 7000	SOIC - DW	Tape and reel	SN74LS374DWR	LS374
0°C to 70°C	SOIC - DW	Tube	SN74S373DW	0070
		Tape and reel	SN74S373DWR	S373
		Tube	SN74S374DW	0074
		Tape and reel	SN74S374DWR	S374
		Tape and reel	SN74LS373NSR	74LS373
	SOP - NS	Tape and reel	SN74LS374NSR	74LS374
		Tape and reel	SN74S374NSR	74S374
	SSOP - DB	Tape and reel	SN74LS374DBR	LS374A
		Tube	SN54LS373J	SN54LS373J
		Tube	SNJ54LS373J	SNJ54LS373J
		Tube	SN54LS374J	SN54LS374J
	CDIP – J	Tube	SNJ54LS374J	SNJ54LS374J
	CDIP - J	Tube	SN54S373J	SN54S373J
		Tube	SNJ54S373J	SNJ54S373J
		Tube	SN54S374J	SN54S374J
–55°C to 125°C		Tube	SNJ54S374J	SNJ54S374J
		Tube	SNJ54LS373W	SNJ54LS373W
	CFP – W	Tube	SNJ54LS374W	SNJ54LS374W
		Tube	SNJ54S374W	SNJ54S374W
		Tube	SNJ54LS373FK	SNJ54LS373FK
	LCCC – FK	Tube	SNJ54LS374FK	SNJ54LS374FK
	LCCC - FK	Tube	SNJ54S373FK	SNJ54S373FK
		Tube	SNJ54S374FK	SNJ54S374FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



#### **Function Tables**

'LS373, 'S373 (each latch)

	INPUTS	OUTPUT	
<u>oc</u>	С	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	Х	Χ	z

'LS374, 'S374 (each latch)

	INPUTS		OUTPUT
oc	CLK	D	Q
L	$\uparrow$	Н	Н
L	$\uparrow$	L	L
L	L	Χ	$Q_0$
Н	X	X	Z

- 1Q

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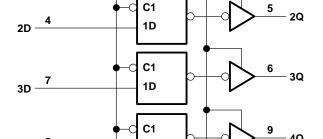
## logic diagrams (positive logic)

'LS373, 'S373
Transparent Latches

C 11

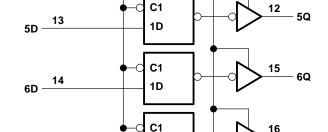
C 11

D 3



1D

4D

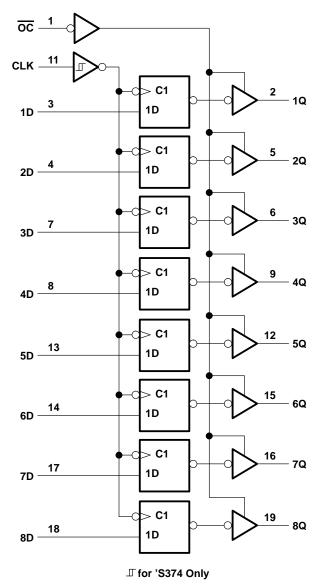


7D 17 1D 7Q 8D 18 8D 19 8Q

☐ for 'S373 Only

Pin numbers shown are for DB, DW, J, N, NS, and W packages.

## 'LS374, 'S374 Positive-Edge-Triggered Flip-Flops



## schematic of inputs and outputs

## 'LS373



'LS374



## SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† ('LS devices)

Supply voltage, V <sub>CC</sub> (see Note 1)		7 V
Input voltage, V <sub>I</sub>		7 V
Off-state output voltage		5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DB package	70°C/W
***	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, T <sub>sto</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

			,	SN54LS'			SN74LS'		UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNII	
Vcc	Supply voltage		4.5	5	5	4.75	5	5.25	V	
Vон	High-level output voltage				5.5			5.5	V	
Іон	High-level output current				-1			-2.6	mA	
loL	Low-level output current				12			24	mA	
	Pulse duration	CLK high	15			15			20	
t <sub>W</sub>		CLK low	15			15			ns	
	Data setup time	'LS373	5↓			5↓				
t <sub>su</sub>	Data setu <b>p</b> time	'LS374	20↑			20↑			ns	
4.	Data hold time	'LS373	20↓			20↓			no	
th	Data hold time	'LS374 <sup>‡</sup>	5↑			01			ns	
TA	Operating free-air temperature				125	0		70	°C	

<sup>‡</sup> The th specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).



NOTES: 1. Voltage values are with respect to network ground terminal.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED			+		SN54LS	1	SN74LS'			UNIT
	PARAMETER	TEST	CONDITION	ISI	MIN	TYP‡	MAX	MIN	TYP <sup>‡</sup>	MAX	UNII
٧ıH	High-level input voltage				2			2			V
V <sub>IL</sub>	Low-level input voltage						0.7			0.8	V
٧ıĸ	Input clamp voltage	$V_{CC} = MIN,$	I <sub>I</sub> = −18 mA				-1.5			-1.5	V
VOH	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = MAX		2.4	3.4		2.4	3.1		٧
V	Low lovel output voltage	$V_{CC} = MIN, V_{IH} = 2 V,$		$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	Low-level output voltage	V <sub>IL</sub> = V <sub>IL</sub> max		I <sub>OL</sub> = 24 mA					0.35	0.5	v
lozh	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V	V <sub>IH</sub> = 2 V,				20			20	μΑ
lozL	Off-state output current, low-level voltage applied	$V_{CC} = MAX,$ $V_{O} = 0.4 V$	V <sub>IH</sub> = 2 V,				-20			-20	μΑ
II	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V				0.1			0.1	mA
lіН	High-level input current	$V_{CC} = MAX$ ,	V <sub>I</sub> = 2.7 V				20			20	μΑ
I <sub>IL</sub>	Low-level input current	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0.4 V				-0.4			-0.4	mΑ
los	Short-circuit output current§	V <sub>CC</sub> = MAX			-30		-130	-30		-130	mA
	Cumply ourrent	V <sub>CC</sub> = MAX,		'LS373		24	40		24	40	A
lcc	Supply current		Output control at 4.5 V			27	40		27	40	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 1)

PARAMETER	FROM	то	TEST CONDITIONS		'LS373		'LS374			UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNII
f <sub>max</sub>			$R_L = 667 \Omega$ , $C_L = 45 pF$ , See Note 3				35	50		MHz
t <sub>PLH</sub>	Data	Any Q	$R_L = 667 \Omega, C_L = 45 pF,$		12	18				no
t <sub>PHL</sub>	Dala	Arry Q	See Note 3		12	18				ns
tPLH	C or CLK	Any Q	R <sub>L</sub> = 667 $\Omega$ , C <sub>L</sub> = 45 pF, See Note 3		20	30		15	28	ns
tPHL	C OI CLK	Ally Q			18	30		19	28	115
<sup>t</sup> PZH	<del>oc</del>	Any Q	$R_L = 667 \Omega, C_L = 45 pF,$		15	28		20	26	ns
t <sub>PZL</sub>	00	Arry Q	See Note 3		25	36		21	28	115
<sup>t</sup> PHZ	<del>oc</del>	Any Q	$R_1 = 667 \Omega, C_1 = 5 pF$		15	25		15	28	ns
t <sub>PLZ</sub>	5	Ally Q	KL = 007 32, CL = 5 pr		12	20		12	20	115

NOTE 3: Maximum clock frequency is tested with all outputs loaded.

fmax = maximum clock frequency

tplH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tPHZ = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level



<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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## schematic of inputs and outputs

'S373 and 'S374

## 'S373 and 'S374



# SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† ('S devices)

Supply voltage, V <sub>CC</sub> (see Note 1)		$\dots \dots \dots \ 7 \ V$
Input voltage, V <sub>I</sub>		5.5 V
Off-state output voltage		5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, T <sub>stg</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

## recommended operating conditions

				SN54S'			SN74S'		UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNII	
Vcc	CC Supply voltage			5	5.5	4.75	5	5.25	V	
Vон	High-level output voltage	-level output voltage						5.5	V	
loh	High-level output current				-2			-6.5	mA	
	Pulse duration, clock/enable	High	6			6			ns	
t <sub>W</sub>	ruise duration, clock/enable	Low	7.3			7.3				
	Data actus tima	'S373	0↓			0↓				
t <sub>su</sub>	Data setup time	'S374	5↑			5↑			ns	
4.	Data hold time	'S373	10↓			10↓				
th	Data noto time	'S374	2↑			2↑			ns	
TA	Operating free-air temperature		-55		125	0		70	°C	



<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

PARA	METER		TES	ST CONDITIONS†		MIN	TYP‡	MAX	UNIT
٧ıH						2			V
V <sub>IL</sub>								0.8	V
٧ıK		$V_{CC} = MIN,$	$I_{I} = -18 \text{ mA}$					-1.2	V
Va	SN54S'	Voo – MIN	\/ 2 \/	V: 0.8 V	Iou - MAY	2.4	3.4		V
VOH	SN74S'	$V_{CC} = MIN,$	$V_{IH} = 2 V$	$V_{IL} = 0.8 V$	IOH = MAX	2.4	3.1		V
$V_{OL}$		$V_{CC} = MIN,$	V <sub>IH</sub> = 2 V,	$V_{IL} = 0.8 V$ ,	$I_{OL} = 20 \text{ mA}$			0.5	V
lozh		$V_{CC} = MAX$ ,	V <sub>IH</sub> = 2 V,	V <sub>O</sub> = 2.4 V				50	μΑ
lozL		$V_{CC} = MAX$ ,	V <sub>IH</sub> = 2 V,	$V_0 = 0.5 V$				-50	μΑ
II		$V_{CC} = MAX$ ,	V <sub>I</sub> = 5.5 V					1	mA
lιΗ		$V_{CC} = MAX$ ,	V <sub>I</sub> = 2.7 V					50	μΑ
IIL		$V_{CC} = MAX$ ,	V <sub>I</sub> = 0.5 V					-250	μΑ
los§		$V_{CC} = MAX$				-40		-100	mA
				Outputs high				160	
			'S373	Outputs low				160	
				Outputs disable	d			190	
ICC		$V_{CC} = MAX$		Outputs high				110	mA
		J.,	'S374	Outputs low				140	
			33/4	Outputs disable	d			160	
				CLK and OC at	4 V, D inputs at 0 V			180	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 2)

PARAMETER	FROM	то	TEST CONDITIONS		'S373		'S374			UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f <sub>max</sub>			$R_L = 280 \Omega$ , $C_L = 15 pF$ , See Note 3				75	100		MHz
t <sub>PLH</sub>	Data	Any Q	$R_L = 280 \Omega, C_L = 15 pF,$		7	12				ns
<sup>t</sup> PHL	Dala	Ally Q	See Note 3		7	12				115
t <sub>PLH</sub>	C or CLK	Any Q	$R_L = 280 \Omega, C_L = 15 pF,$		7	14		8	15	ns
t <sub>PHL</sub>	C OI CLK	Ally Q	See Note 3		12	18		11	17	115
<sup>t</sup> PZH	<del>oc</del>	Any Q	$R_L = 280 \Omega, C_L = 15 pF,$		8	15		8	15	ns
t <sub>PZL</sub>	0	Ally Q	See Note 3		11	18		11	18	115
<sup>t</sup> PHZ	<del>oc</del>	Any Q	$R_1 = 280 \Omega, C_1 = 5 pF$		6	9		5	9	ns
<sup>t</sup> PLZ	UC	Ally Q	N <sub>L</sub> = 200 32, O <sub>L</sub> = 3 μr		8	12		7	12	115

NOTE 3. Maximum clock frequency is tested with all outputs loaded.

f<sub>max</sub> = maximum clock frequency

tpLH = propagation delay time, low-to-high-level output

tphl = propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level



<sup>&</sup>lt;sup>‡</sup> All typical values are at  $V_{CC}$ = 5 V,  $T_A$  = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

# PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. S1 and S2 are closed for tpLH, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
  - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  - F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_{O} \approx 50 \Omega$ ,  $t_{f} \leq 1.5$  ns,  $t_{f} \leq 2.6$  ns.
  - G. The outputs are measured one at a time with one input transition per measurement.
  - H. All parameters and waveforms are not applicable to all devices .

Figure 1. Load Circuits and Voltage Waveforms



## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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### PARAMETER MEASUREMENT INFORMATION **SERIES 54S/74S DEVICES**

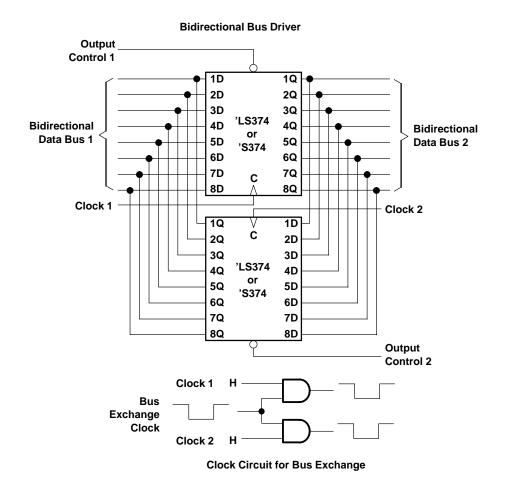


- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. S1 and S2 are closed for tpLH, tpHL, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
  - E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq$  7 ns for Series 54/74 devices and  $t_r$  and  $t_f \le 2.5$  ns for Series 54S/74S devices.
  - F. The outputs are measured one at a time with one input transition per measurement.
  - G. All parameters and waveforms are not applicable to all devices .

Figure 2. Load Circuits and Voltage Waveforms



## TYPICAL APPLICATION DATA



Expandable 4-Word by 8-Bit General Register File





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