1. What happens when the HOLD input to the 8086/8088 is placed at its logic 1 level?

2. What four housekeeping chores are provided by the 8284A clock generator?

3. How many MIPS is the 8086/8088 capable of obtaining when operated with a 10 MHz clock?

4. What main function is provided by the 8288 bus controller when used with 8086/8088 maximum mode operation?

5. Why are memory address decoders important?

6. Modify the NAND gate decoder in Figure 10.13 to select the memory for address range DF800H-DFFFFH. [Note: Must draw circuit to receive full credit]

7. Modify the circuit of the Figure 10.15 to address memory range 70000H-7FFFFH. [Note: Must draw circuit to receive credit]

8. Modify the circuit of Figure 10.19 by rewriting the PLD program to address memory at locations A0000H-BFFFFH for the ROM. [Note: Must draw circuit to receive credit]

9. Develop a 16-bit wide memory interface that contains SRAM memory at locations 200000H-21FFFFH for the 80386SX. [Note: Must draw circuit to receive credit]