

1 Background

Create a synthesizable sequential module that accepts two 4-bit inputs x and y and generates a 4-bit output q based on x and a function selector s. The selector should select the bit-wise operator to be applied to x and y in order to produce q. The output q should be a registered output, and so the module should accept clk signal clk. There should be no unnecessary cycle delays from input to the output.

- 0: and
- 1: or
- 2: xor
- 3: nand
- 4: nor

2 Implementation

The output 'q' was generated in a case block with bitwise operators applied to the inputs 'x' and 'y'. The module implementation along with its testbench can be found in the 'scripts' directory. A sample of the waveform generated is provided:

A table of the inputs and outputs generated in the test bench is also generated:

x	op	y	q	s
1001	&	1010	1000	0
0000	&	1010	0000	0
1110	&	1010	1010	0
1001		1010	1011	1
0101		1010	1111	1
1110		1010	1110	1
1001	^	1010	0011	2
1111	^	1010	0101	2
1110	^	1010	0100	2
1001	~&	1010	0111	3
0000	~&	1010	1111	3
1110	~&	1010	0101	3
1001	~	1010	0100	4
0101	~	1010	0000	4
1110	~	1010	0001	4

x op y q s

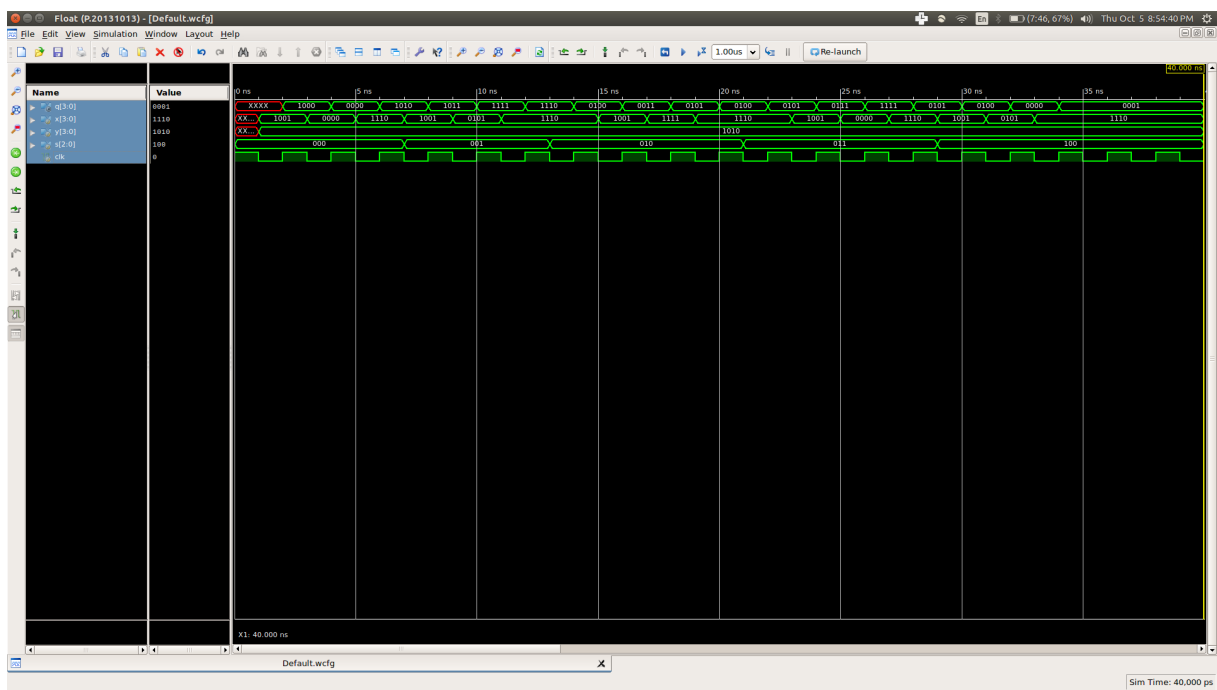


Figure 1: Waveform Generated from Part 4 Test Bench