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CMSC 411 - HW 05

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1. The table below lists parameters for different direct-mapped cache designs.

	Cache Data Size	Cache Block Size
i)	64 kB	1 word
ii)	64 kB	2 words

(a) **Question** Calculate the total number of bits required for the cache listed in the table, assuming a 32-bit address.

Answer

Using:

$$2^{\text{n}} \times (\text{valid field size} + \text{tag size} + \text{block size})$$

where

$$\begin{aligned} \text{tag size} &= 32 - (n + m + 2) \\ n &= log_2(\text{cache data size}) \\ m &= log_2(\text{block size}) \\ \text{valid bits} &= 1 \end{aligned}$$

For design i) total number of bits required:

$$\begin{aligned} n &= log_2(64\text{ kB}) \\ &= 16 \\ m &= log_2(2) \\ &= 1 \\ \text{tag size} &= 32 - (16 + 1 + 2) \\ &= 13 \\ \text{valid bits} &= 1 \\ \text{total bits} &= 2^{16} \times (1 + 13 + 2) \\ &= 2^{20} \text{ bits} \end{aligned}$$

(b) **Question** What is the total number of bits if the cache is organized as a 4-way asso-

ciative with one word blocks?

Answer

2. For a pipeline with a perfect CPI = 1 if no memory-access related stall, consider the following program and cache behaviors.

Data Reads Per 1000 Instructions	**Data Writes Per 1000 Instructions**	**Instruction Cache Miss Rate**	**Data Cache Miss Rate**	**Block Size (Byte)**
200	160	0.20%	2%	8

   (a) **Question** For a write-through, write-allocate cache with sufficiently large write buffer (i.e., no buffer caused stalls), what's the minimum read and write bandwidths (measured by byte-per- cycle) needed to achieve a CPI of 2?

   Answer

   (b) **Question** For a write-back, write-allocate cache, assuming 30% of replaced data cache blocks are dirty, what's the minimal read and write bandwidths needed for a CPI of 2?

   Answer

3. Using the sequences of 32-bit memory read references, given as word addresses in the following table:

6	214	175	214	6	84	65	174	64	105	85	215

For each of these read accesses, identify the binary address, the tag, the index, and whether it experiences a hit or a miss, for each of the following cache configurations. Assume the cache is initially empty.

(a) **Question** A direct-mapped cache with 16 one-word blocks.

Answer

Table 1: A Direct-mapped Cache With 16 One-word Blocks

Memory	Binary	Tag	Index	Hit / Miss
6	00000110			miss
214	11010110			miss
175	10101111			miss
214	11010110			hit
6	00000110			hit
84	01010100			miss
65	01000001			miss
174	10101110			hit
64	01000000			hit
105	01101001			miss
85	01010101			hit
215	11010111			hit

(b) **Question** A direct-mapped cache with two-word blocks and a total size of eight blocks.

Answer

Table 2: A Direct-mapped Cache With Two-word Blocks And A Total Size Of Eight Blocks

Memory	Binary	Tag	Index	Hit / Miss
6	00000110			miss
214	11010110			miss
175	10101111			miss
214	11010110			hit
6	00000110			hit
84	01010100			miss
65	01000001			miss
174	10101110			hit
64	01000000			hit
105	01101001			miss
85	01010101			hit
215	11010111			hit

(c) **Question** A fully associative cache with two-word blocks and a total size of eight words. Use LRU replacement.

Answer

Table 3: A Fully Associative Cache With Two-word Blocks And A Total Size Of Eight Words With LRU Replacement

Memory	Binary	Tag	Index	Hit / Miss
6	00000110			miss
214	11010110			miss
175	10101111			miss
214	11010110			hit
6	00000110			hit
84	01010100			miss
65	01000001			miss
174	10101110			hit
64	01000000			hit
105	01101001			miss
85	01010101			hit
215	11010111			hit

(d) **Question** A 2-way set associative cache with one-word block size and total size of 8 words, while applying LRU replacement policy.

Answer

Table 4: A 2-way Set Associative Cache With One-word Block Size And Total Size Of 8 Words With LRU Replacement Policy

Memory	Binary	Tag	Index	Hit / Miss
6	00000110			miss
214	11010110			miss
175	10101111			miss
214	11010110			hit
6	00000110			hit
84	01010100			miss
65	01000001			miss
174	10101110			hit
64	01000000			hit
105	01101001			miss
85	01010101			hit
215	11010111			hit