CMPE 212, Digital Systems Design
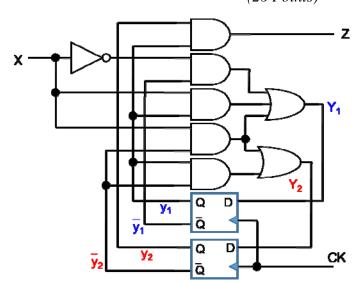
Assignment #5   Due: Wed 5/4/2016

Question 1:   *(26 Points)*

Find the state diagram for the
following sequential circuit assuming
the following state code assignment:

	y_1	y_2
A	0	0
B	0	1
C	1	1
D	1	0

Question 2:   *(20 Points)*

Derive the minimum state diagram of a synchronous sequential circuit that recognizes the input
sequence 1011. Sequences may overlap. For example,

$$x = 0101101100101011010$$

$$z = 0000100100000001000$$

Question 3:   *(30 Points)*

Find the logic diagram of an implementation of the following sequential circuit, given the state
assignment and using:
         (i) D flip flops.   (ii) T flip-flops.

Y_1	Y_2	Y_2			x	
					0	1
0	0	0	→	*A*	*D/0*	*C/0*
0	0	1	→	*B*	*E/0*	*A/1*
0	1	1	→	*C*	*F/1*	*B/0*
0	1	0	→	*D*	*A/1*	*F/1*
1	0	0	→	*E*	*C/0*	*E/1*
1	0	1	→	*F*	*B/0*	*D/1*

Question 4:   *(24 Points)*

Find a reduced state table for the following synchronous sequential circuit using:

    (i) State Partitioning   (ii) An implication table

	0	1
A	*B/0*	*C/0*
B	*D/0*	*E/0*
C	*F/0*	*G/0*
D	*A/1*	*B/1*
E	*C/0*	*D/0*
F	*F/0*	*G/0*
G	*B/0*	*F/0*