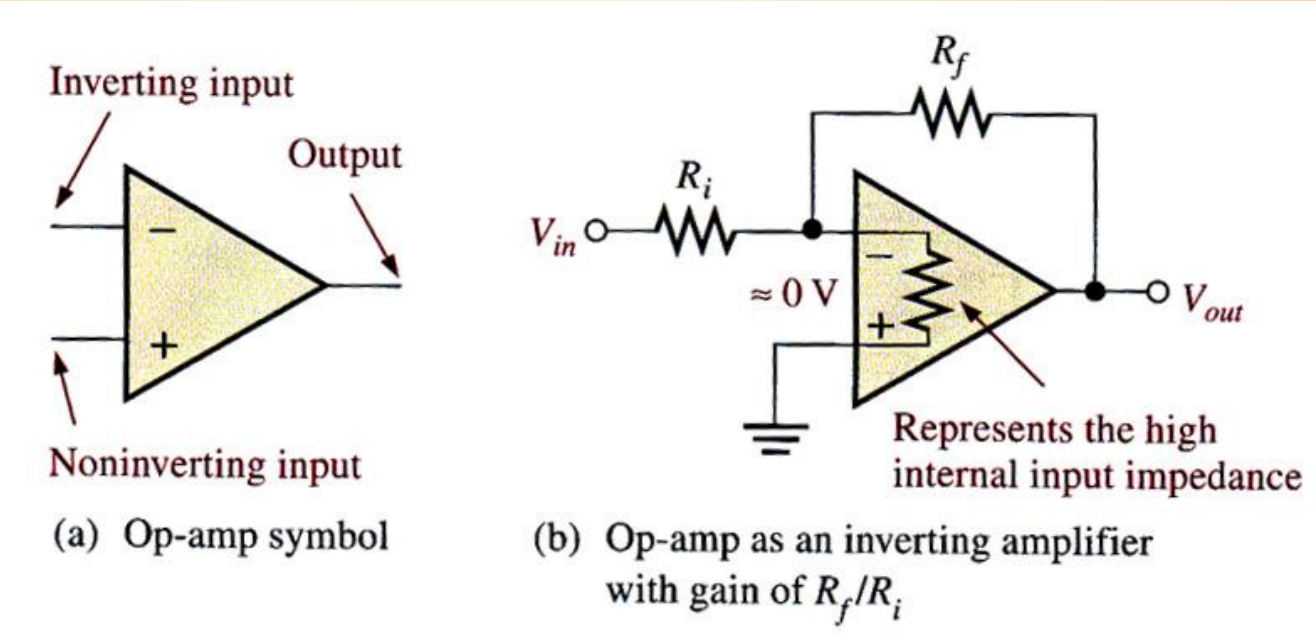
Brief Op-Amp (Operational Amplifier) review:

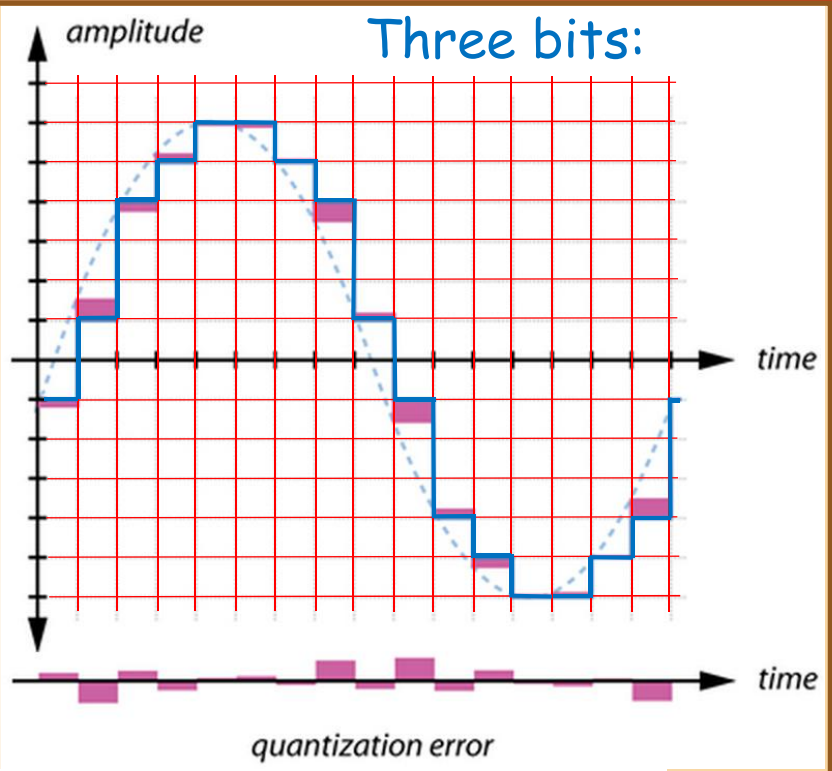
- Op Amps are used heavily for conversion of signals between the analog and digital worlds. The concept of the ideal OpAmp;
  - Input impedance = ∞.
  - Input voltage drop = 0v. – an ideal voltage short across the differential inputs.

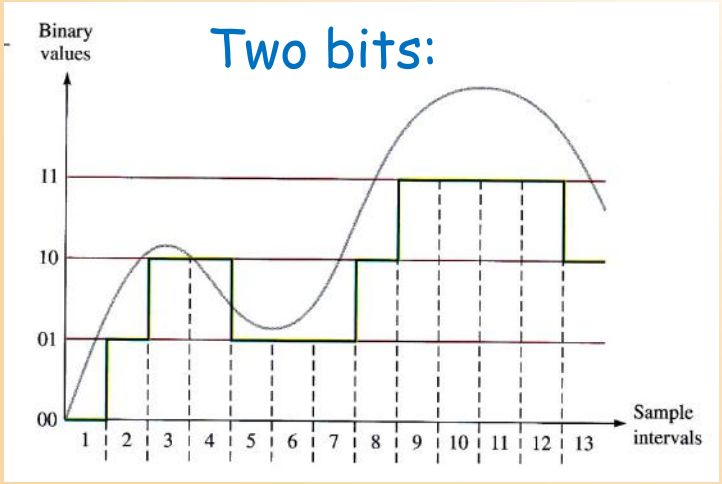


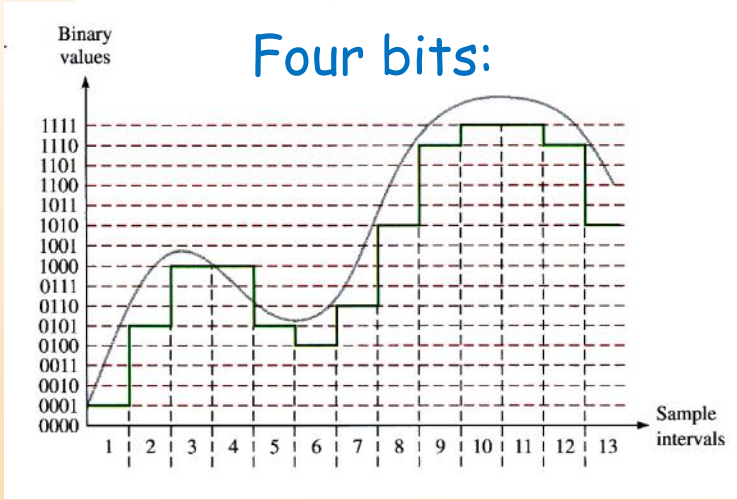
$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i} \qquad V_{out} = -\frac{R_f}{R_i} V_{in}$$

Real Numbers with a Limited # of Bits

- Many physically-based values are best represented with real-numbers as opposed to a discrete number of values. However, in computers we are practically limited in the number of distinct values we can represent.
- We can only pick 2^N real-valued points called quantization levels
- **Quantization**: "rounding" of real number to one of a limited set real-numbered quantization levels
- **Quantization error**: is the difference between a desired real number and its quantized value
- **Coding**: mapping of set of real numbers to a digital code

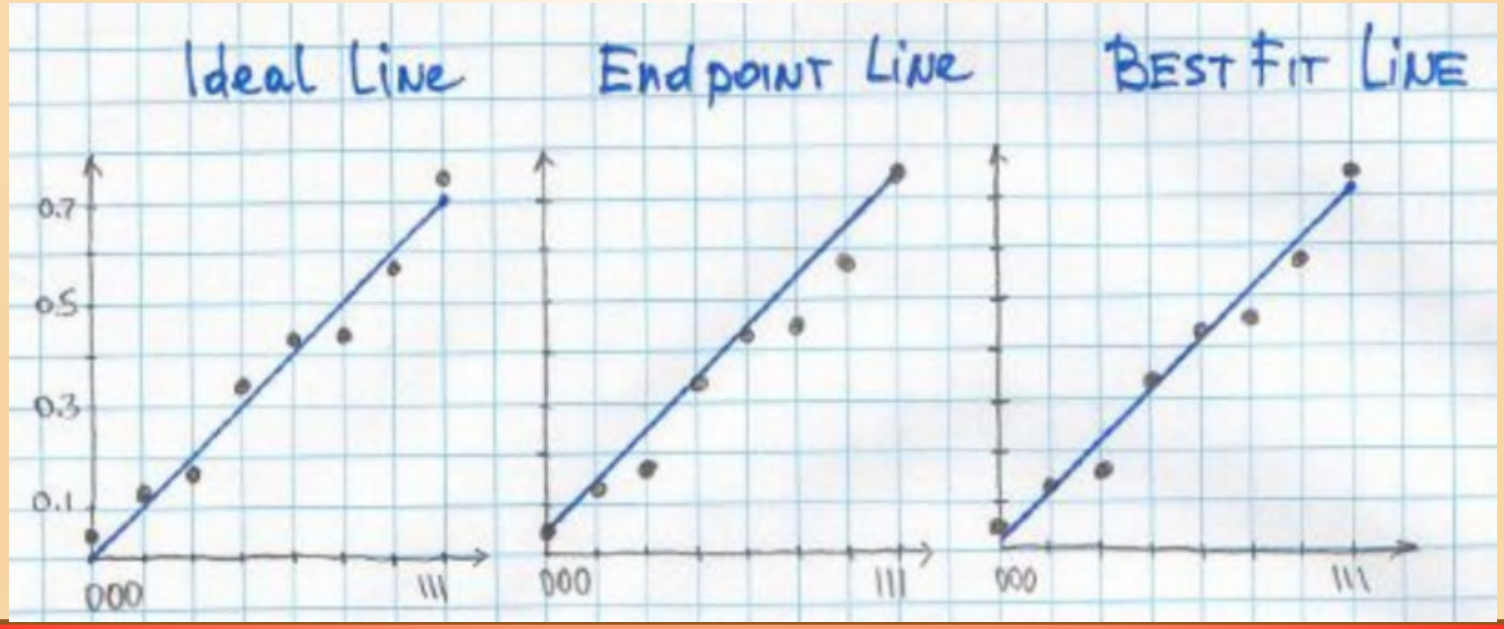






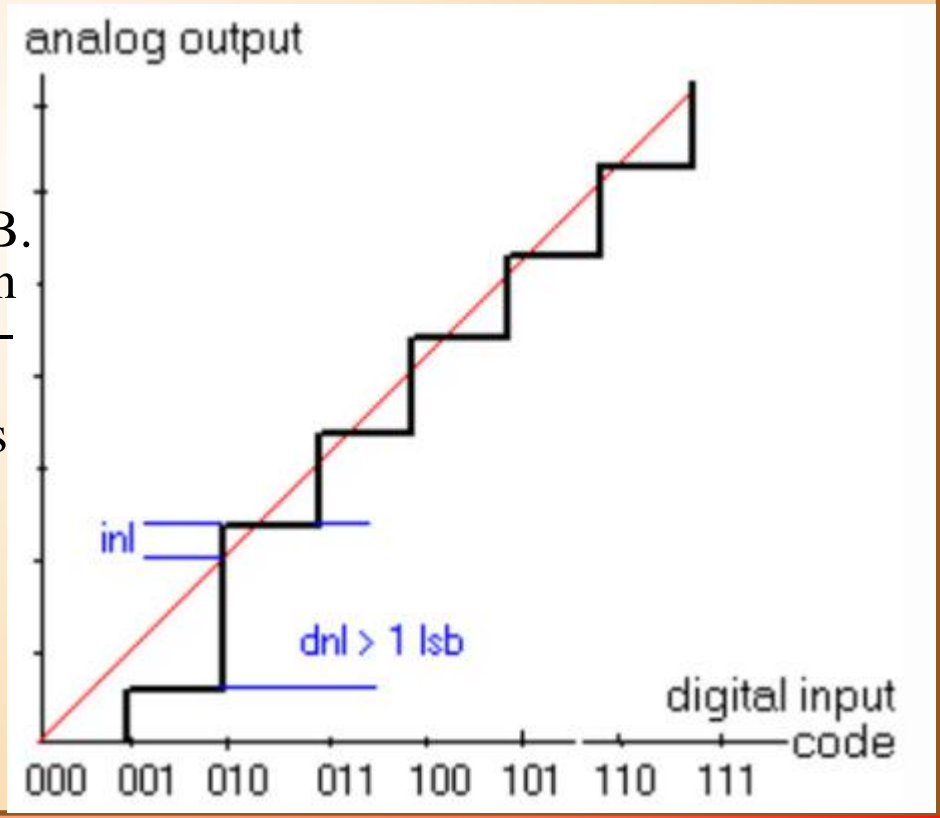
Digital to Analog Converters (DAC) – General Concerns, pt 1:

- **Resolution** - normally given in bits.
  Resolution indicates the smallest increment of its output corresponding to a 1 LSB input code change. For example for 10 bit DAC, 2^10 = 1024 codes, so the resolution is 1/1024 of the output range.
- **Full scale range (FSR)** - maximum output signal for the DAC, specified as current or voltage (ma or V).
  Can be negative ,positive or both.
- **Offset error** - difference between the ideal and actual DAC output when zero digital code applied to the input.
- **Gain error** - the difference between the ideal and actual output when full scale digital code applied to the input. Strongly depends on VREF stability.



Digital to Analog Converters (DAC) – General Concerns, pt 2:

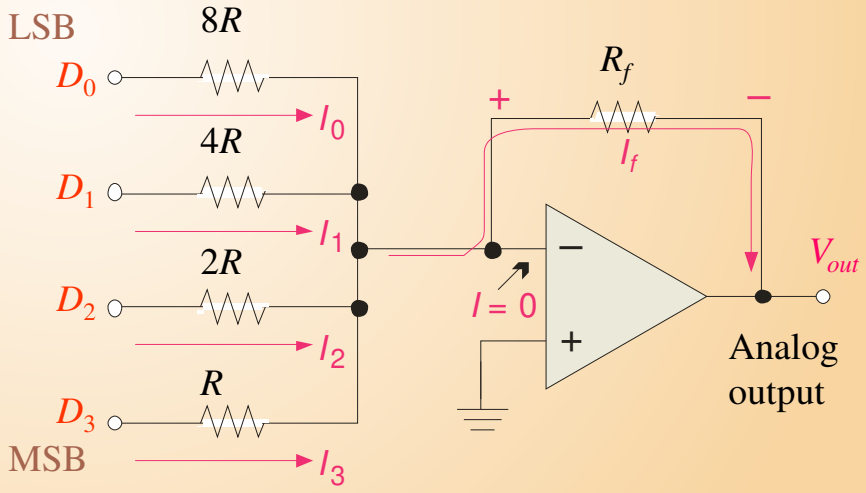
- **Integral nonlinearity**: (acronym **INL**) shows how the output differs from the straight line, weather it is an ideal line or best-fit or end-point.
- - The maximum deviation between the data converter output values and a reference straight line drawn through the first and last output values (after offset and gain errors have been removed). INL defines the linearity of the overall transfer curve .
- **Differential nonlinearity**: (acronym **DNL**) - describes the uniformity of the LSB sizes between DAC codes. DNL represents the error in each step size, expressed in fractions of LSB.
- - is a term describing the deviation between two analog values corresponding to adjacent input digital values. The accuracy of a DAC is mainly determined by this specification. If we were to plot the value of DNL (in LSBs) versus the input digital code.



Binary Weighted Input DAC

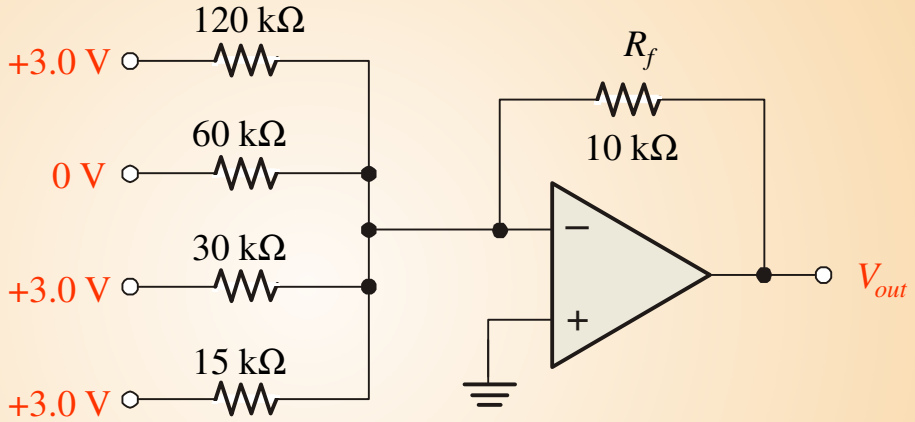
- The binary-weighted-input DAC is a basic DAC in which the input current in each resistor is proportional to the column weight in the binary numbering system.
- It requires:
  - Very precise, accurate resistors and
  - Identical HIGH level voltages for accuracy.

- The MSB is represented by the largest current, so it has the smallest resistor. To simplify analysis, assume all current goes through R_f and none into the op-amp.



Binary Weighted Input DAC - Example

Example A certain binary-weighted-input DAC has a binary input of 1101. If a HIGH = +3.0 V and a LOW = 0 V, what is V_{out}?



Solution

$$I_{out} = -(I_0 + I_1 + I_2 + I_3)$$

$$= -\left(\frac{3.0\text{ V}}{120\text{ k}\Omega} + 0\text{ V} + \frac{3.0\text{ V}}{30\text{ k}\Omega} + \frac{3.0\text{ V}}{15\text{ k}\Omega}\right) = -0.325\text{ mA}$$

$$V_{out} = I_{out} R_f = (-0.325\text{ mA})(10\text{ k}\Omega) = -3.25\text{ V}$$

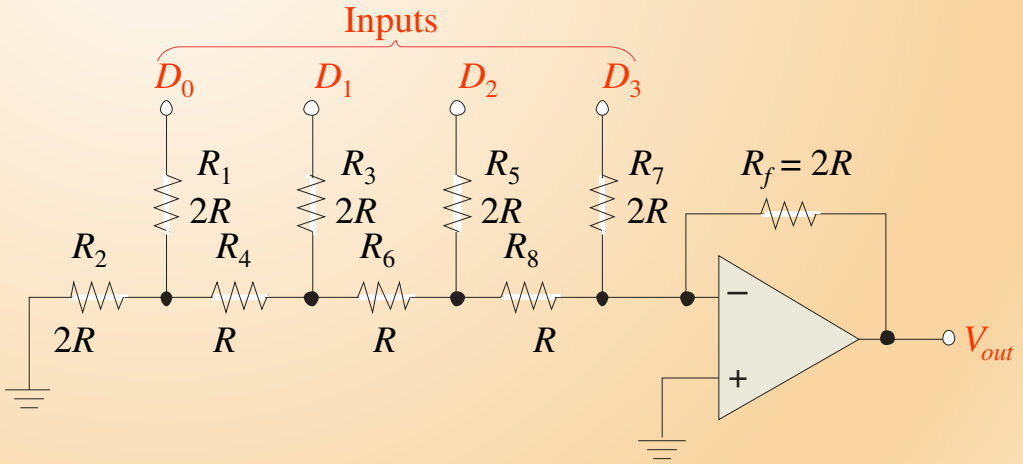
R-2-R Ladder DAC

- The R-2R ladder requires only two values of resistors.
- For accuracy, the resistors must be precise ratios. In integrated circuits this can be readily achieved.
- By calculating a Thevenin equivalent circuit for each input, you can show that the output is proportional to the binary weight of inputs that are HIGH.
- Each input that is HIGH contributes to the output: $V_{out} = -\frac{V_S}{2^{n-i}}$

  where V_S = input HIGH level voltage

  n = number of bits

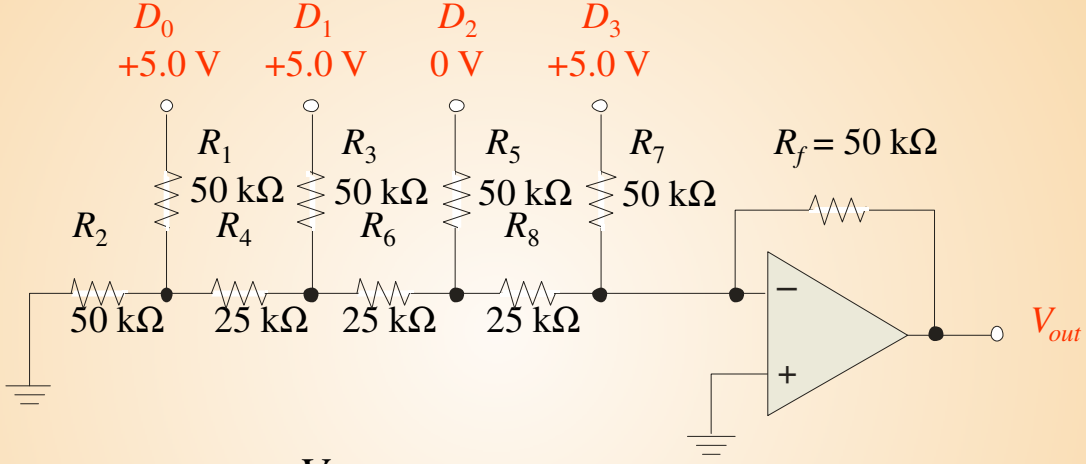
  i = bit number



R-2-R Ladder DAC - Example

Example

An *R-2R* ladder has a binary input of 1011. If a HIGH = +5.0 V and a LOW = 0 V, what is V_{out}?



Solution

Apply $V_{out} = -\frac{V_S}{2^{n-i}}$ to all inputs that are HIGH, then sum the results.

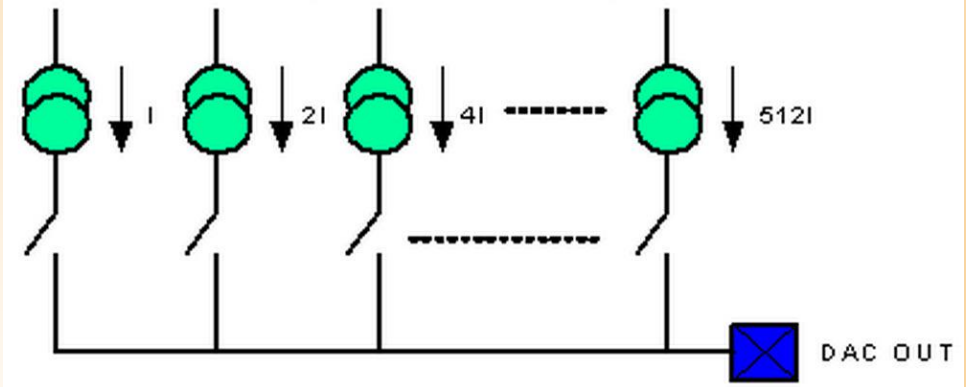
$$V_{out}(D_0) = -\frac{5\text{ V}}{2^{4-0}} = -0.3125\text{ V} \quad V_{out}(D_1) = -\frac{5\text{ V}}{2^{4-1}} = -0.625\text{ V}$$

$$V_{out}(D_3) = -\frac{5\text{ V}}{2^{4-3}} = -2.5\text{ V}$$

Applying superposition, V_{out} = –3.43 V

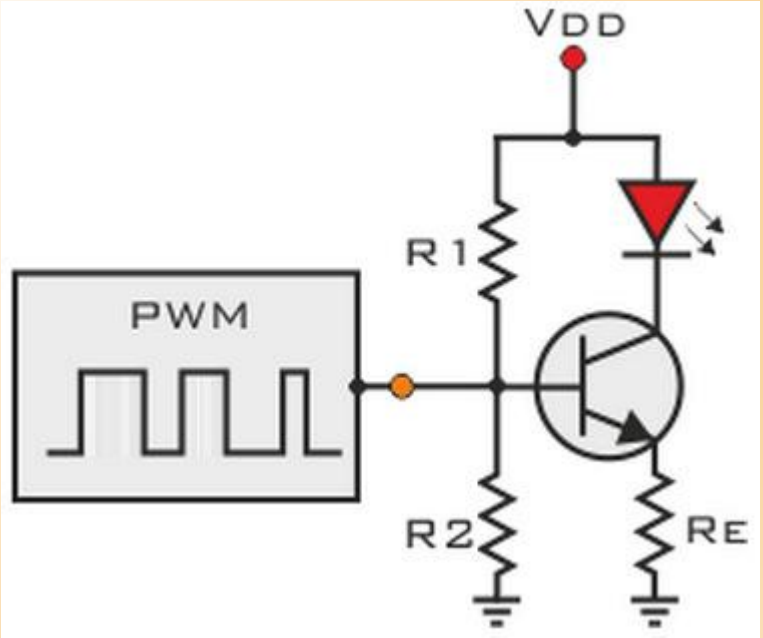
Current-Output DAC

- Output is current instead of voltage
- Common for high-speed converters
- Voltage can be set using a resistor or by a user-selected external high-speed active current-to-voltage converter



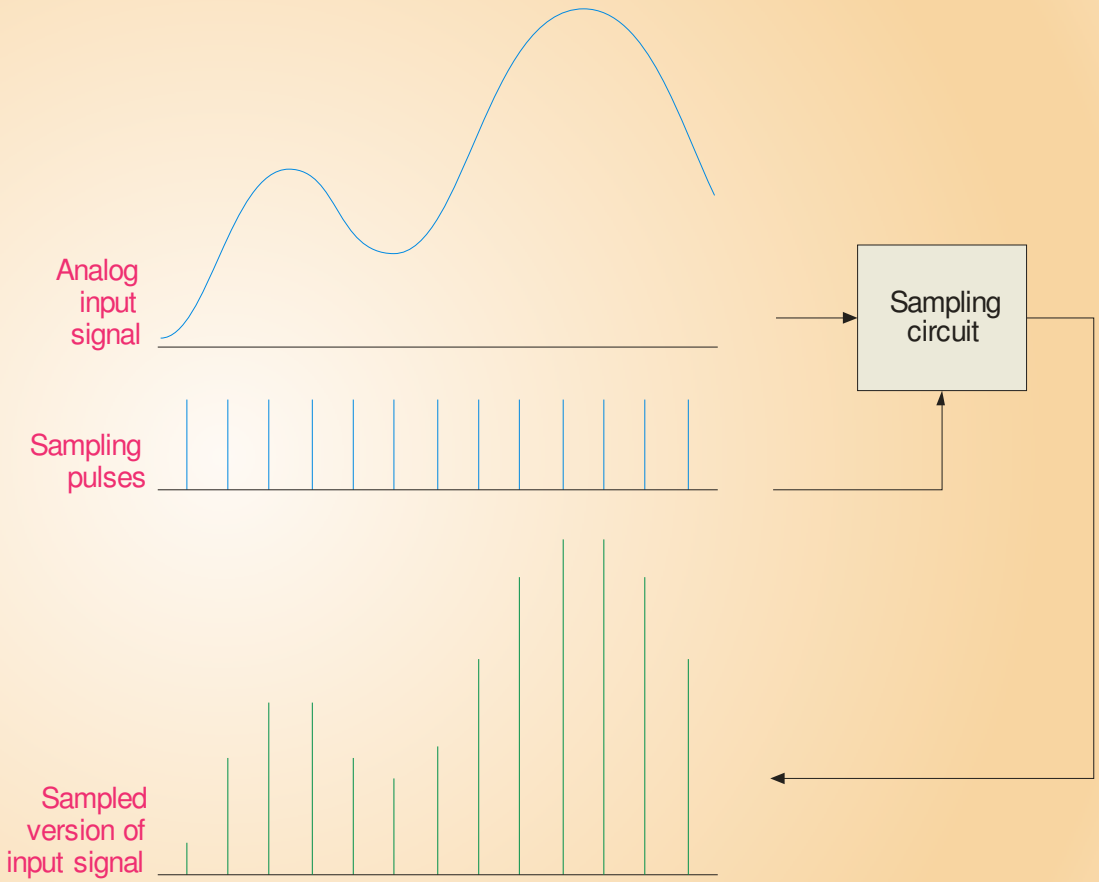
PWM Based DAC

- A cheap DAC can be built using digital driver and a low-pass filter. The duty cycle of the digital signal sets the analog output level.



Analog to Digital Converter – ADC – Sampling

- An analog-to-digital conversion (abbreviated ADC, A/D or A to D) is a process that converts a continuous quantity (continuous in time and possible values) to a discrete-time, discrete value (digital) representation
- For processing, the signal is normally converted to a digital signal by sampling the input.
- ADC is:
  - Mapping to discrete values
  - Updating/defining value at discrete times
- ADCs may use
  - Single or parallel stages
  - Single conversion step or successive approximation steps
  - One or multiple clock cycles
- The various architectures trade off the performance metrics discussed, as well as cost, power, size, etc...



ADC General Features, Architectures

- ADCs may use
  - Single or parallel stages
  - Single conversion step or successive approximation steps
  - One or multiple clock cycles

- The various architectures trade off the performance metrics discussed, as well as cost, power, size, etc...

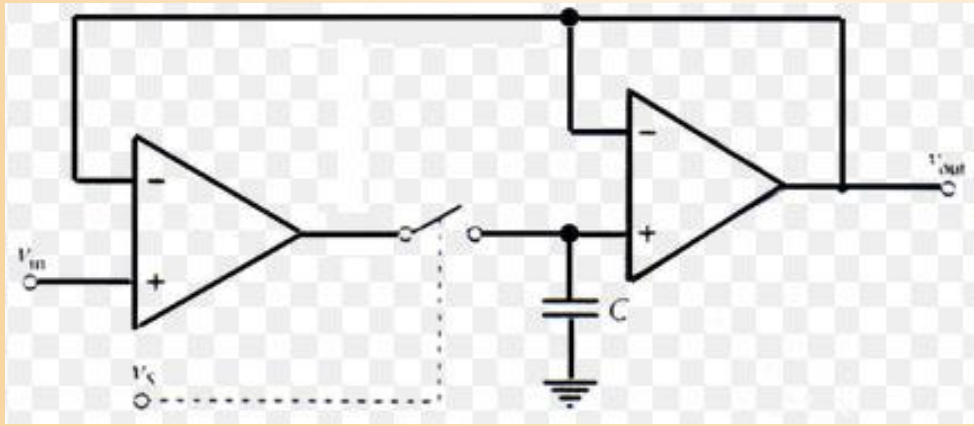
- Common ADC Architectures:
  - **Flash**: uses parallel stages for speed, precision/accuracy is sacrificed by needing many so many parts matched
  - **Pipelined**: uses multiple stages to resolve signal, good throughput but larger latency
  - **Successive Approximation and Algorithmic**: uses multiple iterations to resolve signal, slow
  - **Algorithmic**: uses multiple iterations to resolve signal, slow
  - **Sigma-Delta**: performs fast conversion on signal changes but effectively slow sensing/detections of total signal/large changes

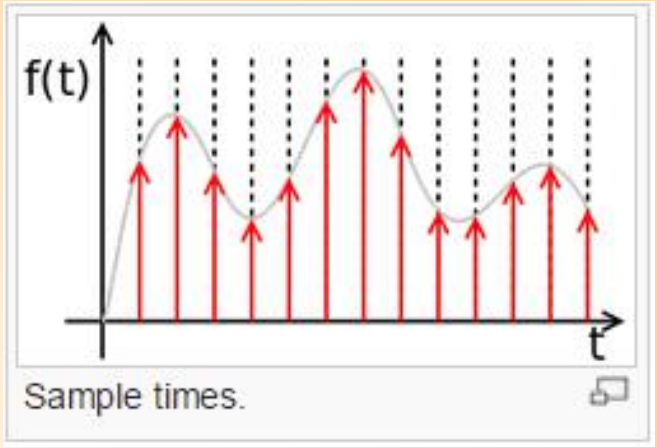
ADC Performance Metrics

- **Sample rate/ throughput**:
  - number of measurements of amplitude per second. Higher sampling rates are better but increase data-rates, power, cost, etc...
  - How fast is fast enough? The commonly-cited value is 2-times the frequency of the highest frequency component into the ADC, (this allows perfect reconstruction of the continuous waveform). Often an analog low-pass filter is used before the ADC to limit the required sampling frequency.
  - Sometimes a technique call oversampling is used: it involves sample faster than needed and digitally averaging results to remove some noise. For AVR, see application note (http://www.atmel.com/images/doc8003.pdf)
- **Latency**: time between sampling a voltage and getting the corresponding value
- **Bit depth**: determines number of discrete values that can be represented, sets bound on combination of precision and rangeof each measurement of amplitude.
- **Precision vs Accuracy**:
  - If the offset of the measured value from the true value maters, you care about accuracy.
  - If you care how small of a voltage step you can resolve you care about precision.
  - Often these ideas are combined under the umbrella term "accuracy"
- **Monolithic**: means that digital codes strictly increase when analog voltage increases

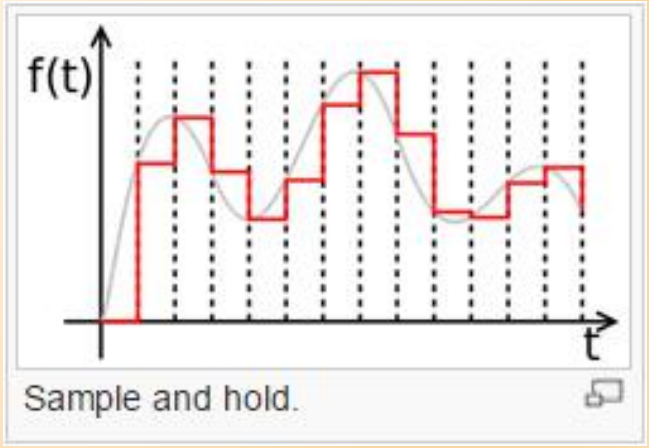
ADC – Sample and Hold (ref Fig 17.11 in text)

- In electronics, a sample and hold (S/H, also "follow-and-hold") circuit is an analog device that samples (captures, grabs) the voltage of a continuously varying analog signal. It then holds (locks, freezes) its value at a constant level for a specified minimum period of time. They are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process.
- For fast operation, a driver must be able to set the capacitor quickly and accurately. For fast settling a small RC is required, i.e. a low output resistance is required by the driver. For this purpose, the ADC datasheet may specify a maximum output impedance for the driver along with a minimum current drive ability.
- Some ADCs include a internal "Track and Hold" buffer to drive the sample capacitance





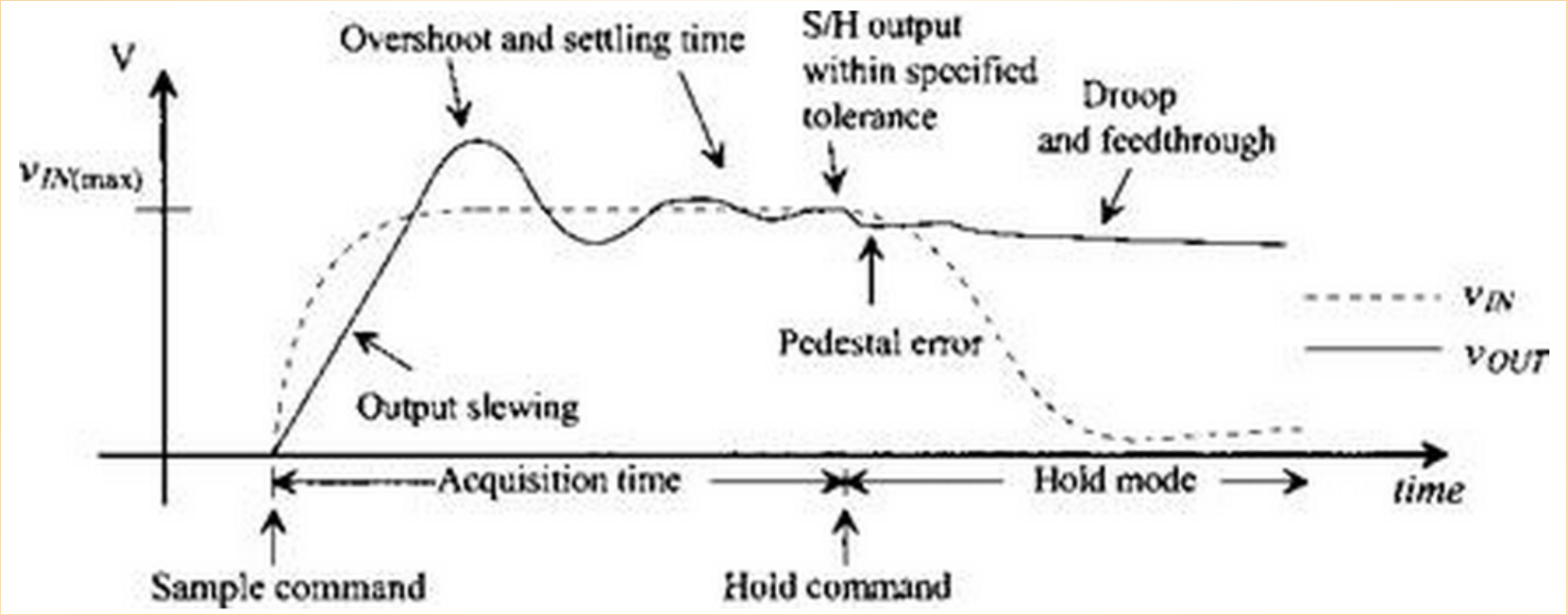
Sample times.



Sample and hold.

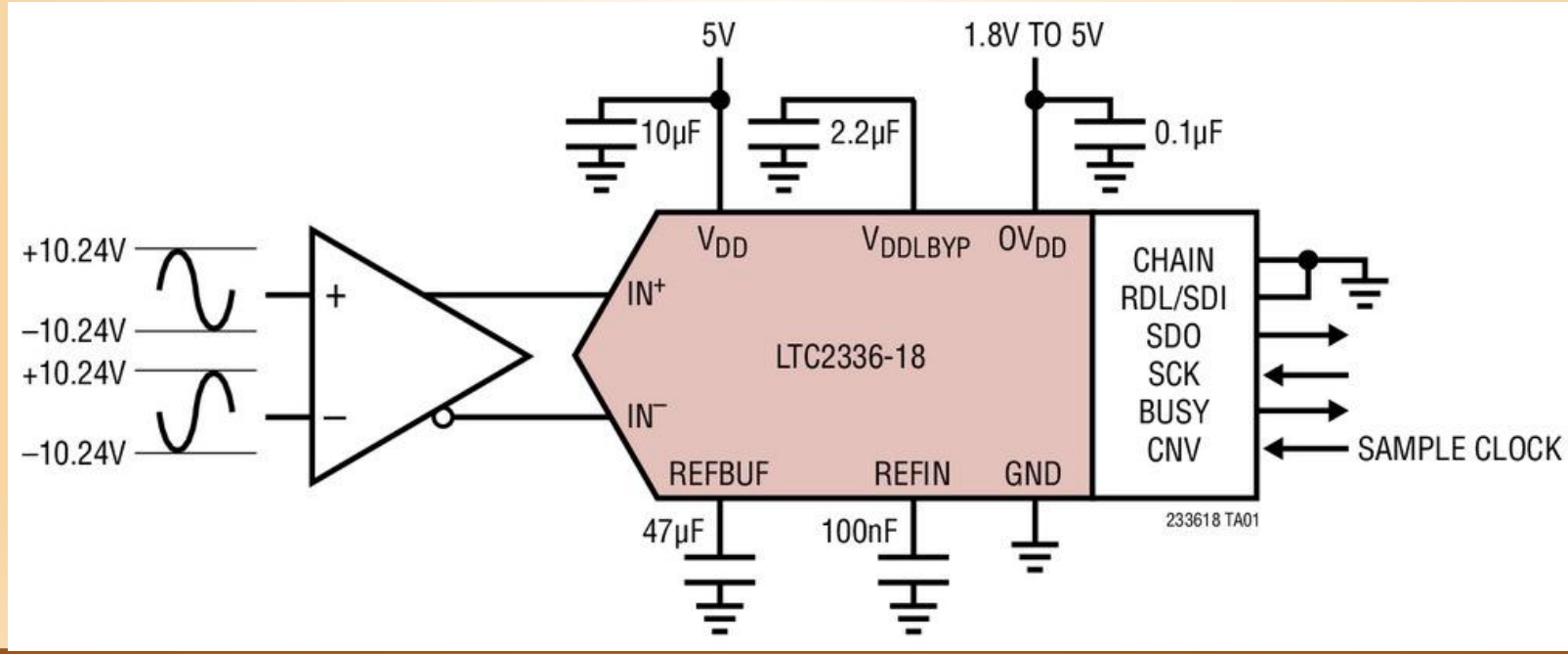
Sample and Hold – Droop, and other concerns

- The switch is implemented with FET that unfortunately leaks current and causes droop during hold.
- So, hold times can not be indefinite and thus ADC's often require a ***minimum*** clock rate to ensure processing happens quickly enough
- Also, as the input is allowed into the Sample and Hold, overshoot (undershoot not shown) ringing and settling time need to be considered as well.



Differential and Pseudo-differential Input

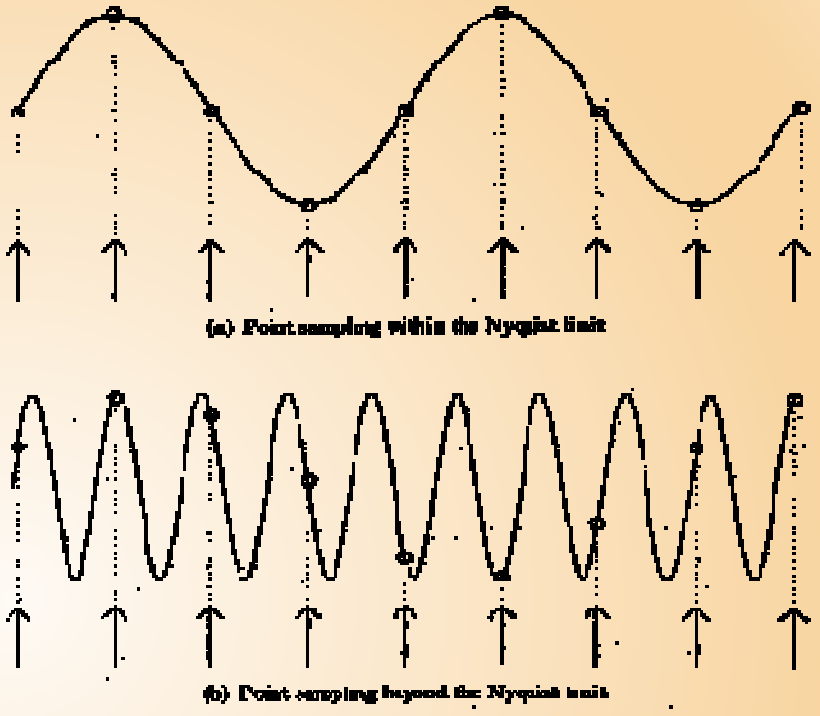
- Differential input is useful when the potential to be measured is not referenced to ground.
- It is also useful for rejecting noise on ground or differences between grounds
- Pseudo-differential is like differential but Vin-pin must be close in terms of voltage to ground. (~.7) and is used only for noise rejection.

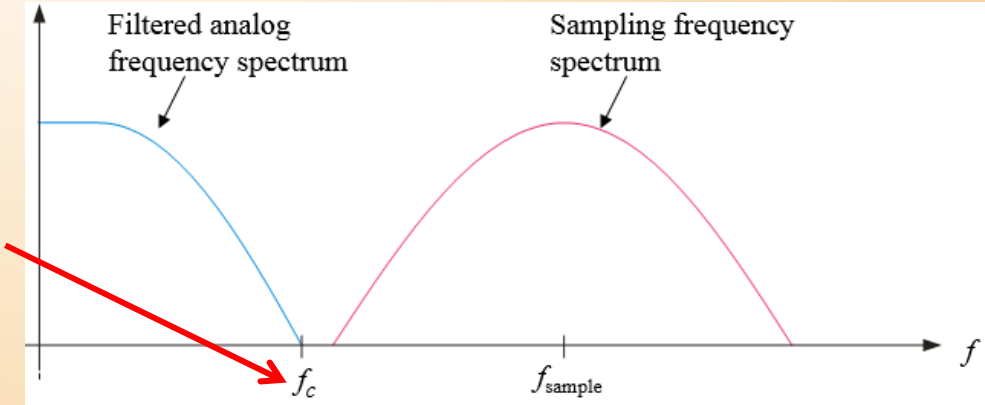


ADC – Anti Aliasing Filter

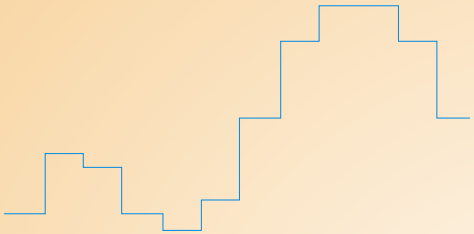
- Most signals have higher frequency harmonic and noise. For most ADCs, the sampling and filter cutoff frequencies are selected to be able to reconstruct the desired signal without including unnecessary harmonics and noise.

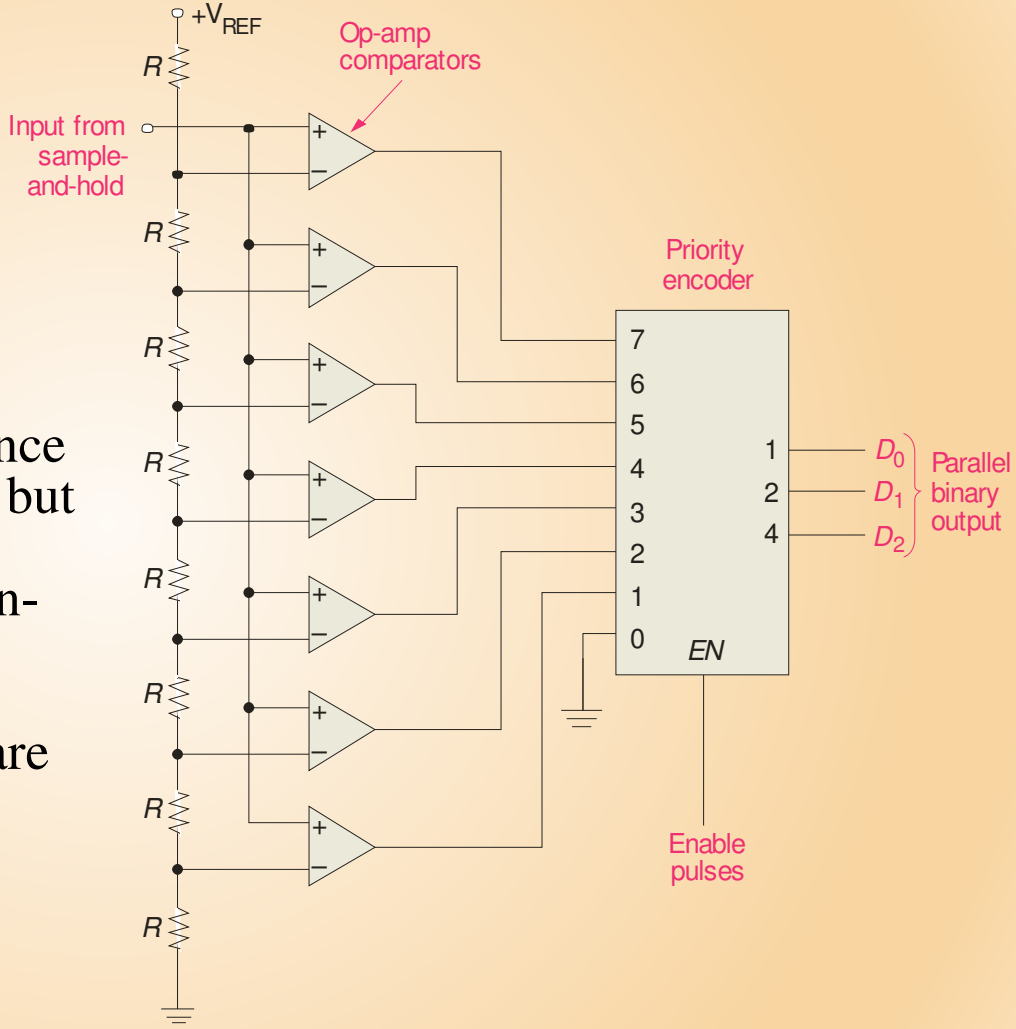
- The anti-aliasing filter is a low-pass analog filter that limits high frequencies in the input signal to only those that meet the requirements of the sampling theorem.
- The filter's cutoff frequency, f_c, is referred to as the **Nyquist frequency** and should be less than ½ f_{sample}.





ADC – Converters: Flash Converter:



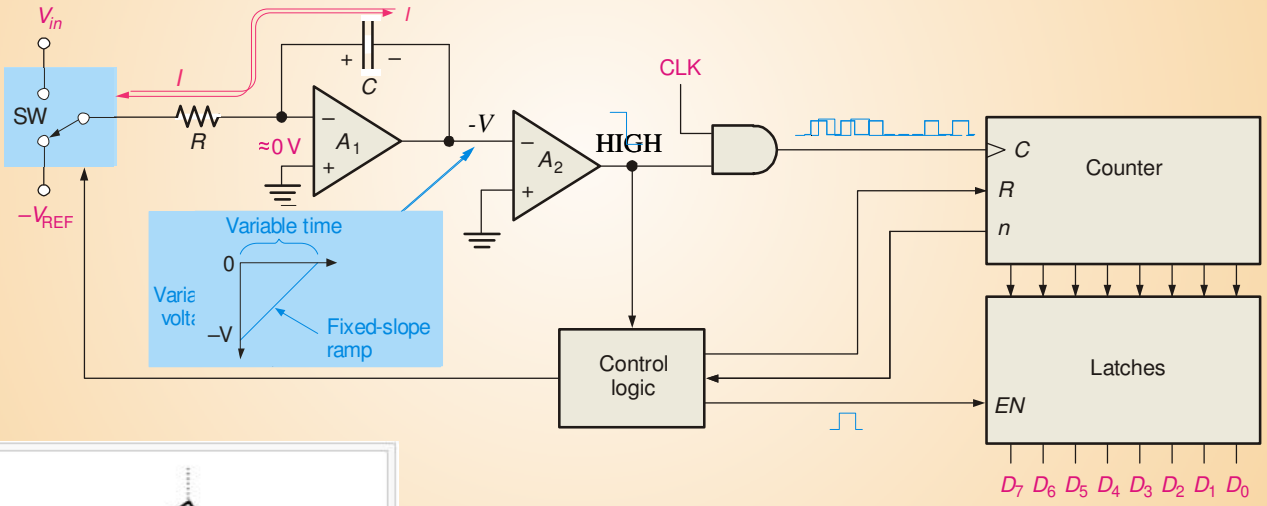


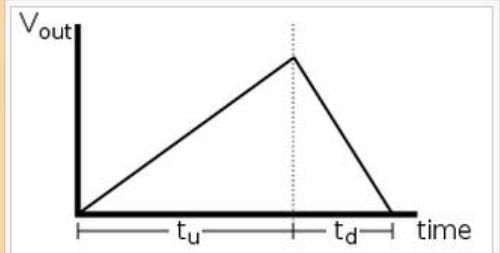
- The flash ADC uses a series high-speed comparators that compare the input with reference voltages. Flash ADCs are fast but require $2^n - 1$ comparators to convert an analog input to an n-bit binary number.
- How many bits of resolution are shown for the example to the right?
- For 8 bits of resolution, how many comparators would be needed?

ADC – Converters: Dual Slope:

- Section 17.4.1 in your textbook for another reference:

  1. The dual-slope ADC integrates the input voltage for a fixed time while the counter counts to *n*.
  2. Control logic switches to the V_{REF} input.
  3. A fixed-slope ramp starts from –*V* as the counter counts. When it reaches 0 V, the counter output is latched.





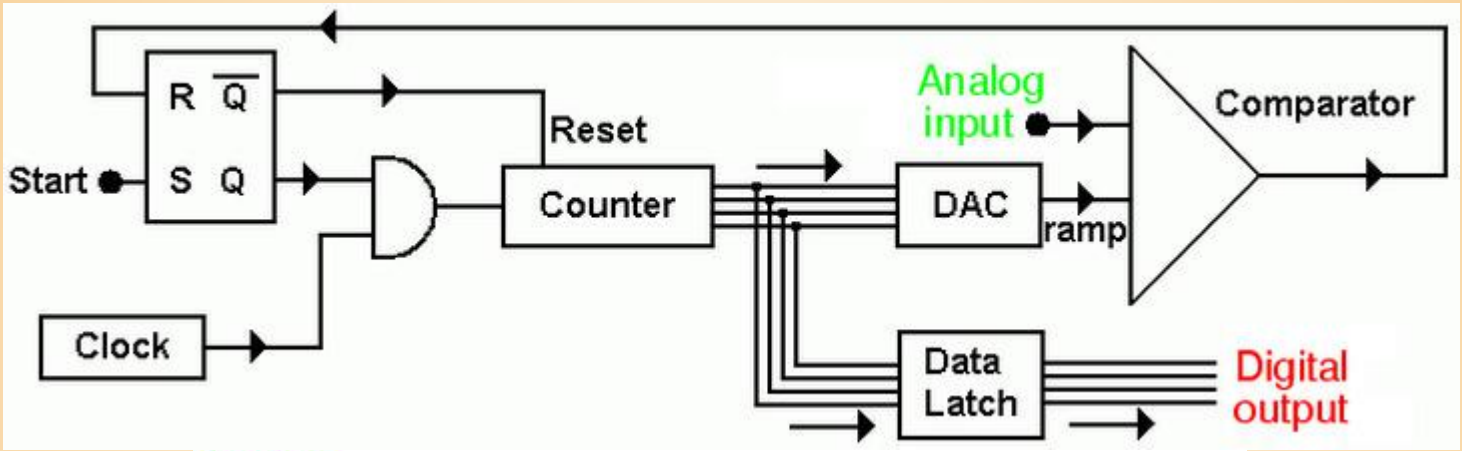
Integrator output voltage in a basic dual-slope integrating ADC

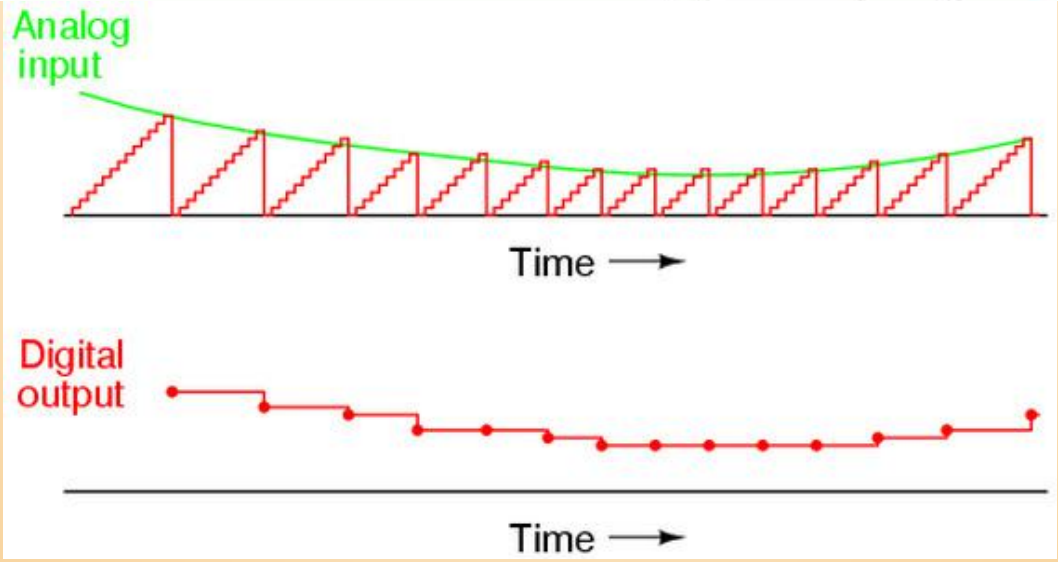
$$V_{out-up} = -\frac{V_{in}}{RC}t_u \qquad V_{in} = -V_{ref}\frac{t_d}{t_u}$$

$$V_{out-down} = -\frac{V_{ref}}{RC}t_d$$

ADC – Digital Ramp

- An analog approximation "guess" is made by increasing a digital code to a DAC. Once the analog approximation crosses the input, waveform is reached, the digital code is saved

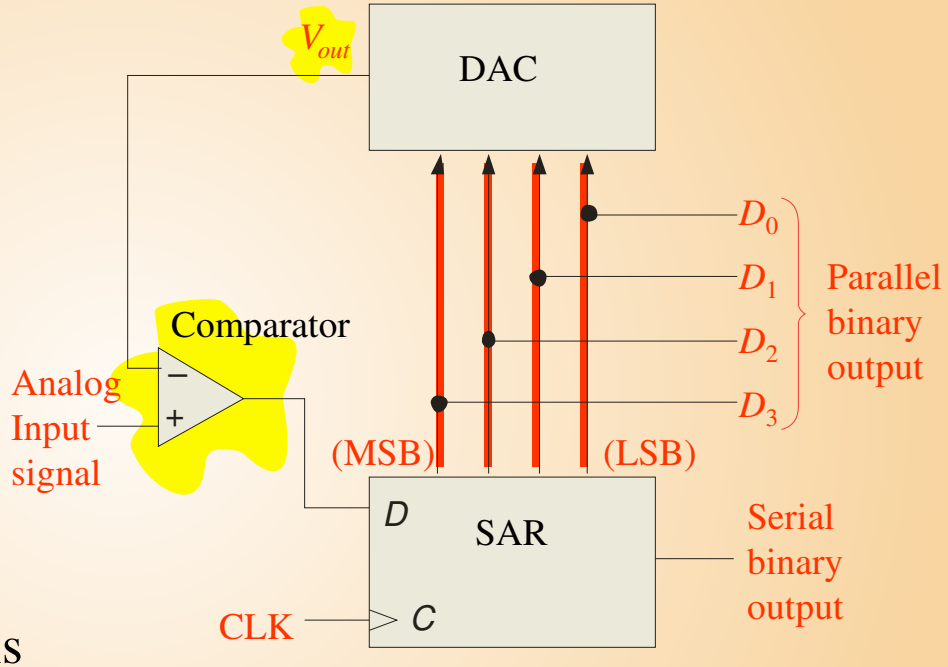




ADC – Converters: Successive Approximation:

- Section 17.4.2 in your textbook for another reference:

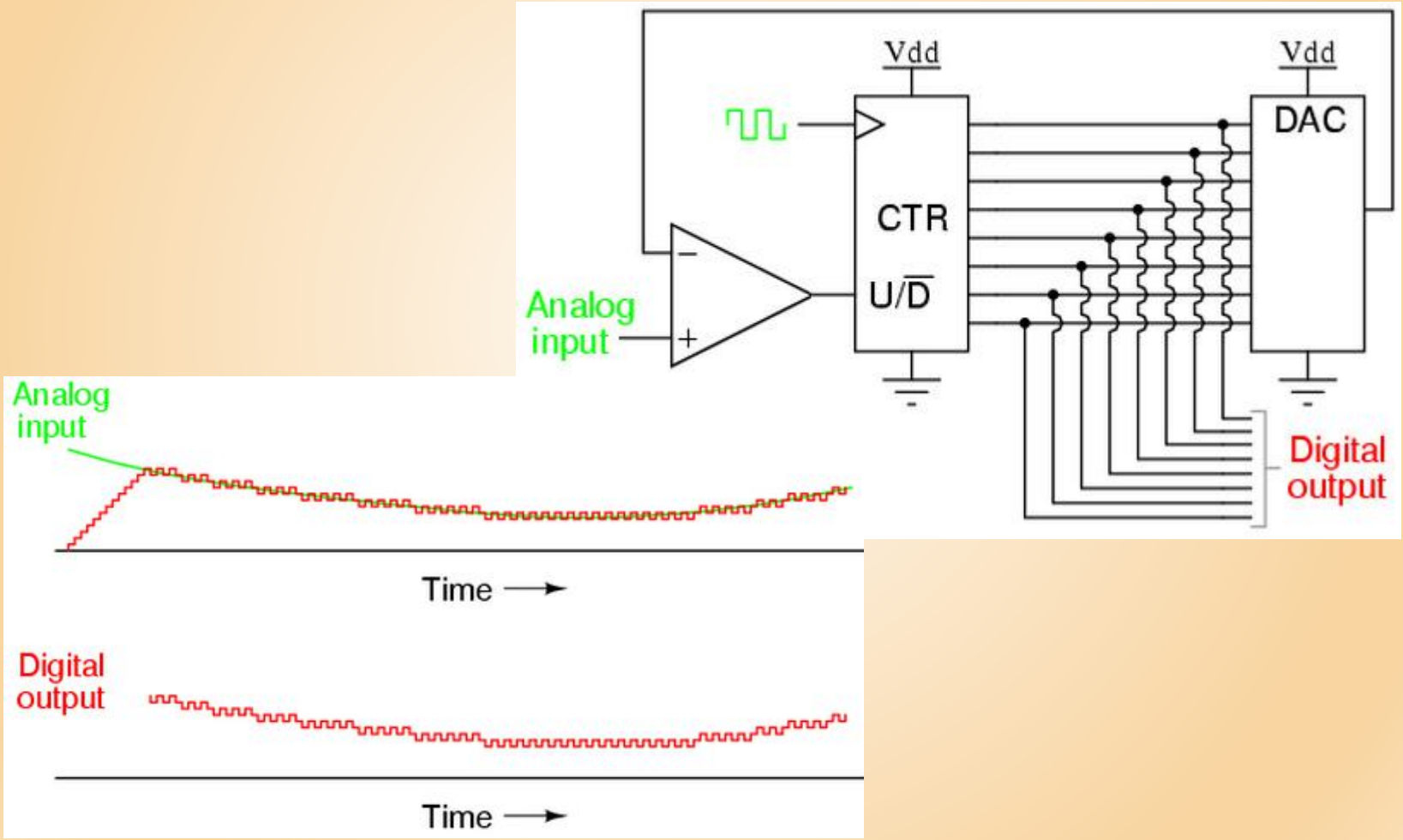
1. Starting with the MSB, each bit in the successive approximation register (SAR) is activated and tested by the digital-to-analog converter (DAC).
2. After each test, the DAC produces an output voltage that represents the bit.
3. The comparator compares this voltage with the input signal. If the input is larger, the bit is retained; otherwise it is reset (0).



The method is fast and has a fixed conversion time for all inputs.

ADC – Digital Ramp

- An analog approximation "guess" is made by increasing a digital code to a DAC. Once the analog approximation crosses the input, waveform is reached, the digital code is saved



ADC – Integrating Reference Ramp

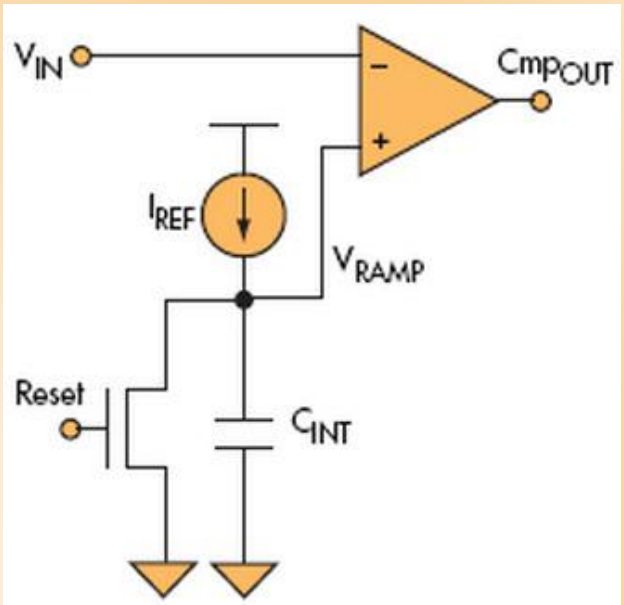
- In its simplest form, it consists of a current source and a capacitor. Charging the capacitor with a current source results in a ramp voltage:

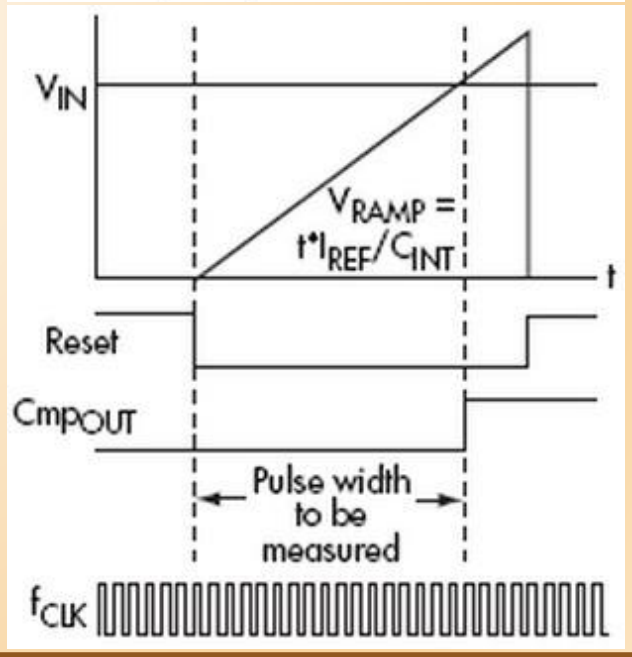
$$V_{RAMP} = \frac{I_{REF}}{C_{INT}} \times t$$

- When the reset is released, the current source charges the capacitor and produces a linear ramp that starts at zero and eventually reaches the value of the input voltage. At this point, the comparator's output goes low, and the input voltage is converted to a pulse width. Measure its width, and you know the input voltage. A reference clock, f_{CLK} can easily measure this time.
- When the reset signal is released, the counter increments on each clock cycle until the comparator output goes high and the counter is no longer gated. The rising edge of the reset line latches the data. The latch now contains the pulse-width value in counts. The relationship between the input voltage and value in counts is:

$$n = V_{IN} \times \frac{C_{INT}}{I_{REF}} \times f_{CLK}$$

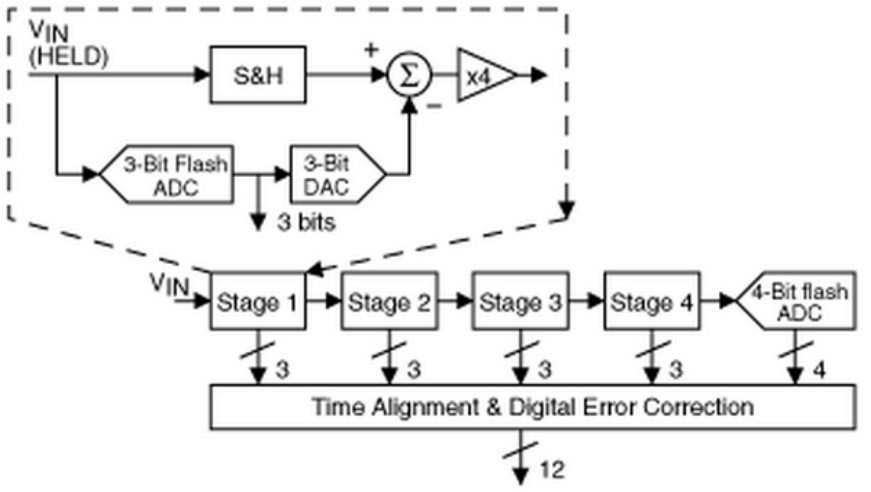
- The number of counts is proportional to the input voltage.

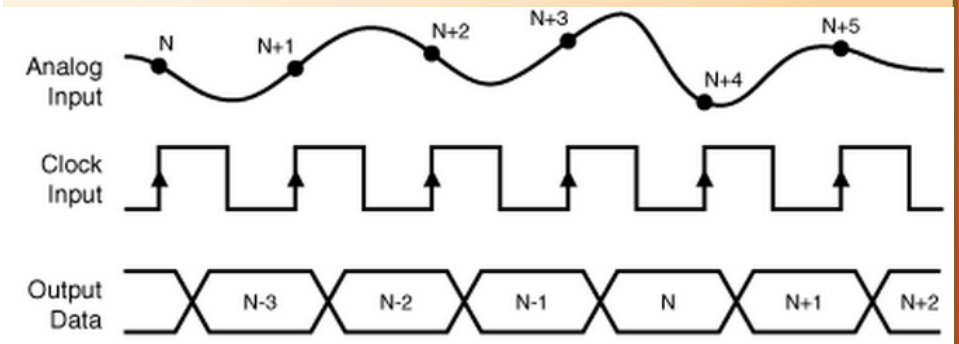




ADC – Pipelined, Algorithm

- The analog input, VIN, is first sampled and held, while the flash ADC in stage one quantizes it to three bits. The 3-bit output is then fed to a 3-bit DAC, and the analog output is subtracted from the input.
- For a **Pipelined Algorithm**, the "residue" is gained-up (multiplied) and fed to the next stage (Stage 2). The gained-up residue continues through the pipeline, providing three bits per stage until it reaches the 4-bit flash ADC, which finds the last 4 LSB bits. If **Pure Pipeline ADC**, the **residue is not multiplied**.
- **Inherent Latency** occurs because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic.
- Note when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput.

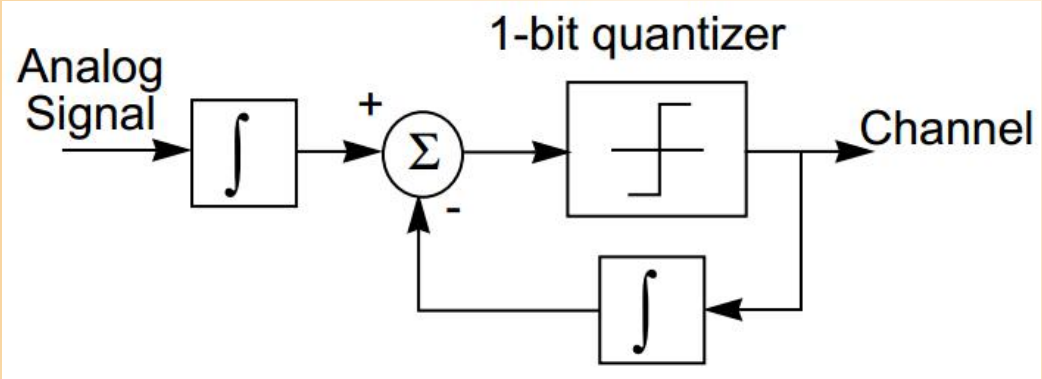


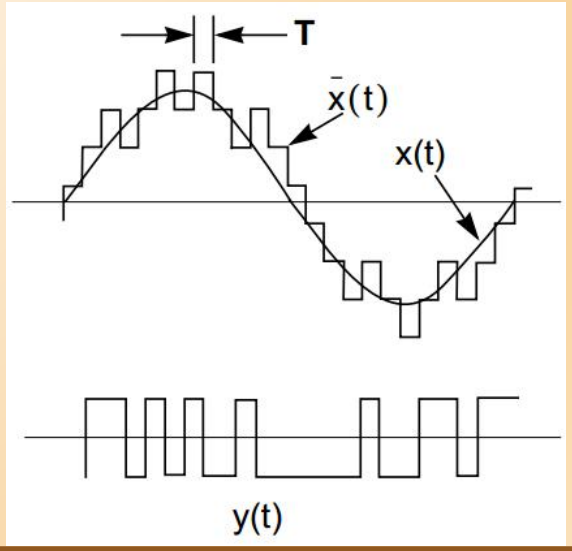


ADC – Sigma-Delta

- Summary: sample signal and sense only changes and do it so fast that only small changes need to be digitized using low-resolution components

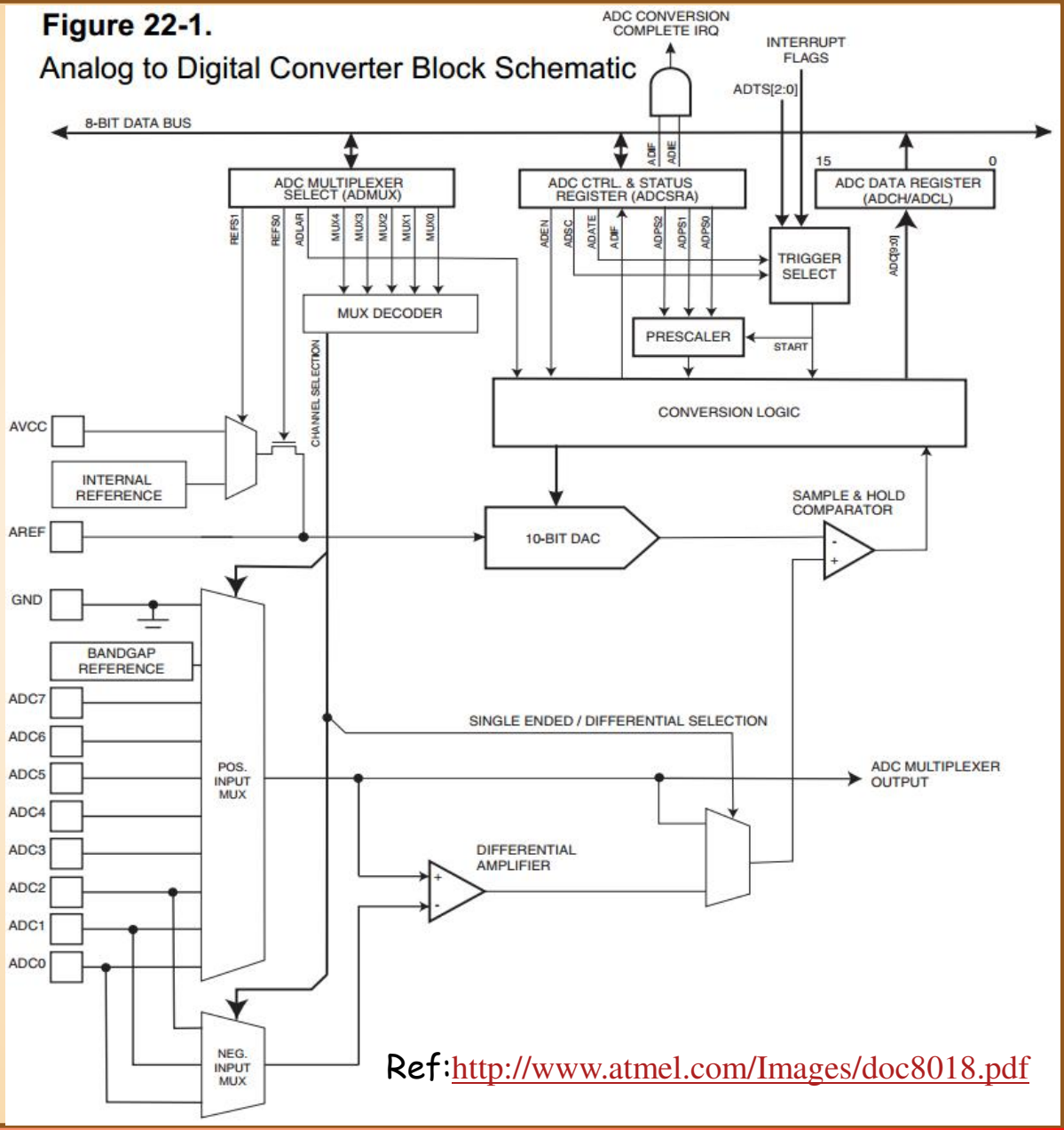
- Delta modulation is based on quantizing the change in the signal from sample to sample rather than the absolute value of the signal at each sample.
- The output of the integrator in the feedback loop tries to predict the input x(t), the integrator; it works as a predictor. The prediction error term is quantized and used to make the next prediction. The quantized prediction error (delta modulation output) is then integrated in the receiver just as it is in the feed back loop; that is, the receiver predicts the input signals.
- The predicted signal is then smoothed with a lowpass filter.
- Ref: http://www.numerix-dsp.com/appsnotes/APR8-sigma-delta.pdf





ADC of Atmega169P

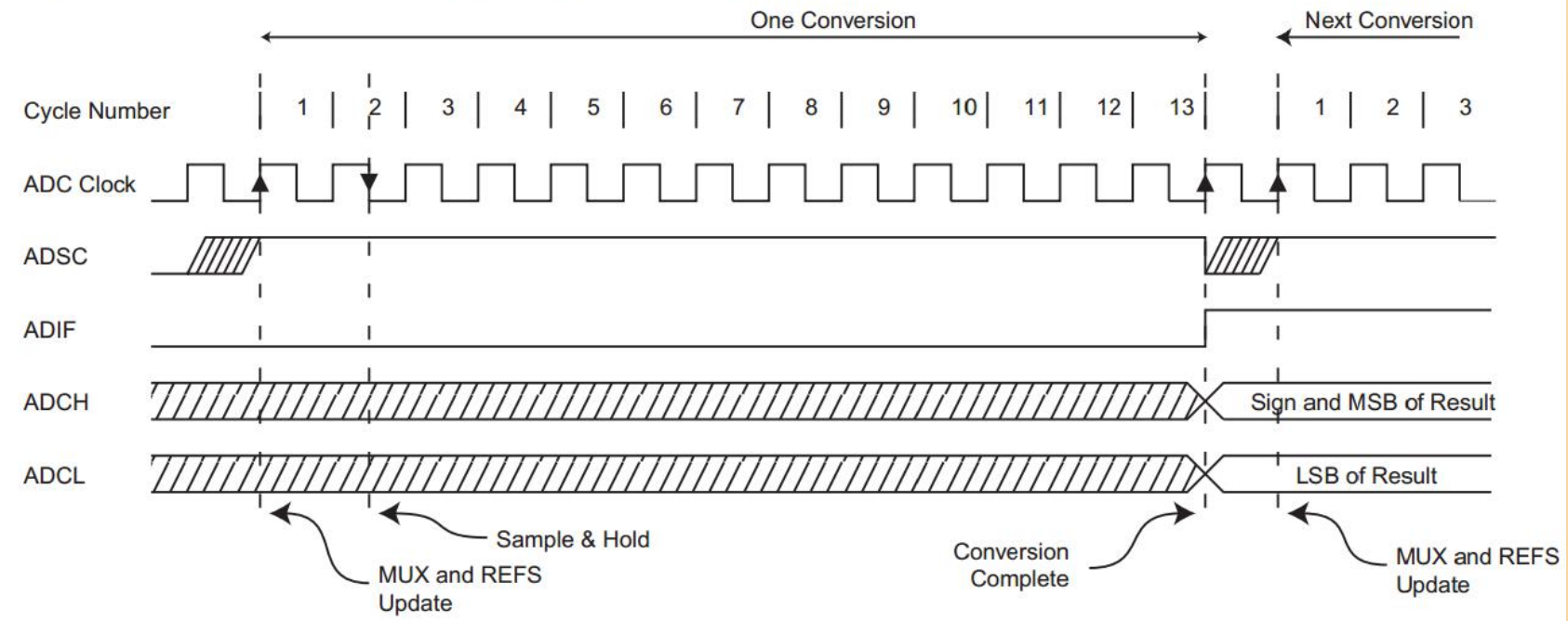
- 10-bit Resolution
- 0 to V_{CC} ADC Input Voltage Range
- ADC clock can be 50KHz to 1MHz
- Full resolution (10 bits)
- frequency range 50KHz-200KHz
- Up to 15 ksps at to get Maximum Resolution (200 kHz ADC clock)
- **NOTE** the 200 kHz ADC clock and compare it to the 15 ksps spec.



Ref:http://www.atmel.com/Images/doc8018.pdf

Conversion Timing

Figure 22-5. ADC Timing Diagram, Single Conversion



- Each conversion takes 13 clocks so:
  - ADC clock = 200KHz----> 200KHZ/13HZ ~15K sample (15ksps)
- More Info: Characterization and Calibration of the ADC on an AVR can be found at:
  - http://www.atmel.com/dyn/resources/prod_documents/doc2559.pdf