CMPE 310: Systems Design and Programming

Course Instructor: Dr. G. Slaughter
(Preferred) Email: gslaught@umbc.edu
Office Hours: ITE 311 MW 11:00-12:00pm[1]
Other Hours: **By Appointment Only**

Teaching Assistants:
Md Qumrul Hasan (mhasan4@umbc.edu)
Office Hours: TR 9:00 – 10 AM
Michael Daugherty (mda1@umbc.edu)
Office Hours: F: 10:00 – 12:00 pm
Grader: Ankit Baingane (ankitb1@umbc.edu)

Lect: MW 2:30-3:45 ITE 233; Lab I: F 1:00 – 2:50 ITE 375; Lab II: F 3:00 – 4:50 ITE 375

Prerequisite: CMPE 212 and CMSC 201

General Course Objectives & Outcomes:
The course's general objective is to introduce students to microprocessors and microprocessor systems. Students will learn the foundations of microprocessor architecture, assembly language and interfacing of peripheral devices. **Upon completion of this course, a student will be able to:**

1. Acquire basic knowledge of the Intel 80x86 microprocessor architecture to identify, formulate, and solve microprocessor based system design problems (ABET E).
2. Acquire a working knowledge of the instruction set for 80x86 microprocessors (ABET A).
3. Program and implement assembly language in the Intel 80x86 (ABET Criterion c)
4. Acquire basic knowledge of the memory and I/O interfaces; address decoding and bus transactions (ABET E).
5. Acquire a working knowledge of the interrupt-based control model, including software and hardware interrupts (ABET E).
6. Write and debug assembly programs using design tools for microprocessor system design, test and evaluation (ABET K)

To be successful, follow these steps:

1. Out-of class: **Read the textbook and the lecture notes** for basic factual information needed for the lecture, lab & HW
2. Lecture: Show up and actively participate by taking notes and attempt all class examples
3. Lab: **Always prepare for lab** and show up and actively participate

Text:
Barry B. Brey, The Intel Microprocessors…, 8th edition, Pearson/Prentice Hall (2009).

Grading:
The distribution weights are as follows:

- 35% Labs (Labs 15%; Project I 10%; Project II 10%)
- 15% HW
- 10% In-class exercises
- 15% Midterm exam
- 25% Final exam

90+ = A, 80+ = B, 70+ = C, 60+ = D, etc.

- **Late penalty is 15% week, limit 45%**
- Late HW & Lab policy: **No late HW or project will be accepted after 11:00 PM on 5/15/17**

Disabilities: If you require accommodation for any physical or learning disability, please see me.
Academic integrity: Cheating in this course will cause you to fail the course. Academic misconduct could result in disciplinary action that may include, but is not limited to, suspension or dismissal (see the full Student Academic Conduct Policy)

[1] I also have an open door policy, so feel free to stop by if the door to my office is open.

Tentative Course Plan

Week	Topic(s)	Reading Chapter	Assign	Due-Weds	Disc-Labs (F)
1/30 2/1	Course Introduction Evolution of the microprocessor	 1	**HW1**	 **HW1**	No Disc/Lab
2/6 2/9	80x86 Architecture Address Space & Data Organization	1.1-1.2	**HW2**		No Disc/Lab
2/13 2/15	80x86 Hardware Specification Bus Timing	9.1-9.5		 **HW2**	Lab0: Intro to CAD Capture CIS
2/20 2/22	Memory Interfaces	10.1-10.2	**HW3**		Lab1: Allegro PCB Design
2/27 3/1	Memory Interfaces Memory Interfaces	10.3 10.1			Project I Assigned Lab2:8086 & Clk gen
3/6 3/8	Memory Interfaces	10.4-10.6		 **HW3**	Lab3. CMOS flash & SRAM memory,16L8
3/13 3/15	Basic I/O Interfaces Basic I/O Interfaces	11.1-11.2 11.3	**HW4A**		No Lab
3/20 3/22	Spring Break				
3/27 3/29	Basic I/O Interfaces	11.3-11.4		 **HW4A†**	Lab4: PPI & Keyboard/ Display Interface
4/3 4/5	**Midterm Review Sheet** **Midterm Exam → Apr. 5**	 1, 9-10			Lab4: PPI & Keyboard/ Display Interface
4/10 4/12	Basic I/O Interfaces	11.4-11.5	**HW4B**		Lab5: PIT
4/17 4/19	Interrupts	6.4-6.5 12		 **HW4B**	Lab6: UART & MAX 235
4/24 4/26	Programming Model Stack Memory	1.3-1.4 3.3, 4.2	**HW5**		Lab7: PIC
5/1 5/3	Addressing Modes Data Movement	3.1-3.2 4.1,4.3,4.5		 **HW5**	Lab8: PCB Design Prelab due at start of lab
5/8 5/10	Arithmetic Instructions Logic Instructions	5.1-5.2 5.1	**HW#6**		Lab9: NASM Project I Report due Project II – In-class Lab
5/15	Logic Instructions	5.4-5.5		**HW#6***	
5/19	**Final Exam (ITE 233)**	1:00 – 3:00 PM			

†Note HW#4A cannot be turned in late solutions will be posted Wednesday evening
***Note HW#6 due on a Monday**
Changes/ Additions to this schedule will be posted on Blackboard