CMPE 212

Principles of Digital Design

Lecture 6

Logic Gates

February 10, 2016

www.csee.umbc.edu/~younis/CMPE212/CMPE212.htm

Lecture's Overview

Previous Lecture:

- ➔ Multiplication and division of binary numbers
  (unsigned numbers, determining the sign of the results)
- ➔ Binary codes (BCD, Character representation)
  (BCD, ASCII, EBCDIC, Unicode, Gray, etc.)
- ➔ Representations for floating point numbers
  (Format, scientific notation, standard notation)
- ➔ Error detect and correction codes
  (weight, Hamming distance, Hamming codes)

This Lecture:

- ➔ Logic gates
- ➔ Relay and transistor based implementation of logic gates

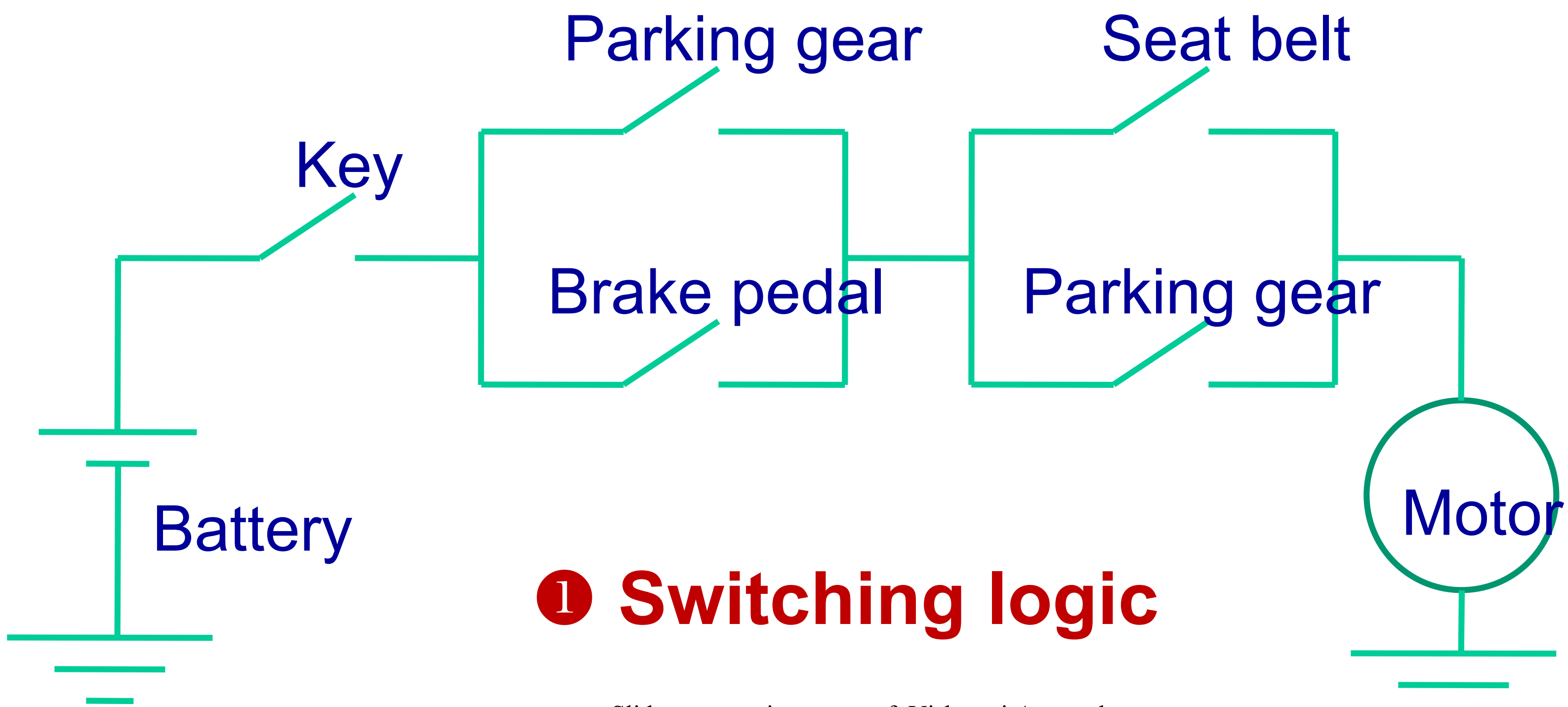
Example: Automobile Ignition

Engine turns on when: Ignition key is applied AND

- Car is in parking gear OR Brake pedal is on

AND

- Seat belt fastened OR Car is in parking gear



❶ **Switching logic**

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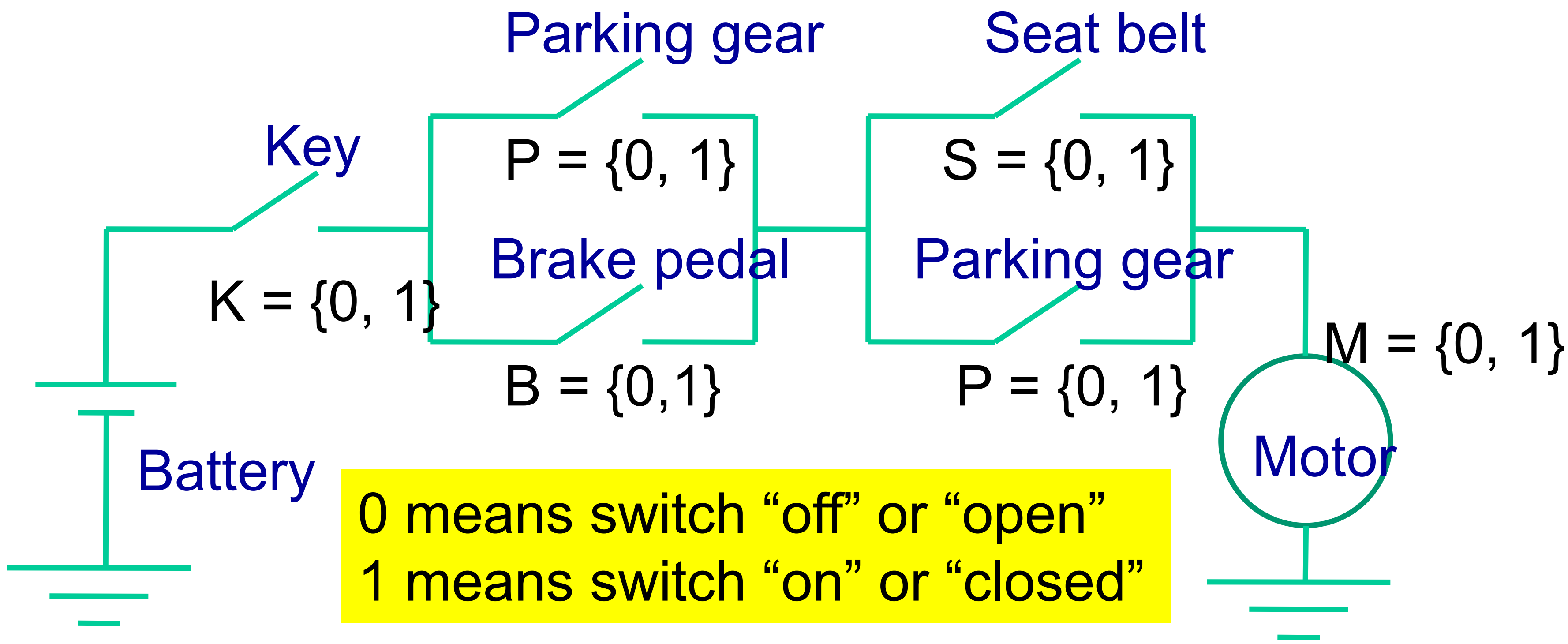
Automobile Ignition Control

❷ Define Boolean Variables



0 means switch "off" or "open"
1 means switch "on" or "closed"

❸ Write Boolean Function

$$M = K \text{ AND } (P \text{ OR } B) \text{ AND } (S \text{ OR } P)$$

$$= K(P + B)(S + P)$$

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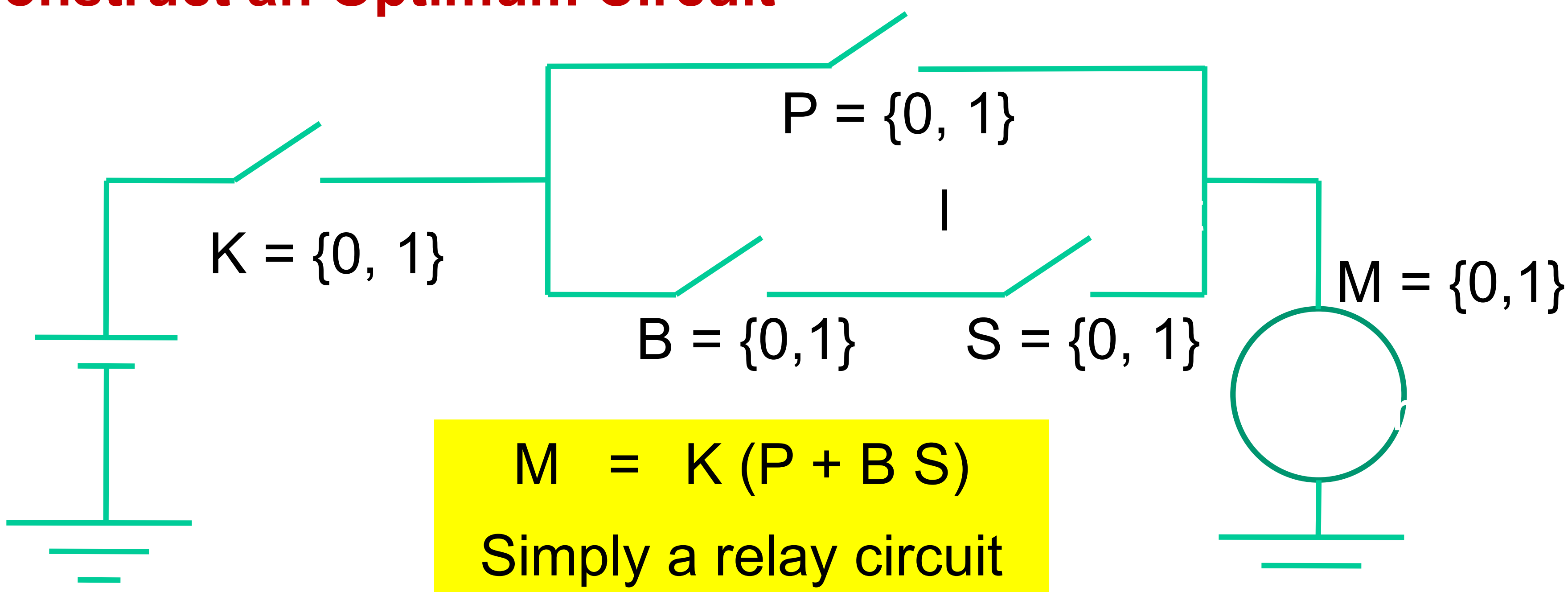
Automobile Ignition Control

❹ Simplify Boolean Function

$$
\begin{aligned}
M &= K(P + B)(S + P) & \\
&= K(P + B)(P + S) & \textit{Commutativity} \\
&= K\,(P + B\,S) & \textit{Distributivity}
\end{aligned}
$$

❺ Construct an Optimum Circuit



$$M = K\,(P + B\,S)$$

Simply a relay circuit

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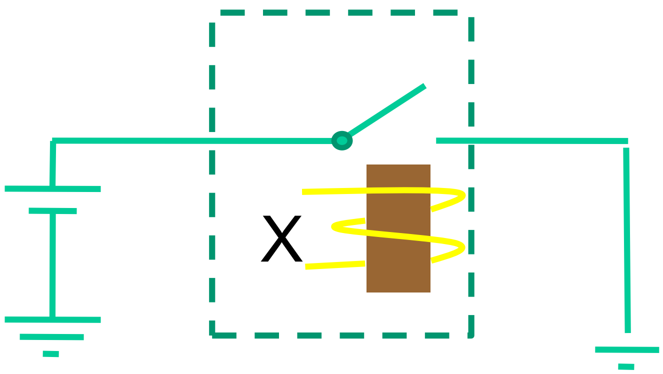
Implementing the Ignition Control

- Switching Devices
  - Electromechanical relays (1940s)
  - Vacuum tubes (1950s)
  - Bipolar transistors (1960 - 1980)
  - Field effect transistors (1980 -)
  - Nanotechnology devices (future)



- Implement the Ignition control using relays
  - An electromechanical relay contains:
    - Electromagnet
    - Current source
    - A switch, spring-loaded, normally open or closed
  - Switch has two states, open (0) or closed (1).
  - The state of switch is controlled by “not applying” or “applying” current to electromagnet

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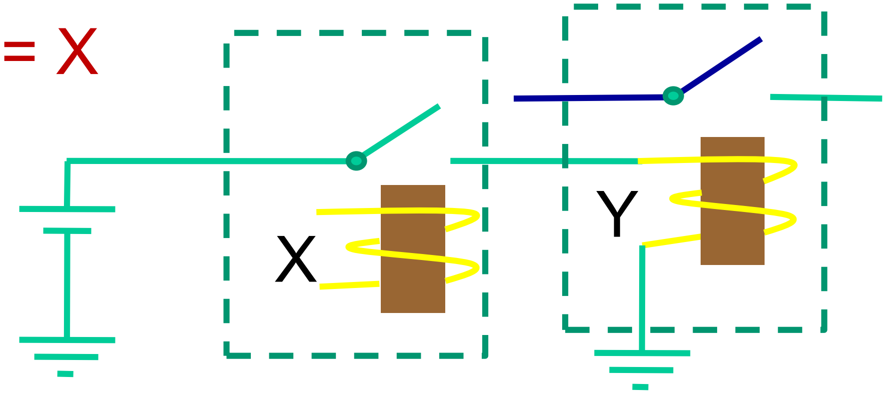
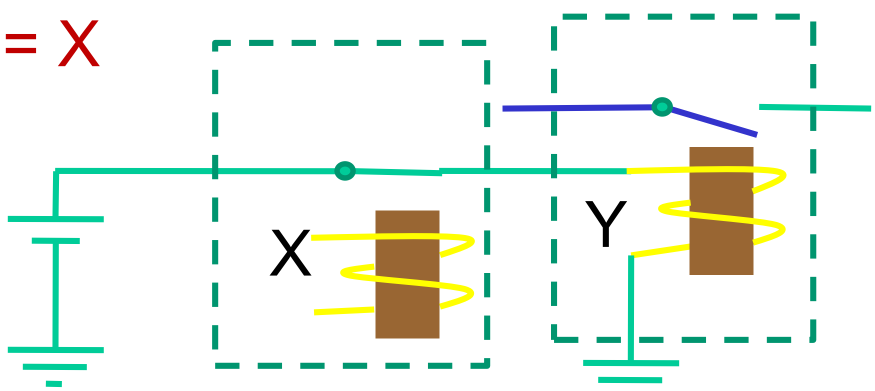
One Switch Controlling Another

$Y = X$



- Switches X and Y are normally open
- Y cannot close unless a current is applied to X

$Y = \overline{X}$

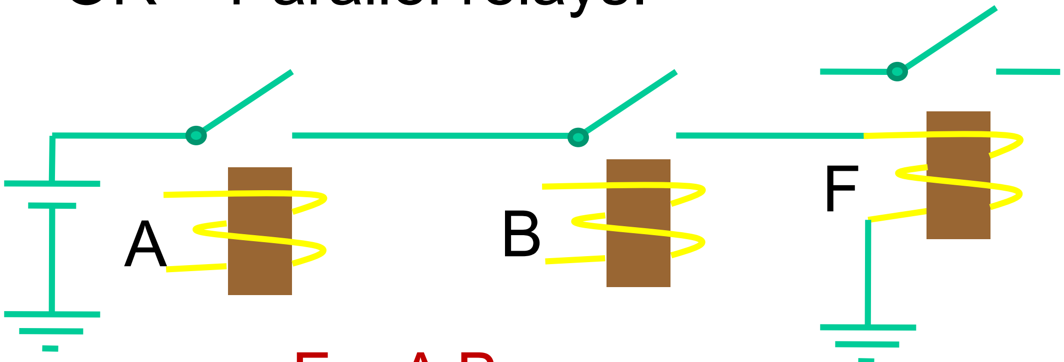


Inverting Switch

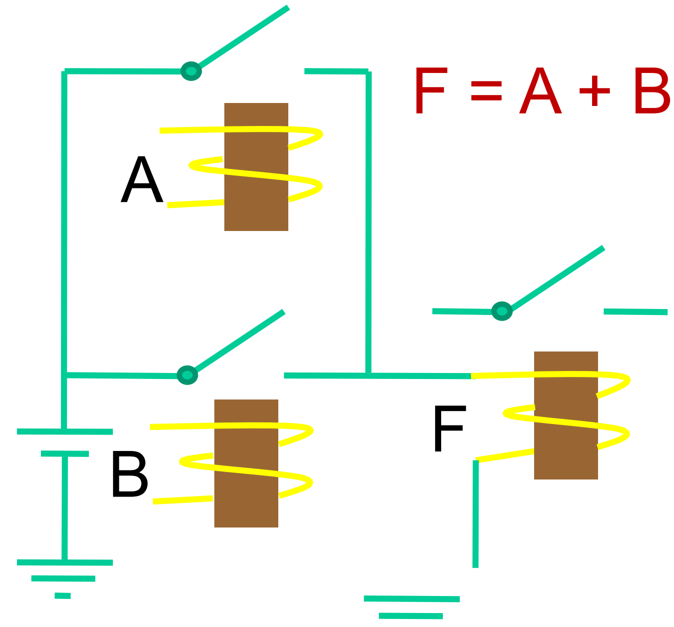
- Normally switch X is closed and Y is open
- Y cannot open unless a current is applied to X

Boolean Operations

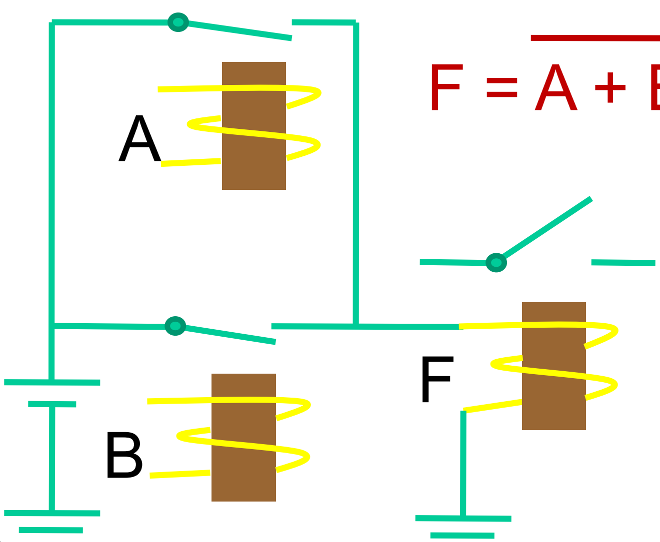
- AND – Series connected relays.
- OR – Parallel relays.



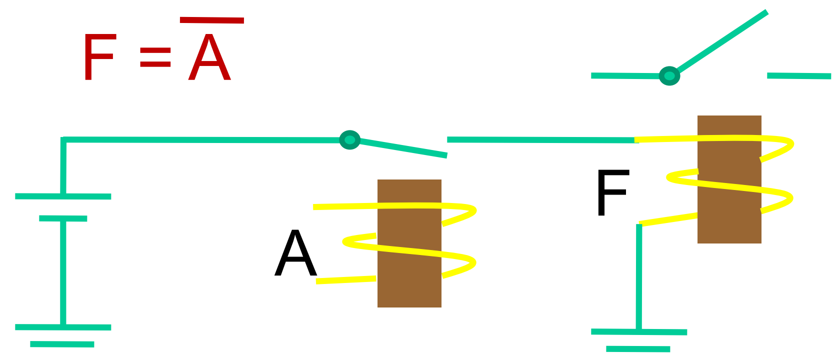
$F = A\,B$



$F = A + B$



$F = \overline{A + B}$



$F = \overline{A}$

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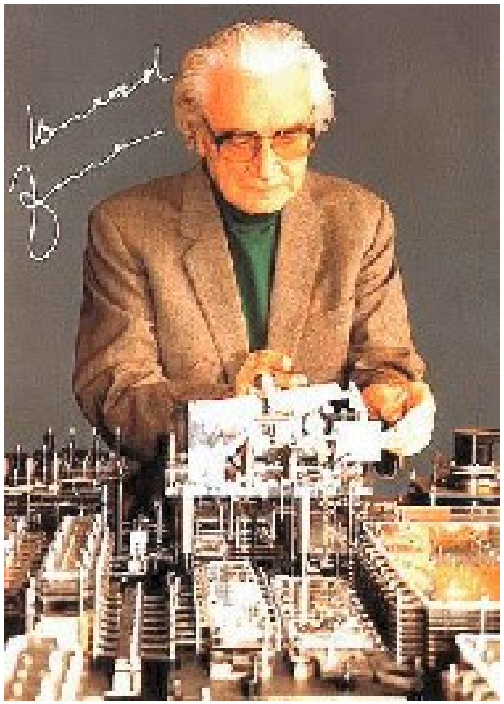
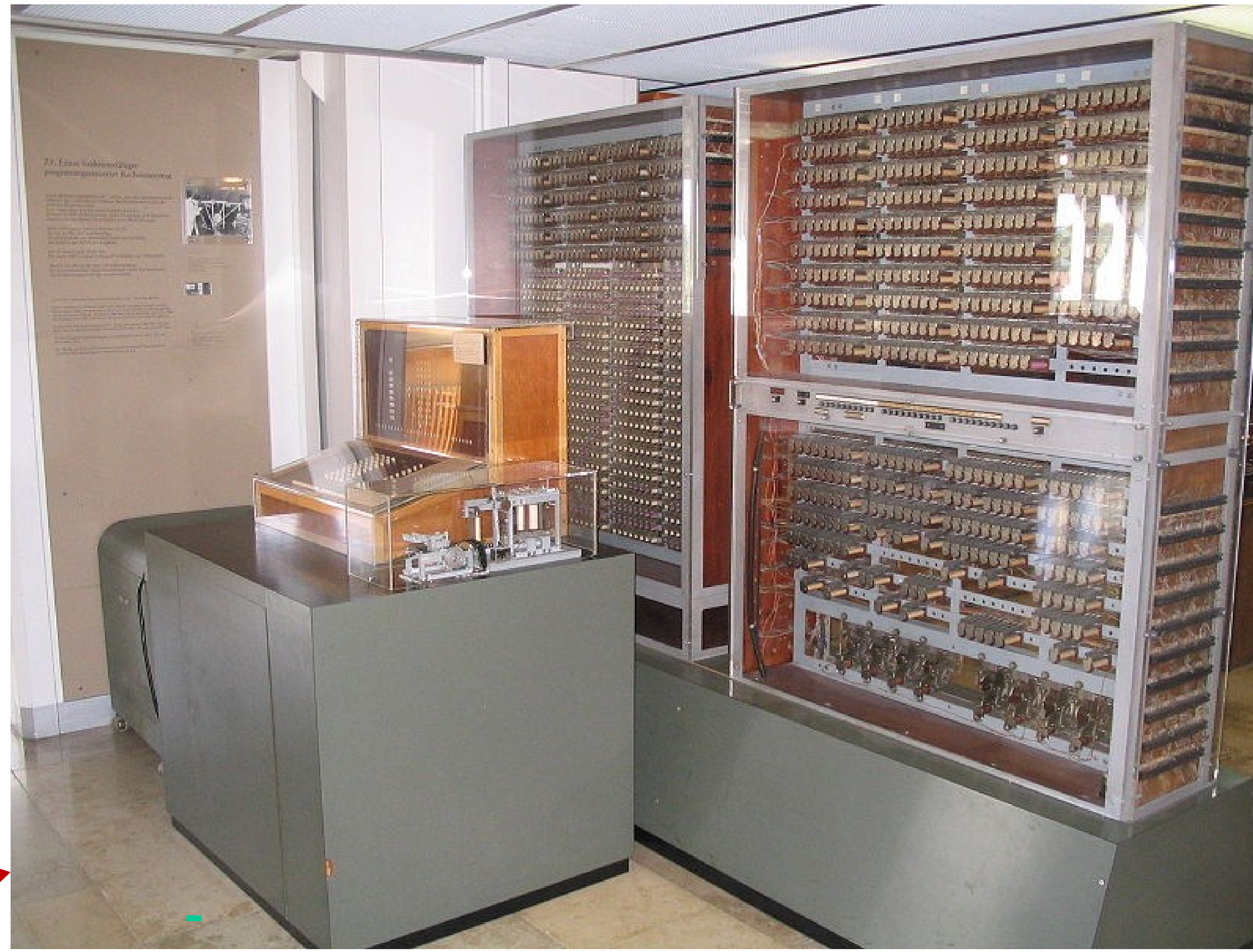
Relay Computers
Conrad Zuse (1910-1995)

Z1 (1938)





Z3 (1941)

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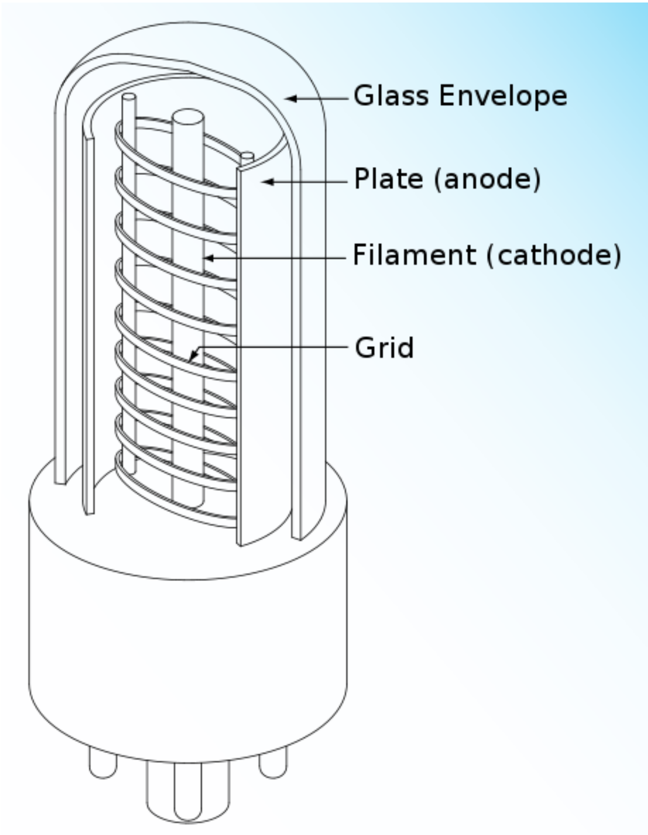
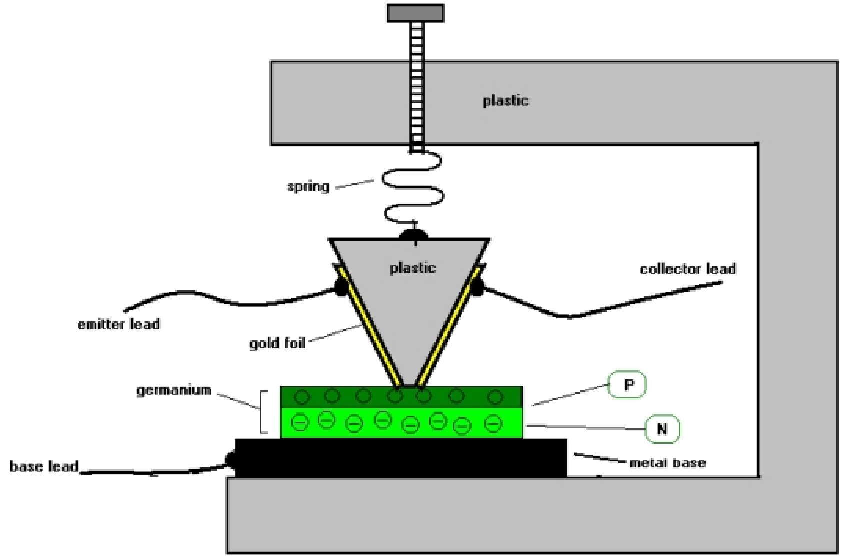
Electronic Switching Devices



Electron Tube
Fleming, 1904
de Forest, 1906



Point Contact Transistor
Bardeen, Brattain, Shockley,
1948, Nobel Prize, 1956

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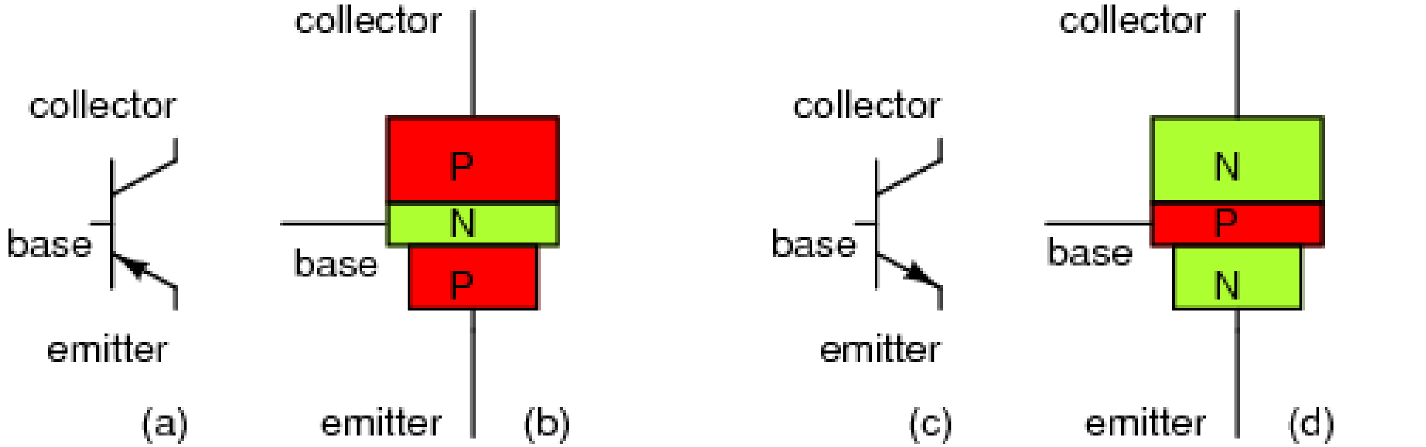
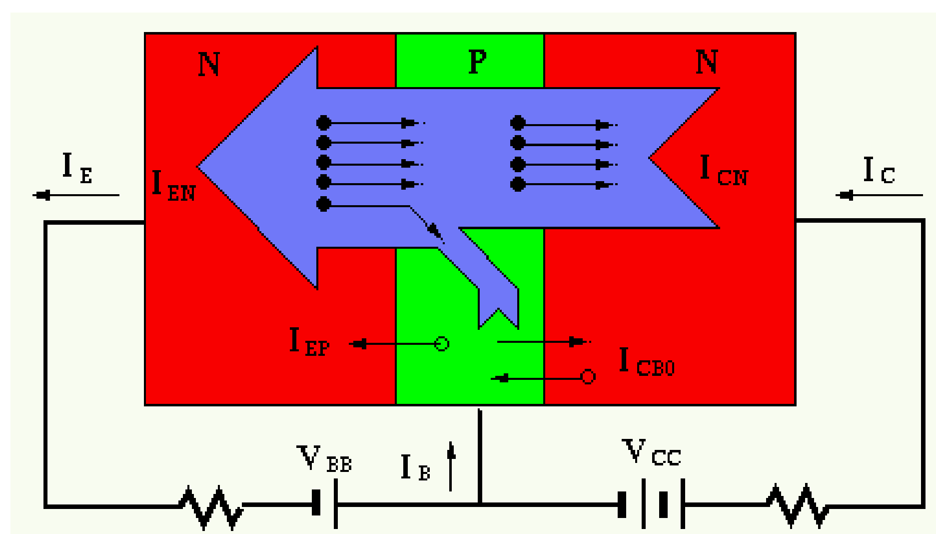
Bipolar Junction Transistor



- *Dipolar*: Charges flow through the base
- *MOSFET*: the base becomes a gate



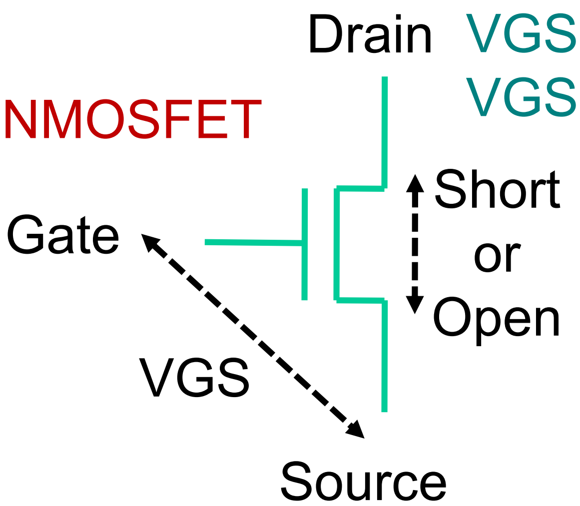
MOSFET

Metal Oxide Semiconductor

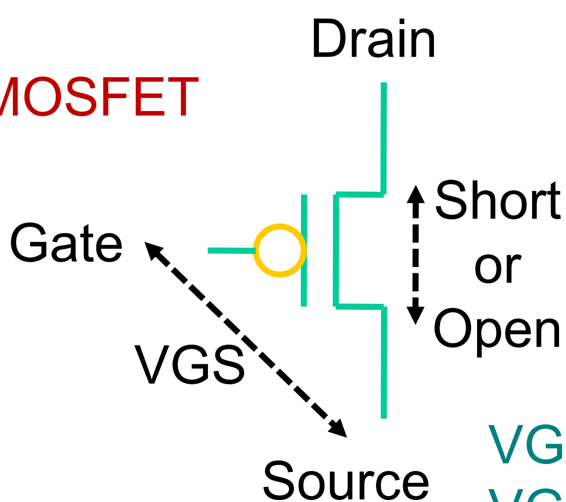
Field Effect Transistor

NMOSFET

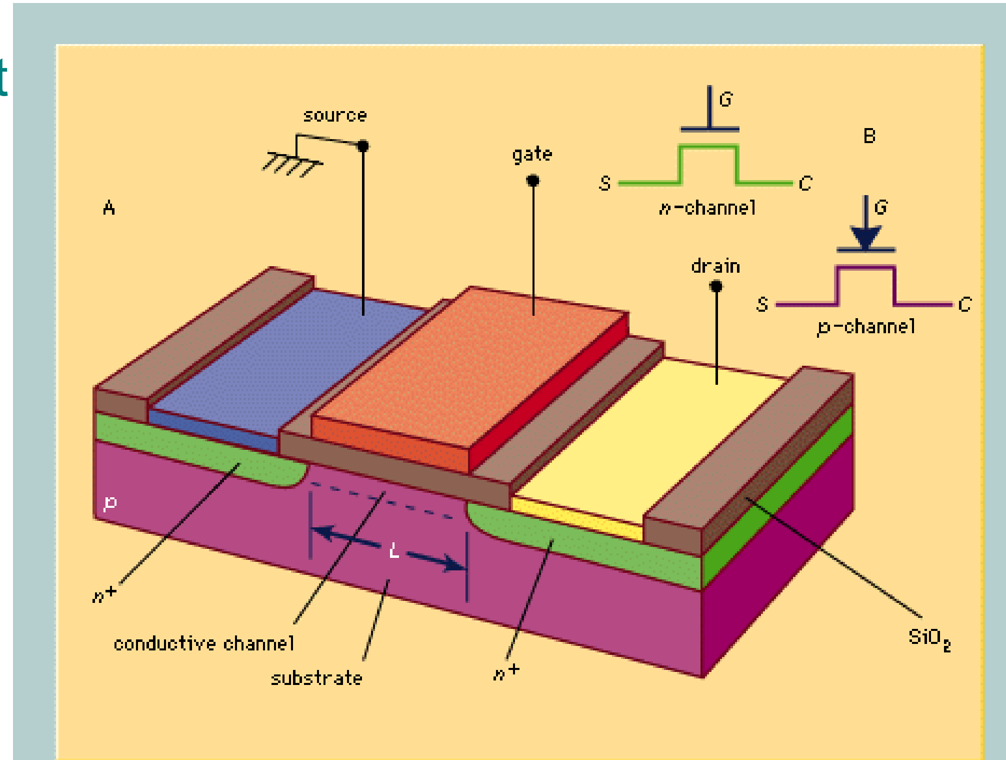
VGS = 0, open
VGS = high, short



PMOSFET



VGS = 0, short
VGS = high, open



Problem: When Gate is on current leakage causes power dissipation

Solution: Complementary MOS

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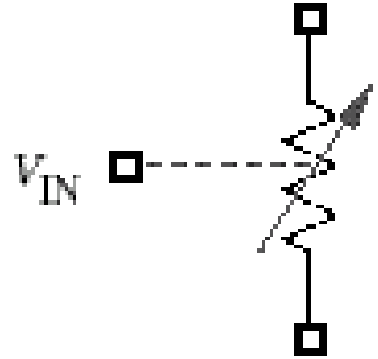
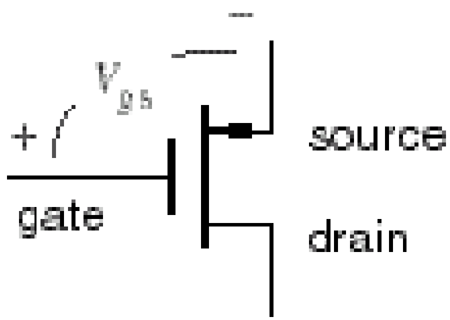
MOS Transistors

Voltage Controlled resistance

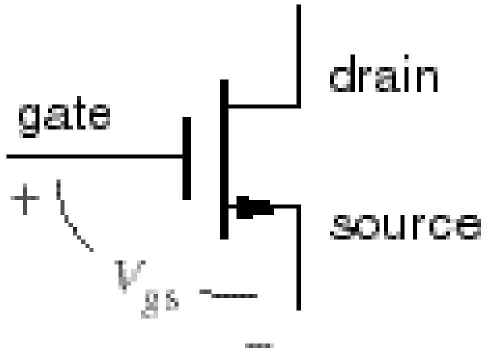


PMOS



Increase V_{gs} ➔ Increase R_{ds}

NMOS

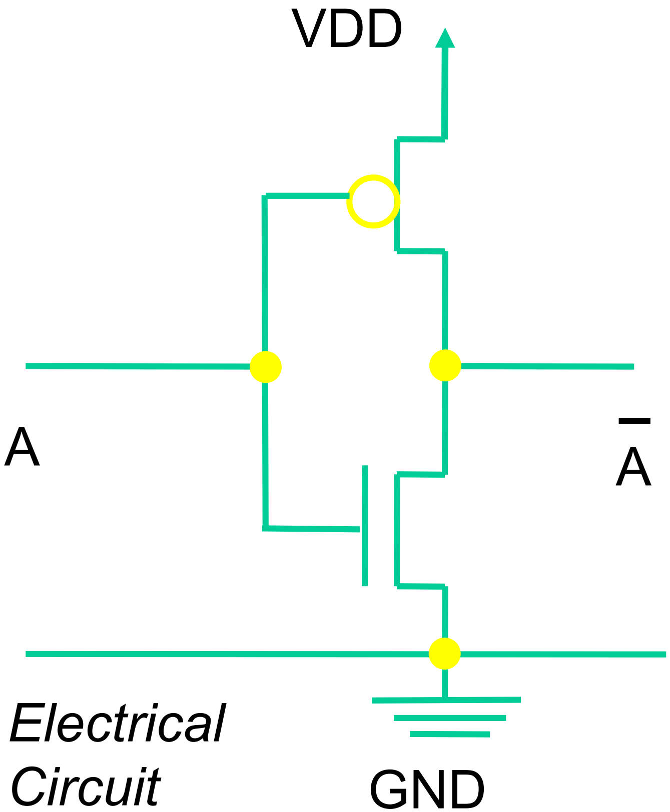


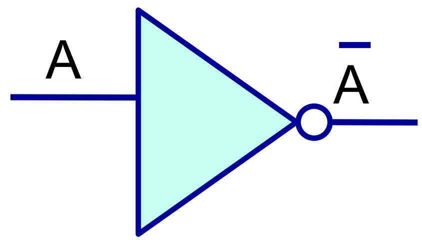
Increase V_{gs} ➔ Decrease R_{ds}

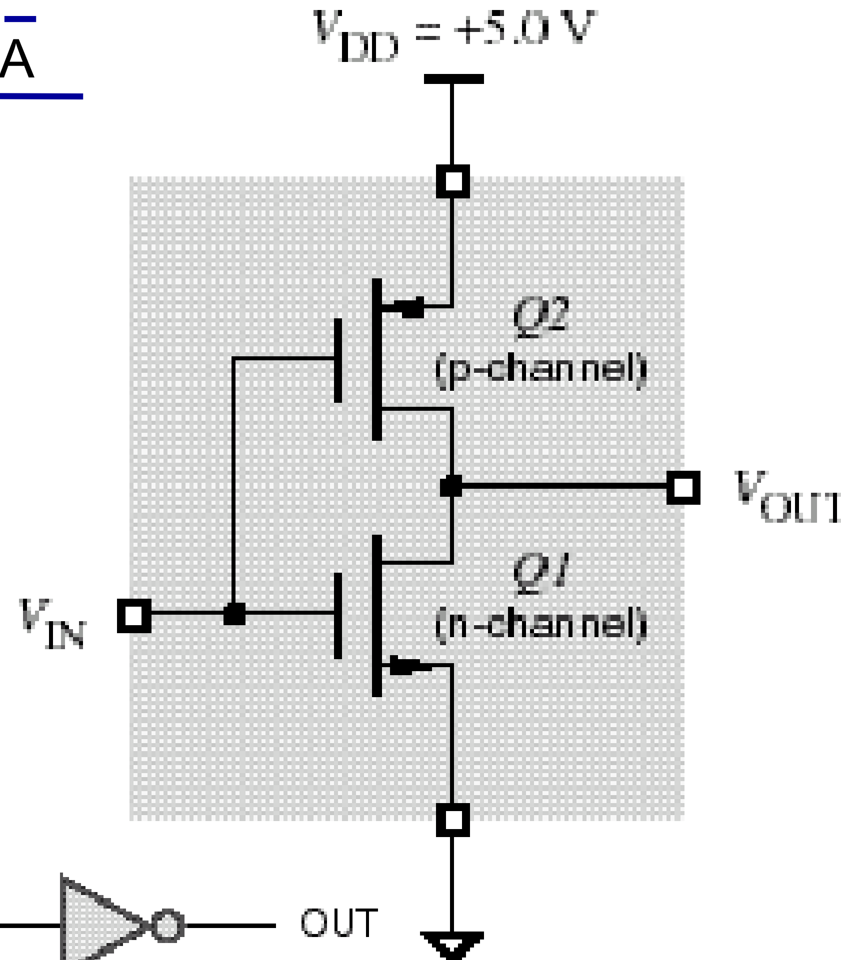
CMOS means using PMOS and NMOS transistors in a complementary way

CMOS Logic Gate: Inverter

PMOS and NMOS transistors are used in a complementary way

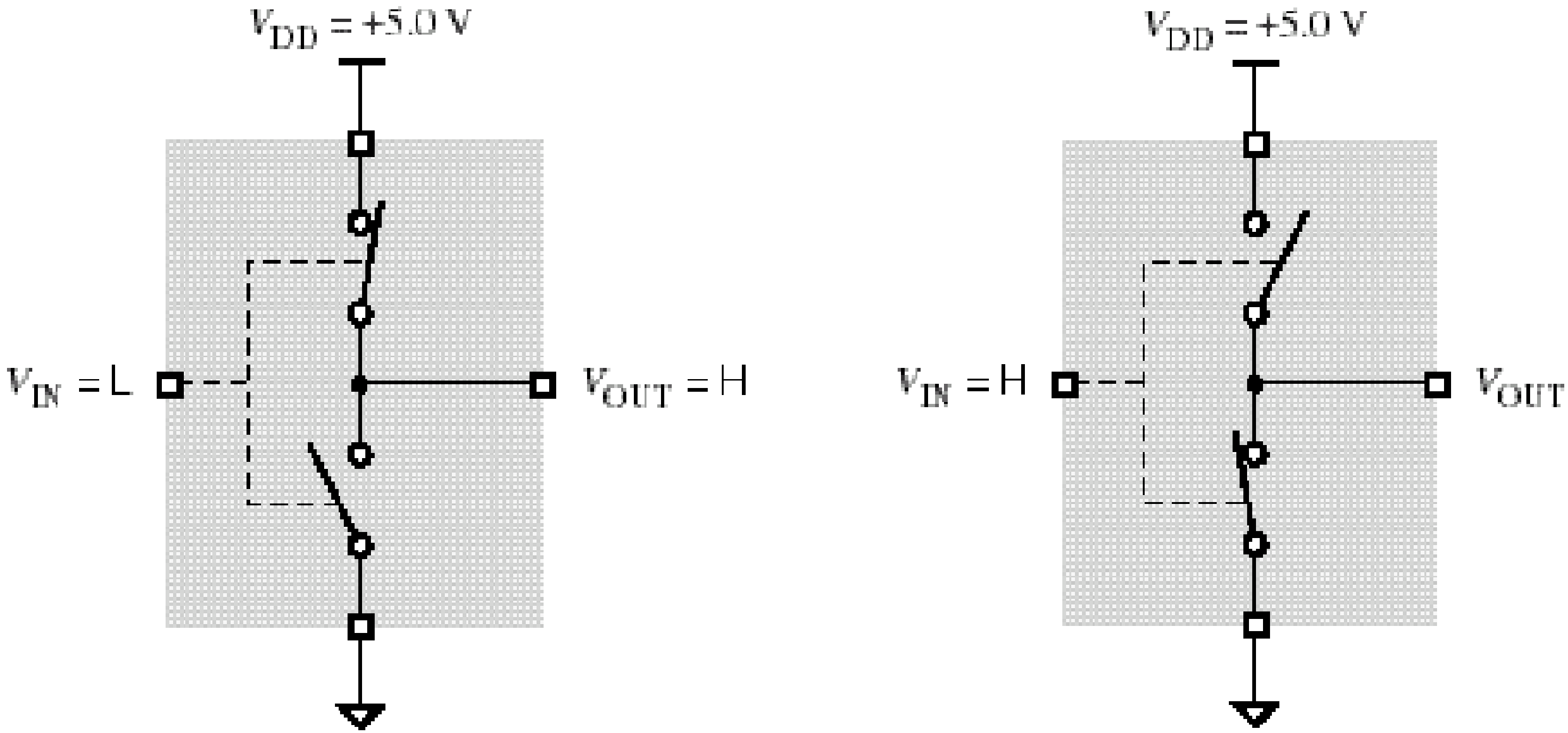






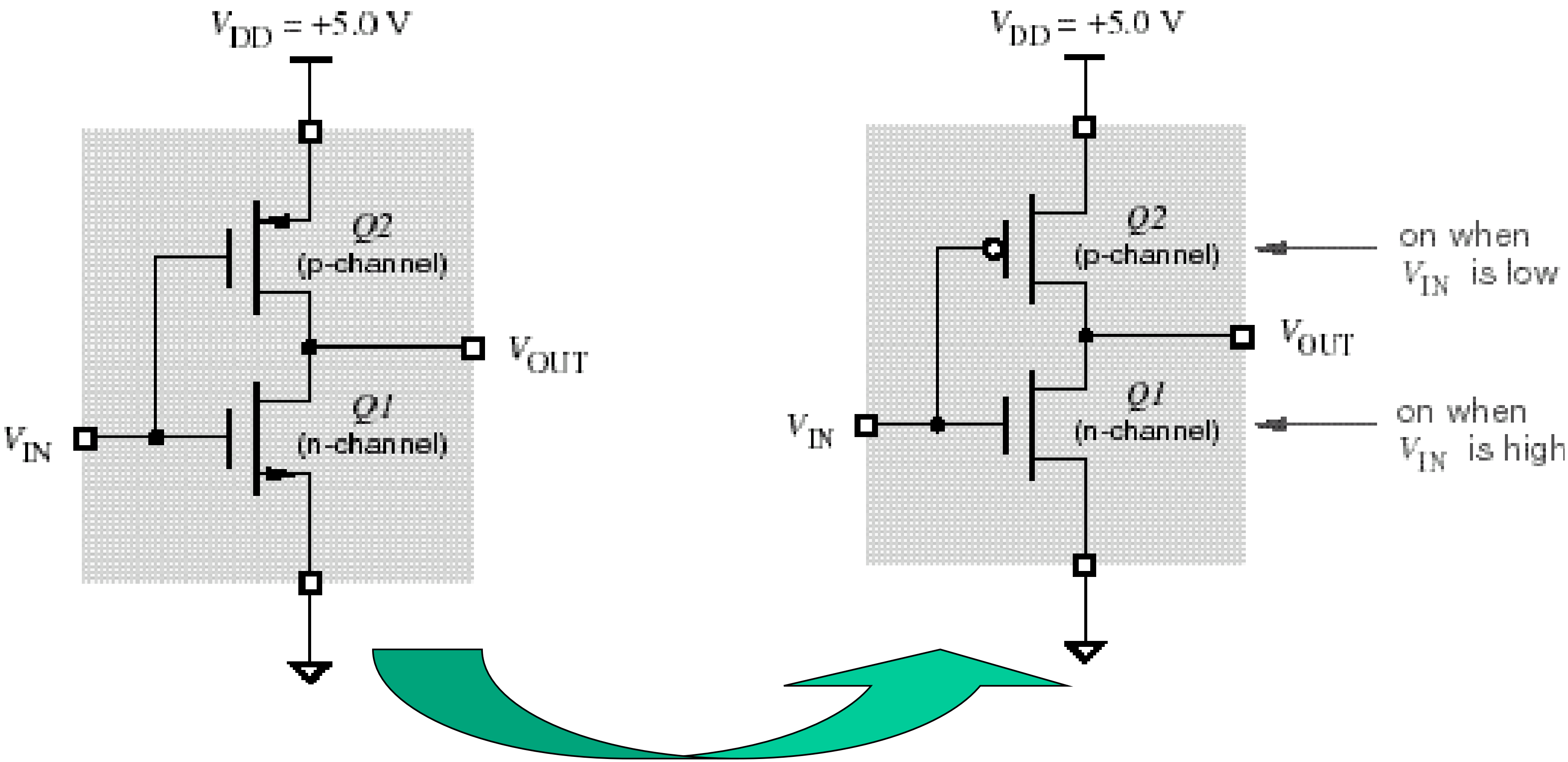
V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

Switch Model



- PMOS and NMOS transistors can be viewed as switches controlled by voltage level applied to the transistor gate

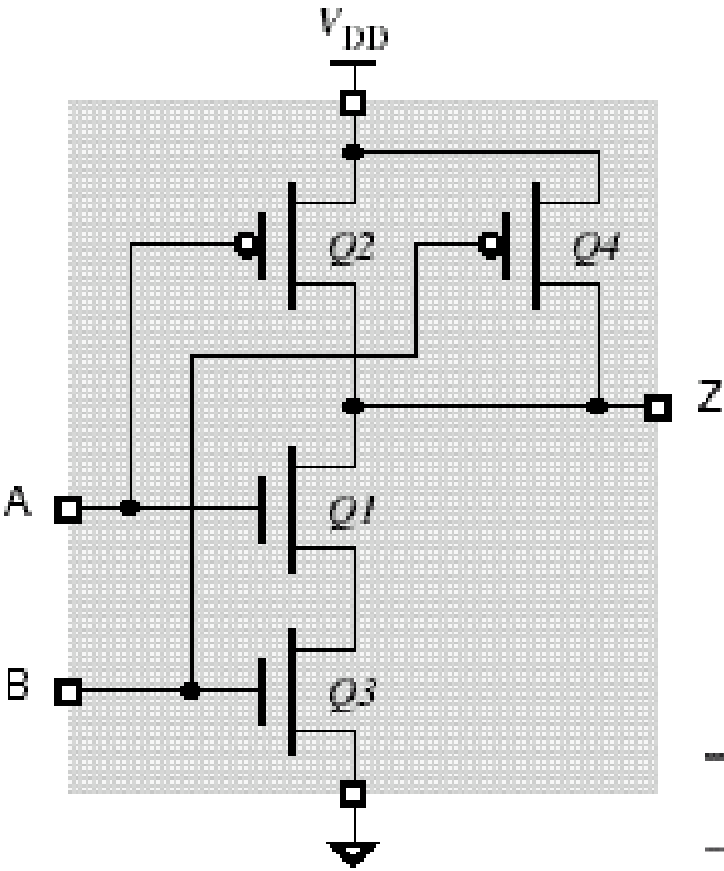
Alternative Transistor Symbols

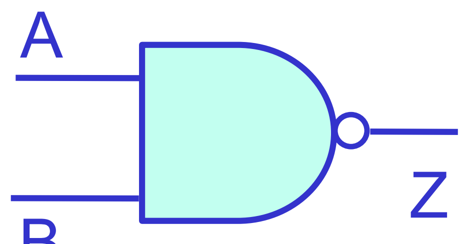


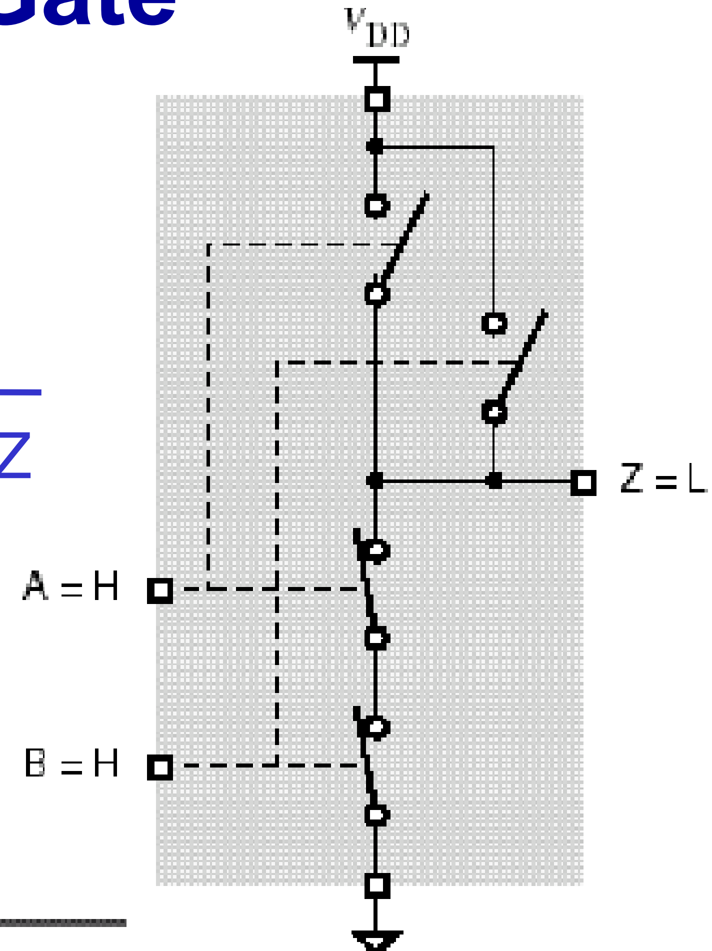
Notice the bubble at the p-channel transistor

CMOS NAND Gate

- Use *2n* transistors for n-input gate



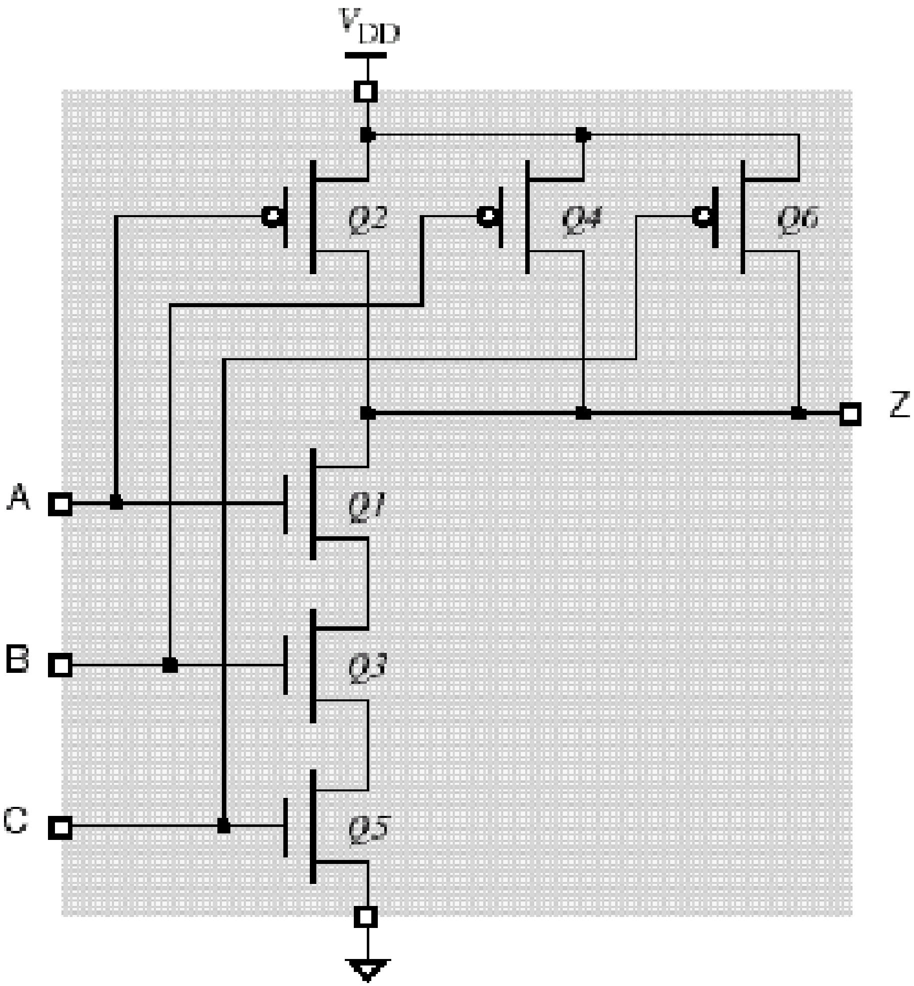




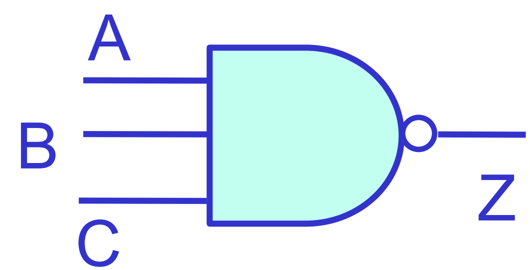
Equivalent to 2 inverters connected in parallel (OR)

A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

3-Input CMOS NAND Gate



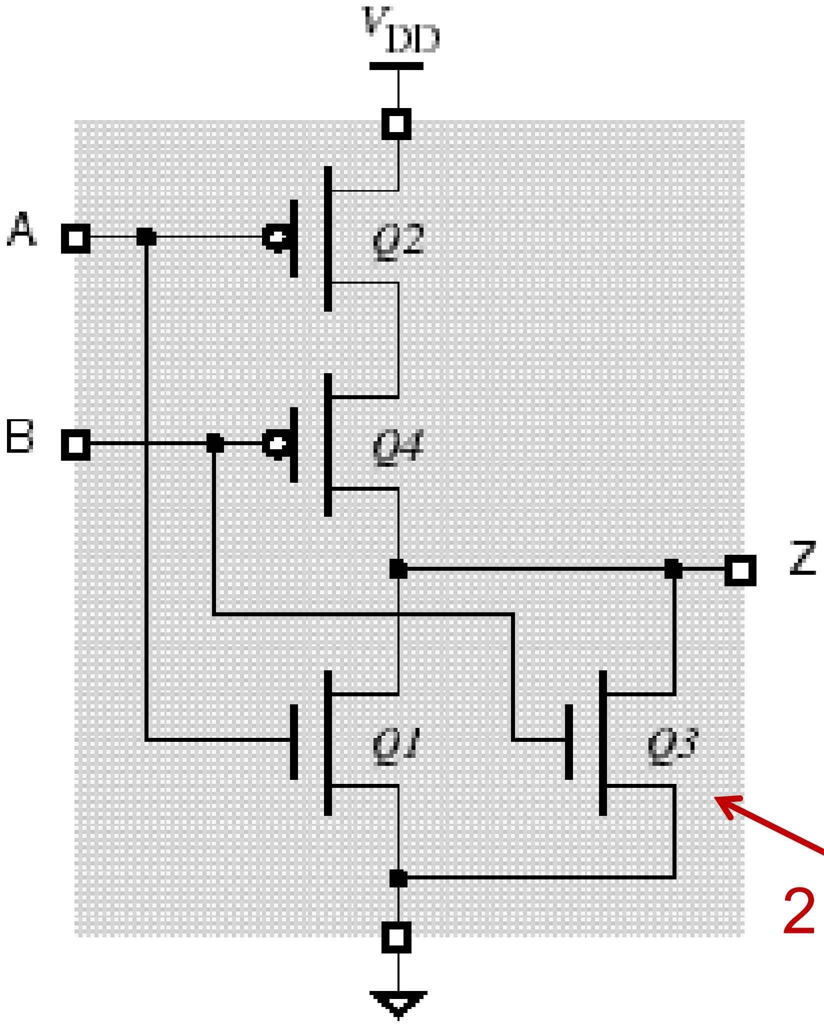
A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	L	off	on	off	on	off	on	H
L	L	H	off	on	off	on	on	off	H
L	H	L	off	on	on	off	off	on	H
L	H	H	off	on	on	off	on	off	H
H	L	L	on	off	off	on	off	on	H
H	L	H	on	off	off	on	on	off	H
H	H	L	on	off	on	off	off	on	H
H	H	H	on	off	on	off	on	off	L

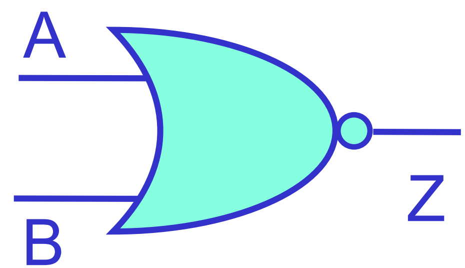


Basically, 3 inverters connected in parallel (OR configuration of relays)

2-Input CMOS NOR Gate

- Like NAND -- *2n* transistors for n-input gate

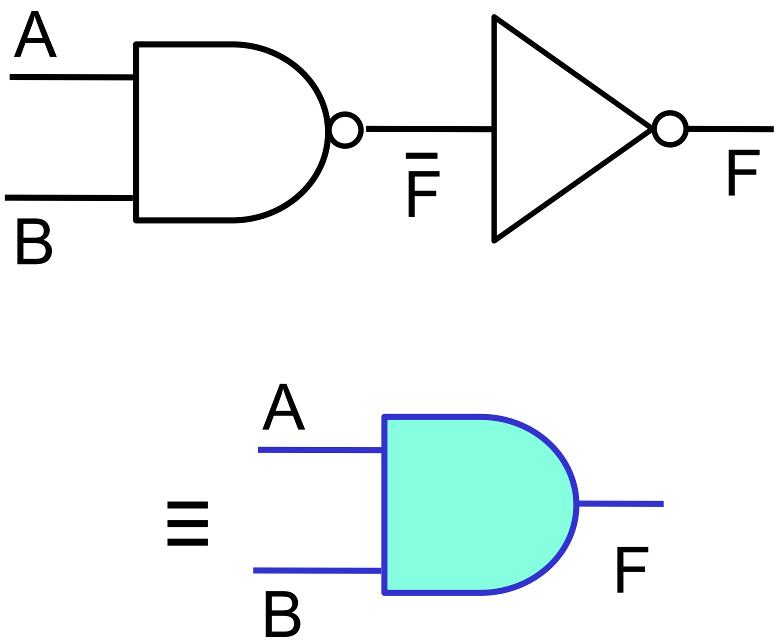


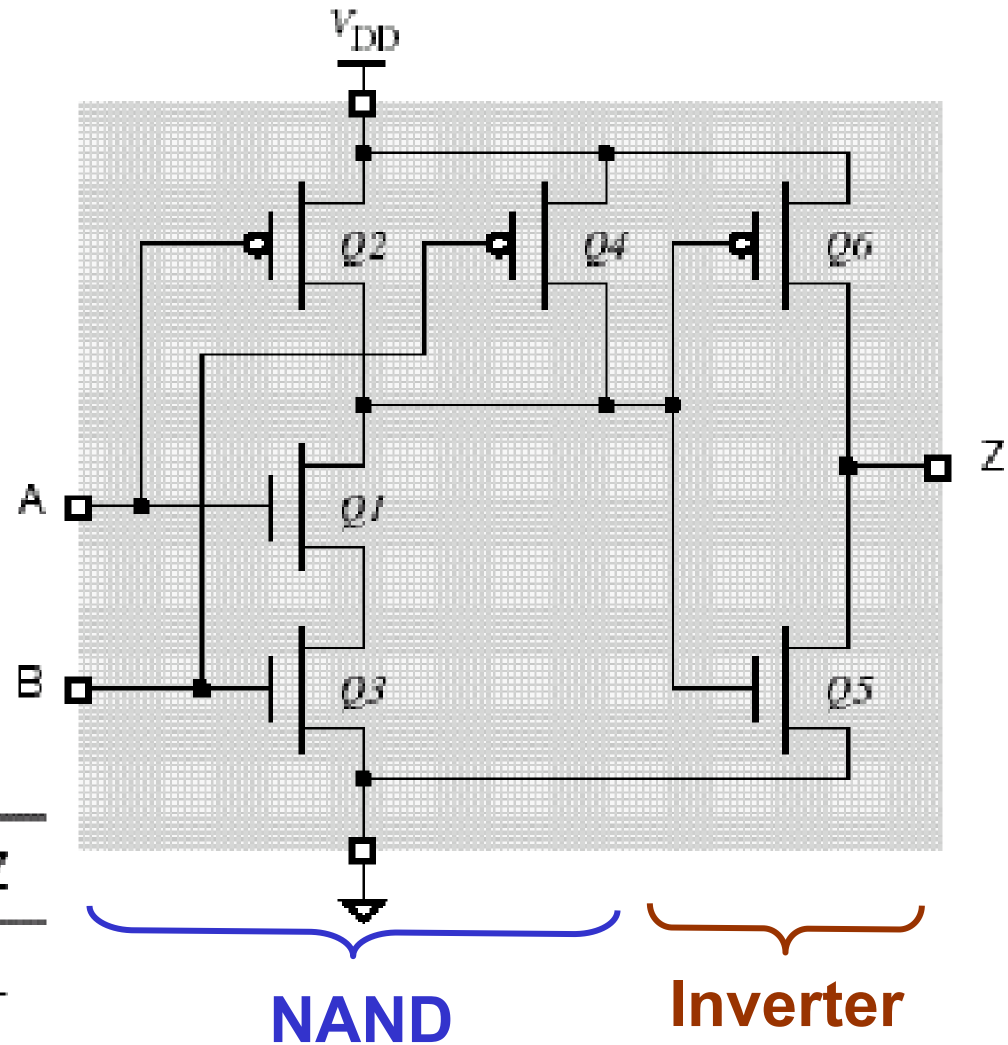


A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

2 inverters connected in series (AND)

2-Input CMOS AND Gate





A	B	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	L
H	L	on	off	off	on	on	off	L
H	H	on	off	on	off	off	on	H

Transistor Count in CMOS Gates

Logic function	Number of transistors	
	1 or 2 inputs	N inputs
NOT	2	-
AND	6	2N + 2
OR	6	2N + 2
NAND	4	2N
NOR	4	2N

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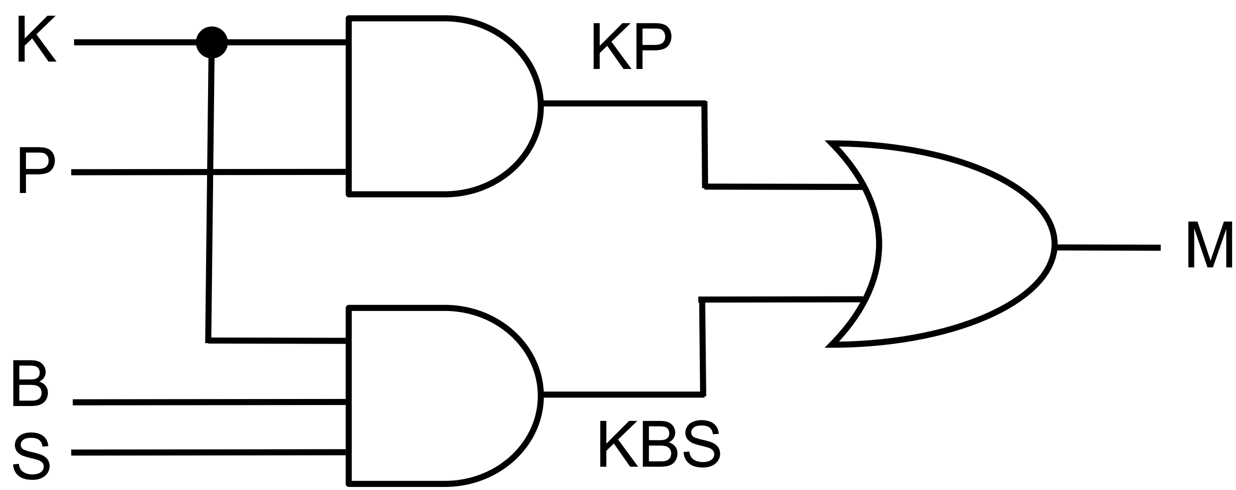
Optimized Ignition Logic

$$M = K(P + B\,S)$$
$$= KP + KBS$$



3 gates, 20 transistors. *Can we reduce transistors?*

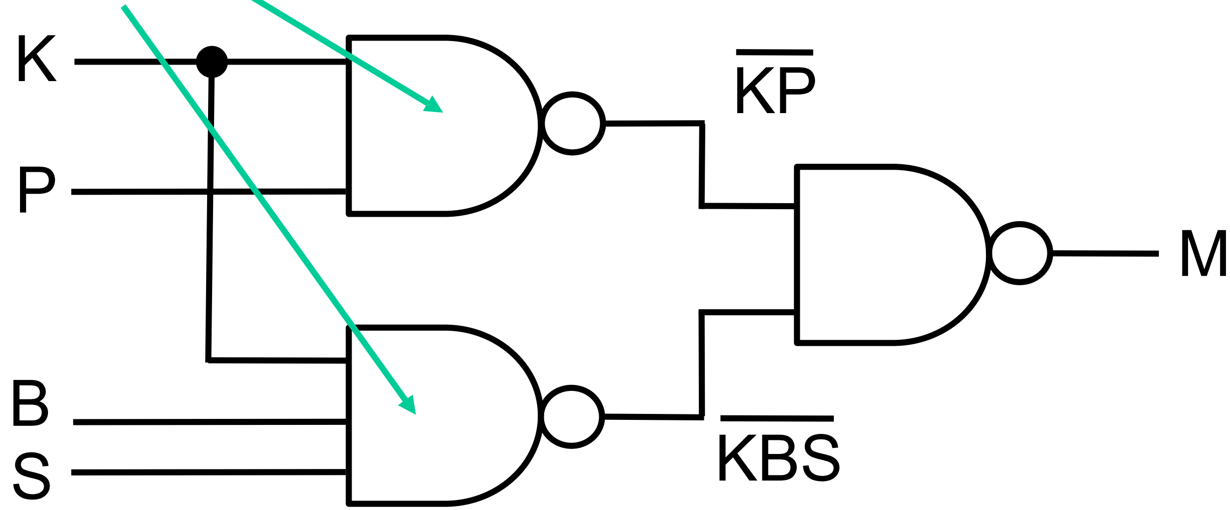
Further Optimization

$$M = K(P + BS)$$

$$= \overline{\overline{KP + KBS}} \quad \text{(Theorem 3, involution)}$$

$$= \overline{\overline{KP} \cdot \overline{KBS}} \quad \text{(De Morgan's theorem)}$$

NAND gates
4+6 transistors



3 gates, 14 transistors.

Conclusion

❑ Summary

➔ Logic Gates

(famous gates, gate symbols)

➔ Circuit implementation of logic gates

(TTL transistors, logic equivalent voltage level, CMOS implementation)

❑ Next Lecture

➔ Switching Functions

Reading supplement from Wakely's Book