About Cadence OrCad Capture CIS:

Capture CIS is an EDA (Electronic Design Automation) tool. It is frequently used to create a schematic design for the **PCB (Printed Circuit Board) and FPGA project**. The simple steps involved in schematic design include placing and connecting parts, running the Design Rules Check, and generating the netlist. This tool is also capable of functional and timing simulations for the FPGA project, board level simulation for the PCB project, and analog/mixed signal simulation using PSpice.

This tutorial is the first of two parts in the PCB project tutorial and will cover all the basic steps involved in creating a schematic netlist for your PCB layout design (for the layout design tutorial see Layout Plus Tutorial).

OrCad Capture CIS Tutorial Part 1:

Opening a New Project File:

Start by opening the Capture CIS software. First go to: Start Menu → All Programs →Cadence → Release 16.6 → OrCad Capture CIS. From the drop-down list, choose "Allegro PCB Design CIS L".

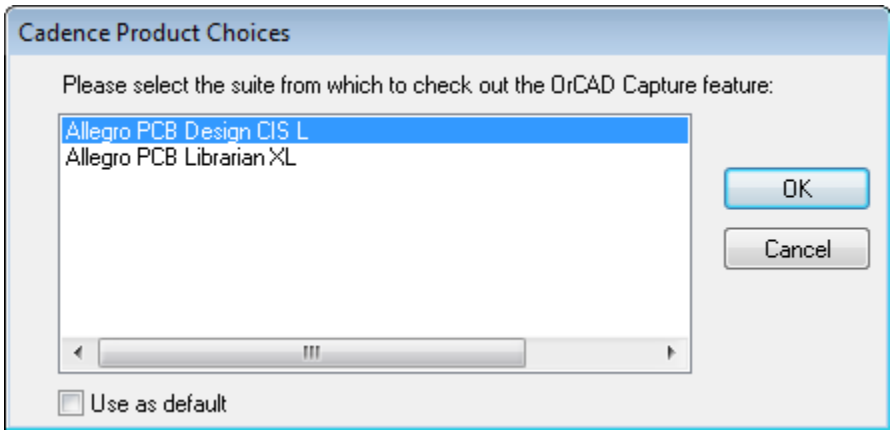


Figure 1

Create a new project file by going to File → New → Project. Give your Project a name (i.e. "Project1"), choose "Schematic," and designate a save path for your project files.

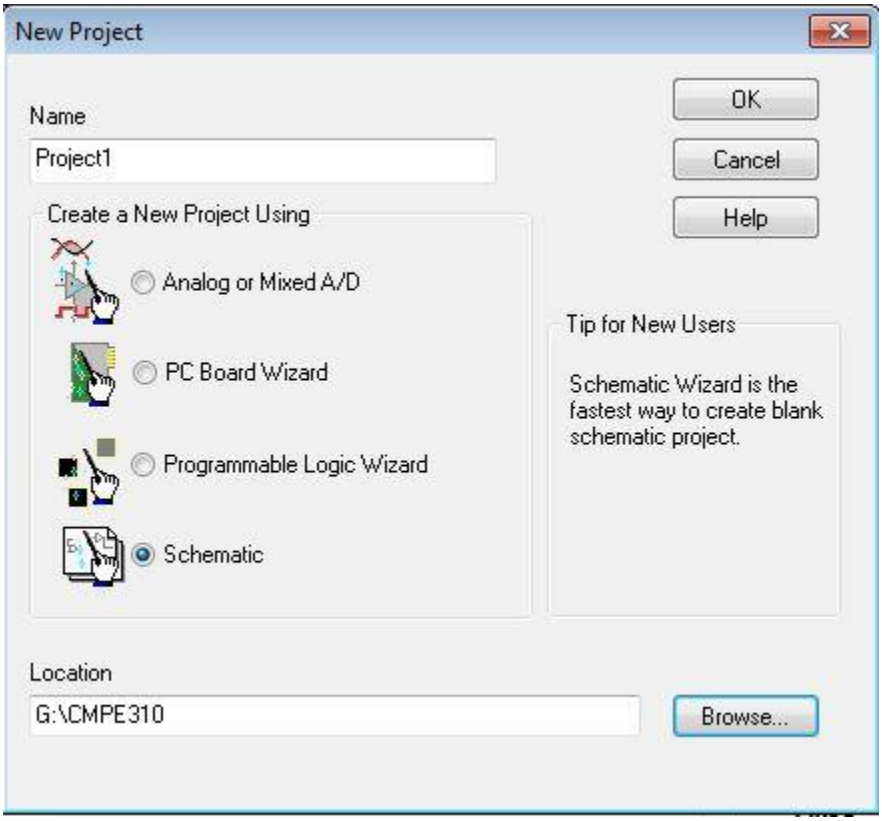


Figure 2

TIPS:

- Using a USB drive to save your project files is highly recommended, as it will come in handy later when you have many files.
- To create a new schematic page, go to the main project window, right click the schematic folder, and select "New Page."

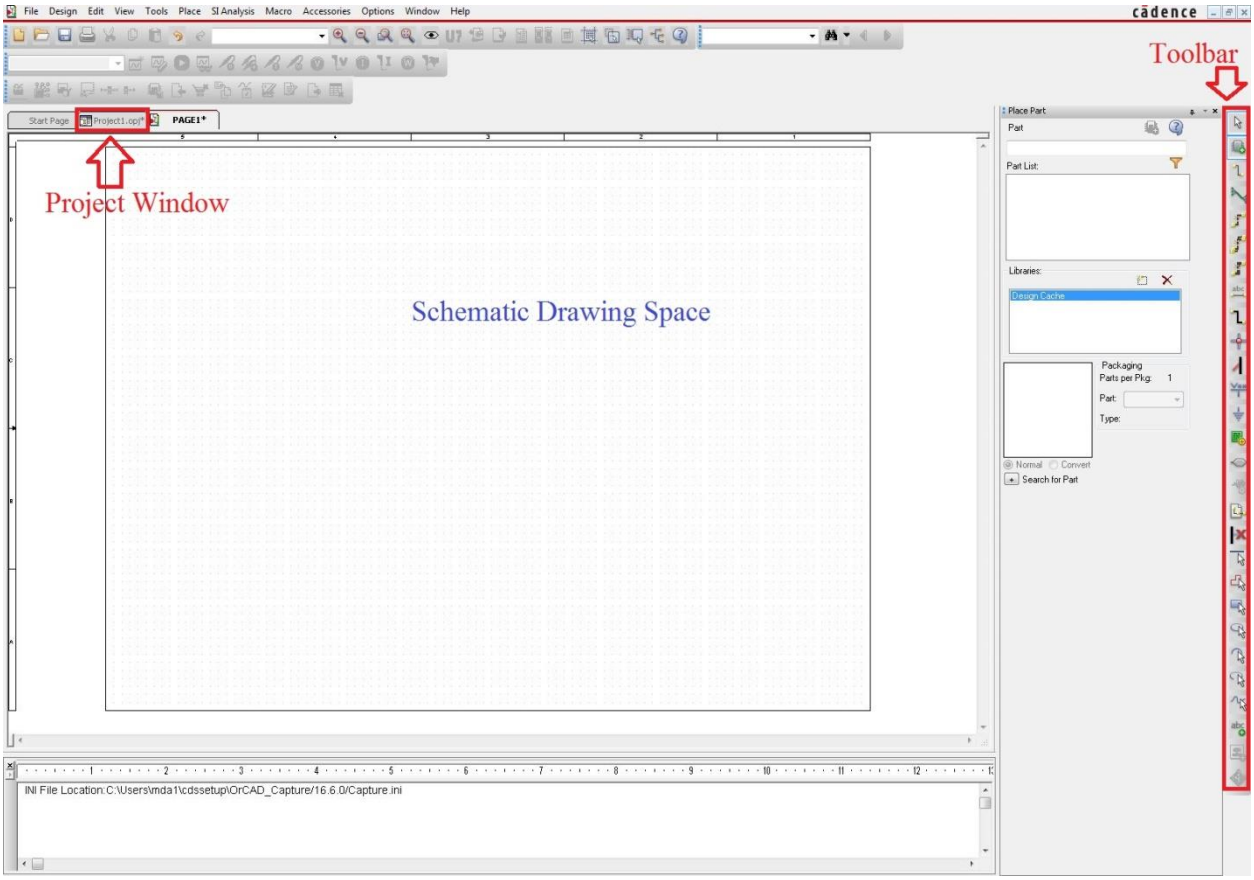


Figure 3

Before You Start Placing Parts:

Before you begin placing any components, first go to the Project window and right click on “Library,” then select “Add File” as shown in Figure 4. If the resulting window is not already in the correct folder, follow the folder path showing in Figure 5. Then select all of the files and folders and click “Open.” The results should look like Figure 6.

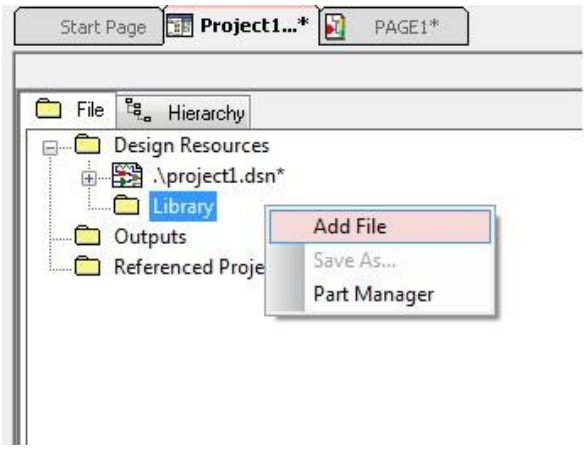


Figure 4

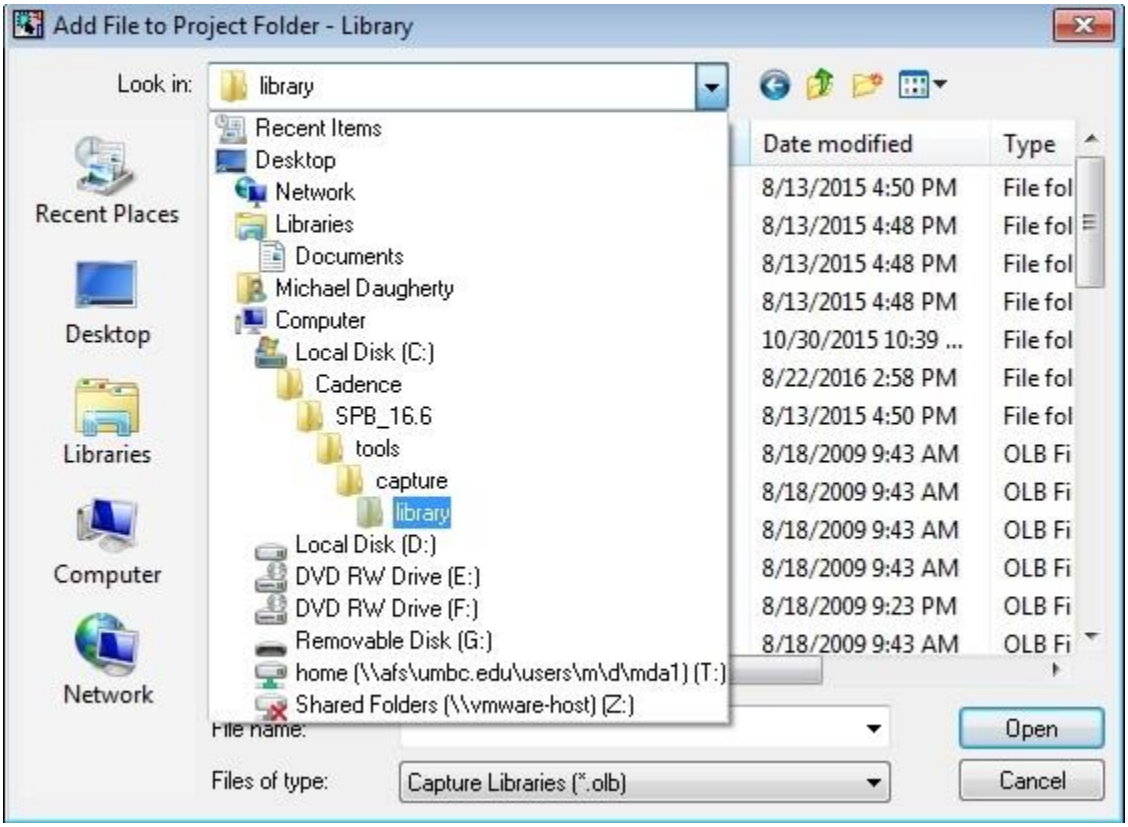
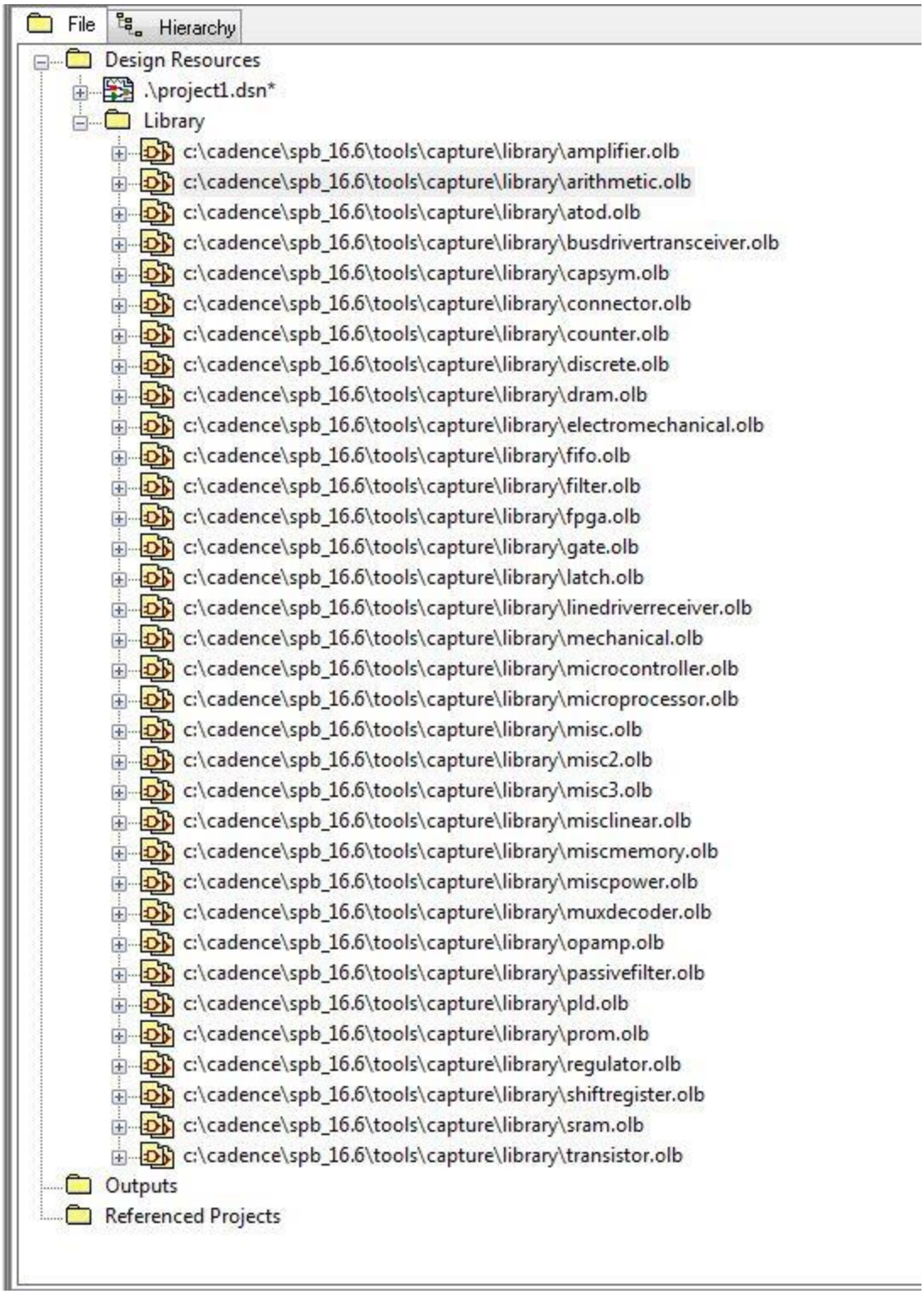


Figure 5


File
Hierarchy
Design Resources
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c:\cadence\spb_16.6\tools\capture\library\amplifier.olb
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c:\cadence\spb_16.6\tools\capture\library\busdrivertransceiver.olb
c:\cadence\spb_16.6\tools\capture\library\capsym.olb
c:\cadence\spb_16.6\tools\capture\library\connector.olb
c:\cadence\spb_16.6\tools\capture\library\counter.olb
c:\cadence\spb_16.6\tools\capture\library\discrete.olb
c:\cadence\spb_16.6\tools\capture\library\dram.olb
c:\cadence\spb_16.6\tools\capture\library\electromechanical.olb
c:\cadence\spb_16.6\tools\capture\library\fifo.olb
c:\cadence\spb_16.6\tools\capture\library\filter.olb
c:\cadence\spb_16.6\tools\capture\library\fpga.olb
c:\cadence\spb_16.6\tools\capture\library\gate.olb
c:\cadence\spb_16.6\tools\capture\library\latch.olb
c:\cadence\spb_16.6\tools\capture\library\linedriverreceiver.olb
c:\cadence\spb_16.6\tools\capture\library\mechanical.olb
c:\cadence\spb_16.6\tools\capture\library\microcontroller.olb
c:\cadence\spb_16.6\tools\capture\library\microprocessor.olb
c:\cadence\spb_16.6\tools\capture\library\misc.olb
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c:\cadence\spb_16.6\tools\capture\library\misc3.olb
c:\cadence\spb_16.6\tools\capture\library\misclinear.olb
c:\cadence\spb_16.6\tools\capture\library\miscmemory.olb
c:\cadence\spb_16.6\tools\capture\library\miscpower.olb
c:\cadence\spb_16.6\tools\capture\library\muxdecoder.olb
c:\cadence\spb_16.6\tools\capture\library\opamp.olb
c:\cadence\spb_16.6\tools\capture\library\passivefilter.olb
c:\cadence\spb_16.6\tools\capture\library\pld.olb
c:\cadence\spb_16.6\tools\capture\library\prom.olb
c:\cadence\spb_16.6\tools\capture\library\regulator.olb
c:\cadence\spb_16.6\tools\capture\library\shiftregister.olb
c:\cadence\spb_16.6\tools\capture\library\sram.olb
c:\cadence\spb_16.6\tools\capture\library\transistor.olb
Outputs
Referenced Projects

Figure 6

Placing Parts:

You can place circuit components by either going to Place → Part, or clicking "p" on the keyboard (make sure the schematic window is the active window). Figure 7 shows the Place Part Dialog Box. You can search for a part through the libraries by typing the part name/number. You can also select one particular library to be searched, or select multiple libraries at a time. Some parts have multiple packages on the same chip (i.e. the 74LS10 has 3 packages of 3-input NAND gates). Capture CIS will automatically place all packages on the same chip before placing a new chip (i.e. You will see the instances of the part as U1A and U1B for packages A and B of instance U1).

To place a component, double click on the highlighted component name and then Click on the schematic work space where you want to place it. You can also place the same part multiple times. To stop placing the part, hit ESC.

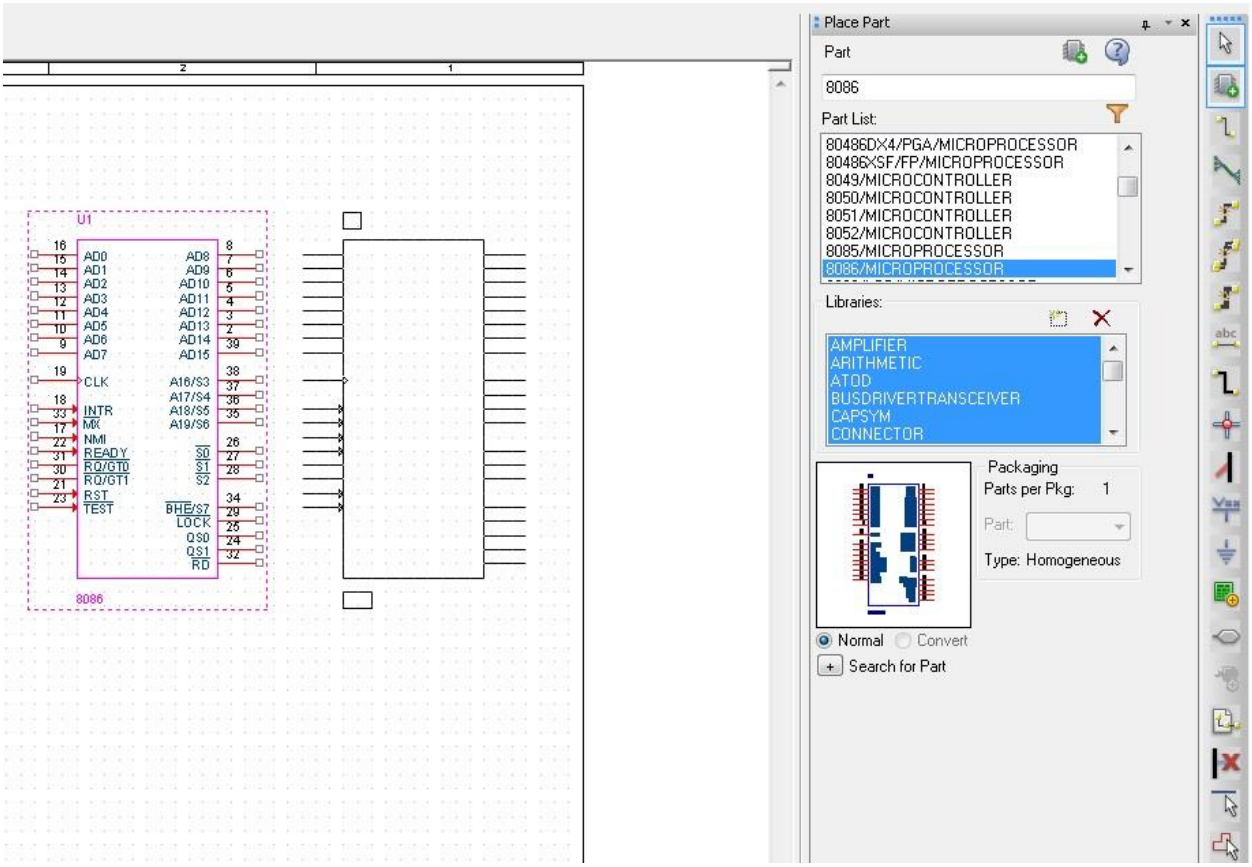

Figure 7

Placing Power Source and Ground:

To place a power source or ground on the schematic, you can either go to the Place menu, or select it on the side toolbar.

Connecting Parts:

Net Alias:

Sometimes, making tons of wire connections on your schematic will make your design look really messy and confusing. One way to clean it up is to use a net alias. A net alias can be place on a wire or bus. To do so, go to the side toolbar or press "n." When the window pops up, type the net name you want to use and click OK. Then, click on the wire or bus that you want to label. If your net alias is something like "A1," then the next time you click will place a net alias of "A2."

Besides the obvious advantages that Net Aliases provide in terms of labeling, they also allow us to clean up our schematic dramatically. By labeling two wires or buses with the same net alias, the software will automatically recognize there is a connection between the two. This allows us to not worry about trying to fit in every wire in a crowded schematic. An example of this is in Figure 8.

On-Page Connections:

There are several ways to connect components that are on the same page of the schematic. First, there are wires. You can find "wire" on the side toolbar or just press "w" to start placing a wire. Make sure you do not connect the wire accidentally to existing connections. Capture CIS will give you a warning (red dot) whenever 2 nets are about to be connected.

In addition to wires, there are Buses. You can find the bus icon on the side toolbar or press "b" to start placing a bus. You'll need to leave a space between the bus and pins for bus entries and wires. Next, create a net alias for your bus. The format for a bus alias is a string followed by [s:e], where s is the bit position of the first net and e is the bit position of the last net. For example, if you want to make a 16-bit address bus called A, you can name it as A[0:15] or A[15:0] (both of them are valid). Now you'll need to make a bus entry to connect between the wire and bus (you cannot connect bus entry directly to a pin, Capture CIS requires a bus, bus entry, and wire to make a pin-to-bus connection). Go to Place → Bus Entry on the main menu or tap "e" and then click on the points along the bus where you want to have entries. After placing all bus entries you need, now place a wire connection between each bus entry to a pin or net. The last step is to make net aliases for all the nets connected to the bus. The net names need to be the same name as your bus alias, except instead of square brackets, you'll need to put the number appropriate for the bit position of the bus you want to connect to. For example, if you want a particular net to be connected to bit 3 of address bus A, you should make the net alias "A3." A Step by Step example can be seen in Figure 9.

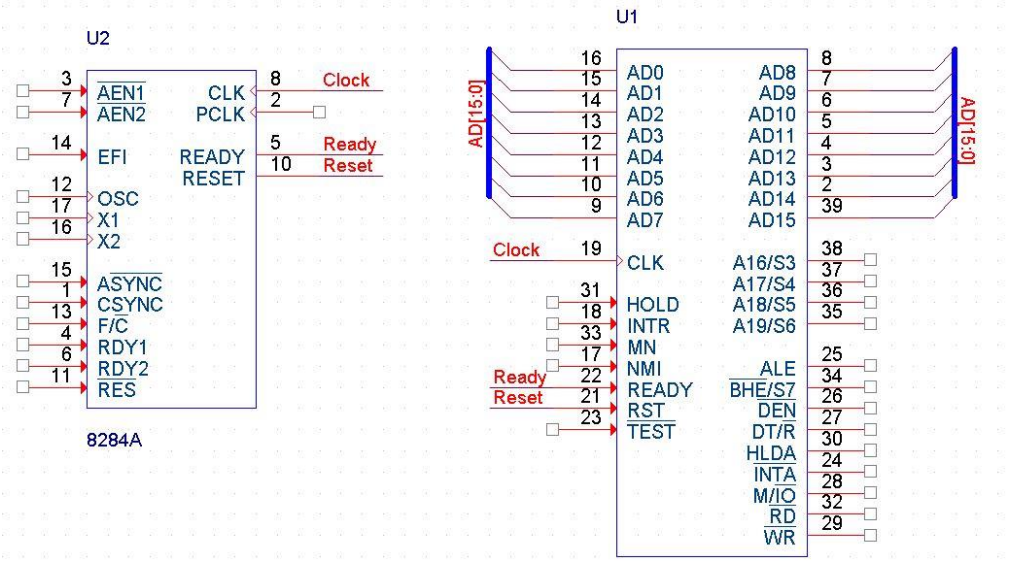

Figure 8

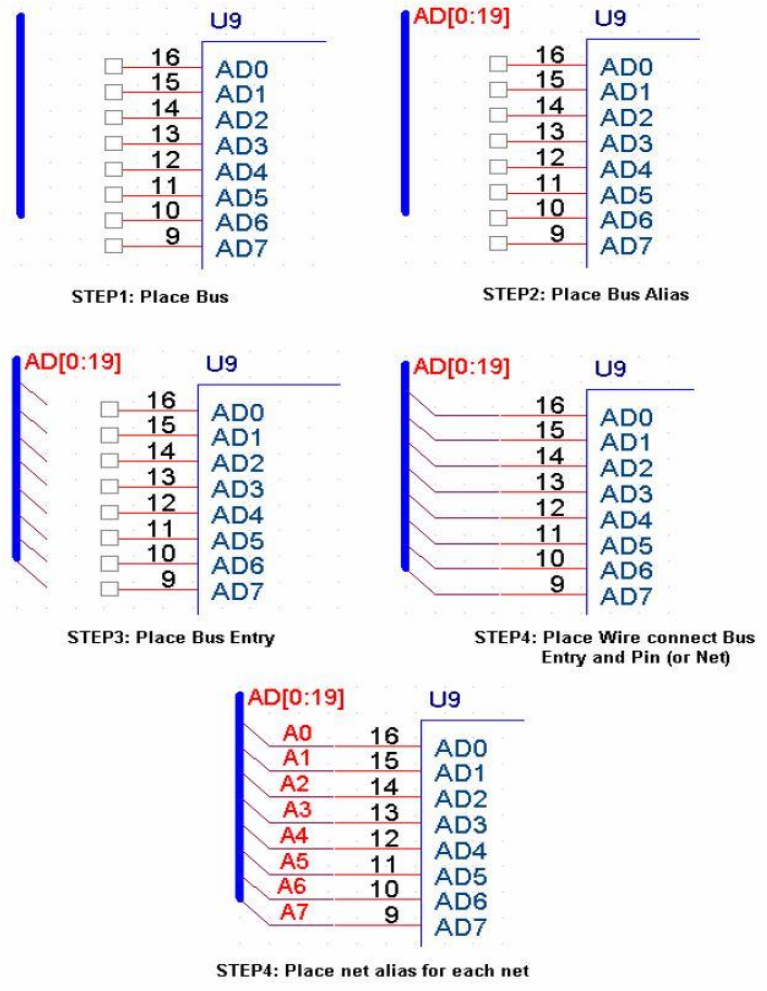

Figure 9

Off-Page Connectors:

In cases where there are multiple pages to a schematic (which you most likely will have), there are off-page connectors to allow connections between them. There are two kinds of off-page connections: On (L) and Off (R) page (as seen in Figure 10). You can use either of the methods (Net Alias or direct connection) to connect either buses or wires to the off-page connectors.

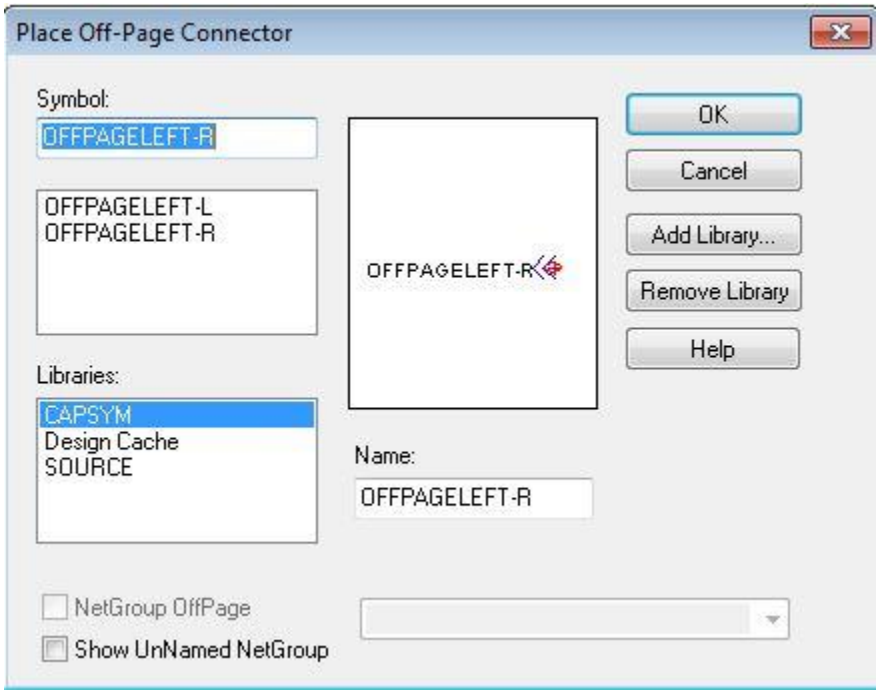

Figure 10

No Connection:

Sometimes there will be pins that are unused and you don't need to connect anywhere. In these cases, the software requires that you place "no-connects" on these pins so it knows that you aren't just forgetting them. To do this, press "x" or go to the side toolbar, and then click on the pins that you have no connections for.

Design Rules Check (DRC):

Running the DRC allows you to perform a kind of debugging. DRC will tell you if you have anything wrong with how you have connected your components (open connections, connecting two outputs, etc). However, DRC will NOT tell you if you have made an incorrect connection, like connecting the wrong address pins. It only tells you if it is theoretically a valid

connection. Do NOT rely on DRC alone to check your work. Just because it says there are no errors, it does NOT mean that your circuit is necessarily right.

To run DRC, click on the Schematic folder in the project window, and go to Tools → DRC. The default settings should be sufficient, but make sure you check off the "View Output" box, then click OK. A box will pop up with any errors or warnings you may have.

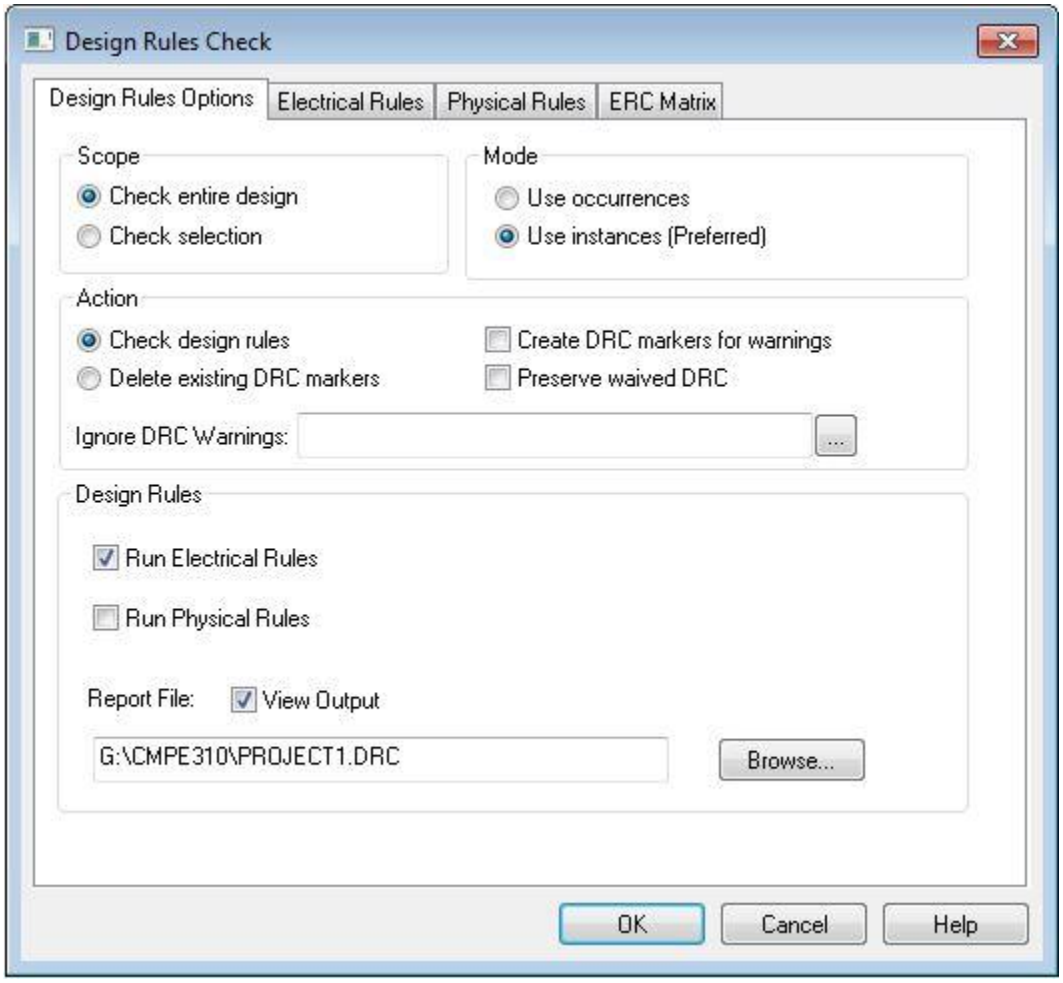

Figure 11