Lab #8 PRE-LAB: DIP Switches, LCD Display & 7-Segment LED Display

Name_____

*****All Schematics and Screenshots must be uploaded in your CMPE 310 BOX I created for you. AND PRESENTED to TA before starting Lab #7.*****

Pre-Lab Task: Create a schematic design for the DIP Switches, LCD Display and 7-segment LED display using Cadence OrCad Capture CIS and the brief handout on building the LED circuit. This is the sixth step of Project I, so make sure you print out the Project I description to keep track of your progress.

Note: LCD display can be found in datasheets.zip folder. Make sure to add the 8086_parts.olb in your project to access the LCD display in the library.

Note: Make sure you add the power terminal block and any other components that are required for all the circuits you have created. You are now ready to put your Project I Documentation.

Note: MUST turn in before start of Lab #7 class.

Lab #8: Allegro PCB Design

*****All Schematics and Screenshots must be uploaded in your CMPE 310 BOX I created for you. AND PRESENTED to TA before leaving lab.*****

Getting Started. The objective of this Lab is to continue from Lab#6 to create a PCB output layout files from layout circuit netlist created using Capture CIS that are suitable for PCB fabrication using Allegro PCB Design for all your Project I board components.

You should complete this lab individually. When you have completed the assignment, raise your hand to get TA's attention, so that you can present your PCB layout to the TA and get your lab signed off before leaving class.

Reading/reference material

- Capture CIS tutorial
- Allegro PCB Design tutorial
- Textbook

Concepts

Illustrate the importance developing skills in using an EDA tool to create schematic and PCB design.

Task: Create PCB output layout files from layout circuit netlist created using Capture CIS for all of your Project I components. This is the seventh step of Project I, so make sure you print out the Project I description to keep track of your progress.

Technical Document due on Friday at 11:00 pm.

*****All Schematic design and Screenshot must be uploaded in your CMPE 310 BOX I created for you.*****