CMPE 310
Systems Design and Programming

L7: Chapter 10 – Memory Interface

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L7 Objectives

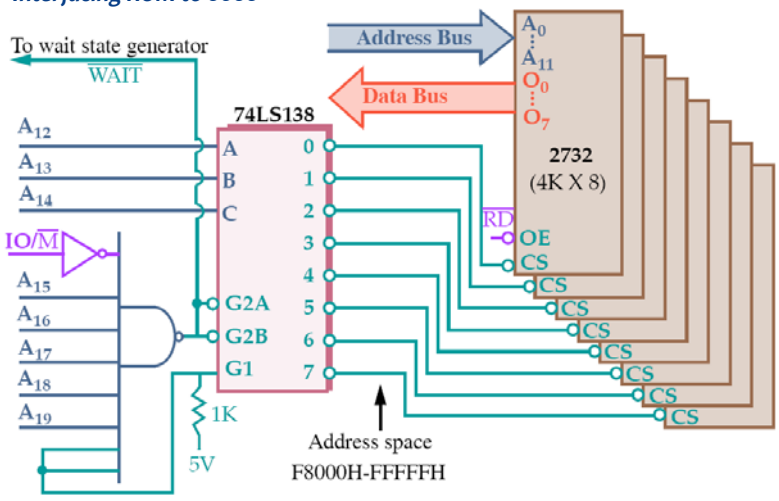
* To interface memory components to x88
* Diagram how EPROM and SRAM modules are connected to x88

8088 (8-bit) memory interface

* The memory systems *sees the 8088 as a device with:*
  * *20 address connections (A_{19} to A_0).*
  * *8 data bus connections (AD_7 to AD_0).*
  * *3 control signals, IO/$\overline{M}$, $\overline{RD}$, and $\overline{WR}$.*
* Interfacing the 8088 with:
  * *32K of EPROM (at addresses F8000H through FFFFFH).*
  * *512K of SRAM (at addresses 00000H through 7FFFFH).*
* The EPROM interface uses a 74LS138 plus **8 2732 (*4K X 8*)** EPROMs.
  * T_{acc} = *450ns* → generation of a wait state.
  * The 74LS138 requires *12ns to decode*
  * The 8088 runs at 5MHz and only allows *420ns for memory to access data.*
  * A wait state adds *200ns* of additional time

8088 (8-bit) memory interface

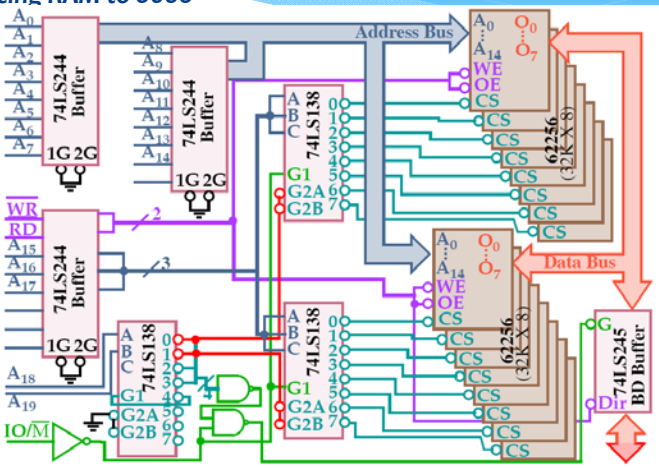
* ***Interfacing ROM to 8088***



* The 8088 cold starts execution at **FFFF0H. JMP to F8000H occurs here.**

8088 (8-bit) memory interface

* *Interfacing RAM to 8088*



* 16 32K RAMs fill memory from 00000H through 7FFFFH, for 512K bytes memory.

8088 (8-bit) memory interface

* The **16 62256s on the previous slide are actually SRAMs.**
  * Access times are on order of *10ns.*
* Flash memory can also be interfaced to the 8088 (see text).
  * Interface at physical address range of 80000H-FFFFFH
  * Similar to a SRAM except that it requires 12V (5.0 or 3.3V newer) for writing via V_{PP} pin
  * However, the write time (*400ms!*) is too slow to be used as RAM (text).

Next Time

* Memory Interfacing
  * 16-bit memory interface