# UART

Discussion III (Version 2.0)

UMBC - CE

September 2, 2015

Version 1.0 - Initial Document
Version 2.0 - Fixed typos and some illogical assumptions !

## Objectives

- Introduce UART (Universal Asynchronous Receiver Transmitter)

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- Interface PC with AVR Butterfly via UART
- Implement UART communications using AVR Assembly

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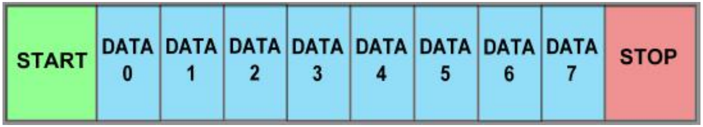
- The baud rate defines the length of each bit as $\frac{1}{baudrate}$

## The UART Frame

- The data to be sent is **framed** by a start bit and a stop bit



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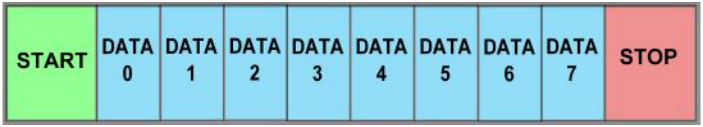

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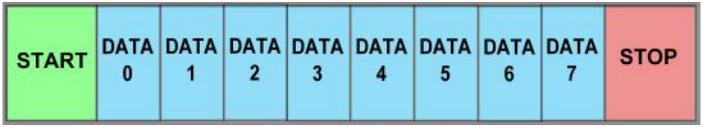

- The start bit is typically a high signal to start the data frame, and the stop bit is typically a low signal, often 1, 1.5 or 2 times as long as the other bits
- Optionally, a parity bit may be transmitted after the data

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- The stop/start bits, parity, hardware/software hand shaking, and baud rate must be configured on both ends

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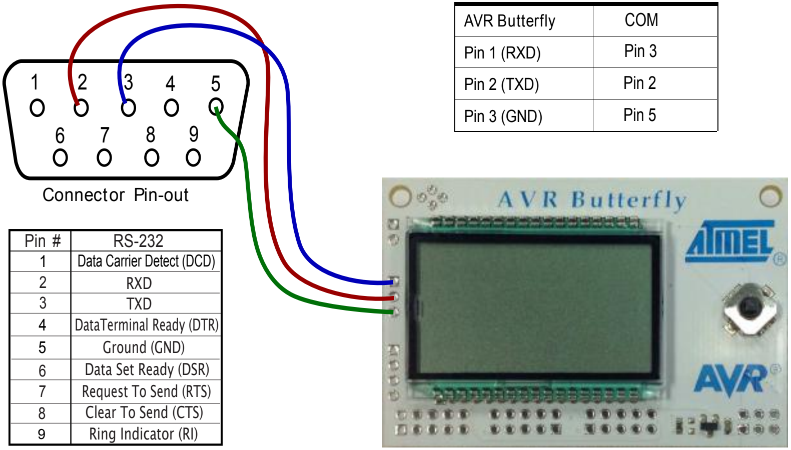
- For Our AVR, the required **registers** have slightly different names and are in the EXTENDED I/O, meaning, we must access them as memory and not as registers

# AVR Butterfly Interfacing

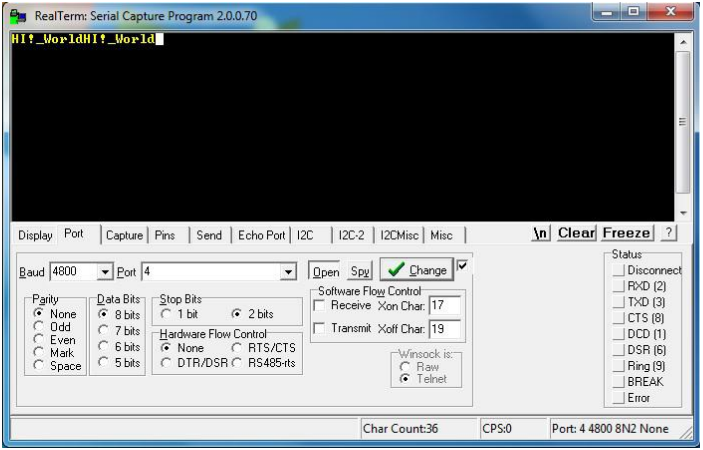
RS232 Communications Port



| AVR Butterfly | COM |
|---|---|
| Pin 1 (RXD) | Pin 3 |
| Pin 2 (TXD) | Pin 2 |
| Pin 3 (GND) | Pin 5 |

| Pin # | RS-232 |
|---|---|
| 1 | Data Carrier Detect (DCD) |
| 2 | RXD |
| 3 | TXD |
| 4 | DataTerminal Ready (DTR) |
| 5 | Ground (GND) |
| 6 | Data Set Ready (DSR) |
| 7 | Request To Send (RTS) |
| 8 | Clear To Send (CTS) |
| 9 | Ring Indicator (RI) |

## RealTerm Settings



```
HI!_WorldHI!_World
```

Baud 4800 Port 4

Parity: [✓ None] Odd Even Mark Space

Data Bits: [✓ 8 bits] 7 bits 6 bits 5 bits

Stop Bits: 1 bit [✓ 2 bits]

Hardware Flow Control: [✓ None] RTS/CTS DTR/DSR RS485-rts

Software Flow Control: Receive Xon Char: 17 Transmit Xoff Char: 19

Winsock is: Raw [✓ Telnet]

Char Count:36 CPS:0 Port: 4 4800 8N2 None

## Interfacing Code

Download interfacing code from your instructor's website (uart.asm)