# CMPE 310
# Systems Design and Programming

**L12:    Chapter 11 – BASIC I/O Interface**

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# L12 Objectives

* Describe the function of each pin of the 8254 PIT
    * Diagram how the 8254 PIT is connected to the x86/88 PC
    * Program the three counters of the 8254 PIT by use of the chip control word

# Programmable Interval Timer: 8254

* Three independent 16-bit programmable counters (**timers**).
    * Each capable of counting in binary or BCD with a maximum frequency of 10MHz.

* Used for controlling real-time events such as real-time clock, events counter, and motor speed and direction control.

* Usually decoded at port address 40H-43H
* Main functions:
    * Generates a basic timer interrupt that occurs at approximately 18.2Hz.
        * Interrupts the microprocessor at interrupt vector 8 for a clock tick.
    * Causes DRAM memory system to be refreshed.
        * Programmed for 15 us on PC to request DMA action
    * Provides a timing source to the internal speaker and other devices.
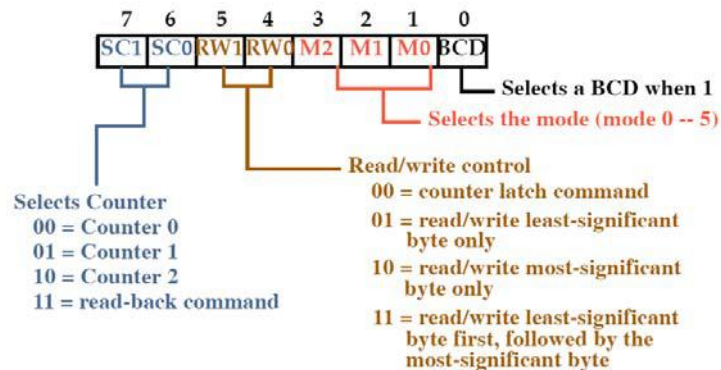
# 8254 Functional Description
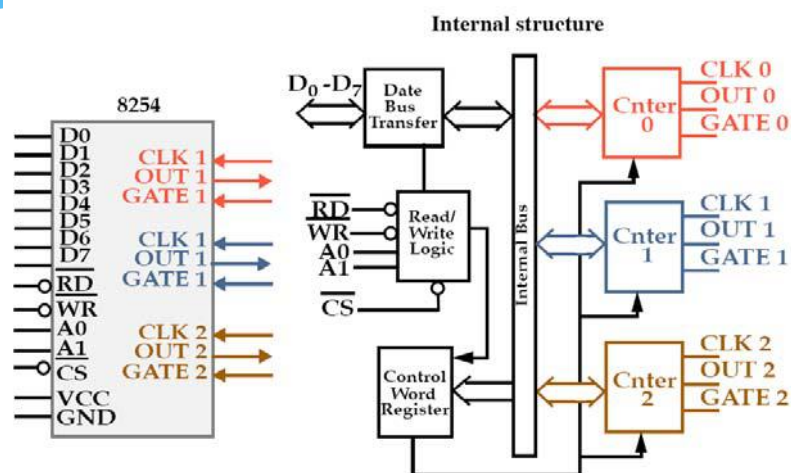
# 8254 Pin Definitions

* **A₁, A₀:** The *address inputs* select one of the four internal registers with the 8254

| A₁ | A₀ | Function |
|----|----|----------|
| 0  | 0  | Counter 0 |
| 0  | 1  | Counter 1 |
| 1  | 0  | Counter 2 |
| 1  | 1  | Control Word |

* **CLK:** The *clock* input is the timing source for each of the internal counters.
    * It is often connected to the PCLK signal from the bus controller.
* **C̄S̄:** *Chip Select* enables the 8254 for programming, and reading and writing.
* **G:** The *gate input* controls the operation of the counter in some modes.
* **OUT:** A *counter output* is where the wave-form generated by the timer is available.
* **R̄D̄/W̄R̄:** *Read/Write* causes data to be read/written from the 8254 and often connects to the IORC/IOWC.

# 8254 Programming

* Each counter is individually programmed by writing a control word, followed by the initial count.
* The control word allows the programmer to select the counter, mode of operation, binary or BCD count and type of operation (read/write).

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RW1 | RW0 | M2 | M1 | M0 | BCD |

— Selects a BCD when 1

— Selects the mode (mode 0 -- 5)

Read/write control
00 = counter latch command
01 = read/write least-significant byte only
10 = read/write most-significant byte only
11 = read/write least-significant byte first, followed by the most-significant byte

Selects Counter
00 = Counter 0
01 = Counter 1
10 = Counter 2
11 = read-back command

# 8254 Programming

* Each counter may be programmed with a count of 1 to FFFFH.
  * Minimum count is 1 all modes except 2 and 3 with minimum count of 2.
* Each counter has a program control word used to select the way the counter operates.
  * If two bytes are programmed, then the first byte (LSB) stops the count, and the second byte (MSB) starts the counter with the new count.
* There are 6 modes of operation for each counter:
  * **Mode 0:** An events counter enabled with G.
    * The output becomes a logic 0 when the control word is written and remains there until N plus the number of programmed counts.

| N | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

CLK

OUT

Count of 7 loaded
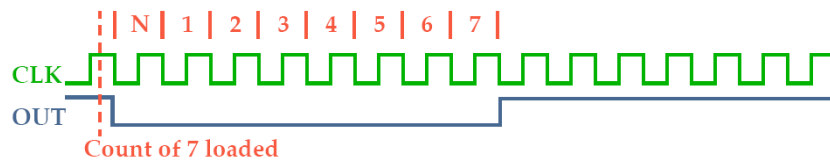
# 8254 Modes

* **Mode 1:** One-shot mode.
  * The G input triggers the counter to output a 0 pulse for the duration of the count.
  * Counter reloaded if G is pulsed again.

| 1 | 2 | 3 | 4 | 5 |

CLK

GATE

OUT

Trigger with count of 5
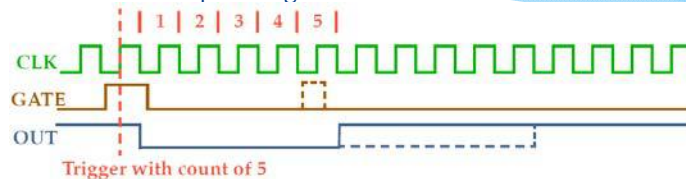
* **Mode 2:** Counter generates a series of pulses that are 1 clock pulse wide.
  * The separation between pulses is determined by the count.
  * The cycle is repeated until reprogrammed or G pin set to 0.

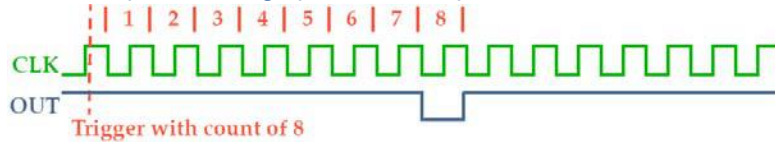| 1 | 2 | 3 | 4 | 5 | 1 | 2 | 3 | 4 | 5 | 1 | 2 | 3 | 4 | 5 |

CLK

OUT

Count of 5 loaded
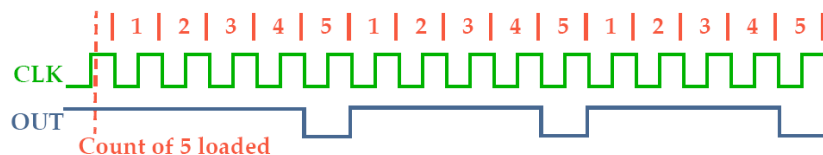
# 8254 Modes

* **Mode 3:** Generates a continuous square-wave with G set to 1.
  * If count is even, 50% duty cycle otherwise OUT is high 1 cycle longer.


Count of 6 loaded
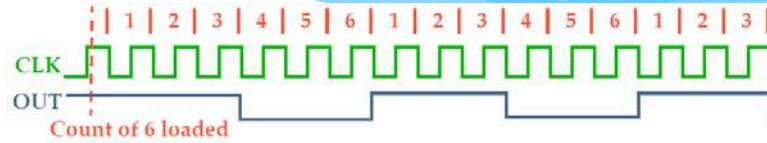
* **Mode 4:** Software triggered one-shot (G must be 1).
  * Count to be decremented by 1 clock pulse
  * Allow counter to produce a single pulse at the output


Trigger with count of 8

* **Mode 5:** Hardware triggered one-shot. G controls similar to Mode 1
  * Functions as Mode 4 except counting is started by a trigger pulse on G.
  * Strobe pulse is output after the count is decrement to 0

# Next Time

* Programmable Communications Interface

STOP