# CMPE 212
# Principles of Digital Design

*Lecture 21*

## Counters Design

April 11, 2016

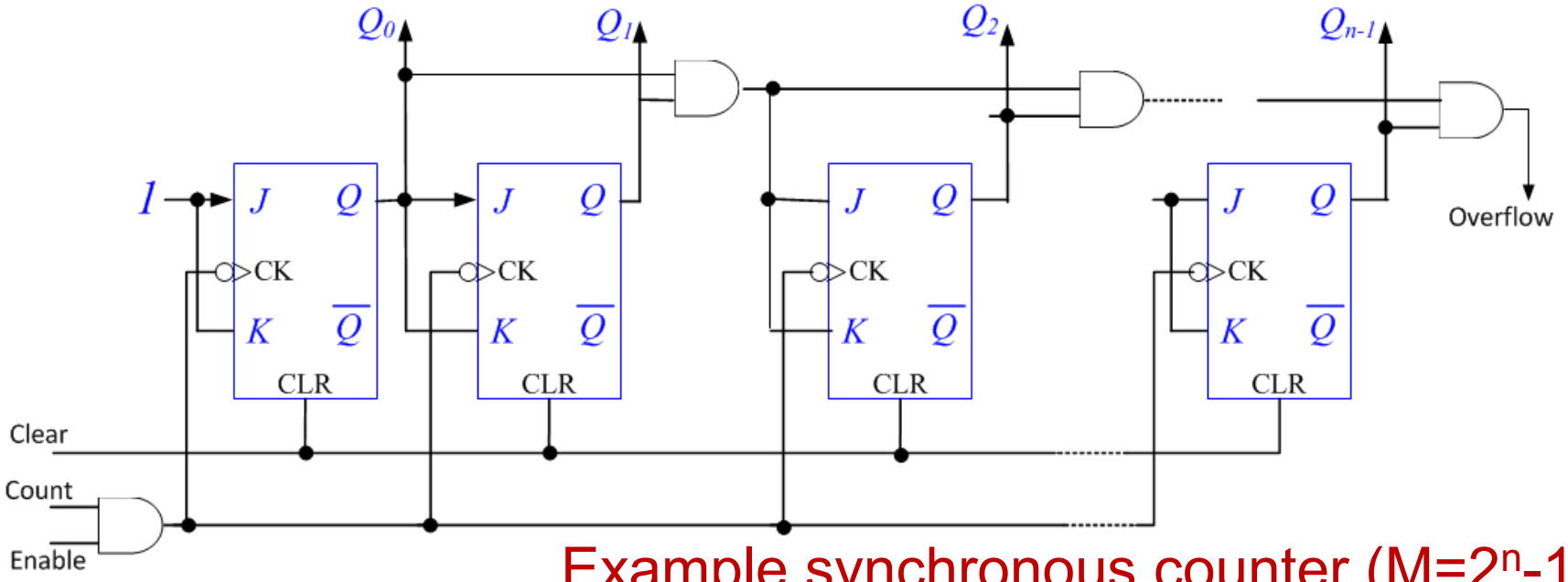
www.csee.umbc.edu/~younis/CMPE212/CMPE212.htm

# Lecture's Overview

- ***Previous Lecture***
  - ➔Register and Shift Registers
    (Design and example applications)
  - ➔ Binary counters
    - ➢ Synchronous counters
    - ➢ Asynchronous counters
    - ➢ Down and up/down counters
- ***This Lecture***
  - ➔ Modulo-N Counters
  - ➔ Synchronous and asynchronous BCD counters
  - ➔ Ring counters (shift registers as counters)
  - ➔ Fractional rate multipliers

# Modulo-N Counters

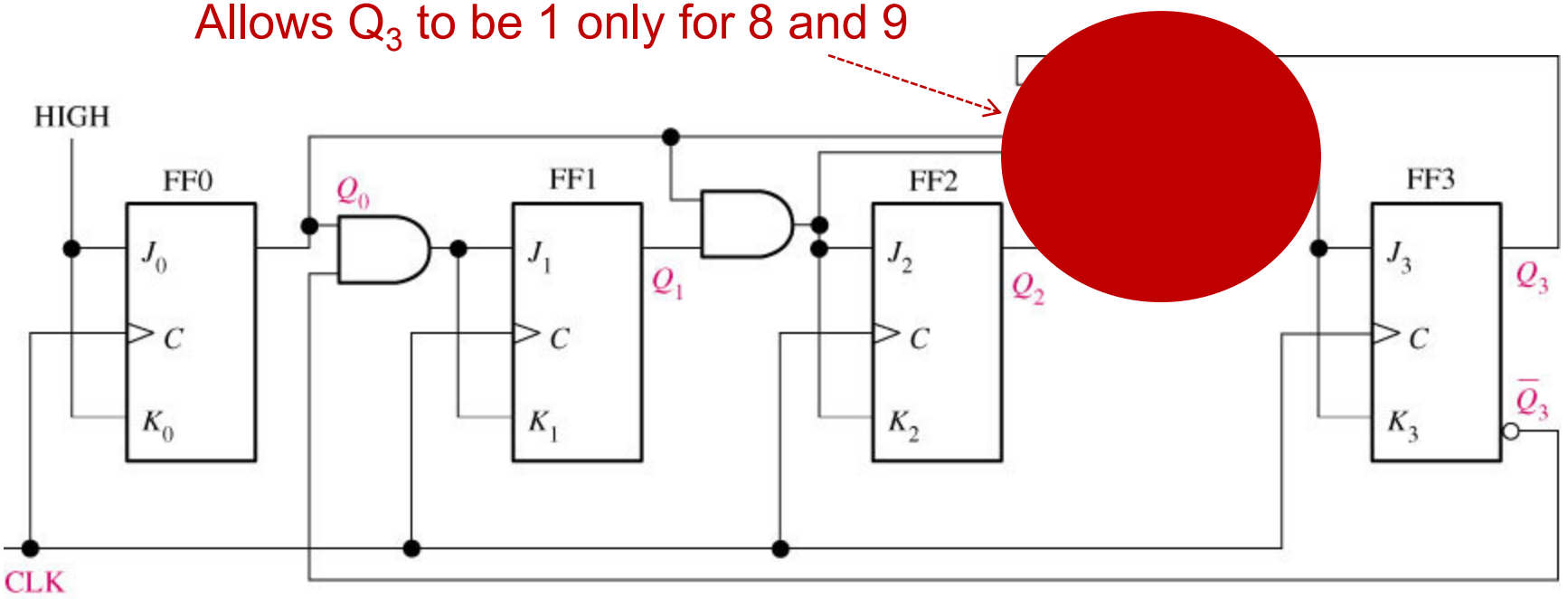
- A counter circuit tracks the multiplicity of transitions is a signal up to an upper bound M, i.e., transitions between the states 0, 1, …, M-1
- A counter of an upper bound of M is called “Modulo M Counter”
- The number of flip flops, *n*, used in a counter imply $M = 2^n-1$
- In many applications a counter is needed with an upper bound N that is less than M, e.g., BCD counters
- Counters can be synchronous, i.e., operation is coordinated by a clock, and asynchronous that operates on the principle of “ready-go”.



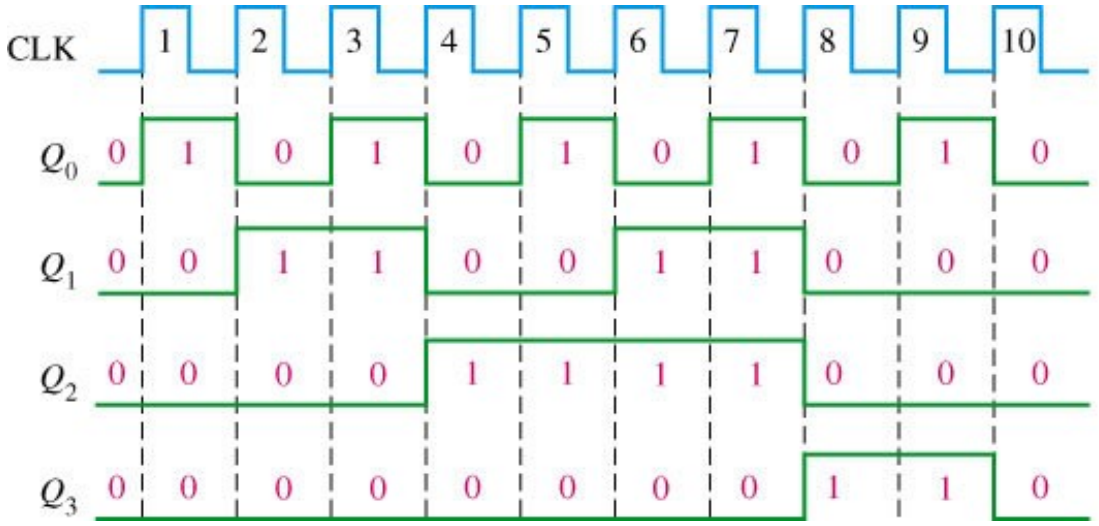

Example synchronous counter ($M=2^n-1$)

# Synchronous BCD (Decade) Counter

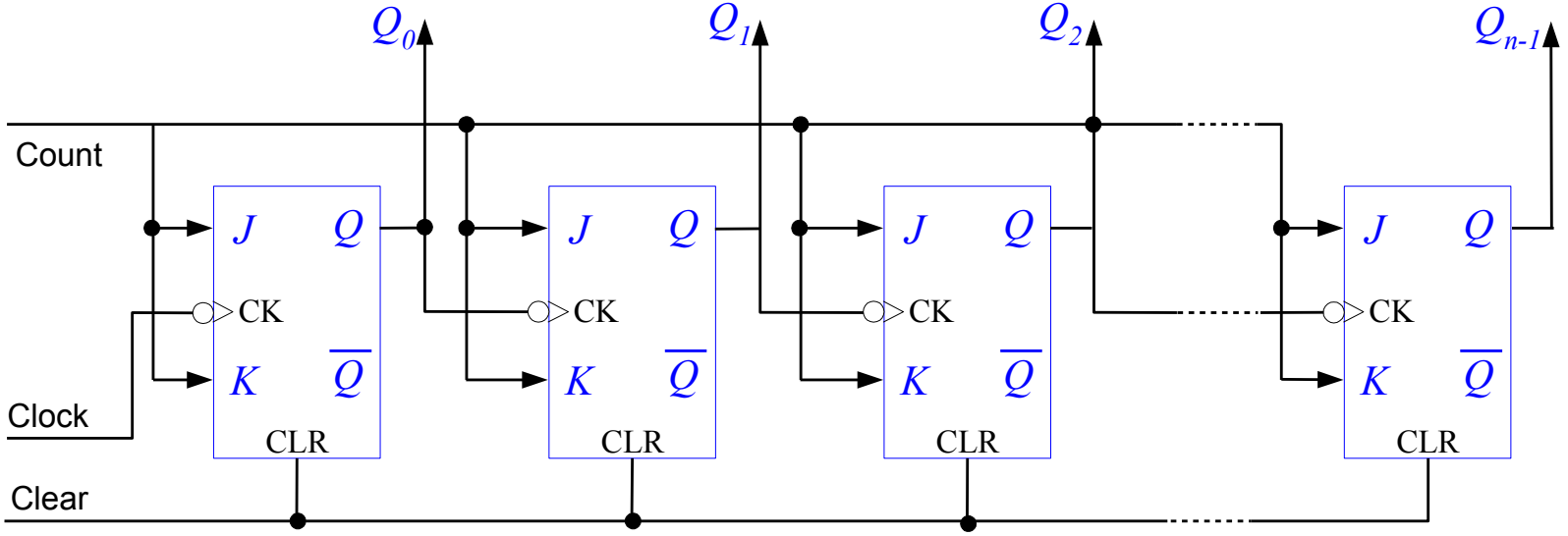
Allows $Q_3$ to be 1 only for 8 and 9




- Idea: similar to $2^n$-1 counters with logic that controls the next state
- Example: The 74LS160 Integrated Circuit



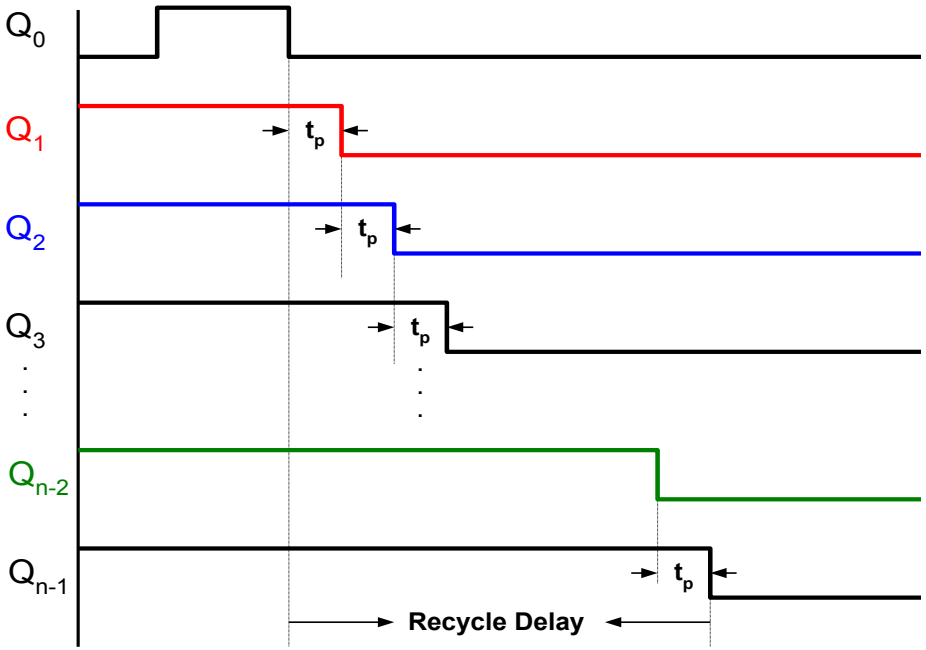
# Asynchronous Binary Counter



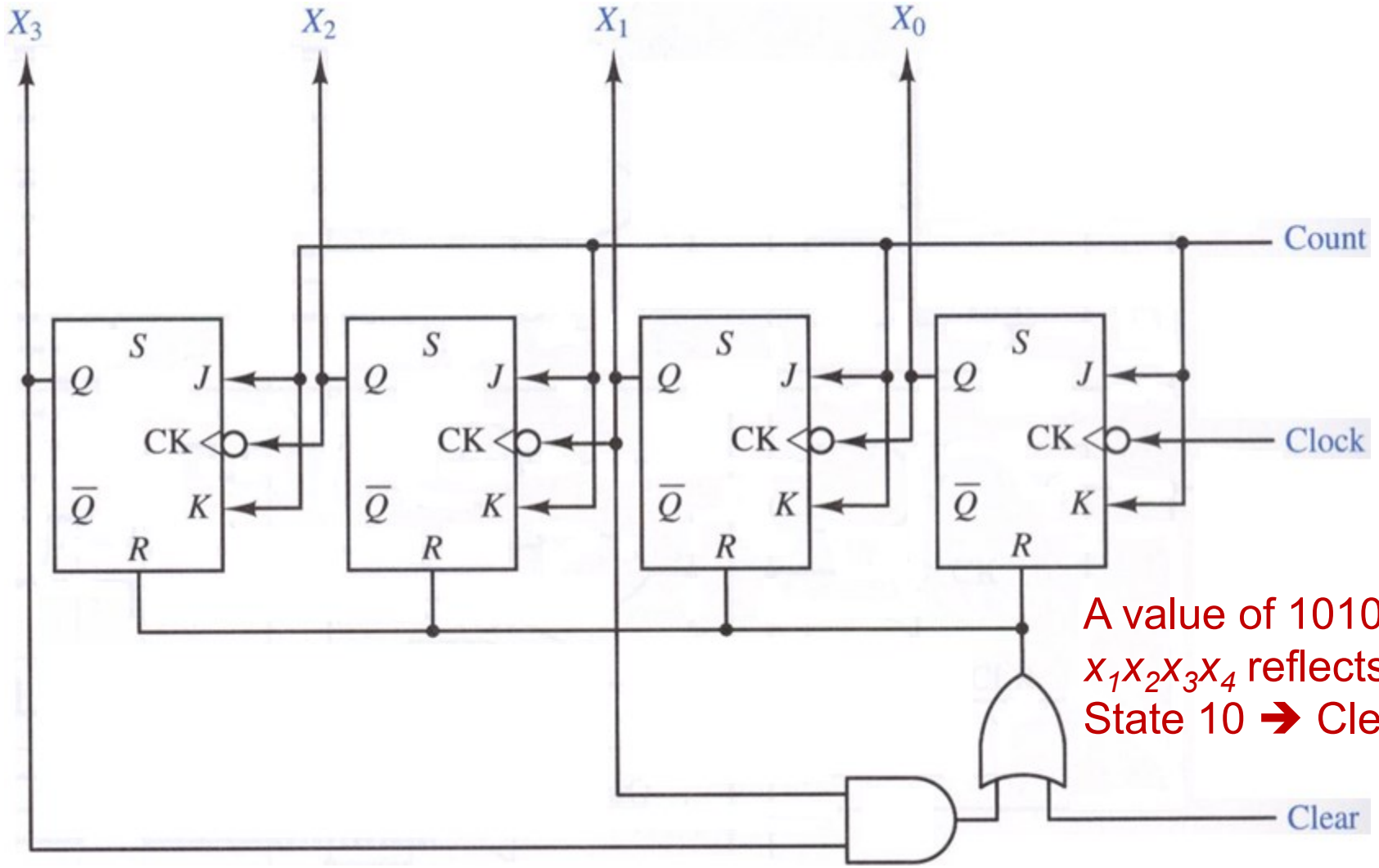

Changes propagate from one flip-flop to the next

Asynchronous ➔ state change is not controlled by a synchronizing clock (ready-go operation)

- Delay is not homogenous and one has to determine the worst case delay to avoid reading the wrong output
- Recycling back to zero is not instantaneous, $(n\text{-}1)t_p$

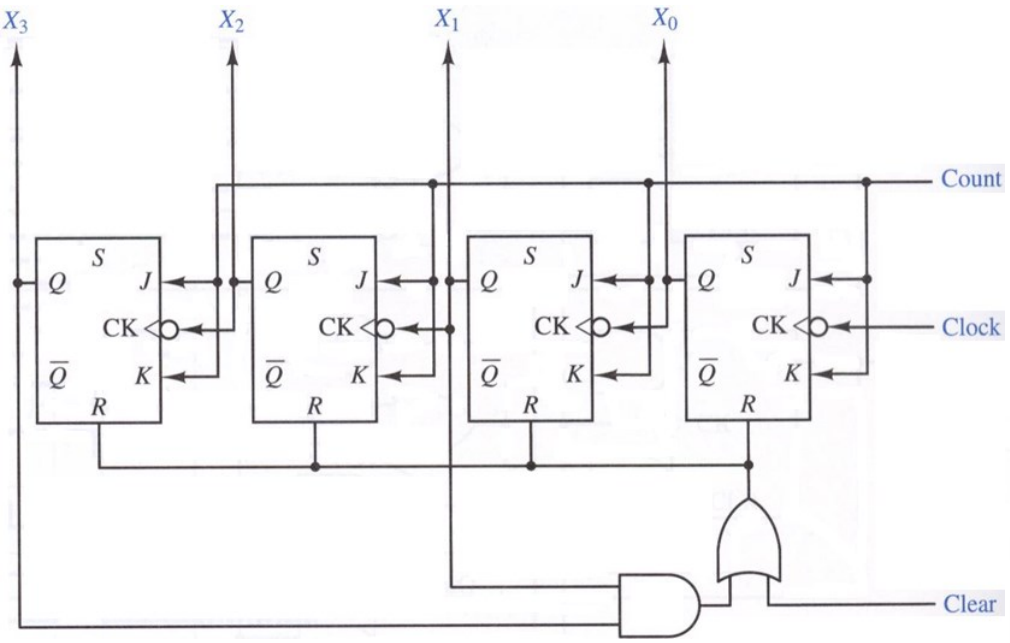


# Asynchronous BCD (Decade) Counter

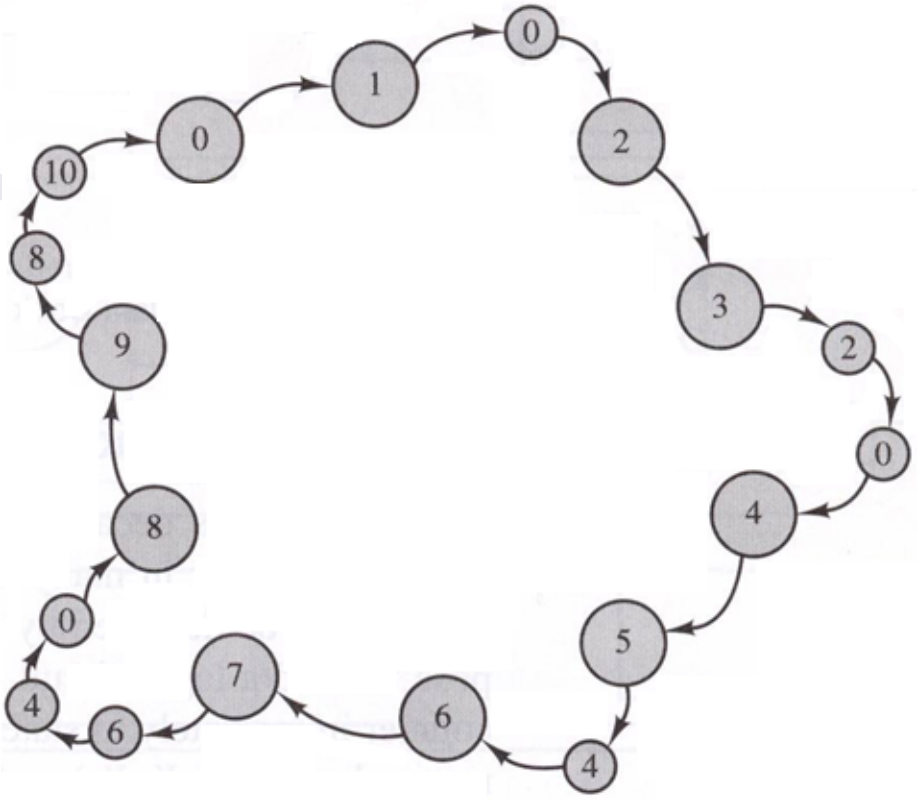



- Add combinational logic to detect number 9 ($10^{th}$ state) and reset the counter to zero (state 0)

# Asynchronous BCD counter

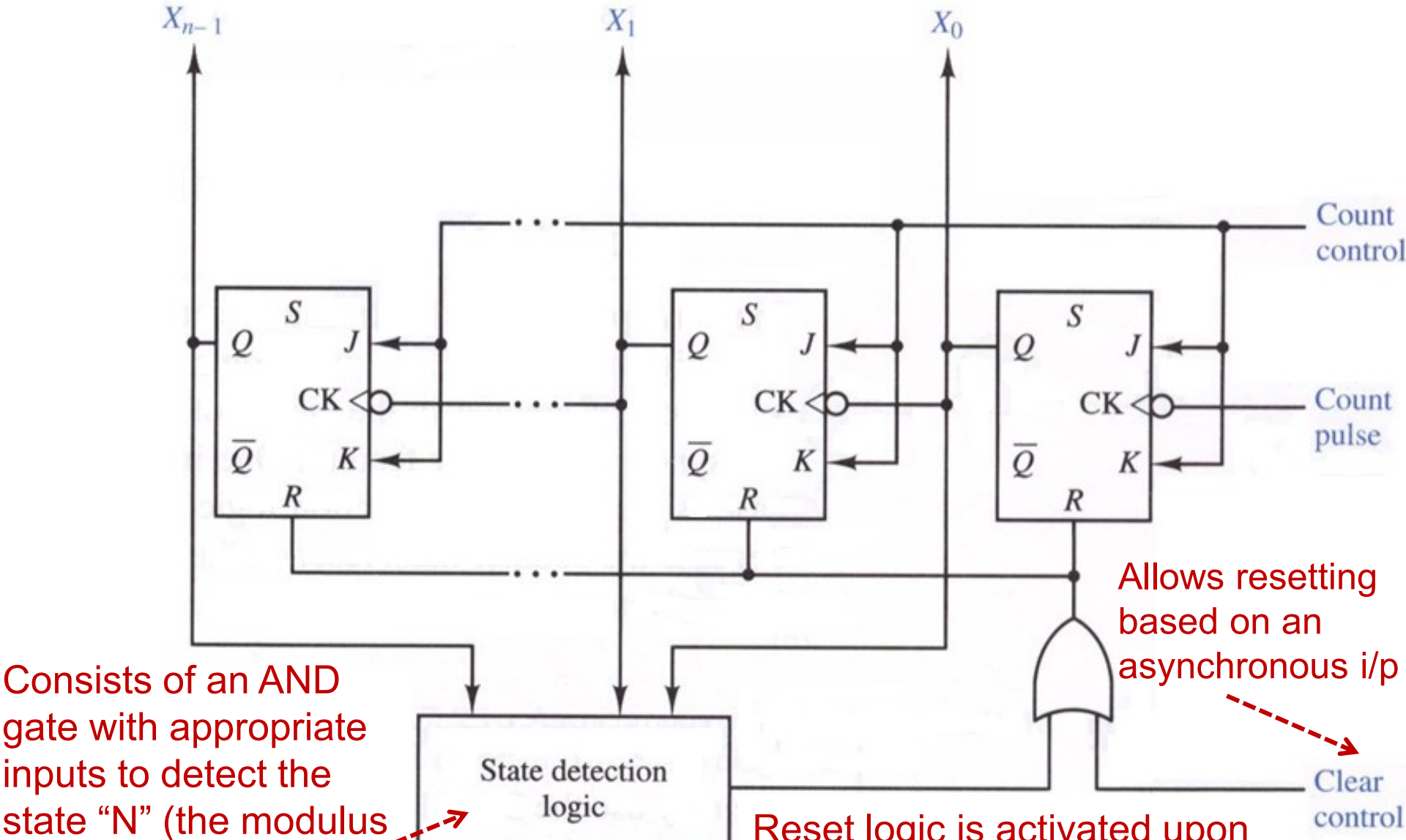



Large circles denote steady states and small circles reflects intermediate states visited in transition




- Transition between two states may pass multiple intermediate states due to the ripple effect
- The most unstable output is in transition between 7 and 8.

# General Modulo-N Asynchronous Counter




Consists of an AND gate with appropriate inputs to detect the state "N" (the modulus of the counter)

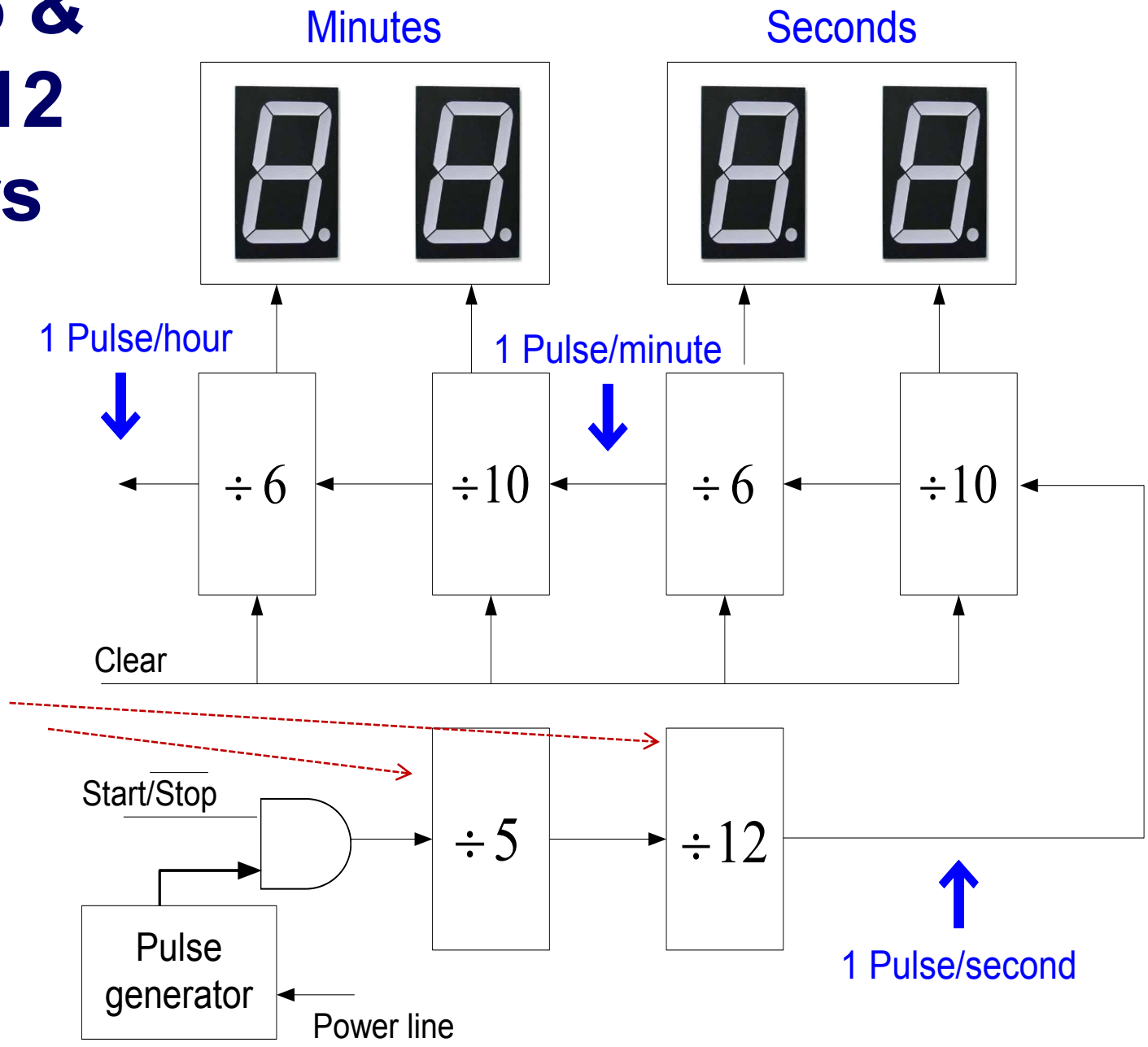
Allows resetting based on an asynchronous i/p

Reset logic is activated upon reaching counter's terminal state

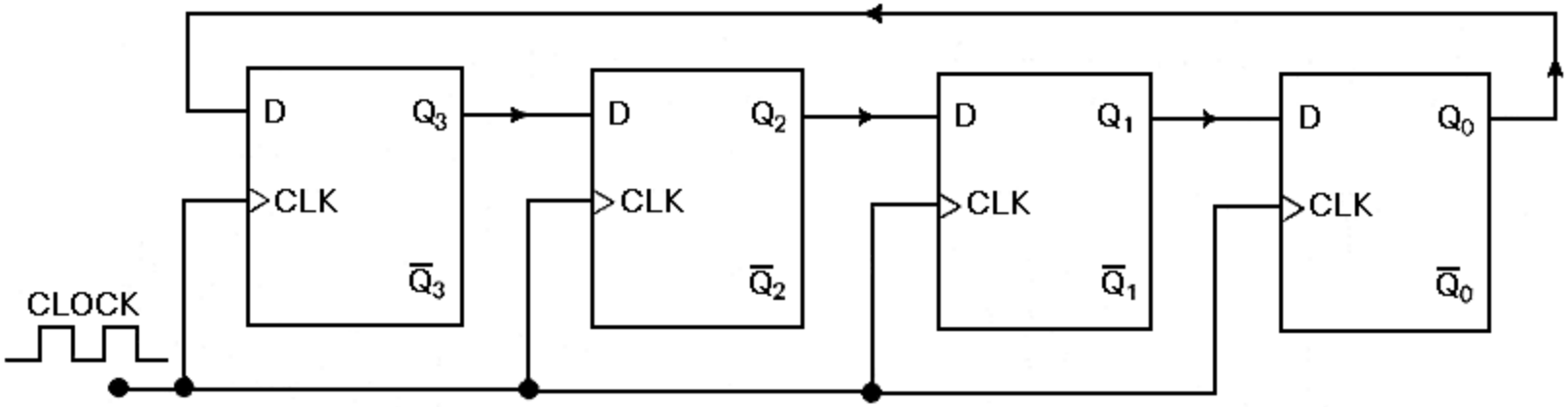
# Modulo-6 & Module-12 Counters

Example: digital timer generator

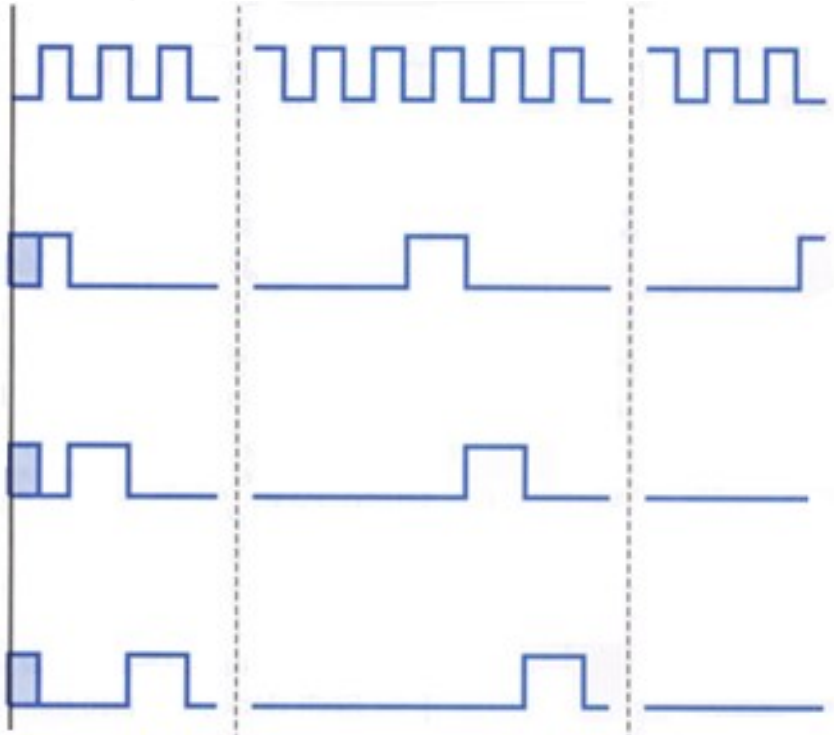
Uses 60-hertz power line ➔ divide by 60 (modulo 60)



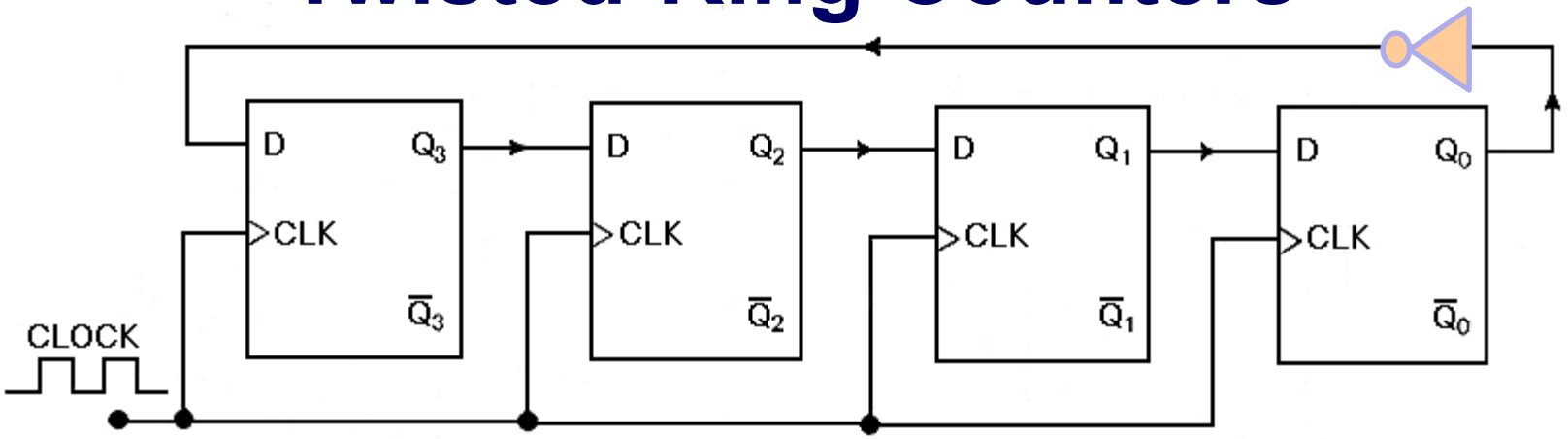
# Ring Counters

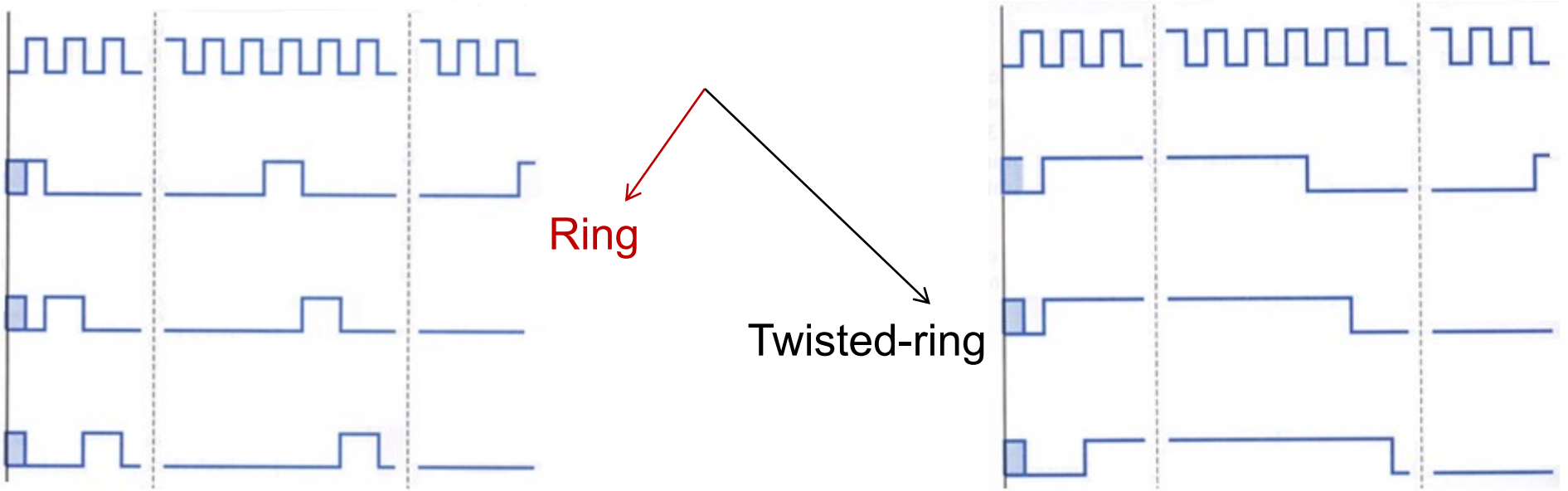



- Shift registers can be considered as counters when the serial output is fed back as a serial input ➔ ring
- A ring counter is a sequential circuits that has 1 flip flop per state
- If only bit is set to “1”, such “1” will circulate around the register (works like sequential decoder)



# Twisted-Ring Counters

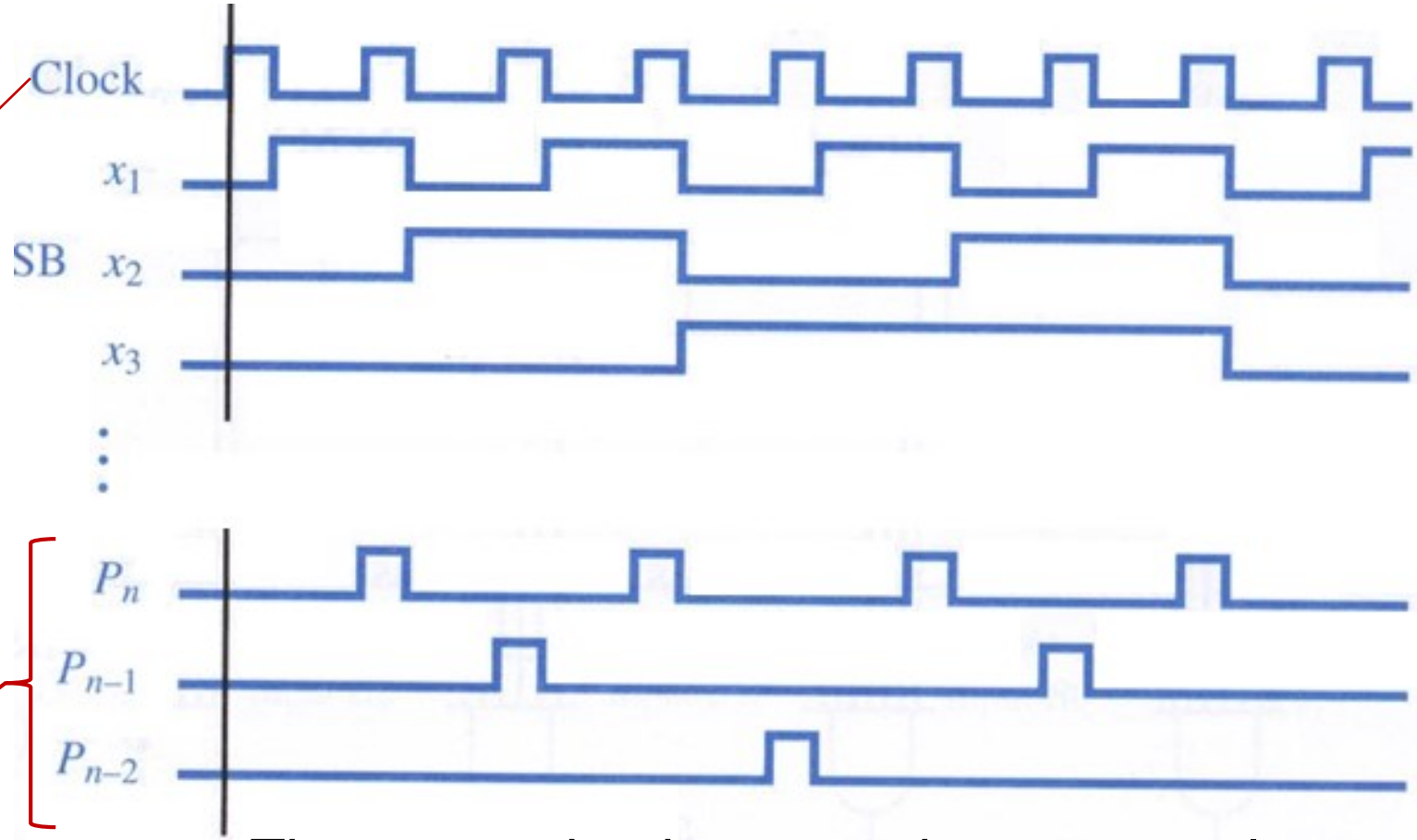



- *Twist-ring counter* (or *Johnson Counter*): a ring counter with an inverter in the feedback loop is called
- Number of states = 2N (due to the inverter)

# Digital Fractional Rate Multipliers

- Transforms a stream of input clock pulses, e.g. clock, into controlled stream of output pulses

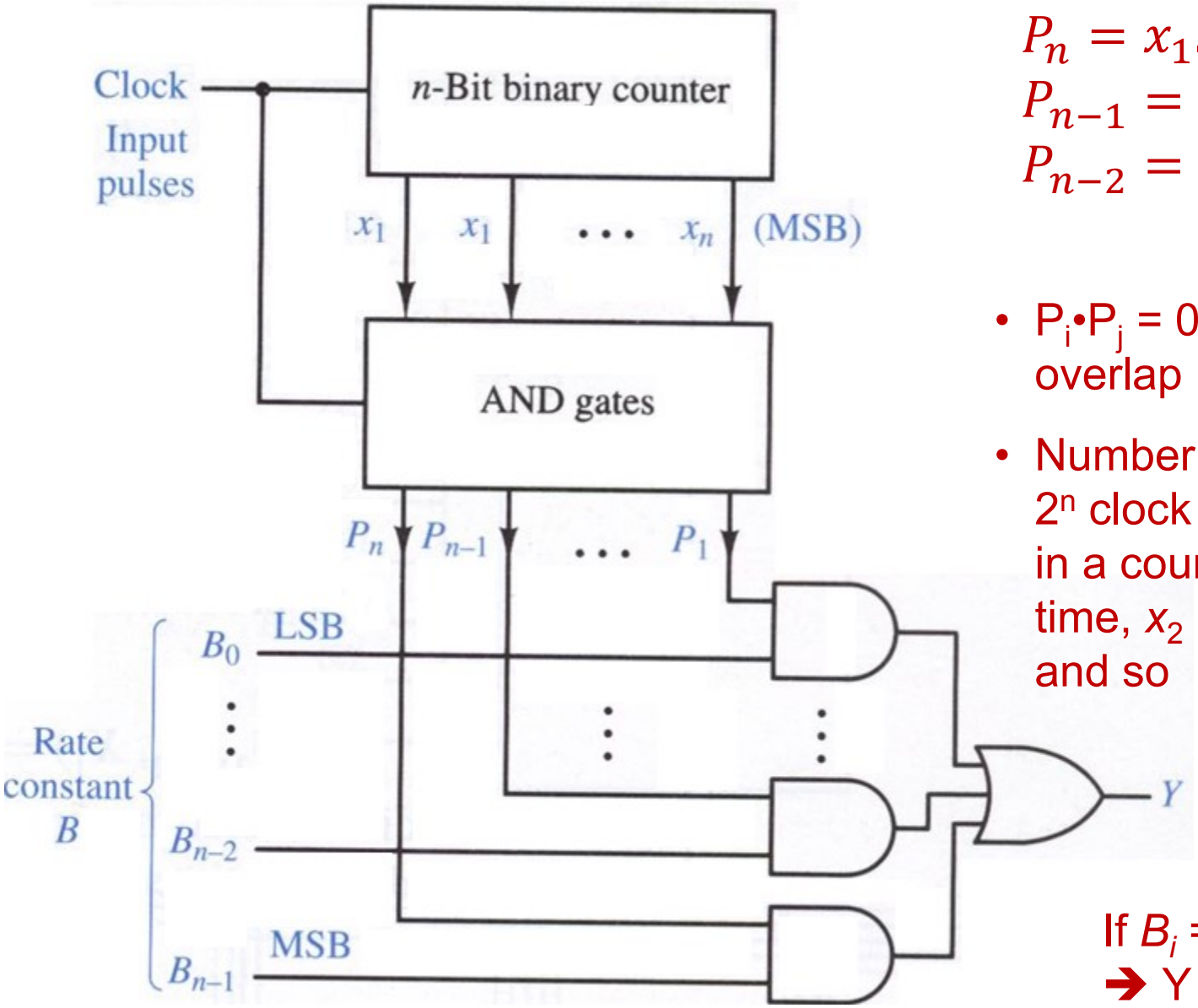



Clock drives an n-bit binary counter with outputs $X_1 \ldots X_n$

Produce non-overlap pulse trains $P_1 \ldots P_n$

- The separation between the output pulses obtained by the fractional multiplier will vary

# Digital Fractional Rate Multipliers




$$P_n = x_1.Clock$$
$$P_{n-1} = \overline{x_1}.x_2.Clock$$
$$P_{n-2} = \overline{x_1}.\overline{x_2}.x_3.Clock$$
$$\ldots\ \ldots$$

- $P_i \bullet P_j = 0$ ➔ $P_i$ and $P_j$ do not overlap
- Number of pulses in $P_i$ per $2^n$ clock cycles is $2^{i-1}$, since in a counter $x_1$ is on ½ of the time, $x_2$ is on ¼ of the time, and so

$$Y = \sum B_{i-1}.P_i$$

If $B_i = 1$ for $i = 0, 1, ..n-1$
➔ Y = clock

# Conclusion

- ***Summary***
  - ➔ Modulo-N Counters
  - ➔ Synchronous and asynchronous BCD counters
  - ➔ Counter resetting
  - ➔ Ring counters (shift register as a counter)
  - ➔ Fractional rate multipliers
- ***Next Lecture***
  - ➔ Synchronous sequential circuits models
  - ➔ Sequential circuits analysis
  - ➔ Synthesis of synchronous sequential circuits

Reading assignment: Sections 7.3 – 7.6 in the textbook