University of Maryland Baltimore County
Department of Computer Science and Electrical Engineering

CMPE 212L, Principles of Digital Design Laboratory

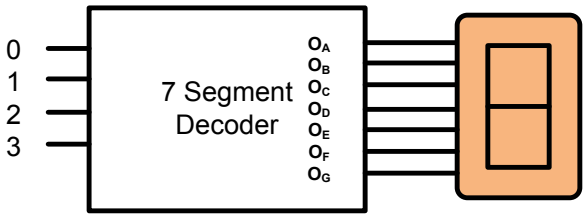
Project #1 Due: Fri 3/11/2016

Objective

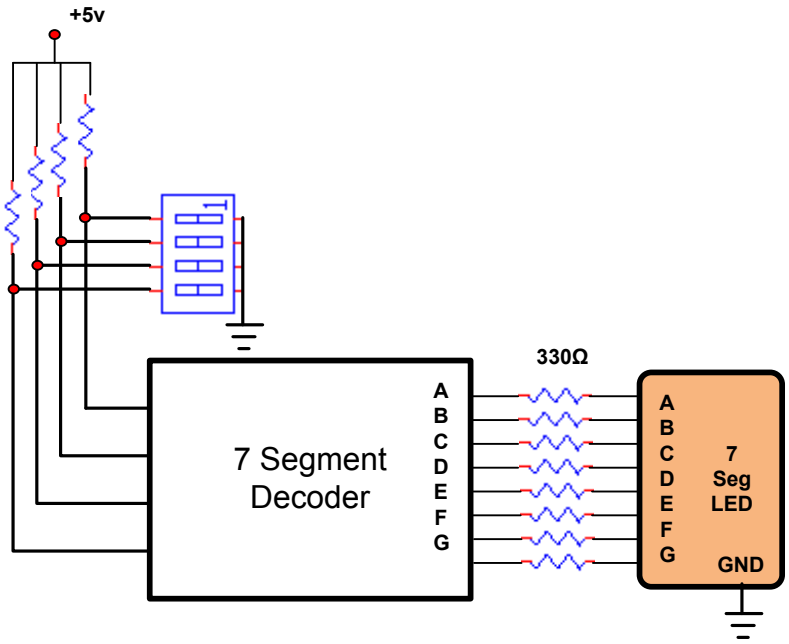
The objective of this project is to experiment the design and implementation of a combinational circuit.

Project Description

Alarm clocks and old-time calculator used seven-segment LED displays to display digits and sometimes letters. For this project, you will design a combinational logic circuit which will accept a four-bit binary number as input and display the decimal value up to 9, and the letter "H" if the decimal value exceeds 9. In other words, the first ten permutations, 0000 – 1001 should be interpreted as decimal digits and the remaining permutations 1011-1111 should correspond to "H", indicating Hexadecimal. You are to design the combinational circuit of the 7-Segment decoder. Your design should have seven outputs – one for each segment of a display digit as follows.

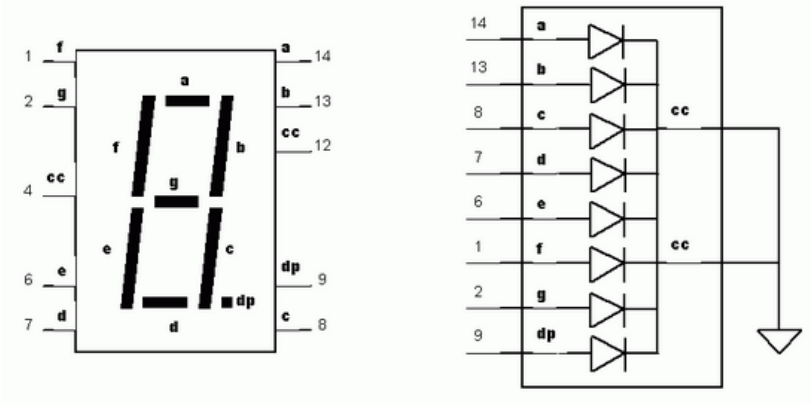


The designed logic can be verified using the following setup.

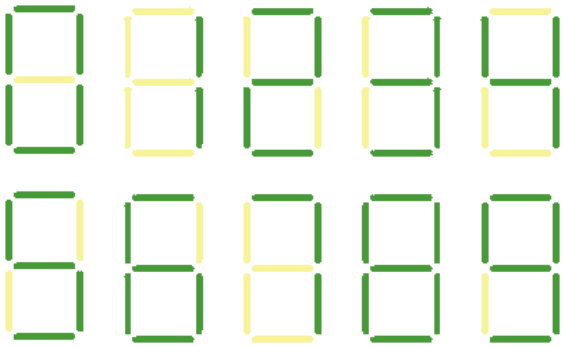


You should have MAN74 7-segement display in your box. The embedded LEDs in the MAN74 are designed to operate at 20 mA. Therefore, choose any resistor values between 250 Ω and 1KΩ to limit

current through the LED. Connect the "CC" terminals (Common Cathode) on the MAN74 to ground. "DP" is the decimal point, which we do not need.



In order to unify the display of all decimal digits, the following figure shows what LED's need to turn on for each digit. Please note that '1' is displayed with the right-most LED's, and the '9' needs to have bottom LED turned on for its base.



Data Sheets

- The data sheet for 7-seg LED can be found here: http://pdf1.alldatasheet.com/datasheet-pdf/view/89363/ETC/TOS5121.html. For the MAN074, the datasheet can found on http://www.eng.auburn.edu/~niuguof/2210lab/data%20sheets/MAN74A_7seg_display.pdf
- The difference between Anode and Cathode based LEDs will be explained in the lab discussion.

To Do

- The designed logic should have minimum number of gates, try to simplify so that it will help in wiring.
- The design should be verified using Verilog with a test bench covering all the test cases.
- The Verilog should be designed in 'structural model', using only 2-, 3- and 4-input gates.

Project Report

- A project report is due on Feb 29, 2016. Make sure to explain your design, reductions and simulation results of the Verilog.

Submission

- On Feb 26, 2016, the design has to be implemented in the bread board and the output should be displayed in the 7-segment LED.
- Once the implementation is complete, the TA will verify the outputs with any random input.
- The submission deadline for the report and Verilog files (including testbench) is Feb 29, 2016. Submit ***all files*** using blackboard.

  Please do NOT email your project submissions to the TA or the instructor, unless you have a problem with for your blackboard account.

Important Notes:

- This has to be an individual work; any act of plagiarism will be penalized and reported.
- You MUST come to the lab on Feb 26, 2016 with your completed design and schematic.
- On Oct/11, the first group can start their lab at noon and end at 2:00pm. The second group can go from 2:00pm until 4:00pm. This will allow sufficient time for implementing your design. If you have a schedule conflict with your time slot, please let us know.
- On Feb 26, 2016, there will be no discussion session. The lab will start at 2:00pm and run until 4:00pm. This will allow sufficient time for implementing your design