Lab #6: UART, DB-9 and MAX235

Name_____

*****All Schematics and Screenshots must be uploaded in your CMPE 310 BOX I created for you. AND PRESENTED to TA before leaving lab.*****

Getting Started. The objective of this Lab is to continue from Lab#5 to create a schematic design for the UART (16550), DB-9 serial connector, MAX235, and their accompanying circuitry by placing and connecting the parts, running the Design Rules Check, and generating the netlist using the Cadence OrCad Capture CIS software.

You should complete this lab individually. When you have completed the assignment, raise your hand to get TA's attention, so that you can present your schematic layout to the TA and get your lab signed off before leaving class.

Reading/reference materialor

- Capture CIS tutorial
- Allegro PCB Design tutorial
- Textbook

Concepts

Illustrate the importance developing skills in using an EDA tool to create schematic and PCB design.

Task: Create a schematic design for the UART, DB-9 serial connector and MAX235 using Cadence OrCad Capture CIS. This is the fifth step of Project I, so make sure you print out the Project I description to keep track of your progress. Information on MAX235 is provided in Lab slides.

You can use discrete gate ICs, 3-to-8 decoder, 2-to-4 decoder or 16L8 (preferable) for decoding various addresses. Include the 16L8 programs if you decided to use them for decoding. Consider using the least number of chips required to perform IO and memory decoding.

*****All Schematic design and Screenshot must be uploaded in your CMPE 310 BOX I created for you.*****