CMPE 310
Systems Design and Programming

L15: Chapter 12 – Interrupts

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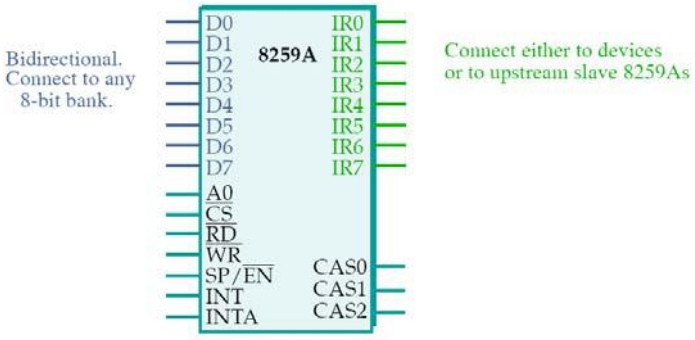
L15 Objectives

* Describe the function of each pin of the 8259 PIC chip
* Diagram how the 8259 is connected to the x86/88 PC
* Program the 8259 PIC (Initialization & Operation)

8259A Programmable Interrupt Controller

- The 8259A adds 8 vectored priority encoded interrupts to the microprocessor.
- It can be expanded to 64 interrupt requests by using one master 8259A and 8 slave units.

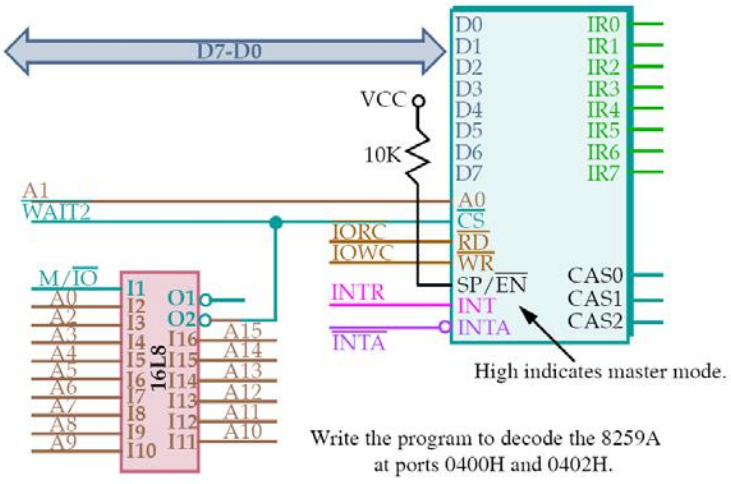


- $\overline{CS}$ pin must be decoded. Other connections are direct to microprocessor.
- The $\overline{WR}$ pin must have an I/O bank write pulse

8259A Programmable Interrupt Controller

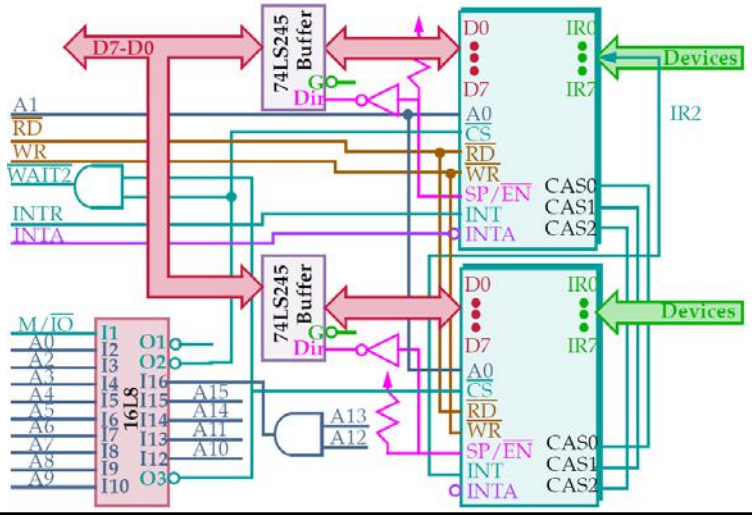
- The meaning of the other connections:
  - $\overline{WR}$: write input connects to a write strobe signal ($\overline{IOWC}$).
  - $\overline{RD}$: read input connects to the $\overline{IORC}$ signal.
  - INT: interrupt output connects to the INTR pin on the microprocessor.
  - $\overline{INTA}$: interrupt acknowledge input connects to the $\overline{INTA}$ pin on the microprocessor.
  - A0: address input selects different command words in the 8259A.
  - $\overline{CS}$: Chip select enables the 8259A for programming and control.
  - SP/$\overline{EN}$: Slave Program (input that programs the device as 1 for master, 0 for slave)/Enable Buffer (output that controls the data bus transceivers when in buffered mode).
  - CAS2-CAS0: cascade lines are used as outputs from the master to the slaves in cascaded systems.

A single 8259A connected to the 8086



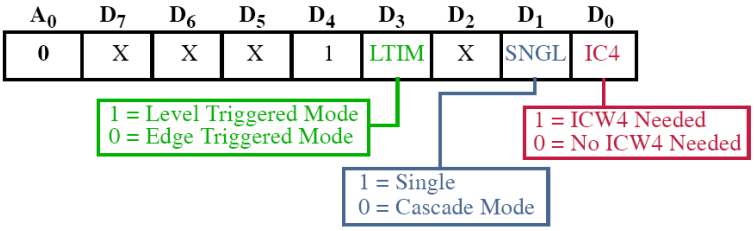
Write the program to decode the 8259A at ports 0400H and 0402H.

Cascading multiple 8259As connected to the 8086



Programming the 8259A

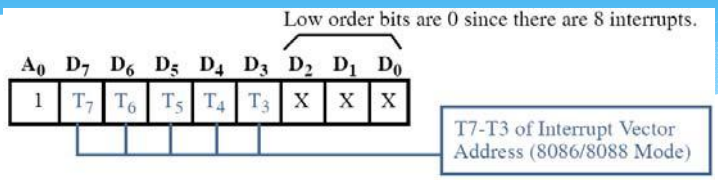
- Programmed by ***Initialization (ICWs)*** and ***Operation (OCWs)*** Command Words.
- There are 4 ICWs.
  - At power-up, ICW1, ICW2 and ICW4 must be sent.
  - If ICW1 indicates cascade mode, then ICW3 must also be sent.
- ICW1:



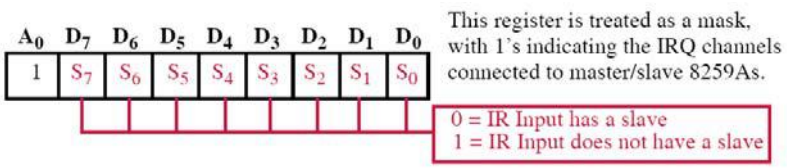
- LTIM indicates if IRQ lines are positive edge-triggered or level-triggered.
- D7-D5 & D2 always 0 for x86 CPU

Programming the 8259A

- ICW2:

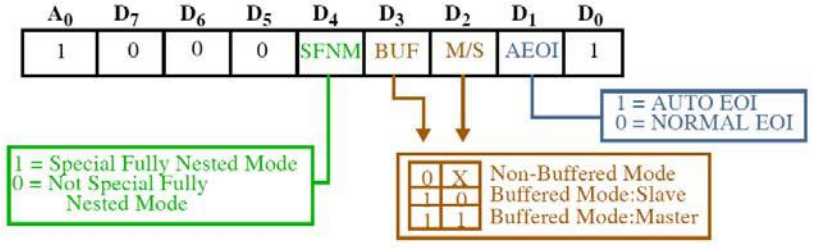


  - These bits determine the vector numbers used with the IRQ inputs.
    - For example, if programmed to generate vectors 08H-0FH, 08H is placed into these bit positions.
- ICW3:



Programming the 8259A

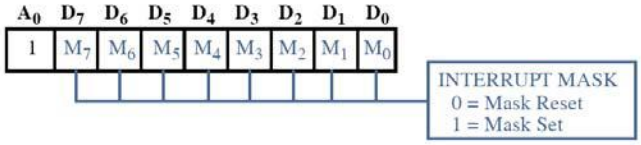
* ICW4:



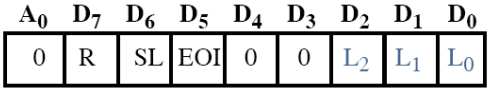
* AEOI, if 1, indicates that an interrupt automatically resets the interrupt request bit, otherwise OCW2 is consulted for EOI processing.
* Fully nested mode allows the highest-priority interrupt request from a slave to be recognized by the master while it is processing another interrupt from a slave.

Programming the 8259A

* The Operation Command Words (OCWs) are used to control the operation of the 8259A.
  * OCW1:



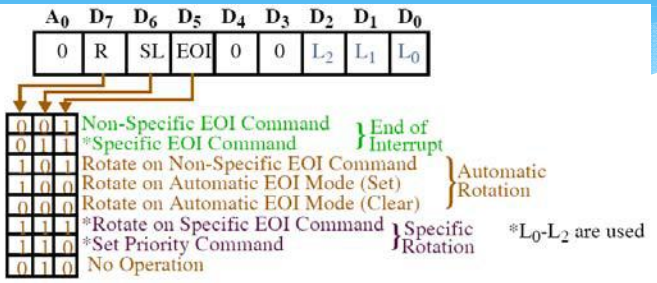
  * OCW1 is used to read or set the interrupt mask register.
    * If a bit is set, it will turn off (mask) the corresponding interrupt input.
  * OCW2:



  * Only programmed when the AEOI mode in ICW4 is 0.
  * Allows you to control priorities after each interrupt is processed

Programming the 8259A

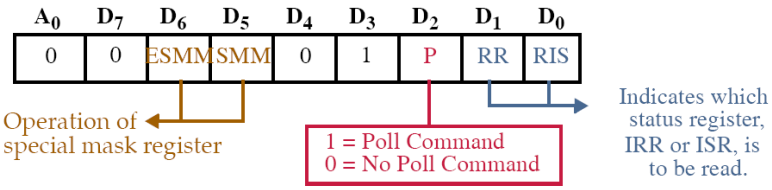
OCW2:



- ***Non-specific EOI:*** Here, the ISR sets this bit to indicate EOI. The 8259A automatically determines which interrupt was active and re-enables it and lower priority interrupts.
- ***Specific EOI:*** ISR resets a specific interrupt request given by L_2-L_0. Rotate commands cause priority to be rotated with regards to the current one being processed.
- ***Set priority:*** allows the setting of the lowest priority interrupt (L_2-L_0).

Programming the 8259A

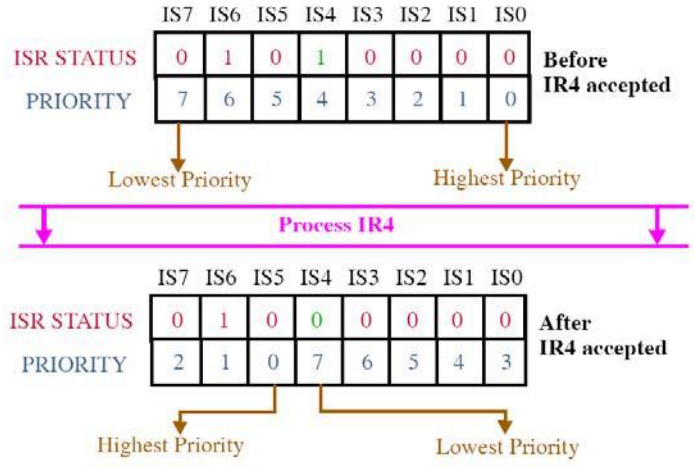
- OCW3:



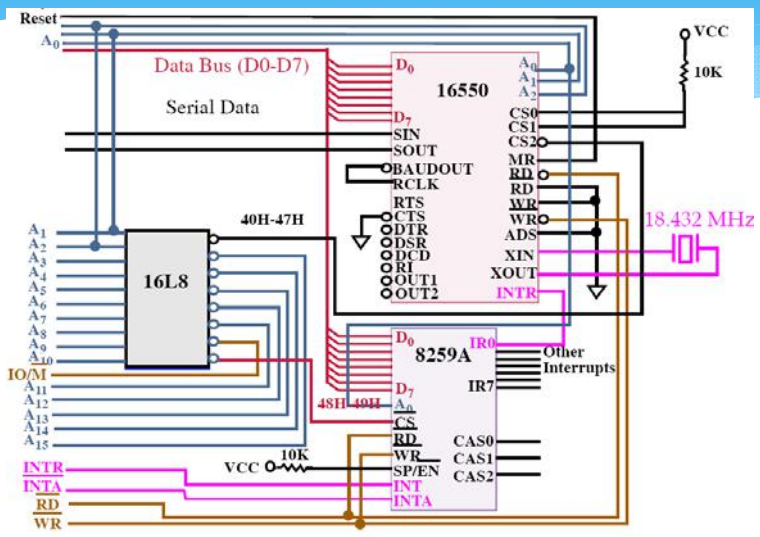
- If polling is set, the next read operation will read the poll word.
  - If the leftmost bit is set in the poll word, the rightmost 3 bits indicate the active interrupt request with highest priority.
- Allows ISR to service highest priority interrupt.
- There are three status registers, Interrupt Request Register (IRR), In-Service Register (ISR) and Interrupt Mask Register (IMR).
  - IRR: Indicates which interrupt request lines are active.
  - ISR: Level of the interrupt being serviced.
  - IMR: A mask that indicates which interrupts are on/off.

Programming the 8259A

- ISR update procedure with rotating priority configured.



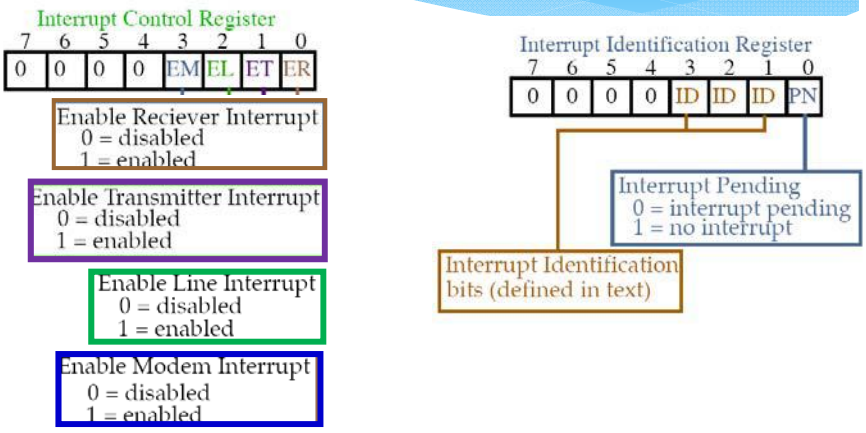
Interfacing 16550 UART using 8259A



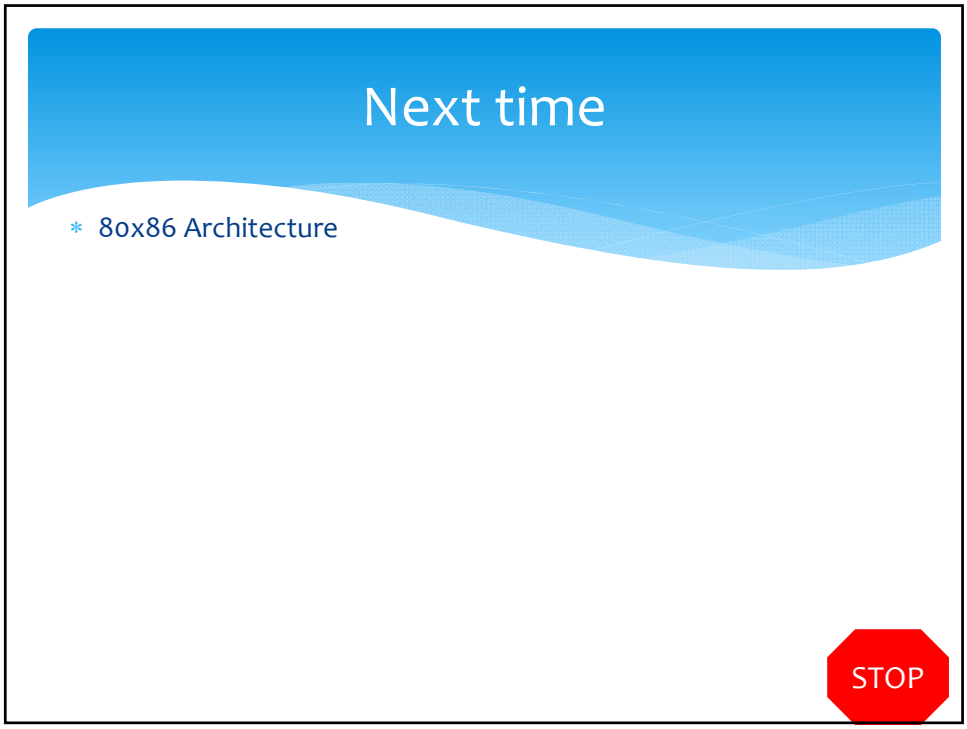
Interfacing 16550 UART using 8259A

- In the following configuration, the 16550 is connected to the 8259A through IR_0.
- An interrupt (IR_0) is generated, if enabled through the interrupt control register, when either:
  - The transmitter is ready to send another character.
  - The receiver has received a character.
  - An error is detected while receiving data.
  - A modem interrupt occurs.
- The16550 is decoded at 40H and 47H.
- The 8259A is decoded at 48H and 49H.
- Program in text shows the steps involved in programming both devices.
  - Since the 16550 generates only one interrupt request for each of the above interrupts, the 16550 must be polled.
  - Examining the interrupt identification register of the 16550

16550 UART Interrupts



Text gives ISR programming examples that show initialization and operation.


Next time
8ox86 Architecture
STOP