Question: 02
DATE: October 6, 2017
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1 Background

Using synthesizable procedural code, create a module that with every clock cycle outputs a 1-bit value that represents the input 5 clock cycles prior. The module should also support an asyncronous reset that allows the initial outputs to be zero until the first input propogates to the output.

2 Implementation

The output 'y' was generated as a simple delayed assignment to the input 'x'. The module implementation along with its testbench can be found in the 'scripts' directory. A sample of the waveform generated is provided:

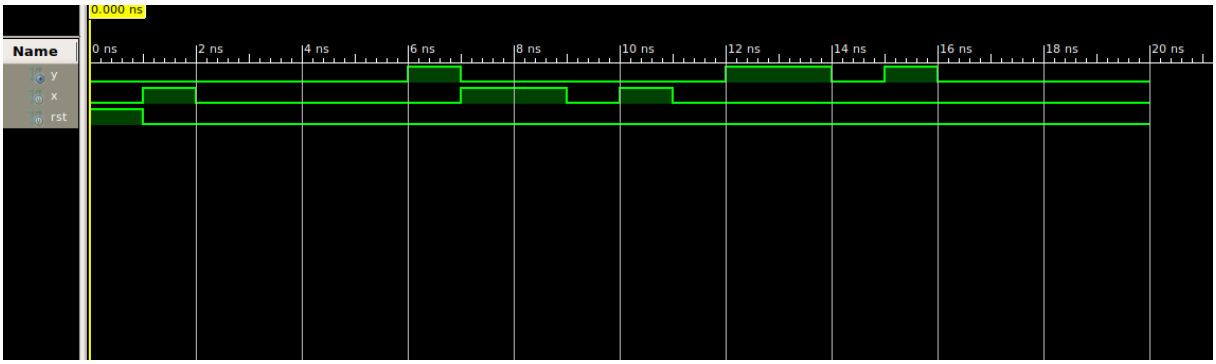

Figure 1: Waveform Generated from Part 2 Test Bench