CMPE 314: Principles of Electronic Circuits

Dr. Yan

Lab 05 Report

Common Emitter Amplifier Circuit

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1. **Objective**

   Construct and study the common-emitter amplifier circuit.

2. **Equipment**
   a. Resistors;
      i. Given: 1 × 560 Ω, 1 × 2.2 kΩ
      ii. Computed: 1 × 470 Ω, 2 × 4.7 kΩ, 1 × 6.8 kΩ, 1 × 15 kΩ, 1 × 22 kΩ, 1 × 47 kΩ
      iii. Potentiometer: 1 × 2 MΩ
   b. Capacitor; 1 × 1 µF
   c. Transistor; 1 × 2N3904 NPN
   d. Breadboard, DC power supply, digital multi-meter(s), oscilloscope, function generator

3. **Background**

   A common-emitter amplifier is one of three basic single-stage bipolar-junction-transistor (BJT) amplifier topologies, typically used as a voltage amplifier. In this circuit, the base terminal of the transistor serves as the input, the collector is the output, and the emitter is common to both.

4. Procedures

4.1 Part A. Pre-lab Exercise

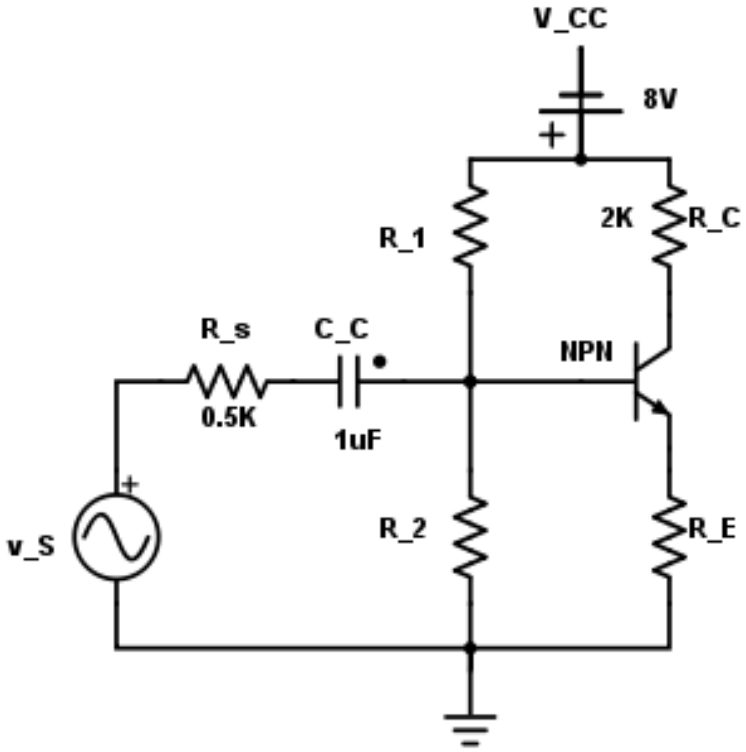

Figure 1: Common Emitter Amplifier with an NPN Transistor

a. Assuming $\beta_F = 100$, study the circuit from Figure 1.
b. Determine the values of R_1, R_2, and R_E so that the Q-point is in the middle of the forward active region $V_{CEQ} = 4$ V. Calculate I_{BQ}, I_{CQ}, and V_{CEQ}.
c. Repeat step b. so that the Q-point is near the cut-off region.
d. Repeat step b. so that the Q-point is near the saturation region.

4.2 Part B. Lab Procedures

a. Set $V_{CC} = 8$ V. Use the values given and computed in the pre-lab for R_1, R_2, R_C and R_E such that the Q-point is in the middle of the forward active region.
b. Measure I_{BQ}, I_{CQ} and V_{CEQ} and compare against the calculated values. Find the DC forward current gain.
c. Connect the sinusoidal voltage source v_s with amplitude ±100 mV and at frequency 10 kHz to the circuit. Record down both the input voltage v_s and output voltage v_o waveforms using the oscilloscope. Comment on the phase relationship. Find the small signal voltage gain and compare to the theoretical value.

d. Increase the input sinusoidal voltage, and record down any signal distortion. Comment on whether it is due to cutoff clipping or saturation clipping. What is the maximum symmetric swing?
e. Use a potentiometer as load resistor (20 MΩ). Vary and measure the resistance, record down the output waveforms. Comment how the small signal gain is influenced by the value of the load resistance, and the output impedance of the amplifier circuit.
f. Plot the DC and AC load lines.
g. Change R_1 or R_2 value (near the cutoff region). Repeat steps b. to d.
h. Change R_1 or R_2 value (near the saturation region). Repeat from step b. to d.

5. Results

For computing the resistor values, only the portion of the circuit affected by the DC voltage was considered.

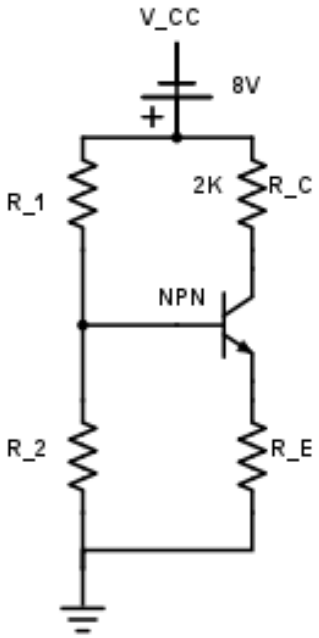

Figure 2: DC Portion of Common Emitter Amplifier with an NPN Transistor

Computation for the circuit with its Q-Point in the middle of the forward active region:

$\because V_{CEQ} = 4\,V\ (middle\ of\ the\ forward\ active\ region), V_{CC} = 8\,V, R_C = 2\,k\Omega$

$R_E = \frac{V_{BE(on)}(R_C+R_E)}{V_{CC}-V_{CEQ}} = \frac{(0.7)(2000+R_E)}{8-4} \rightarrow R_E = 424.24\,\Omega$

$R_{TH} = 0.1(1+\beta)R_E = 0.1(1+100)(424.24) = 4284.82\,\Omega$

$I_{EQ} = I_{CQ} = \frac{V_{CC}-V_{CEQ}}{R_C+R_E} = \frac{8-4}{2000+424.24} = 0.00165\,A = 1.65\,mA$

$V_{TH} = \frac{I_{EQ}}{1+\beta} + V_{BE(on)} = \frac{0.00165}{1+100} + 0.7 = 0.7$

$V_{TH} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right) = 1.537\,V$

$\because R_{TH} = \frac{R_2R_1}{R_1+R_2}$

$\therefore R_1 = 24708.0\,\Omega, R_2 = 5875.9\,\Omega$

$\therefore I_{CQ} = 1.62\,mA, I_{BQ} = 0.0162\,mA$

Computation for the circuit with its Q-Point near the cut-off region:

$\because I_{CQ} = 0.0148\ (near\ the\ cutoff\ region)$

$$0.0000148 = \frac{V_{TH} - V_{BE}(on)}{R_{TH} = (1+\beta)R_E}$$

$V_{TH} = 0.777\ V$

$$\because V_{TH} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right), R_{TH} = \frac{R_2 R_1}{R_1 + R_2}$$

$R_1 = 42765.77\ \Omega, R_2 = 5339.71\ \Omega$

$I_C = 0.148\ mA, I_B = 0.00148\ mA$

Computation for the circuit with its Q-Point near the saturation region:

$\because I_C = 3\ mA\ (near\ the\ saturation\ region), V_{CEQ} = 0.7\ V$

$$\frac{I_{CQ}}{\beta} = \frac{V_{TH} - V_{BE}(on)}{R_{TH} + (1+\beta)R_E} = \frac{V_{TH} - 0.7}{4284.82 + (101)(424.24)} \rightarrow V_{TH} = 2.11\ V$$

$$\because V_{TH} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right), R_{TH} = \frac{R_2 R_1}{R_1 + R_2}$$

$R_1 = 16298.7\ \Omega, R_2 = 6679.7\ \Omega$

$I_C = 3.02\ mA, I_B = 0.030\ mA$

After all the resistor values for all the different regions were computed, the DC part of the circuit was constructed, as per Figure 2. The resistance values for the Q-point were selected as R_1 = 22 kΩ and R_2 = 4.7 kΩ. I_{BQ}, I_{CQ} and V_{CEQ} were measured and the outputs are displayed below:

Table 1: Transistor Voltage and Current Measured at Q-point

	V_{CEQ} (V)	I_{CQ} (mA)	I_{BQ} (mA)
Measured	3.78	1.5	0.2
Computed	4	1.62	0.0162

The sinusoidal voltage source was added, along with the other components to construct the circuit from Figure 1. The following waveform was captured:

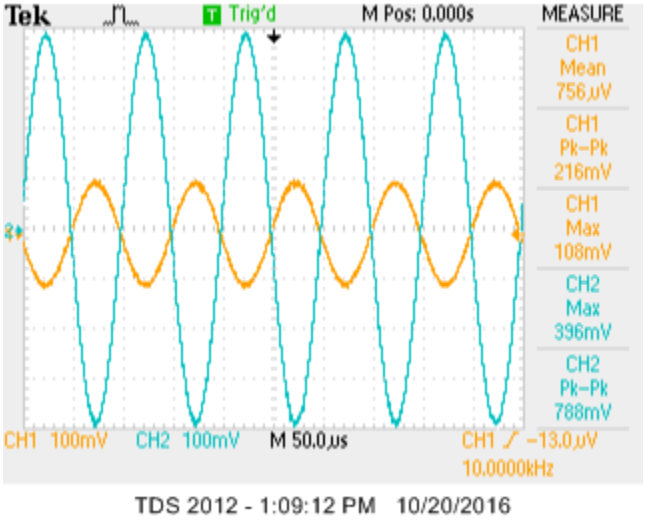

Figure 3: Input and Output Voltages of the Circuit at Q-Point

The voltage gain, A_v, can be computed with the relationship:

$$A_v = \frac{R_C}{R_C} \approx \frac{v_o}{v_i} \rightarrow \frac{2200}{470} \approx \frac{396}{108} \rightarrow 4.68 \neq 3.66$$

although the voltage gain can be observed from the input and output voltages themselves, it does not agree with the ratio of the resistors. The error may be due to the different resistor values used for the simulation of the circuit since resistors with the exact computed values were not available.

The input voltage was increased until the output starting to appear distorted, and the maximum symmetric swing was determined to be 900 mV.

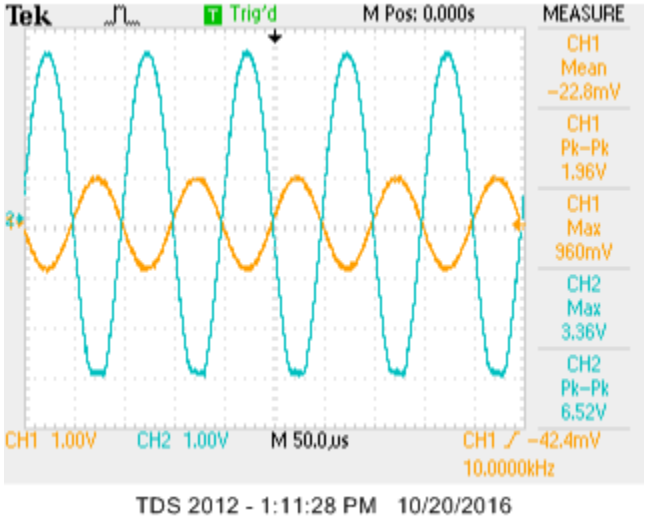

Figure 4: Input and Output Voltages at the Maximum Symmetric Swing

The load lines were then calculated for the circuit constructed.

The DC load line was computed with the relationship: $I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$

The AC load line was computed with the relationship: $i_c = \frac{V_{CE}}{R_C}$

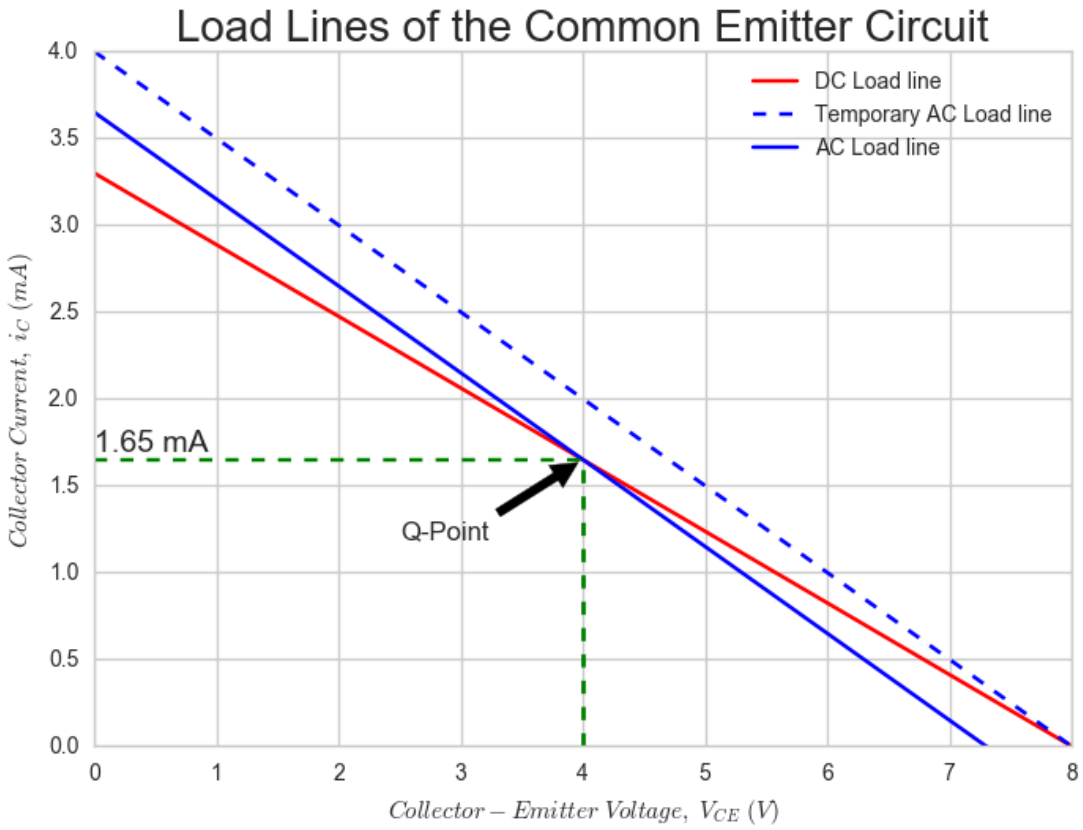

Figure 5: DC and AC load lines of the Circuit Constructed

Due to constraints in time, only the DC portions of the cut-off and saturation region analysis were completed.

The resistance values for the circuit such that its Q-point was near the cut-off region were selected as R_1 = 22 kΩ and R_2 = 4.7 kΩ. I_{BQ}, I_{CQ} and V_{CEQ} were measured and the outputs are displayed below:

Table 2: Transistor Voltage and Current Measured with its Q-point in the Cut-Off Region

	V_{CEQ} (V)	I_{CQ} (mA)	I_{BQ} (mA)
Measured	7.97	0.1	0
Computed	8	0.148	0.00148

The resistance values for the circuit such that its Q-point was near the saturation region were selected as R_1 = 22 kΩ and R_2 = 4.7 kΩ. I_{BQ}, I_{CQ} and V_{CEQ} were measured and the outputs are displayed below:

Table 3: Transistor Voltage and Current Measured with its Q-point in the Saturation Region

	V_{CEQ} (V)	I_{CQ} (mA)	I_{BQ} (mA)
Measured	0.61	2.9	0
Computed	0.7	3.02	0.0302

The tolerance for the ammeter inside the multimeter used was not able to measure very low magnitudes of current, so I_{BQ} appeared to be negligibly zero.

6. Conclusion

There were several aspects of this lab that yielded outputs with significant errors. If more time was permitted, and more preparation was made by the team members especially in the pre-lab assignment, the issues would have been resolved. Nevertheless, a voltage gain was demonstrated and even with an error in this lab report, provided better insight on small signal waves.