Lab #2: Beginner 8086 Board Designer

Name_____

All Schematics and Screenshots must be uploaded in your CMPE 310 BOX I created for you.
AND PRESENTED to TA before leaving lab.

Getting Started. The objective of this project is to use knowledge gain from Lab#0 and Lab#1 to create a schematic design for the x86 and its accompany clock generator circuitry by placing and connecting part, running Design Rules Check, and generating netlist using Capture CIS.

You should complete this lab individually. When you have completed the assignment, raise your hand to get TA's attention, so that you can present your schematic layout to the TA and get your lab signed off before leaving class.

Reading/reference material

- Capture CIS tutorial
- Project I description

Concepts

Illustrate the importance developing skills in using an EDA tool to create schematic and PCB design.

Problem: Create a schematic design for the x86 and its accompany clock generator using Capture CIS. This is to get you started on Project I. So make sure to print out Project I description.

*****All Schematic design and Screenshot must be uploaded in your CMPE 310 BOX I created for you**.***