CMPE 310
Systems Design and Programming

L4: Chapter 9 – 8086/8088 Hardware Specifications

UMBC
AN HONORS UNIVERSITY IN MARYLAND

L4 Objectives

* Describe the pin-outs of the x86/88
* Understand the difference between MN/$\overline{MX}$ mode of operation
* Understand the DC Characteristics of the 86/88
* Understand the function of the clock generator
* Diagram a fully demultiplex the AD bus

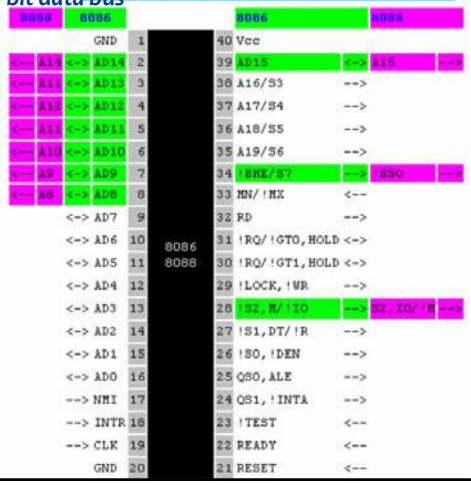
Microprocessor interfacing

* What information/signals should a processor take as input?

* What information/signals should a processor send as output?

8086/88 Device Specifications

* Both are packaged in 40-pin DIP (Dual In-Line Packages)
  * 8086: 16-bit microprocessor with a ***16-bit data bus***
  * 8088: 16-bit microprocessor with an ***8-bit data bus***



8086/88 Device Specifications

Power Supply Requirements for 8086/88

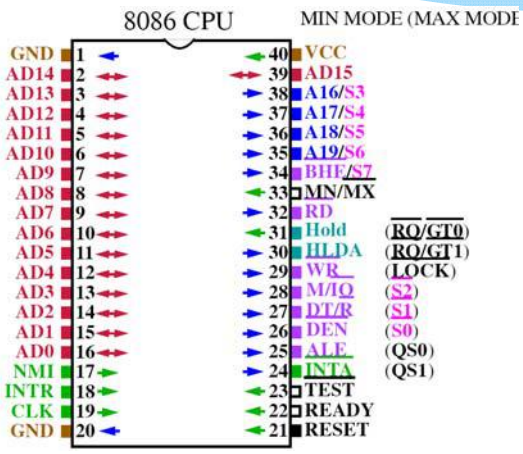
- Voltage: 5V (i.e. V_{DD} is 5V)
  - Power Supply Current:
  - 8086/88: TTL Version 360/340 mA, with temp spec 32 to 180 °F
  - 80C86/80C88: CMOS Version 10 mA, with temp spec -40 to 225 °F
- DC Characteristics: Input/Output current levels:

INPUT Logic level	Voltage	Current	OUTPUT Logic level	Voltage	Current
0	0.8V max	+/- 10uA max	0	0.45V max	+2mA max
1	2.0V min	+/- 10uA max	1	2.4V min	- 400uA max

- Output Logic 0 is not compatible with standard devices → reduced noise immunity
- Yields a 350mV noise immunity for logic 0. This limits the loading on the outputs.

8086/88 Device Specifications

8086/88 Pinout



8086/88 Device Specifications

- ***AD15-AD0.***
  - Multiplexed address(ALE=1)/data bus(ALE=0).
- ***A19/S6-A16/S3 (multiplexed).***
  - High order 4 bits of the 20-bit address (A_{19}-A_{16}) OR status bits S_6-S_3.
- ***$M/\overline{IO}$.***
  - Indicates if address is a Memory or IO address.
- ***$\overline{RD}$.***
  - When 0, data bus is receptive to data from either memory or I/O device.
- ***$\overline{WR}$.***
  - A strobe pin to indicate that µP is outputting data to memory or an I/O device. When 0, data bus contains valid data for memory or I/O.
- ***ALE (Address latch enable)***
  - When 1, address/data bus contains a memory address or I/O port number.
- ***DT/$\overline{R}$ (Data Transmit/Receive)***
  - Data bus is transmitting/receiving data from external bus.
- ***$\overline{DEN}$ (Data bus Enable)***
  - Activates external data bus buffers.

8086/88 Device Specifications

8086/88 Pin-outs

- ***S7, S6, S5, S4, S3, $\overline{S2}$, $\overline{S1}$, $\overline{S0}$***
  - ***S7:*** Logic 1, S6: Logic 0.
  - ***S5:*** Indicates condition of IF flag bits.
  - ***S4-S3:*** Indicate which segment is accessed during current bus cycle:

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{S2}$, $\overline{S1}$, $\overline{S0}$: Indicate function of current bus cycle (decoded by 8288).

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
0	0	0	Interrupt Ack
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

8086/88 Device Specifications

- ***INTR***
  - When 1 and IF=1, µP prepares to service interrupt. INTA becomes active after current instruction completes.
- ***$\overline{INTA}$***
  - Interrupt Acknowledge generated by the µP in response to INTR.
- ***NMI***
  - Non-maskable interrupt. Similar to INTR except IF flag bit is not verified and interrupt is vector 2 (causes INT 2).
- ***CLK***
  - Provides the basic timing signal to µP, clock input must have a duty cycle of 33%
- ***VCC/GND***
  - Power supply (+ 5.0 V + 10%) and GND (0V)
- ***MN/$\overline{MX}$***
  - Min/max mode, select minimum (5V) or maximum mode (0V) of operation.

8086/88 Device Specifications

- ***$\overline{BHE}$/S7***
  - Bus High Enable. Enables the most significant data bus bits (D15-D8) during a read or write operation.
- ***READY***
  - Used to insert wait states (controlled by memory and IO for reads/writes) into the µP.
- ***RESET***
  - µP resets if this pin is held high for 4 clock periods.
- ***$\overline{TEST}$***
  - An input that is tested by the WAIT instruction
  - If TEST = 0, WAIT instruction becomes a NOP; TEST=1, µP enters into wait state till TEST = 0. Commonly connected to the 8087 coprocessor.
- ***HOLD***
  - Requests a direct memory access (DMA). When 1, µP stops and places address, data and control bus in high-impedance state; when 0, µP execute software normally.
- ***HLDA (Hold Acknowledge)***
  - Indicates that the µP has entered the hold state.

8086/88 Device Specifications

* $\overline{RQ/GT_1}$ and $\overline{RQ/GT_0}$
  * Request/grant pins request/grant direct memory accesses (DMA) during maximum mode operation.
* $\overline{LOCK}$
  * Lock output is used to lock peripherals off the system. Activated by using the LOCK: prefix on any instruction.
* QS_1 and QS_0
  * The queue status bits show status of internal instruction queue.

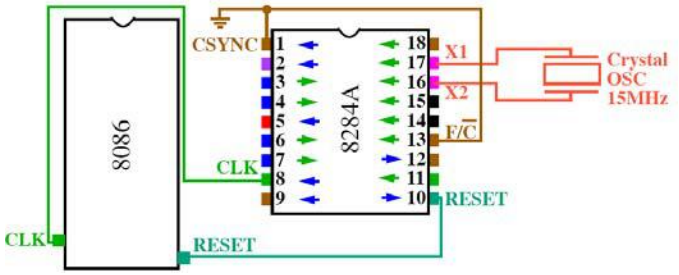
System clock

* Used to synchronize both internal and external operations
* Generated by external oscillator
* Specified in terms of frequency or cycle time
  * Cycle time = 1 / frequency
  * E.g. 20 MHz clock → cycle time = $1 / 20 \times 10^6 = 50$ ns
* x86 specifics
  * 86/88→ 5 MHz (Internal clock: $^1/_3$ frequency of CLK)
  * 386 → Valid internal frequencies 16, **20**, 25, 33 MHz (½ frequency of CLK)
  * One (internal) cycle: 1 "T state"

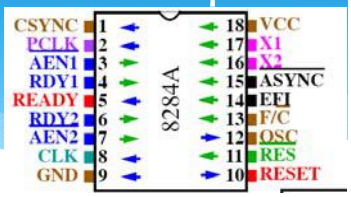
8284A Clock Generator

* 8284A is an ancillary component to 8086/88
  * Clock generation
  * RESET synchronization
  * READY synchronization
  * TTL-level Peripheral clock signal

Connection of the 8284 and the 8086.



8284A Clock Generator Pin Description

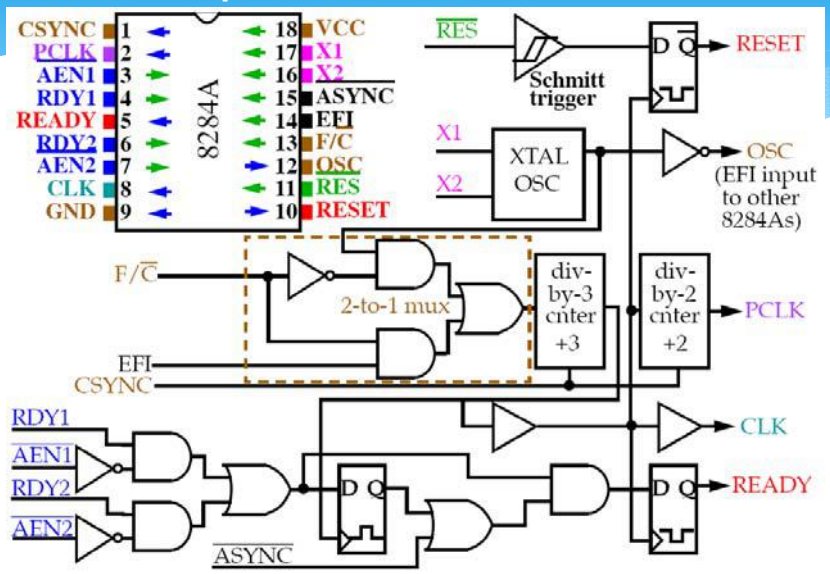


* $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$
  * Address enable - these signals are provided to qualify the RDY1 and RDY2 signals
* RDY1 and RDY2
  * Bus ready – these signals along with address enable signals control the insertion of wait states
* $\overline{\text{ASYNC}}$
  * Ready Synchronization – Selects either one or two stages of synchronization for RDY1 and RDY2.
* X1 and X2 (crystal in)
  * Crystal Oscillator – for connection to an external crystal oscillator
* F/$\overline{\text{C}}$
  * Frequency/Crystal Select – chooses the clocking source for 8284A
  * If this pin is held high, an external clock is provided to EFI input pin
* EFI
  * External frequency input – auxiliary source of external clock/timing

8284A Clock Generator Pin Description

* CLK
  * Clock Output pin – provides clock to x86 processors. CLK freq. is 1/3 of crystal (or EFI) and has 33% duty cycle
* PCLK
  * Peripheral Clock – 1/6 of the crystal (or EFI) freq and has 50% duty cycle
* OSC
  * Oscillator output – A TTL level signal to be used as EFI for another 8284A
* RES
  * Reset input – Active low. Typically connected to an RC network for power-on reset
* RESET
  * Reset Output – connected to x86 µP reset input pin
* CSYNC
  * Clock Synchronization pin – used with **EFI** to have a synchronous clocking mechanism. If internal crystal is used, this pin & **F/C** must be grounded

8284A Clock Generator

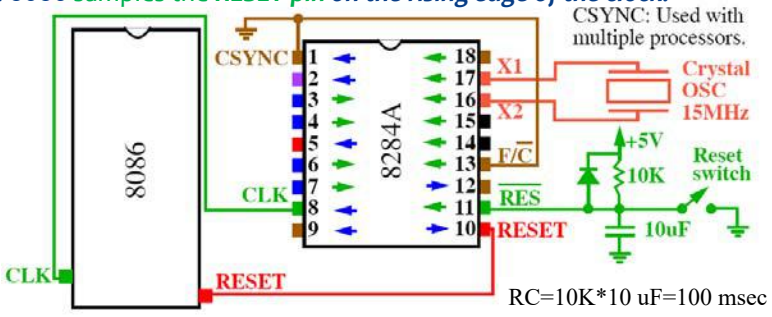


Clock generation

- Crystal is connected to X1 and X2.
- XTAL OSC generates square wave signal at crystal's frequency which feeds:
  - An inverting buffer that provides the OSC output signal which is used to drive the EFI input of other 8284As.
- 2-to-1 MUX
  - F/C selects XTAL or EFI external input.
  - The MUX drives a divide-by-3 counter (15MHz to 5MHz).
  - This drives:
    - The ***READY flipflop (READY synchronization).***
    - A second ***divide-by-2 counter (2.5MHz clk for peripheral components).***
    - The ***RESET flipflop.***
    - ***CLK which drives the 8086 CLK input.***

RESET Operation

- Negative edge-triggered flip-flop applies the RESET signal to the 8086 on the falling edge.
- The 8086 samples the ***RESET pin on the rising edge of the clock.***



- Correct reset timing requires that the ***RESET input to the microprocessor becomes a logic 1*** *in 4 clocks after power up and stay high for at least 50μs.*

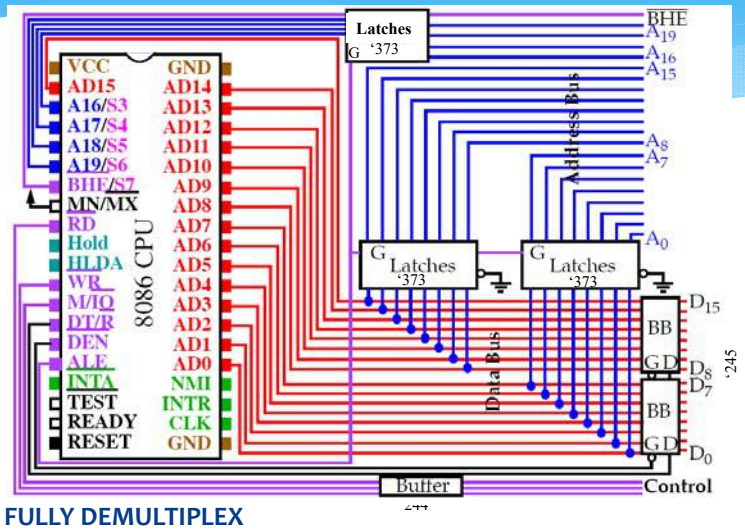
BUS Buffering and Latching

- Before connecting to any peripheral or memory, the x86 buses need to be demultiplexed
  - If there are a number of components in the system, the buses should be buffered
  - Memory and I/O require that the address remain valid and stable throughout the read or write cycle
    - If buses are **multiplexed**, the address changes at memory or I/O, will cause them to **read or write data** in the wrong locations

BUS Buffering and Latching

- X86 systems have three buses
  - Address
  - Data
  - Control
- The Address and Data bus are ***multiplexed* due to pin limitations on the 8086.**
  - The ALE pin is used to control a set of latches.
- All signals MUST be buffered
  - Buffered Latches for A_0-A_{15}.
  - Control ('244) and A_{16}-A_{19} + ***BHE ('373) are buffered separately.***
  - Data bus buffers must be bi-directional buffers.
- In a 8086 system, the memory is designed with two banks
  - High bank contains the higher order 8-bits and low bank the lower order 8-bits
  - Data can be transferred as 8 bits from either bank or 16-bits from both
  - ***$\overline{BHE}$ pin selects the high-order memory bank***

BUS Buffering and Latching



FULLY DEMULTIPLEX

Next time

* Bus Cycle

STOP