CMPE 310
Systems Design and Programming

L8: Chapter 10 – Memory Interface

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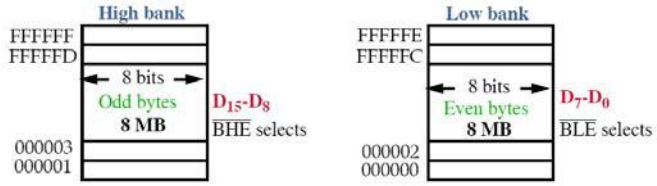
L8 Objectives

* To interface memory components to x86 – Pentium
* Diagram how EPROM and SRAM modules are connected to x86 – Pentium

8086 - 80386SX (16-bit) memory interface

- These machines differ from the 8088/80188 in several ways:
  - The data bus is *16-bits wide.*
  - The IO/$\overline{M}$ pin is replaced with M/$\overline{IO}$ (8086/80186) and $\overline{MRDC}$ and $\overline{MWTC}$ for 80286 and 80386SX.
- $\overline{BHE}$, ***Bus High Enable***, control signal is added.
- Address pin A_0 (or $\overline{BLE}$, ***Bus Low Enable***) is used differently.
- The 16-bit data bus presents a new problem:
  - The microprocessor must be able to read and write data to any 16-bit location in addition to any 8-bit location.
  - The data bus and memory are divided into banks:



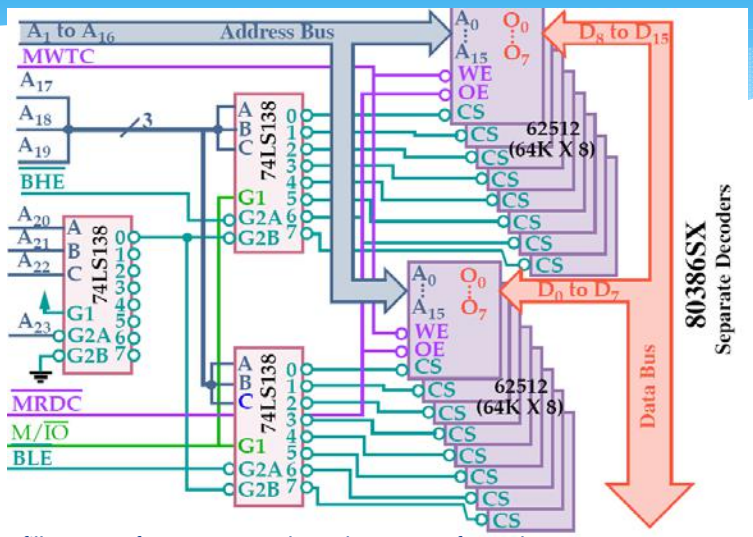
8086 - 80386SX (16-bit) memory interface

BHE and BLE are used to select one or both:

$\overline{BHE}$	$\overline{BLE}$	*Function*
0	0	Both banks enabled for 16-bit transfer
0	1	High bank enabled for an 8-bit transfer
1	0	Low bank enabled for an 8-bit transfer
1	1	No banks selected

- Bank selection can be accomplished in two ways:
  - Separate write decoders for each bank (which drive $\overline{CS}$) OR
  - A separate write signal (strobe) to each bank (which drive $\overline{WE}$).
    - Note that 8-bit read requests in this scheme are handled by the microprocessor (it selects the bits it wants to read from the 16-bits on the bus).
- Note in either method that A_0 does not connect to memory and bus wire A_1 connects to memory pin A_0, A_2 to A_1, etc.

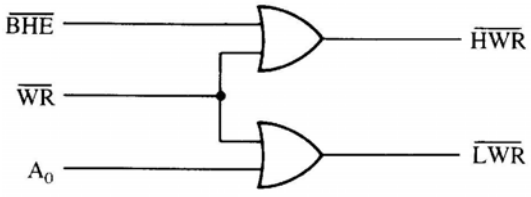
16-bit memory interface (separate decoders)



* 16 64K RAMs fill memory from 000000H through FFFFFFH, for 1M bytes memory

16-bit memory interface (separate write strobe)

* A separate write strobe for each memory bank can be generated to handle bank selection by using a 74LS32 OR gate to combine A_0 or $\overline{BHE}$ with $\overline{WR}$
  * $\overline{WR}$ is generated by using the $\overline{MWTC}$
  * Only require 1 decoder to select a 16-bit wide memory



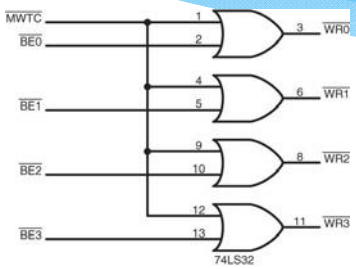
* See text for *Separate Write Strobe* scheme plus some examples of the integration of EPROM and SRAM in a complete system.
  * It is just an application of what we've been covering.

80386DX and 80486 (32-bit) memory interface

- 80386DX and 80486 have 32-bit data buses and therefore 4 banks of memory.
  - *32-bit, 16-bit and 8-bit* transfers are accomplished by different combinations of the bank selection signals $\overline{BE3}$, $\overline{BE2}$, $\overline{BE1}$, $\overline{BE0}$.
  - The Address bits A_0 and A_1 are used within the microprocessor to generate these signals.
    - They are *don't cares* in the decoding of the 32-bit address outside the chip (using a PLD such as the **PAL 16L8).**
  - The high clock rates of these processors usually require ***wait states*** for memory access.

80386DX and 80486 (32-bit) memory interface

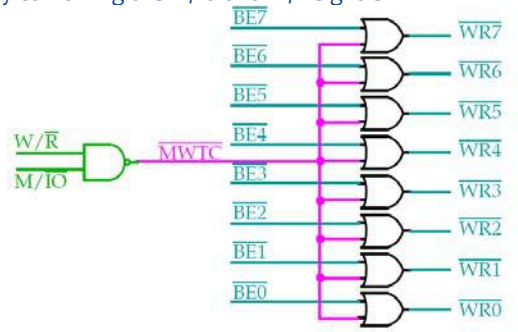
- Separate write strobes are developed, by using a simple 74LS32 OR gate



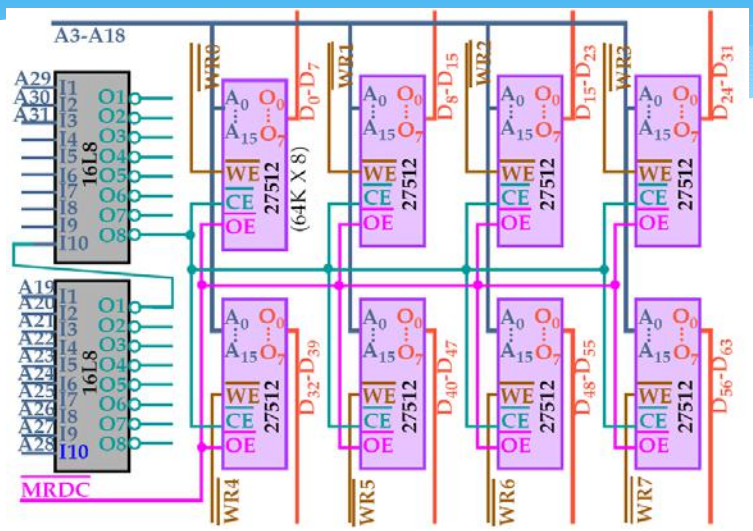
- A memory interface for 80386DX or 80486 **requires four bank write strobes for each memory** bank and decoding a 32-bit address.
- There are no integrated decoders, such as the 74LS138, that can easily accommodate a memory interface for the 80386DX or 80486
  - **PLD is often used for bank write signal generation** because of its sizeable address bits

Pentium (64-bit) memory interface

* The Pentium, Pentium Pro, Pentium II and III contain a 64-bit data bus.
  * Therefore, 8 decoders or 8 write strobes are needed as well as 8 memory banks.
  * The write strobes are obtained by combining the bank enable signals ($\overline{BEx}$) with the $\overline{MWTC}$ signal.
  * $\overline{MWTC}$ is generated by combining the $\overline{M/IO}$ and $\overline{W/R}$ signals.



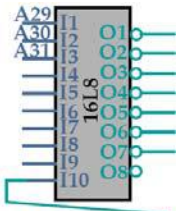
Pentium (64-bit) memory interface



* *Select 512K RAM memory components (FFF80000-FFFFFFFF)*

Pentium (64-bit) memory interface

In order to map previous memory into addr. space *FFF80000H-FFFFFFFFH*




```
;pins 1   2   3   4   5   6   7   8   9   10
      A29 A30 A31 NC  NC  NC  NC  NC  NC  GND
;pins 11  12  13  14  15  16  17  18  19  20
      U2  CE  NC  NC  NC  NC  NC  NC  NC  VCC

Equations:
  /CE = /U2 * A29 * A30 * A31
```


```
;pins 1   2   3   4   5   6   7   8   9   10
      A19 A20 A21 A22 A23 A24 A25 A26 A27 GND
;pins 11  12  13  14  15  16  17  18  19  20
      A28 U2  NC  NC  NC  NC  NC  NC  NC  VCC

Equations:
  /U2 = A19 * A20 * A21 * A22 * A23 * A24 * A25 *
        A26 * A27 * A28
```

* Use a 16L8 to do the $\overline{WR0}$ - $\overline{WR7}$ decoding using $\overline{MWTC}$ and $\overline{BE0}$ - $\overline{BE7}$.
* See the text -- Figure 10-37.

Next Time

* IO Interface