University of Maryland Baltimore County
Department of Computer Science and Electrical Engineering

CMPE 212L, Principles of Digital Design Laboratory

Experiment #4 Friday 2/19/2016

Objective

Multiple input gates are very useful in a digital design. For example to examine whether a number equals to zero, one can perform an OR of all N-bits and check the output. However, the fabrication process does not allow arbitrary large numbers of inputs for a gate. So, we have to implement the same function with gates with fewer inputs. The input to output delay varies according to the design methodology. Having multi-level gates will boost the delay. In this laboratory, you will implement two designs as an alternative of a 5-input AND gate and measure the input to output delay in each case.

Required Equipment

- 7408: includes four 2-input AND gates.
- 7411: includes triple 3-input AND gates.
- (10K ohms) resistors, breadboard, power supply, multi-meter.

Experiments:

1. Implement the first design in which the signals propagate through all intermediate gates sequentially. It takes (N-1) gate delays for the input signal to affect the output (Since the output of each gate depends on the output value of the previous one) (Figure 1).
2. Implement the second design in which the availability of 3-input gates is leveraged. In this design, each signal propagates through fewer gates (Figure 2).
3. Keep all signals HIGH except for the first input (that passes through the critical path) which we call signal "A" from now on.
4. Connect "A" to a square waveform with 0 and 5 as low and high voltage levels.
5. Connect the input signal ("A") to one channel of the oscilloscope and the output of first design (Output1) to the second channel. Measure input-output delay.
6. Repeat step 5 for the output of the second design (Output2) and compare the two delays. You can also connect the two outputs (of the first and second design) to oscilloscope channels and observe their delay difference directly.

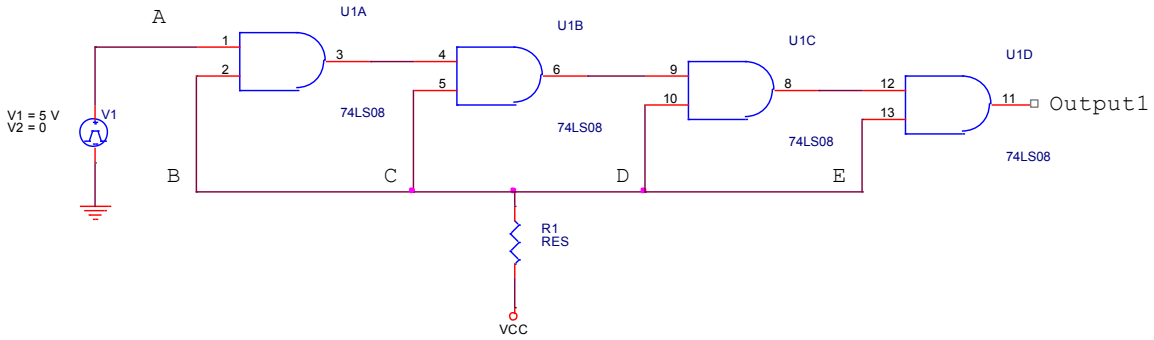

Figure 1 - First Design

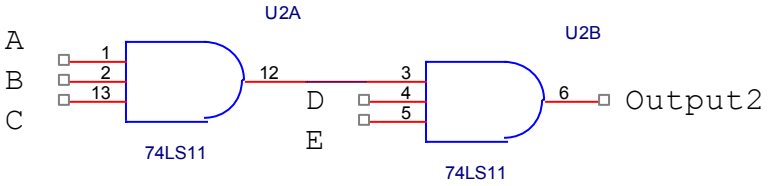

Figure 2 - Second Design

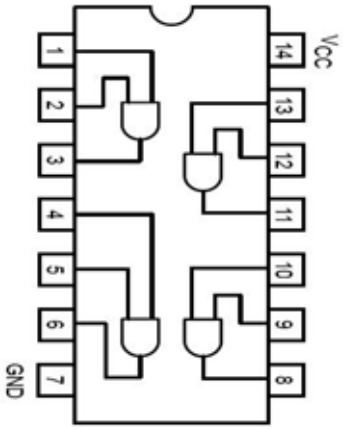

Figure 2 - 7408 Pin Assignment

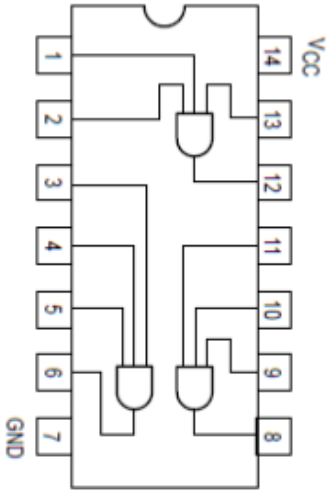

Figure 1 - 7411 Pin Assignment