

# HW 1: Tools Introduction

## CMPE 415

## UMBC

Prof. Ryan Robucci

Assigned Sept 14, 2016; Due Sept 21, 2017; students working in identified pairs are allowed to collaborate without restriction on this assignment but each students should install the software and complete steps on their computer and submit independantly

### 1 Objective

The objective of this lab is to learn the fundamental components of the Xilinx FPGA tools required to enter and assemble HDL code using a schematic entry tool and program an FPGA. This includes integrating HDL into a schematic, as well as creating and updating symbols.

### Prerequisite

\* Install Xilinx 14.7. If prompted include any options to install support for Spartan 3 processors.

\* Additional Note

While trying to work on Xilinx on OS windows 8.1 and above, if you come across error "-pn.exe stopped working", please follow the below steps.

Method 1:

1) Right click on ISE Design Suite 14.7 directory and click on properties.

2) Select Tab "Shortcut" and rename the Target path

E:\14.7\ISE\_DS\settings64.bat to E:\14.7\ISE\_DS\settings32.bat

E:\14.7\ISE\_DS\ISE\bin\nt64\ise.exe to E:\14.7\ISE\_DS\ISE\bin\nt\ise.exe

3) Click Apply and Ok

Method 2:

1) Go to C:\Xilinx\14.7\ISE\_DS\ISE\lib\nt64

Rename libPortability.dll to libPortability.dll.orig

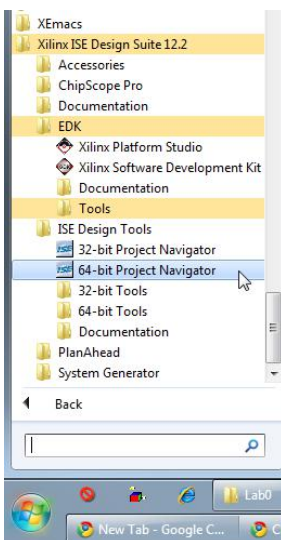
Rename libPortabilityNOSH.dll to libPortability.dll

### 2 Intro

In this lab you will program an FPGA to display a rectangle on a monitor using a VGA cable. You will first create an implementation with an error in it and view the results. You will then modify the code, update the symbol in the schematic, and wire the schematic correctly to control the color of the rectangle using switches.

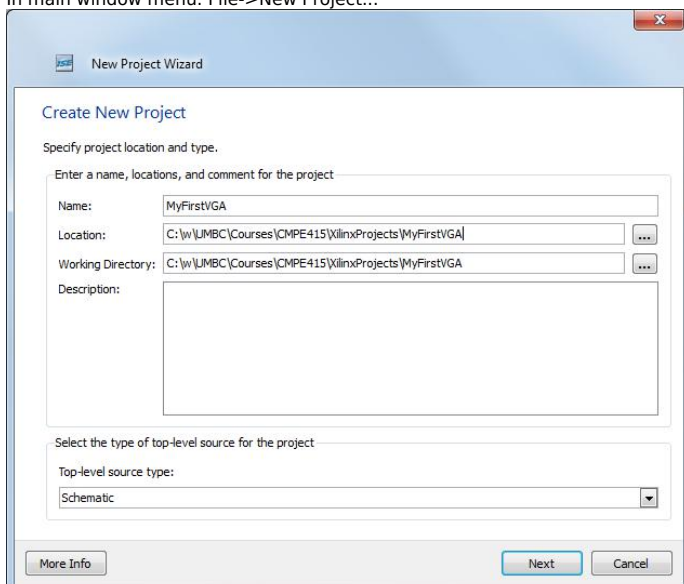
### 3 Tutorial Steps

#### 3.1 Start Xilinx Tool



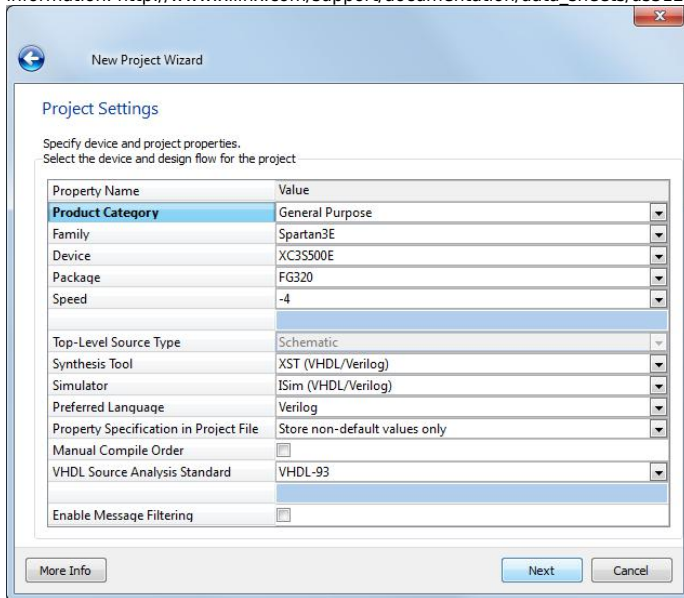
#### 3.2 Create New Project

1. In main window menu: File->New Project...

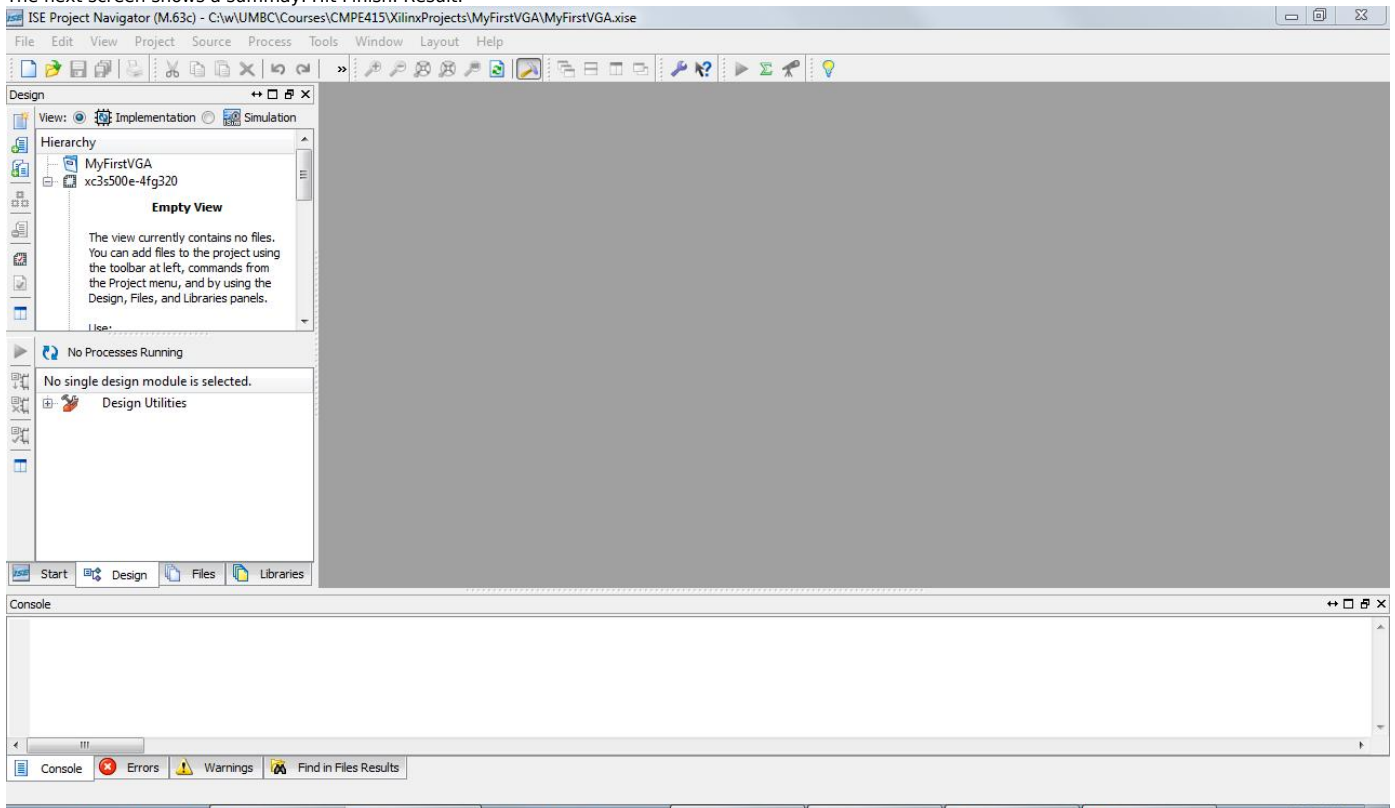


2. You'll now need to enter information about the FPGA. You can look in "Spartan-3E FPGA Family: Data Sheet" under Package Marking (page 6). To find this

information. [http://www.xilinx.com/support/documentation/data\\_sheets/ds312.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf)

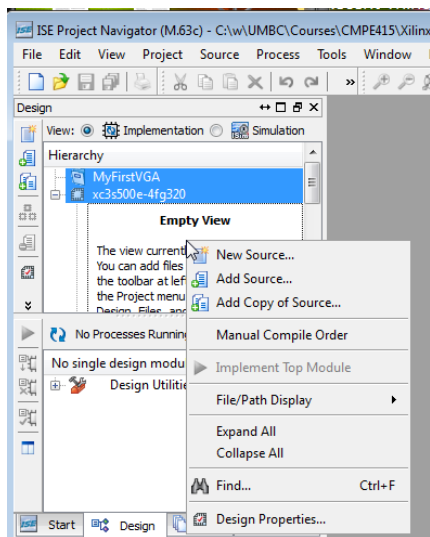


3. The next screen shows a summary. Hit Finish. Result:

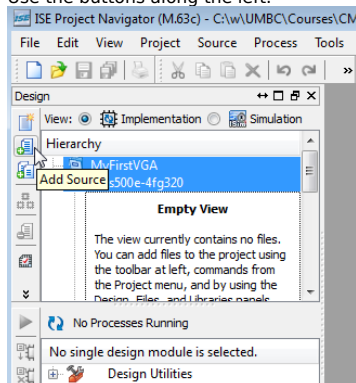


### 3.3 Downloaded HDL Module and Add to project

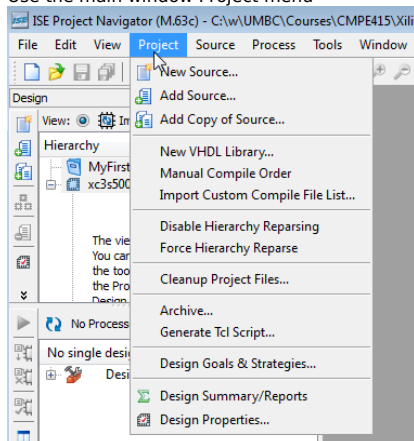
1. Download a free HDL description of implementation of a vga module to a temporary directory or to your project directory. Our other module will be implemented using Verilog, but we can integrate Verilog and VHDL modules together in the schematic if desired. Here are examples of the type of vga modules for which you are looking. Make sure to respect any restrictions the authors place on copyrighted code that you use.
  - [http://web.mit.edu/6.111/www/f2005/code/jtag2mem\\_6111/vga\\_sync.v](http://web.mit.edu/6.111/www/f2005/code/jtag2mem_6111/vga_sync.v) Verilog implementation (I suggest this one.)
  - [http://www.ece.gatech.edu/academic/courses/fpga/Xilinx/downloads/vga\\_sync.vhd](http://www.ece.gatech.edu/academic/courses/fpga/Xilinx/downloads/vga_sync.vhd) VHDL implementation (handles blanking internally)
  - [http://jjackson.eng.ua.edu/courses/ece480/assignments/vga\\_sync.vhd](http://jjackson.eng.ua.edu/courses/ece480/assignments/vga_sync.vhd) VHDL implementation with parameters to set various resolutions (also, implements a "video\_on" signal instead of a "blank" signal)
2. There are three places to access the project functions, such as adding a source. You can use any of the following (a,b,c):
  - a. Right-click in the Hierarchy plane



b. Use the buttons along the left.

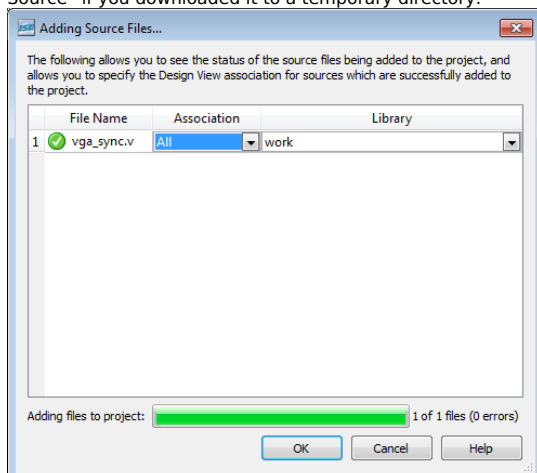


c. Use the main window Project menu

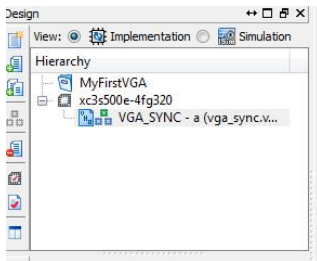


3. The three functions for sources are:

- New Source - starts wizard to create a new source file (Verilog, VHDL, Schematic, etc...), creating a shell if desired, and adds it for use in the project.
- Add Source - Allows you to point to a source file in the project directory or anywhere else and include it for use in the project
- Add Copy of Source - Creates a copy of the source file in the project directory and adds the copy for use in the project
  - Add the downloaded HDL file using option (b) "Add Source" if you initially downloaded the file to project directory and use option (c) "Add Copy of Source" if you downloaded it to a temporary directory.

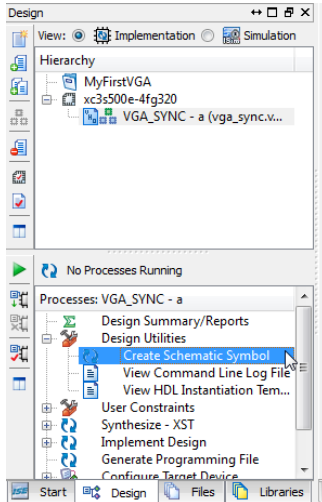


- You will now have a new source listed.

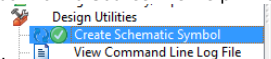


### 3.4 Creating a Symbol

1. Select the new HDL source in the Hierarchy panel. In the lower panel expand Design Utilities and double-click "Create Schematic Symbol".



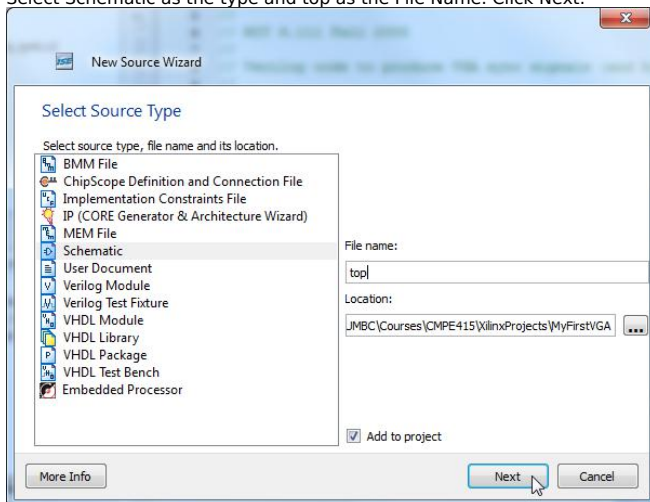
If needed, see help of: Creating a Schematic Symbol from a Source File Help->Help Topics



2. Notice the green check mark added upon success.

### 3.5 Create Top Schematic

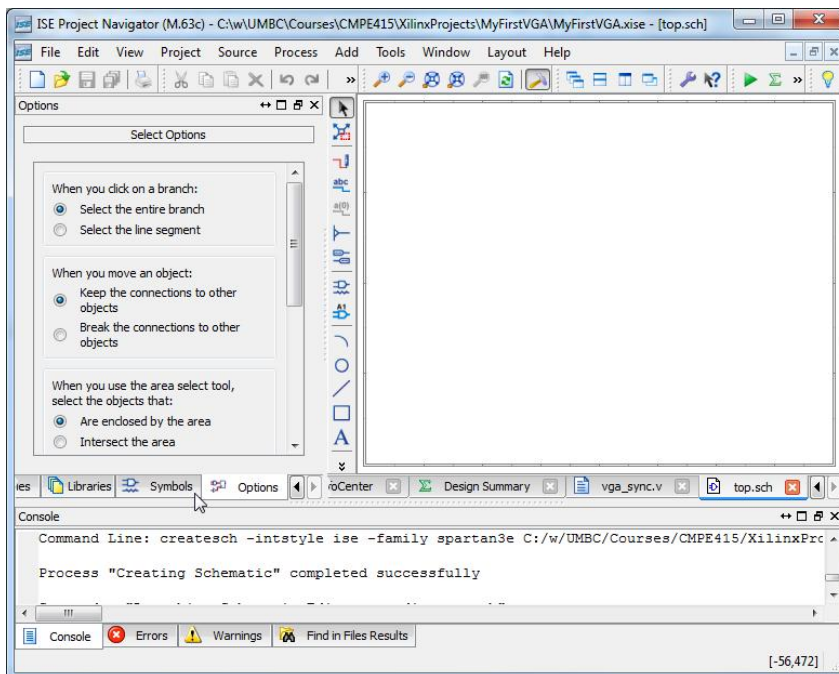
1. Using the main window Project menu, the buttons along the left, or a right-click in the Hierarchy view create a new source.
2. Project->New Source...
3. The New Source Wizard opens
4. Select Schematic as the type and top as the File Name. Click Next.



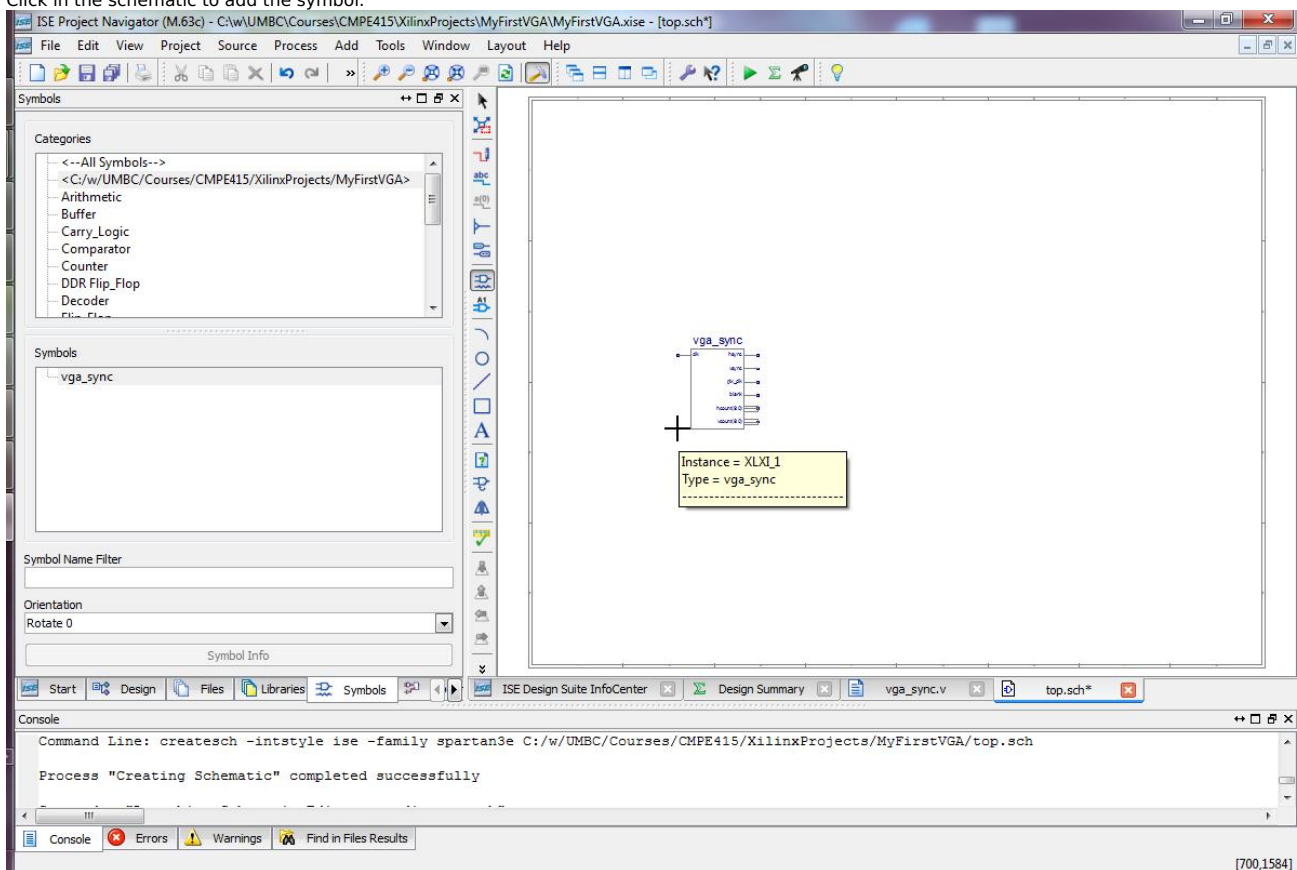
5. Click Finish in the following window.

### 3.6 Add Symbol

1. With your fresh schematic showing, select the Symbols tab as pointed out by the cursor in the picture. (use the scroll buttons just to the right if not shown)

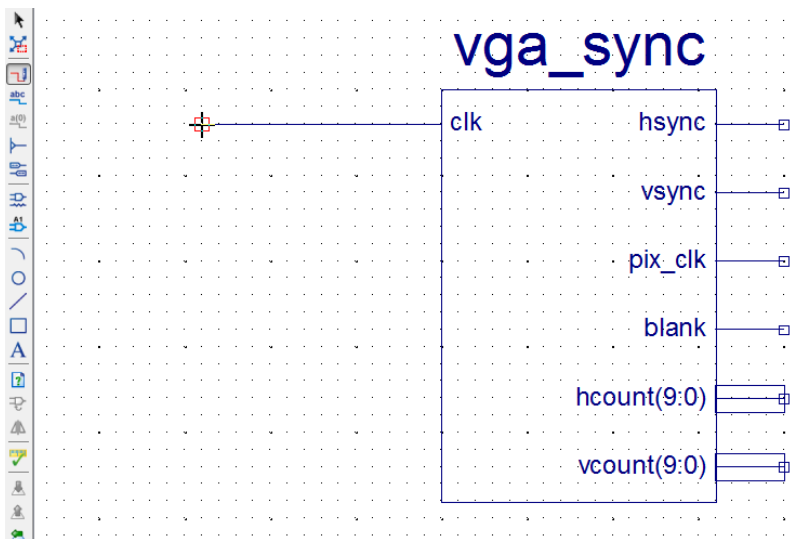


2. Under Categories, select your current project.
3. Under symbols, select your new symbol
4. Click in the schematic to add the symbol.

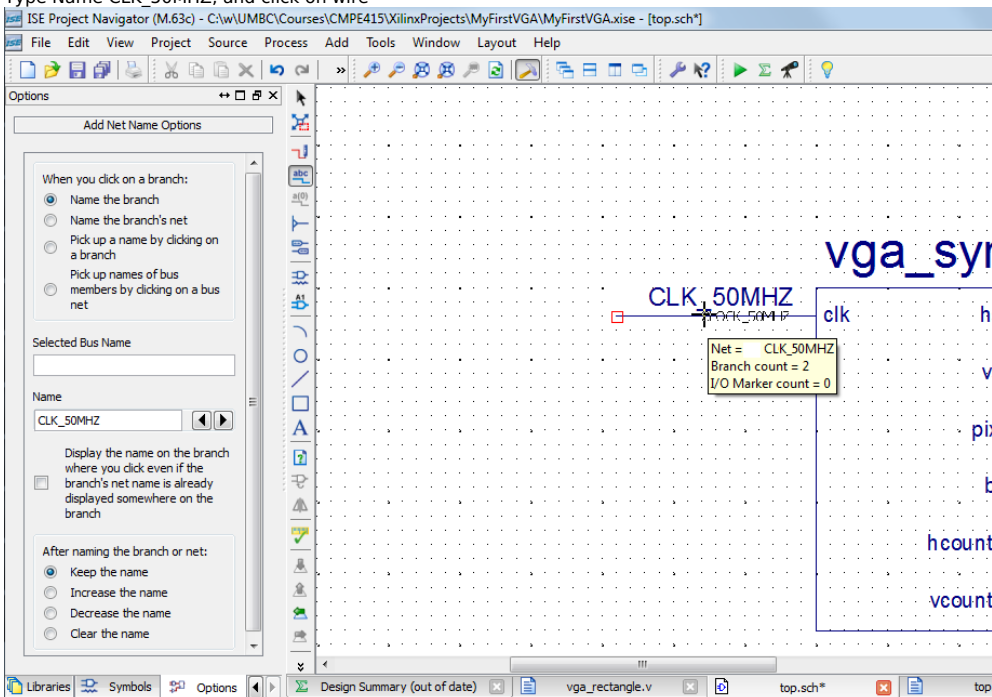


### 3.7 Add wire, name it, and and pin

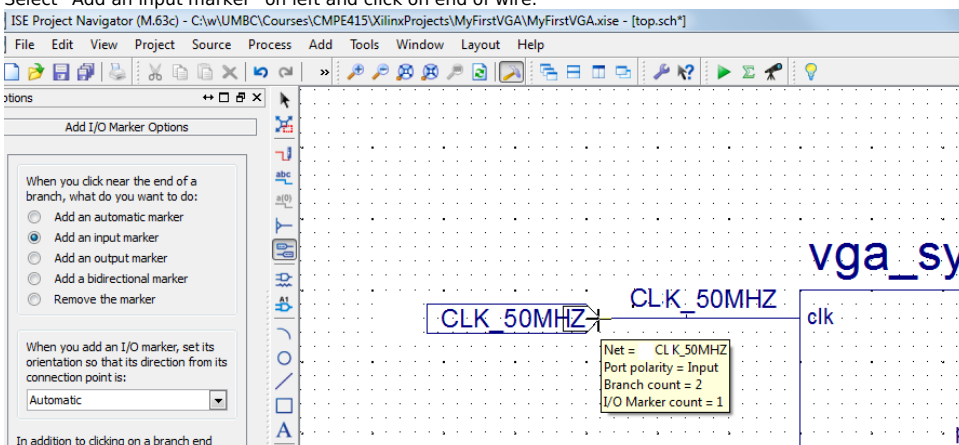
1. Using Add menu or other documented means, choose Add->Wire
2. Click twice to add a simple wire as shown.



3. Add->Net Name
4. Type Name CLK\_50MHZ, and click on wire

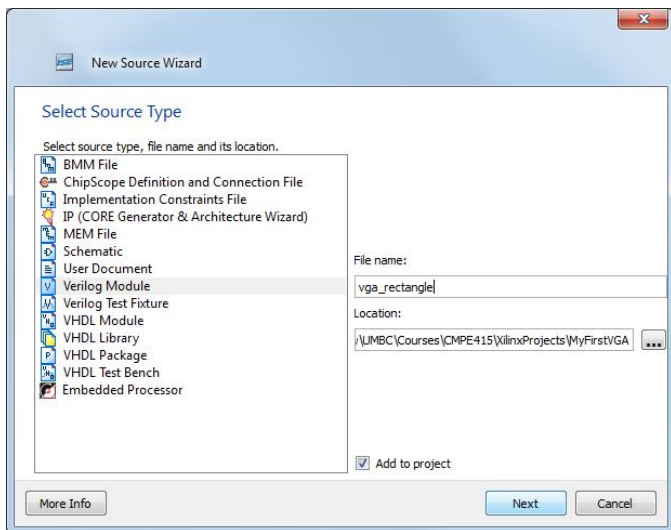


5. Next, add pin (I/O Marker): Use Menu Add->I/O Marker
6. Select "Add an input marker" on left and click on end of wire.

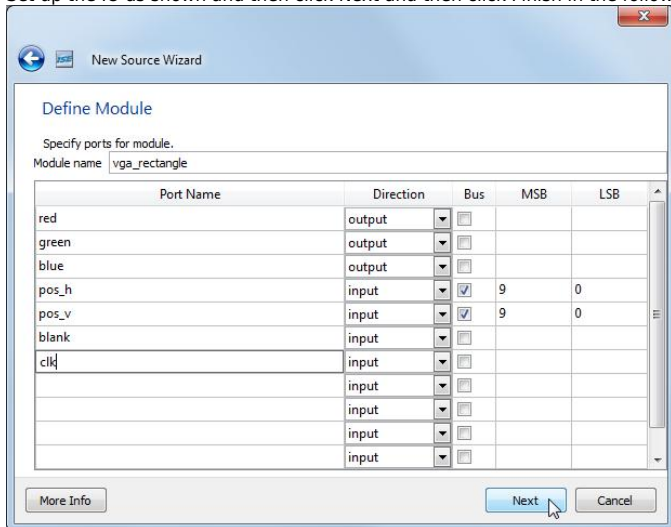


### 3.8 Add New Source for rectangle display driver using Source Wizard

1. Main window menu: Project->New Source
2. Select Verilog Module, enter File name vga\_rectangle, click Next



3. Set up the IO as shown and then click Next and then click Finish in the following window.



4. You should now have a shell created with port definitions. Set the reg, green, and blue outputs as registers. Implementing registers avoids glitching (not that it is critical here).  
change

```
output red,
output green,
output blue,
```

to

```
output reg red,
output reg green,
output reg blue,
```

5. Add the following module code which takes the coordinates as inputs and outputs the color:

```
parameter WIDTH = 20;
parameter HIEGHT = 100;
parameter X_LEFT = 320;
parameter Y_BOTTOM = 240;

//addinal intermediate logic signal wires
wire flag_on_rect; //high only when over rectangle
wire [9:0] x,y; //traditional cartesean coordinates, (left, bottom)=(0,0)

//combinatorial logic to calculate x,y coordinate system
assign x = pos_h;
assign y = 480 - pos_v;

//combinatorial logic to decide if present pixel is over a desired rectange region
assign flag_on_rect = x >= (X_LEFT) &&
    x < (X_LEFT + WIDTH) &&
    y >= (Y_BOTTOM) &&
    y < (Y_BOTTOM + HIEGHT);

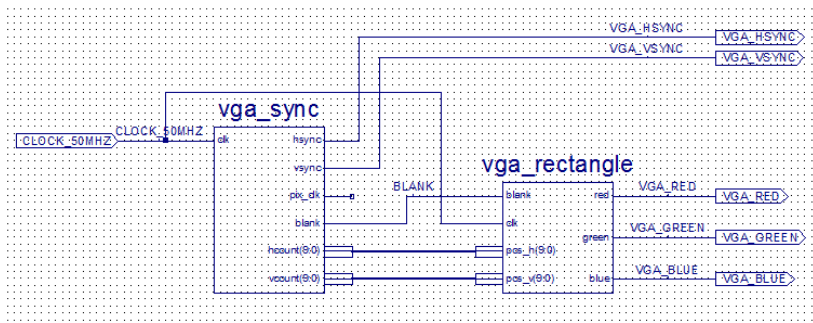
//combinatorial logic and registers (sequential logic) that load on rising clock edge
always @(posedge clk) begin
    red <= flag_on_rect & ~blank;
    green <= ~flag_on_rect & ~blank;
    blue <= flag_on_rect & ~blank;
end
```

6. Save the file and generate a symbol as before

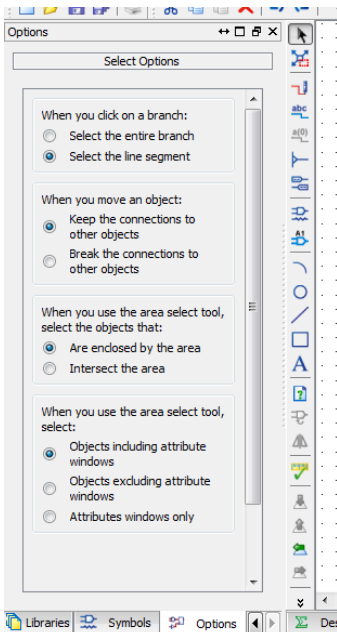
### 3.9 Complete Top Schematic

1. Complete the schematic as follows, including the output markers (be sure to make them as output markers, not input markers)



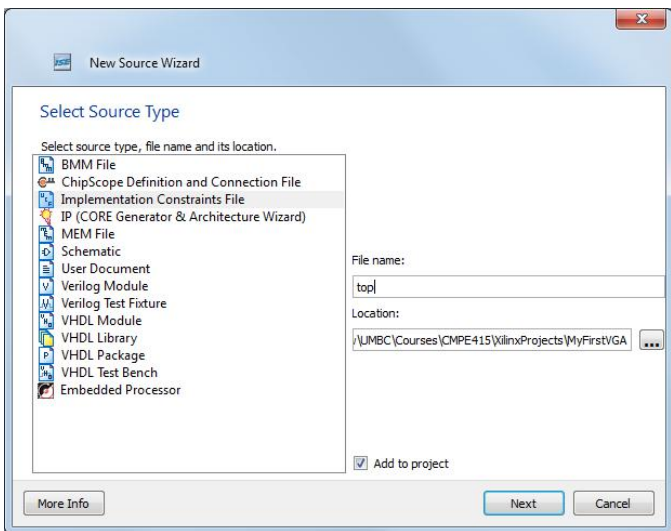


- Note the IMPORTANT OPTIONS for the Select(Arrow) tool. Thoroughly understand the first three options, reading the documentation as necessary. Understanding these options could save you a lot of time.



### 3.10 Define Pin Locations

1. We need to add a user constraint file. Use the new source wizard or create one called top: Project->New Source...



2. Click Next then Finish.

Page 57 of the development board user guide provides pin locations for the vga port:

[http://www.digilentinc.com/Data/Products/S3EBOARD/S3EStarter\\_ug230.pdf](http://www.digilentinc.com/Data/Products/S3EBOARD/S3EStarter_ug230.pdf)

Appendix B provides an Example User Constraints File (UCF) for the starter board, starting on page 159.

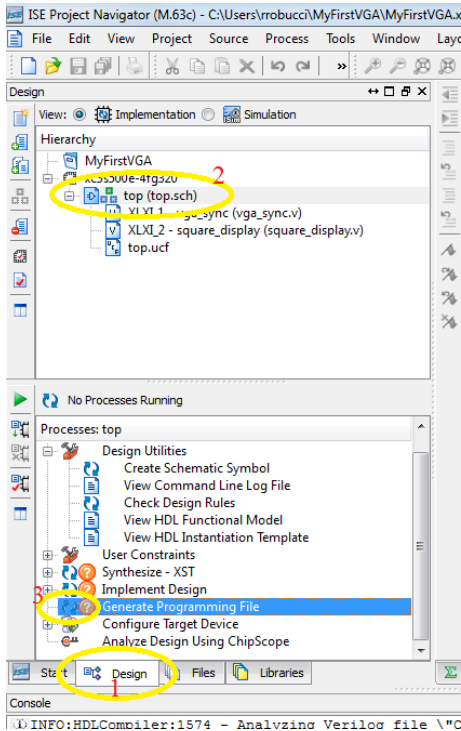
3. Copy the following lines to your UCF:

```
# === Clock inputs (CLK) ===
NET "CLK_50MHZ" LOC = "C9" | IOSTANDARD = LVCMOS33 ;
# Define clock period for 50 MHz oscillator (40%/60% duty-cycle)
NET "CLK_50MHZ" PERIOD = 20.0ns HIGH 40%;
# === VGA Port (VGA) ===
NET "VGA_BLUE" LOC = "G15" | IOSTANDARD = LVTTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_GREEN" LOC = "H15" | IOSTANDARD = LVTTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_HSYNC" LOC = "F15" | IOSTANDARD = LVTTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_RED" LOC = "H14" | IOSTANDARD = LVTTTL | DRIVE = 8 | SLEW = FAST ;
NET "VGA_VSYNC" LOC = "F14" | IOSTANDARD = LVTTTL | DRIVE = 8 | SLEW = FAST ;
```

### 3.11 Synthesize, Implement, and Generate Programming File



1. On the left, bring up the design view by clicking the design tab
2. Then in the Hierarchy plan, select the top module in the design, top.sch
3. Finally, DOUBLE-CLICK Generate Programming File in the plane below.
  - “Synthesize” and “Implement Design” are run automatically as needed.
    - Synthesize maps your design to a circuit based on FPGA build blocks.
    - Implement Design maps the circuit to the FPGA including place and route.



### 3.12 Program FPGA

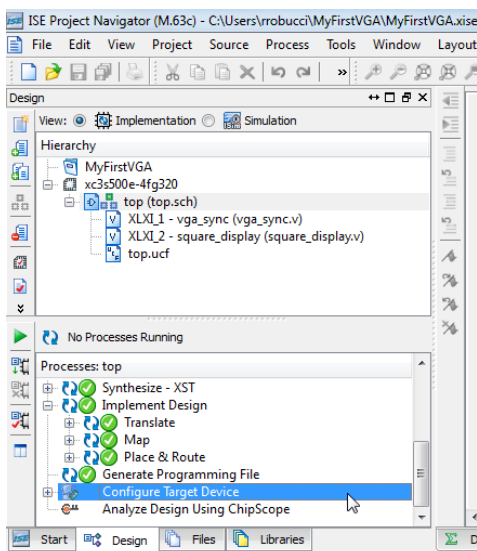
We will use the JTAG interface to program the FPGA. While normally separate from the FPGA board, the USB-to-JTAG interface is conveniently built into our starter board.

1. Set Jumper J30 to JTAG Setting  
M0=open  
M1=short  
M2=open

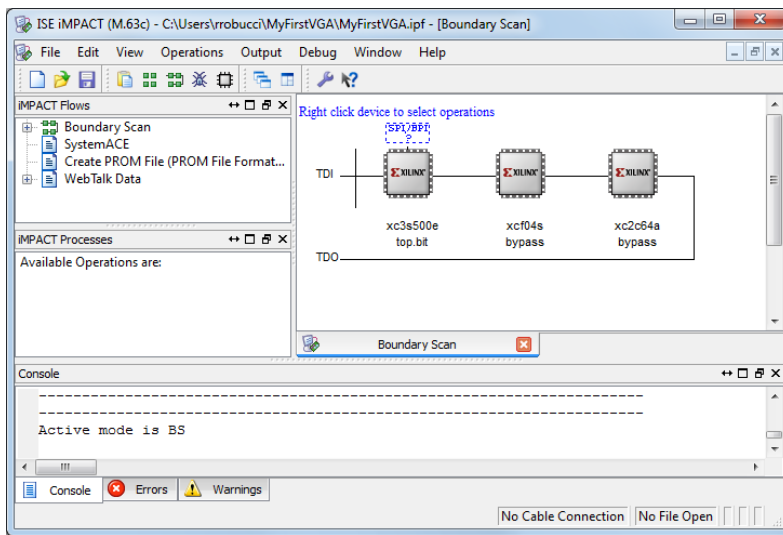
DO NOT DISCARD JUMPERS, JUST PLACE THEM SO THEY ARE ATTACHED TO ONE PIN TO CREATE OPEN:



2. Connect USB Cable from board to computer
3. Plug in the board's power adaptor to the board's power connector and a 120 V outlet. Turn on the board using the power switch near the power connector.
4. Double-Click “Configure Target Device” under “Generate Programming File”

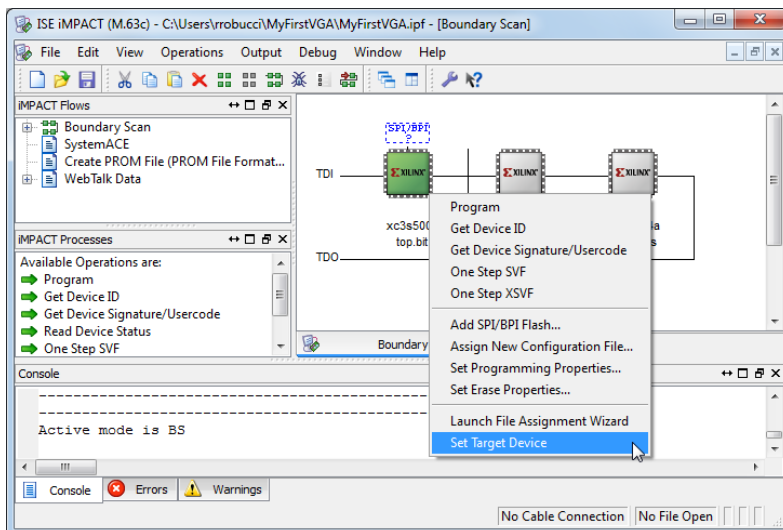


Result:

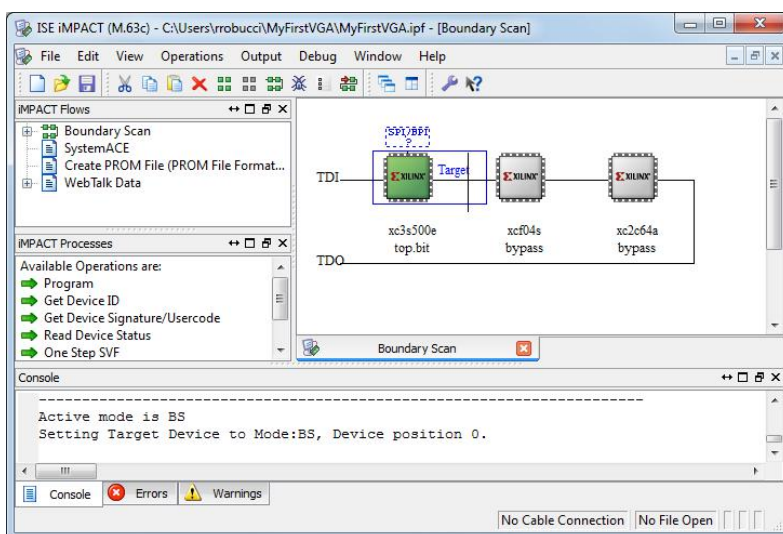


**IF YOU DONT HAVE THIS RESULT SHOWING THE DEVICE CHAING THE FIRST TIME YOU RUN THE TOOL, USE INTRUCTIONS IN SECTION 5 TO MANUALLY START iMPACT, PROGRAM YOUR DEVICE, AND SAVE YOUR CHAIN CONFIGURATION (.ipf file)**

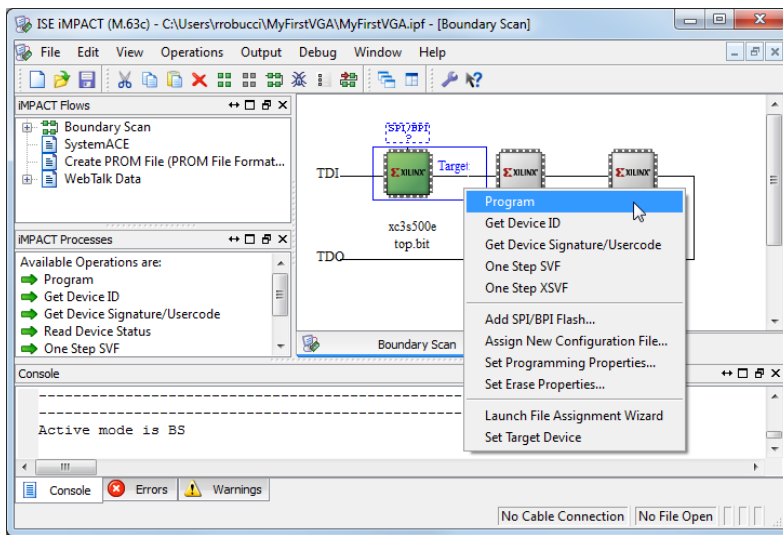
5. Right-click the xc3s500e device and select "Set Target Device"



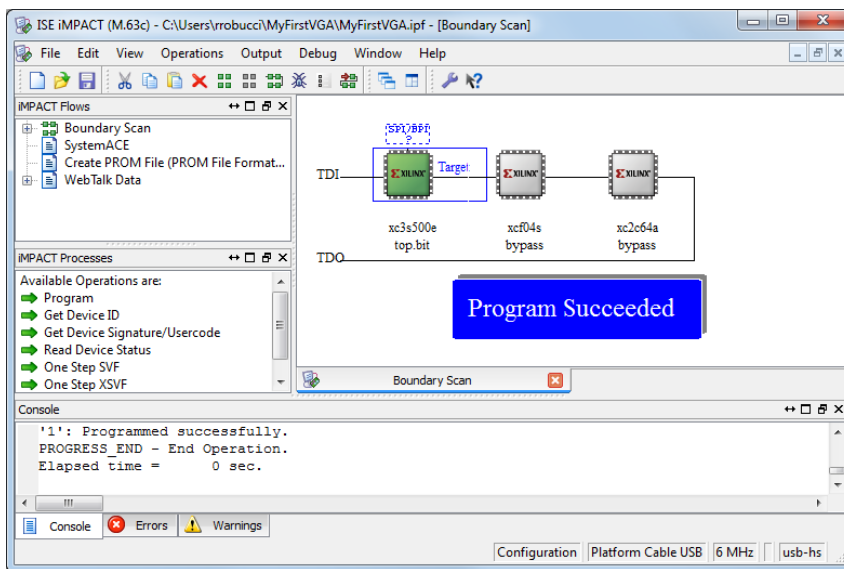
Result:



6. In iMPACT, goto File->Save Project so that you aren't prompted to do this again when starting iMPACT.



Result:



### 3.13 Connect to Monitor

Connect a VGA cable to the starter board and a monitor. You should see a magenta/purple rectangle on a blue background.

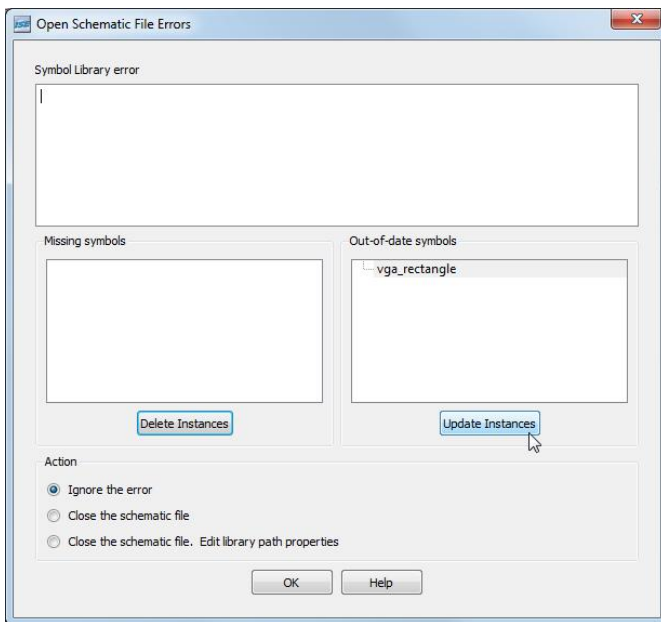
## 4 Your Design Assignment:

Modify the design to have the ability to change the color of the rectangle based on switch positions.

- The background should be black
- The color of the rectangle should be determined by turning on one of three switches, otherwise the rectangle is black.
- The three switches should correspond to yellow, cyan, and magenta. Having more than one switch on at a time is a “don’t care” condition.

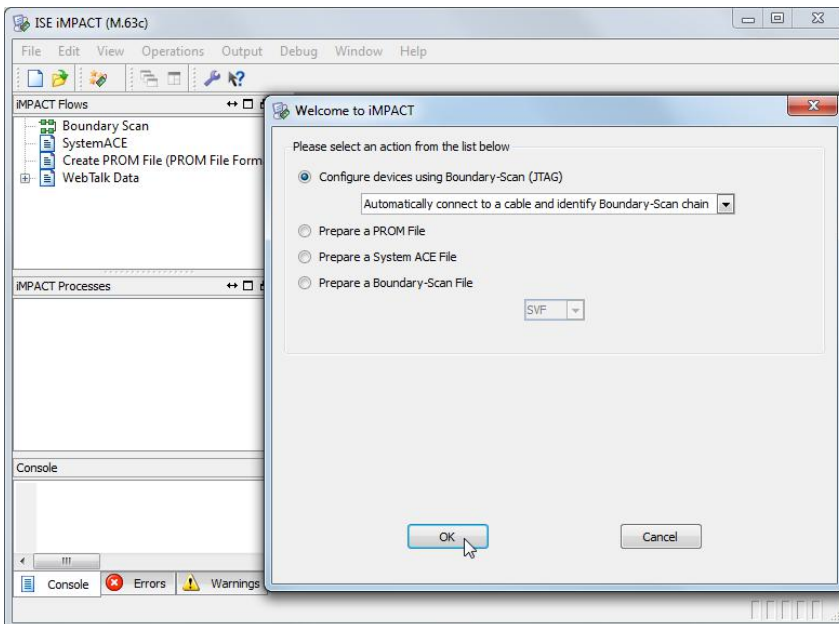
The board’s user manual provides a color chart in the VGA port section. It also provides and all the pin location information needed to add the appropriate information to your *user constraints file* for the switched.

NOTE: When you update the port definitions of a module, you need to manually regenerate the symbol by running “Create Schematic Symbol” again. When you reopen a schematic with that symbol, it will present you with the option to update them. Just click “Update Instances”.

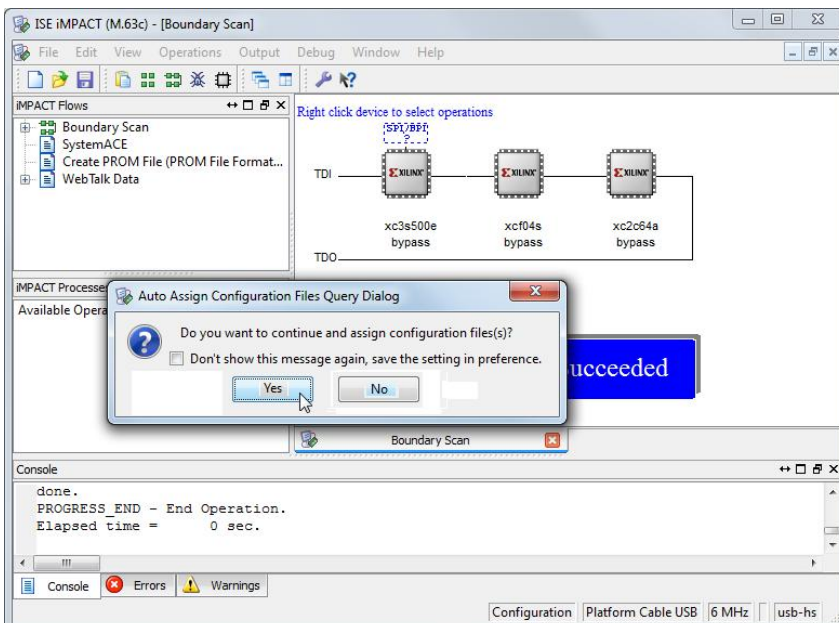


## 5 Running iMPACT Manually

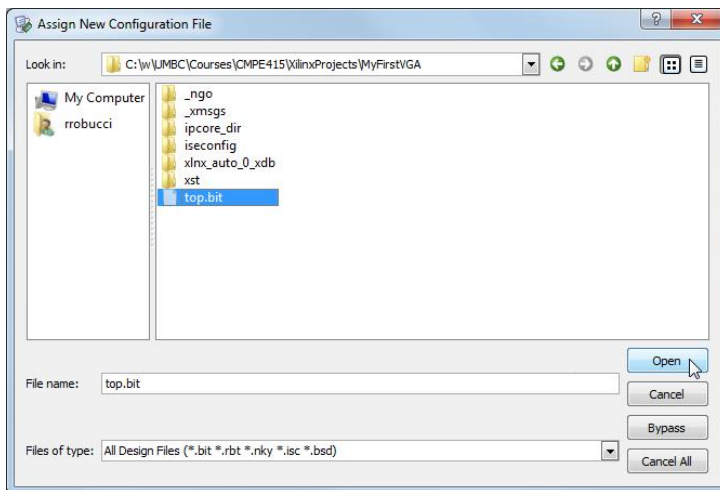
1. In ISE main menu: Tools->iMPACT. Reply Yes/OK to any prompts.
2. In iMPACT menu, Edit->Launch Wizard...



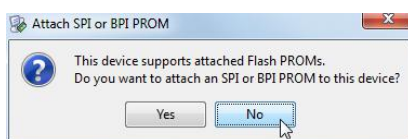
3. Click OK
4. Click YES in following window.



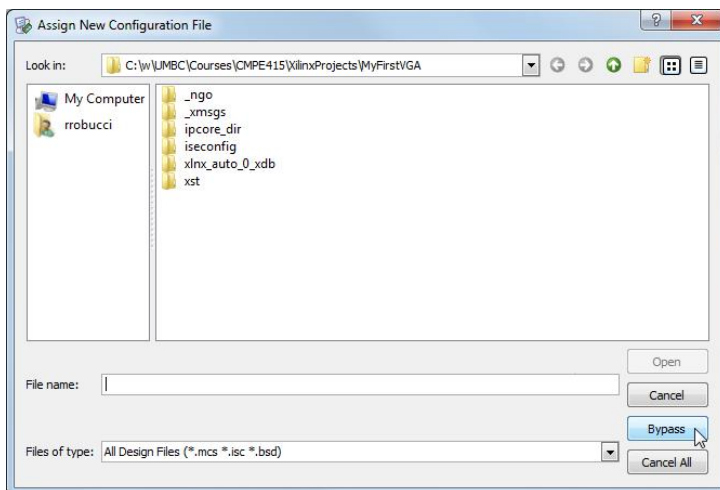
5. Select your bit file:



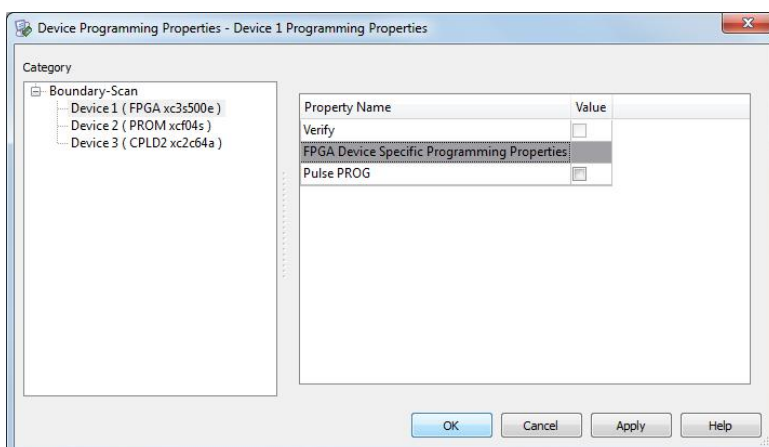
6. Select no (we will not load anything onto the FPGA ROM)



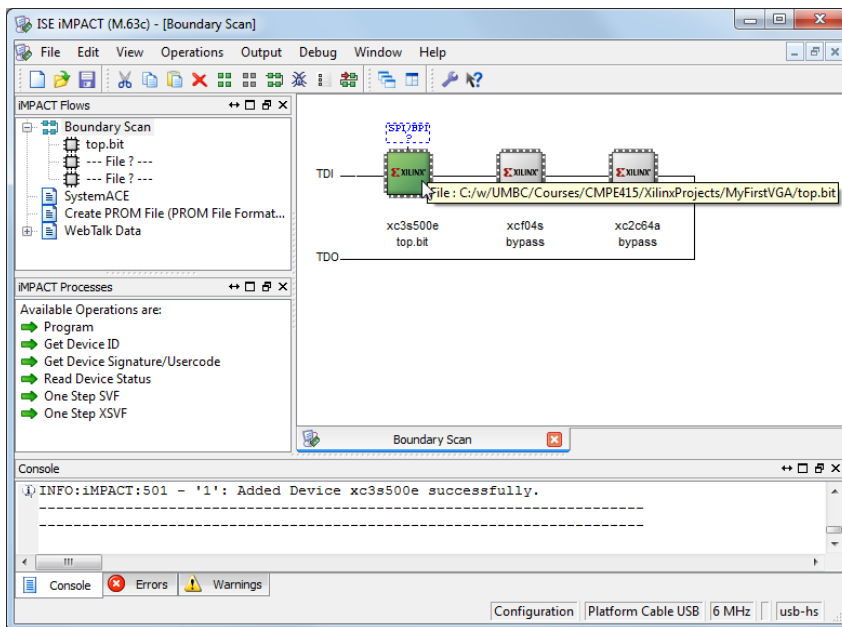
7. For the following two devices, select bypass:



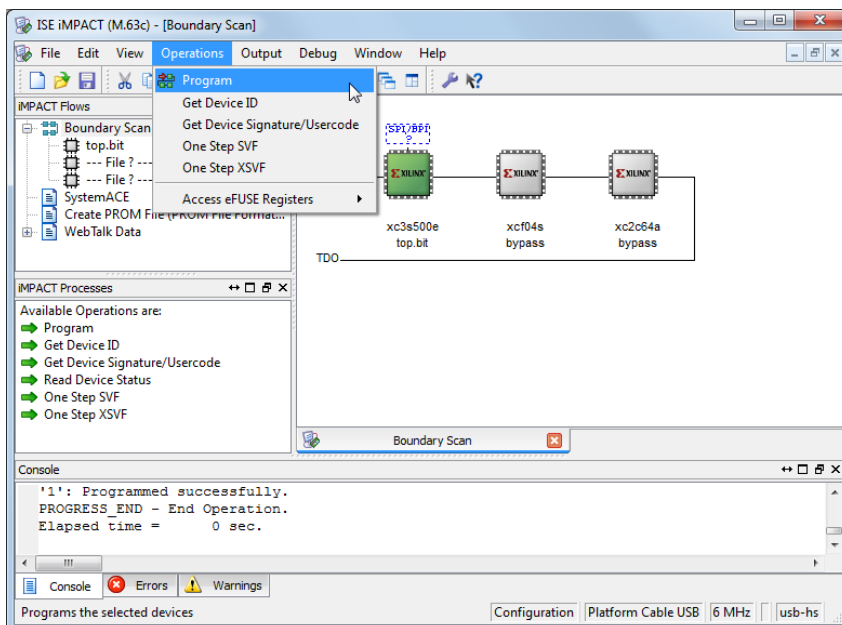
8. Just HIT OK HERE:



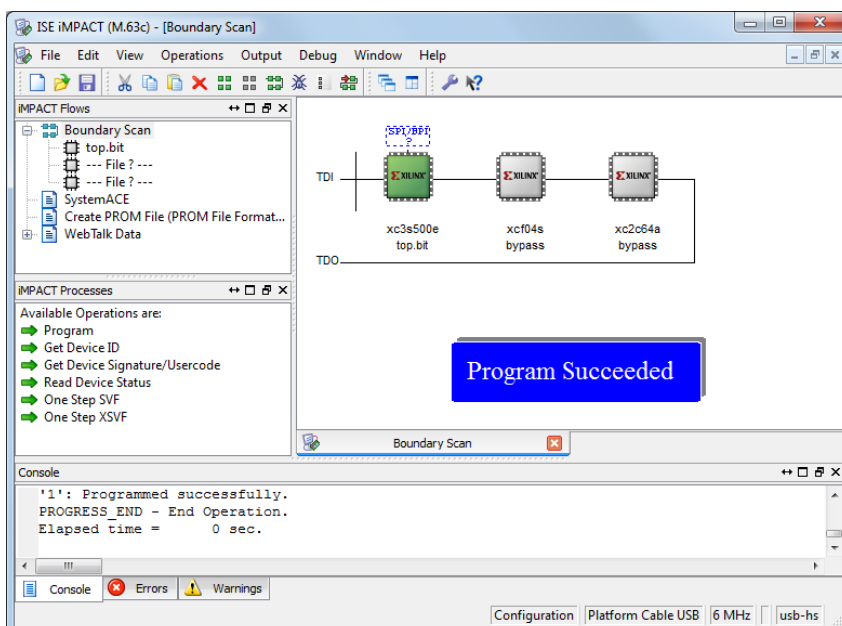
9. Select FPGA device:



10. Program device:



Result:



11. Use File ->Save Project to save chain configuration.

***When you update your programming file (.bit) you may have to reload it by right-clicking the first device in the chain, the FPGA, and using “Assign New Configuration File.”***