CSE260 Assignment - 4

Deadline - 8th September, 11:59 PM

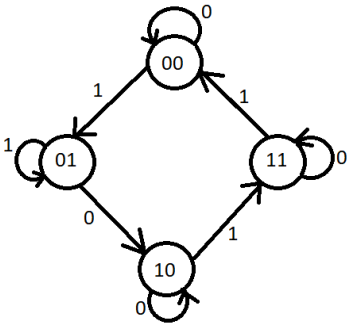
Marks: 10

Assignment must be handwritten. Scan and upload PDF in the given google form

Graded Problems

Question 1

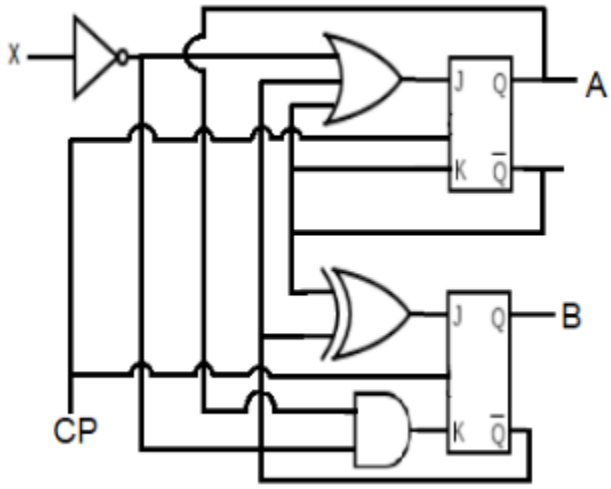
Given the state diagram as follows, get the sequential circuit using SR flipflop. Show all necessary tables.



Ungraded Problems (Only for practice, Not required to submit with assignment):

Question 1

Draw the state diagram for the given circuit.



Question 2

Implement the following counter using T flip flop

CSE110 -> CSE111 -> CSE220 -> CSE221 -> CSE331 -> CSE221 -> CSE321 -> CSE110

Question 3

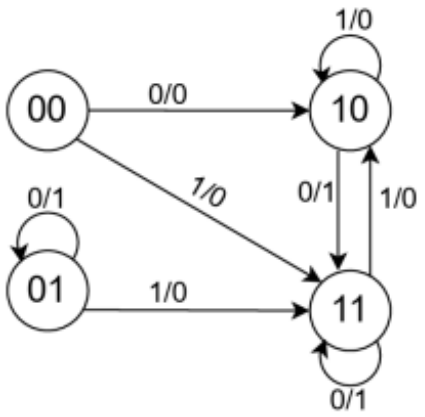
Implement 3 bits up/down counter using D flip flop

Question 4

Given the state diagram as follows, get the sequential circuit using

i. SR flipflop.

ii. JK flipflop.



Question 5

Implement the following counter using D flip flop

A -> B -> C -> B -> D -> B -> A

Question 6

What is the total capacity of a 2^{32} x 16 memory?

Question 7

Draw the block diagram for a 1024x16 RAM.

Question 8

3->4->6->10->12->13->15->3

a. Implement the given counter using JK flip-flop.

b. Implement the given counter using T flip-flop.

NB: For states not given in question, please move to the initial state as per question.**Question 9**

Design a 3-bit Parallel Adder using only 8:1 Mux(s)

Question 10

Draw and complete the timing diagram for the following circuit, where all the flip-flops are positive-edge-triggered. Clock Pulse(CLK) and TA waveforms are given