Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment # 7: Function Implementation Using a 4x1 MUX.

Objective:

- To get familiarized with ***74153[MUX];***
- To gain experience working with practical circuits.

Required Components:

1. IC 74153
2. IC 7408
3. IC 7432
4. IC 7404

Function:

F(A, B, C, D) = Σ(1, 2, 4, 5, 6, 9, 12, 13)

Procedure:

We will implement a given logic function using a 4×1 multiplexer. The experiment is divided into two checkpoints:

1. **Checkpoint 1** – Test a 4×1 MUX to ensure it works correctly.
2. **Checkpoint 2** – Implement the given logic function using the MUX.

Checkpoint 1: Testing a 4x1 mux

We will use the 74153 IC, which contains two 4×1 MUXes in one package. For this experiment, we will use MUX-1 (the left one).

MUX-1 Pin Configuration:

Inputs:	Selectors:	Output:	Power:	Enable (Strobe) Pins:
Pin 3 → I3 Pin 4 → I2 Pin 5 → I1 Pin 6 → I0	Pin 2 → S1 Pin 14 → S0	Pin 7 → Y	Pin 16 → +5v Pin 8 → GND	Pin 1 (MUX-1 Enable) → GND Pin 15 (MUX-2 Enable) → GND

Setup:

- Connect Pin 16 to +5V and Pin 8 to GND.
- Ground both Enable pins → Pin 1 and 15.
- Connect four input switches to the **MUX input pins** → Pin 6, 5, 4, 3.
- Connect another two switches to the **selector pins** → Pin 2, 14.
- Connect Output (Pin 7) to an LED.

Testing the MUX:

MUX input lines				Selectors		Output
I3	I2	I1	I0	S1	S0	Y
0	0	0	1	0	0	1
1	1	1	0	0	0	0
0	0	1	0	0	1	1
1	1	0	1	0	1	0
0	1	0	0	1	0	1
1	0	1	1	1	0	0
1	0	0	0	1	1	1
0	1	1	1	1	1	0

Check if the MUX output matches the Expected Output in the table. If there is any mismatch, re-check wiring and ensure enable pins are grounded.
Checkpoint 1 - Completed.

Checkpoint 2: Implementing the function

Find the mux input logics:

- The given function has four input variables: A, B, C, D.
- We are using a 4×1 MUX which requires two selector pins.
- We will use:
  C → S1 (Selector 1)
  D → S0 (Selector 0)
- This means the MUX input lines (I0, I1, I2, I3) will be defined in terms of only A and B.

Now complete the table for variable A and B.

	I0	I1	I2	I3
A’B’	0	1	2	3
A’B	4	5	6	7
AB’	8	9	10	11
AB	12	13	14	15

Find the equations:

I0 = _____ I2 = _____
I1 = _____ I3 = _____

Setup:
Once you have derived the Boolean equations for all four MUX input lines (I0–I3):

- Take two new inputs from two switches — these will be A and B.
- Using A and B, build the logic circuits for each equation you found for I0, I1, I2, and I3.
- Connect the outputs of these logic circuits to their corresponding MUX input pins.

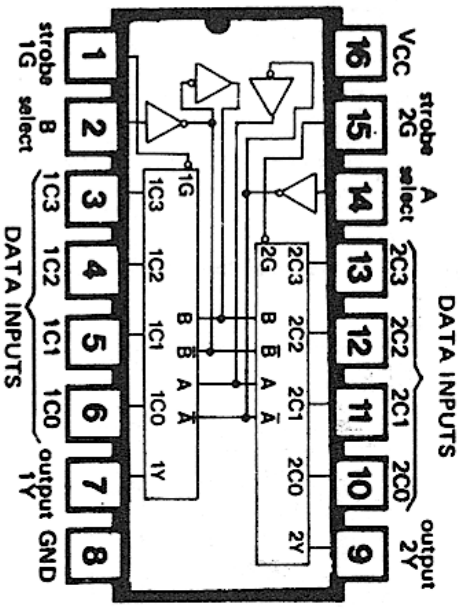
Testing the circuit:

	A	B	C(S1)	D(S0)	I3	I2	I1	I0	F
0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0	1
2	0	0	1	0	0	1	0	0	1
3	0	0	1	1	0	0	0	0	0
4	0	1	0	0	0	0	0	1	1
5	0	1	0	1	0	0	1	0	1
6	0	1	1	0	0	1	0	0	1
7	0	1	1	1	0	0	0	0	0
8	1	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	1	0	1
10	1	0	1	0	0	0	0	0	0
11	1	0	1	1	0	0	0	0	0
12	1	1	0	0	0	0	0	1	1
13	1	1	0	1	0	0	1	0	1
14	1	1	1	0	0	0	0	0	0
15	1	1	1	1	0	0	0	0	0

Check if the MUX output matches the Expected Output in the table. If there is any mismatch, re-check wiring and ensure enable pins are grounded.
Checkpoint 2 - Completed.

Explanation:
Lets take an input = 12. So, ABCD = 1100
CD is basically the selector bits S1, S0. So, the input line I0 will be selected.
So, we will have to activate this line by giving 1 as input in this line. Finally, check the Logic equation for the I0 input. Put the value of A and B in that equation. If it evaluates to 0, the MUX output will be 0 else 1.

Pin Diagrams of 74153[MUX] IC:



IC Description:

The IC has two identical 4:1 multiplexers:

- MUX 1: Uses inputs 1C0 to 1C3, output 1Y
- MUX 2: Uses inputs 2C0 to 2C3, output 2Y

Selection Lines: Both MUXs share the same select lines: A and B

Strobe Pins (1G and 2G): Both of these pins are active-low enable pins; So, keep both 1G and 2G pins connected with 0V or "GND"

Report:

Your report must have the following segments:

1. Name of the Experiment.
2. Objective.
3. Required Components.
4. Experimental Setup - Draw the circuit diagrams for both functions.
5. Results - Draw the truth tables of both functions:
6. Discussions - Answer the following questions:
    a) Design a full adder using 4:1 Mux(s).
    b) Design a 2-bit Parallel adder using exactly 4 8:1 Mux(s)
    c) Design a 2-bit Parallel adder cum subtractor using exactly 4 8:1 Mux(s) and if you need any logic gates build that also using Mux. (You can choose any size mux here.)