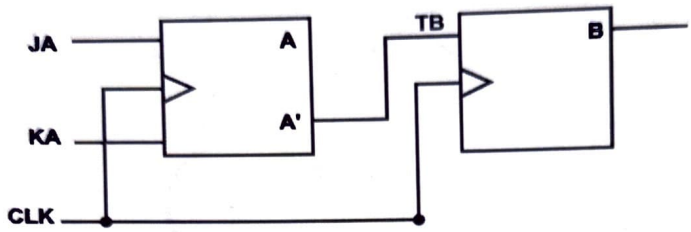
BRAC UNIVERSITY
Inspiring Excellence

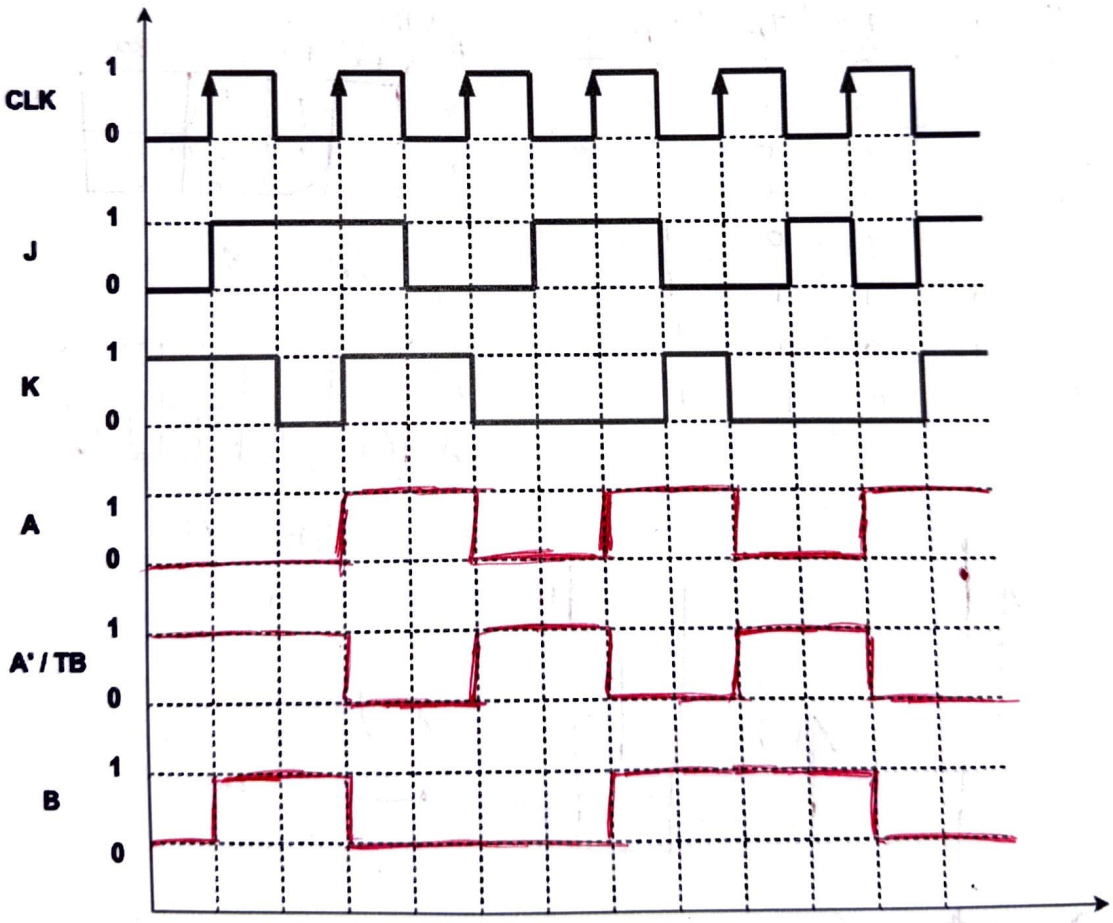
CSE260: Digital Logic Design
Summer 2025
Quiz - 04
Duration: 30 minutes

A

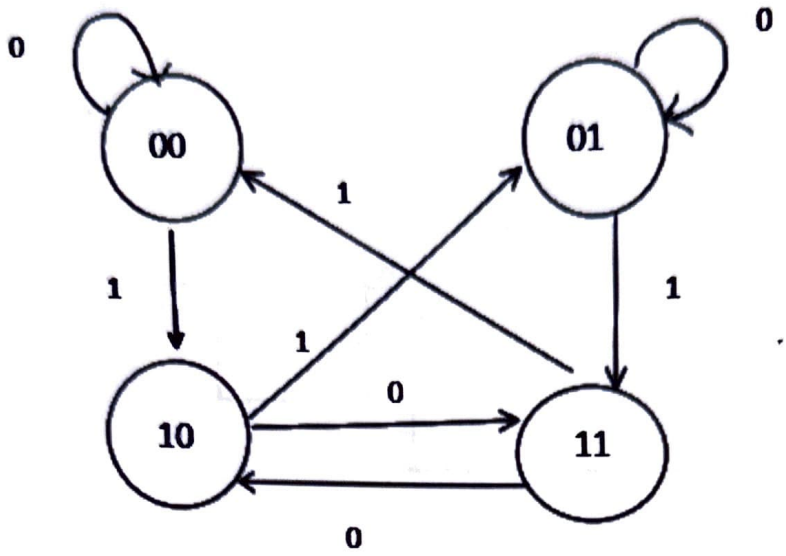
Name: Solution.	ID:	Section:

1. Complete the timing diagram for the following Flip-flop circuit diagram. The FF is positive-edge triggered.

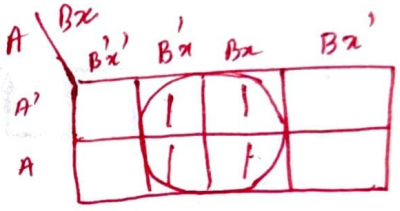




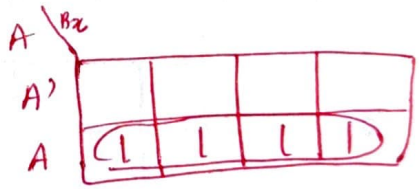
2. Convert the State diagram to a Circuit diagram using T flip-flops



A	B	X	A+	B+	TA	TB
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	1	1	1	1	0
1	0	0	1	1	0	1
1	0	1	0	1	1	1
1	1	0	1	0	0	1
1	1	1	0	0	1	1



$TA = X$



$TB = A$