
The Phase-locked Loop (PLL)

3.1. Introduction

The phase-locked loop (PLL) is a loop device (Figure 3.1) which ensures that the frequency or the phase of a voltage-controlled oscillator (VCO) is locked to the frequency of an external signal (reference signal). The VCO is an integral part of the phase-locked loop.

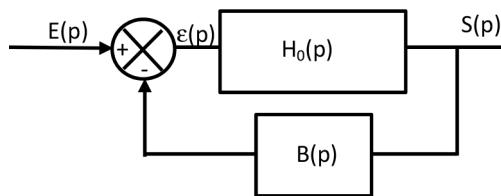


Figure 3.1. Structure of a looped system and servo control

Such a closed system consists of a direct chain whose transfer function is defined by $H_0(p)$, and the feedback loop has a transfer function denoted by $B(p)$. The output quantity $S(p)$ is locked to the input quantity $E(p)$. In this context, a global transfer function of the system can also be defined:

Open-loop transfer function:

$$H_{BO} = H_0(p) \cdot B(p)$$

p : Laplace variable.

When processing sinusoidal signals, $p = j\omega$, ω is the pulsation of the signal under consideration.

Closed-loop transfer function:

$$H(p) = \frac{H_0(p).B(p)}{1+H_0(p).B(p)}$$

3.2. Relationship between frequency and instantaneous phase

In a phase-locked loop, control is achieved at the frequency or phase level. It is important to highlight the link between these two quantities. For greater clarity, it is assumed that the signals to be locked are sinusoidal and respectively denoted by v_1 and v_2 (Figure 3.2). For the present case, they have the same frequency.

$$v_1 = V_{M1} \cdot \sin(\varphi_1)$$

$$v_2 = V_{M2} \cdot \sin(\varphi_2)$$

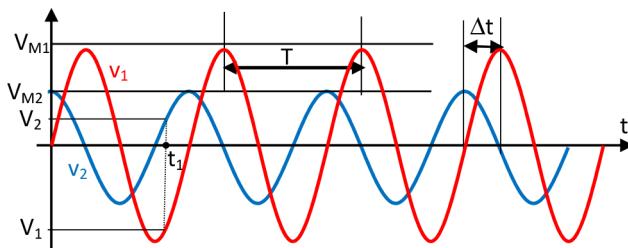


Figure 3.2. Phase shift between two signals. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

At time $t = t_1$, we have:

$$\varphi_1(t_1) = \text{Arcsin}\left(\frac{V_1}{V_{M1}}\right)$$

$$\varphi_2(t_1) = \text{Arcsin}\left(\frac{V_2}{V_{M2}}\right)$$

The phase shift existing between the two signals v_1 and v_2 is defined by $\Delta\varphi$:

$$\Delta\varphi \text{ (radians)} = \varphi_1 - \varphi_2 = 2\pi \frac{\Delta t}{T}$$

When considering, for example, the signal $v_1(t)$, the latter can be written as follows:

$$v_1(t) = V_{M1} \cdot \sin(\varphi_1(t)) = V_{M1} \cdot \sin(\omega_1 t + \theta_1).$$

The frequency $f_1 = (\omega_1 / 2\pi)$ of signal $v_1(t)$ is constant. It has a phase at the origin that is non-zero, and which is equal to θ_1 .

The parameter $\varphi_1(t)$ represents the instantaneous phase of $v_1(t)$. The vector representation of voltage $v_1(t)$ is shown in Figure 3.3. It provides a good signification of both the instantaneous phase and the pulse or angular velocity $\omega_1(t)$.

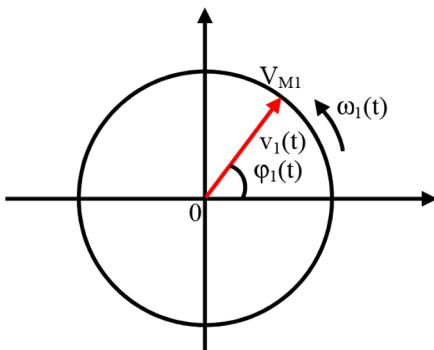


Figure 3.3. Vector representation of voltage v_1

The instantaneous pulse or angular velocity $\omega_1(t)$ of voltage $v_1(t)$ that expresses the rotation velocity (or rate of change) of the instantaneous phase can be written as follows:

$$\omega_1(t) = \frac{d\varphi_1(t)}{dt}$$

The instantaneous frequency of a signal is linked to the instantaneous pulse by:

$$f_1(t) = \frac{\omega_1(t)}{2\pi}$$

In the case of a sinusoidal signal that has a fixed frequency $f_1 = \omega_1 / 2\pi$, the phase variation over time is linear (Figure 3.4).

The slope of the curve represents the pulsation or instantaneous rotation velocity.

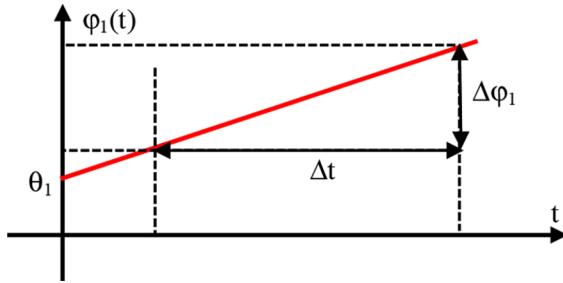


Figure 3.4. Variation of the instantaneous phase in time for a sinusoidal signal

When the phase difference between two sinusoidal signals $v_1(t)$ and $v_2(t)$ is constant, (very frequent case in phase-locked loops (PLL)) it can be stated that the two signals have the same frequency.

In effect, we have:

$$v_1 = V_{M1} \cdot \sin(\varphi_1) = V_{M1} \cdot \sin(\omega_1 t + \theta_1).$$

$$v_2 = V_{M2} \cdot \sin(\varphi_2) = V_{M2} \cdot \sin(\omega_2 t + \theta_2).$$

Quantities θ_1 and θ_2 are considered to be constants (phase at the origin). It can be seen that when we have:

$$\varphi_1(t) - \varphi_2(t) = \text{constant},$$

we get:

$$\frac{d[\varphi_1(t) - \varphi_2(t)]}{dt} = 0 = \omega_1 - \omega_2$$

$$f_1 = f_2$$

3.3. Origin of the phase-locked loop

The development of the phase-locked loop is related to signal transmission and, more specifically, to amplitude modulation. It should be recalled that in order to transmit a signal over long distances, the modulation process of the signal to be transported has to be ensured by a carrier signal.

3.3.1. Amplitude modulation principle

In the case of amplitude modulation, a high-frequency carrier is employed. The useful signal (which contains the information to be transported) is carried by the amplitude of the carrier, as indicated in Figure 3.5.

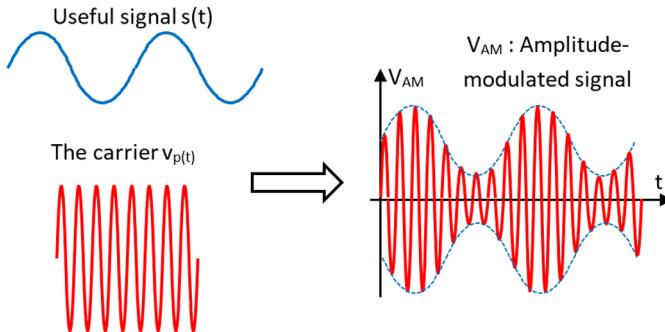


Figure 3.5. Amplitude-modulated signal

The carrier is a high-frequency sinusoidal signal defined by:

$$v_p(t) = E \cos(2\pi F_p t);$$

where F_p is the frequency of the carrier.

The useful signal $s(t)$ can have a form that will depend on the information to be transmitted. In this case, a sinusoidal type was chosen in order to facilitate the understanding of phenomena. Therefore, the carrier envelope will follow the shape of the sinusoidal signal that represents the useful signal to be transmitted.

The expression of the amplitude-modulated signal can be defined in a general framework by the expression:

$$V_{AM} = (E + s(t)) \cdot \cos(2\pi F_p t) = E(1 + k \cdot s(t)) \cdot \cos(2\pi F_p t)$$

with $k = (1/E)$

When the useful signal to be transmitted is of sinusoidal shape, it can be written as:

$$S(t) = S \cos(2\pi f t)$$

where f is the frequency of the signal to be transmitted.

The amplitude-modulated signal will have as expression:

$$V_{AM} = (E + S \cdot \cos(2\pi ft)) \cdot \cos(2\pi F_p t)$$

$$V_{AM} = E \left(1 + \frac{S}{E} \right) \cos(2\pi ft) \cos(2\pi F_p t)$$

The factor $m = (S/E)$ is called the modulation index. This factor must be comprised between 0 and 1. Otherwise, we have overmodulation.

3.3.2. Amplitude demodulation principle

After modulation, the signal is transmitted through the atmosphere by means of a transmitting antenna. At reception, it is imperative to recover the useful signal. To this end, the process of demodulation has to be carried out. The usual circuit that is used for this demodulation process makes use of a diode and low-pass filtering. Its schematic diagram is presented in Figure 3.6.

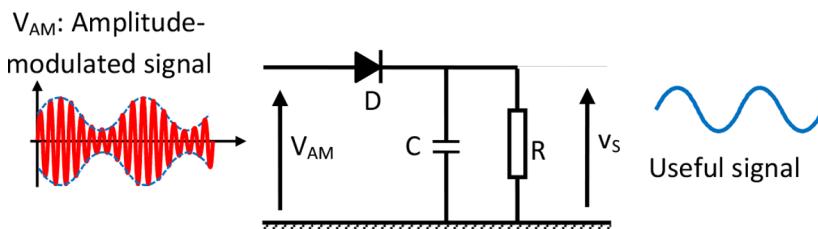


Figure 3.6. Demodulation circuit

Normally, when the modulated wave reaches the input, the low-frequency useful signal carried by the carrier wave has to be recovered on output. It will be seen that a few problems will need to be solved in order to be able to exactly obtain the initial useful modulating signal.

The shape of the output signal will especially depend on the time constant of the output RC circuit. It is naturally assumed that the modulated signal was significantly amplified to overlook the effect of the potential barrier of the diode.

Consider the case where the time constant RC is large compared to the period of the low-frequency modulating signal: $RC > T = (1/f)$.

During the positive half-wave, the capacitor will almost instantaneously charge through the dynamic resistance R_d of the diode (R_d is very small and can be considered to be zero in the ideal case).

Once the output voltage is greater than the input voltage, the diode starts blocking and the capacitor will tend to discharge through resistance R .

This discharge is not complete for a single period of the low-frequency signal $s(t)$ but partial due to the fact that the time constant $RC > T$. The signal obtained on output under these conditions is schematically presented in Figure 3.7.

It is easy to see that the shape of the output signal is far from representing the initial low-frequency modulating signal.

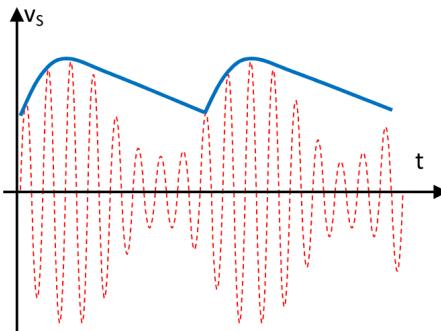


Figure 3.7. Signal obtained at the output of the demodulation circuit when $RC > T$

To further approximate a fairly correct demodulation, a compromise is adopted for the time constant.

It would be necessary that:

$$T_p < RC < T$$

where T is the modulating low-frequency signal period and T_p is the carrier period.

This condition on the time constant will allow the capacitor to not completely discharge during a carrier period and to try to follow the envelope of the modulated signal that represents the useful low-frequency signal.

This approach is interesting but does not enable us to exactly recover the shape of the initial modulating signal due to the fact that despite this compromise on the time constant, the capacitor will partially discharge over one carrier period.

The signal that will be recovered on output will be distorted by errors, as shown in the diagram representative of the output signal of Figure 3.8.

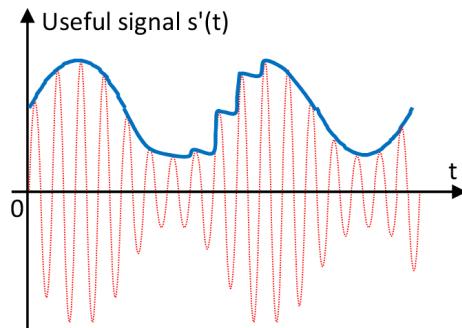


Figure 3.8. Signal obtained at the output of the demodulation circuit when $T_p < RC < T$

The signal obtained on output actually does not conform to the initial signal. To solve this noise issue in the demodulated signal, synchronous demodulation is employed, which yields much more interesting results.

3.3.3. Synchronous demodulation principle

Synchronous demodulation requires a signal that must be absolutely synchronous with the carrier. It is at this level that the origin of the phase-locked loop (PLL) takes place.

The PLL will make it possible to reconstruct the carrier from the modulated signal. From there, the useful low-frequency modulating signal can easily be extracted, as shown in Figure 3.9.

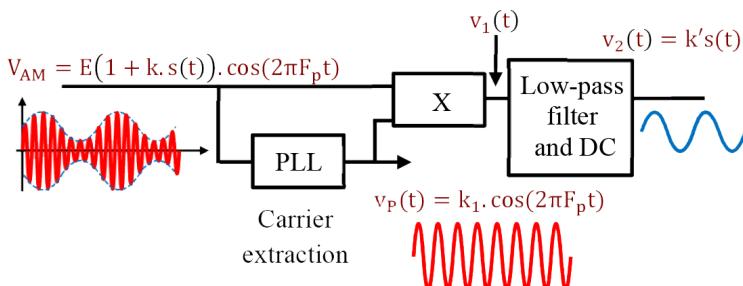


Figure 3.9. Synchronous demodulation using a phase-locked loop (PLL)

The phase-locked loop will enable the extraction of the carrier from the amplitude-modulated signal.

The amplitude-modulated signal and the signal representing the carrier, which can be found at the PLL output, are simultaneously applied to a multiplier.

As a result, the following signal is obtained at the multiplier output:

$$v_1(t) = E(1 + k \cdot s(t)) \cdot \cos(2\pi F_p t) \cdot k_1 \cdot \cos(2\pi F_p t)$$

$$v_1(t) = E \cdot k_1 (1 + k \cdot s(t)) \cdot \cos^2(2\pi F_p t)$$

$$v_1(t) = \frac{1}{2} E \cdot k_1 (1 + k \cdot s(t)) \cdot (\cos(4\pi F_p t) + 1)$$

After filtering high-frequency signals ($2F_p$) as well as the DC component, the result at the demodulation circuit output is a signal $v_2(t)$ proportional to the useful signal $s(t)$.

$$v_2(t) = \frac{1}{2} E \cdot k \cdot k_1 \cdot s(t) = k' s(t)$$

Thereby, as a result, the useful wave (or information) is retrieved without any alteration.

3.4. Phase-locked loop (PLL)

3.4.1. Advantages of the phase-locked loop

Phase-locked loops (PLLs) are widely used in information processing and data transmission processes.

A PLL is a system that can synchronize the instantaneous phase of two signals. PLLs are employed in a wide range of application areas. These applications can be summarized into two large families.

Phase-locked loops can be utilized as very narrow bandpass filters. This type of procedure is very interesting, for example, for recovering a signal masked by noise or for reconstructing the carrier (during the synchronous demodulation of an AM signal, for example).

Phase-locked loops can be utilized as frequency multipliers. This is the case, for example, in generators or frequency synthesizers.

It should also be noted that the PLL is nowadays the main focus in current subject areas, for instance, in chaotic communication.

3.4.2. PLL principle and operation

3.4.2.1. Description of a PLL

A PLL contains three essential basic components (Figure 3.10):

- a phase comparator;
- a low-pass filter;
- a voltage-controlled oscillator (VCO).

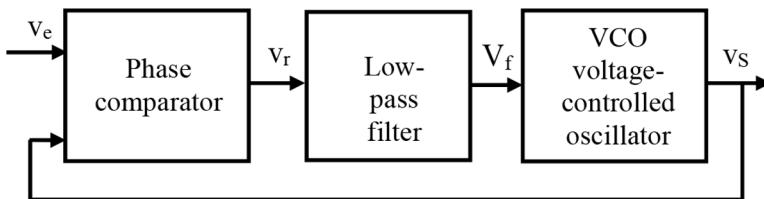


Figure 3.10. Schematic diagram of a phase-locked loop (PLL)

The expressions of the input and output signals are respectively:

$$v_e = V_1 \sin(\phi_e) \text{ and}$$

$$v_s = V_2 \sin(\phi_s)$$

where ϕ_e and ϕ_s are the respective instantaneous phases of the input signal v_e and output signal v_s .

$$\omega_e = \frac{d\phi_e}{dt}$$

$$\omega_s = \frac{d\phi_s}{dt}$$

with $f_e = (\omega_e/2\pi)$ and $f_s = (\omega_s/2\pi)$.

$\omega_e (f_e)$ and $\omega_s (f_s)$ are the instantaneous pulses (frequency) of the input and output signals respectively.

The phase comparator compares the instantaneous phase φ_e of a periodic signal on input to the instantaneous phase φ_s provided by the VCO. For analog signals, this comparator is often a multiplier.

For digital signals, this phase comparator is usually formed by an “XOR” or “OR-EXCLUSIVE” logic gate or a sequential logic circuit.

When the loop is locked ($f_s = f_e$), voltage v_r at the phase comparator output comprises harmonics of order $2f_e$ and more as well as a slow variable component proportional to the phase shift existing between the input signal (or reference signal) v_e and the signal v_s at the VCO output.

3.4.2.2. Operation

As has been specified, the phase-locked loop is a phase or frequency servo control. The PLL locks the frequency of a voltage-controlled oscillator to a reference signal injected on input.

The heart of the PLL is the VCO that provides on output a sinusoidal or square signal whose instantaneous frequency $f_s(t)$ depends on the control voltage V_f .

The phase comparator develops a voltage $v_r(t)$ that is related to the phase shift between input and output signals, “ v_e ” and “ v_s ” respectively. The low-pass filter eliminates higher frequencies and gives to its output the average value of the voltage $v_r(t)$ or its slowly varying component by removing all of the high-frequency harmonics.

In the absence of a signal applied on input, the VCO operates at its own oscillation frequency F_0 .

When a signal of frequency f_e is applied on input, the loop enters a transient state, where $v_r(t)$ and V_f vary in a complex fashion. This transient state is called locking or capture.

At the end of the transient state, the loop is locked and the frequency of the voltage-controlled oscillator (VCO) is equal to that of the input signal.

The frequency of the signal at the VCO output will depend on the value of the control voltage V_f .

The relation between the control voltage and the frequency of the VCO output signal in the ideal case is in general expressed by:

$$f_s = F_0 + \frac{F_{\max} - F_{\min}}{V_{f\max} - V_{f\min}} V_f$$

where F_0 is the natural frequency of the VCO, and F_{\max} and F_{\min} are respectively the maximal and minimal frequencies that the voltage-controlled oscillator is able to cover.

The frequency f_s can be more simply expressed as a function of the control voltage that is originating from the low-pass filter.

$$f_s = F_0 + K_{VCO} \cdot V_f$$

where K_{VCO} is the VCO transfer coefficient. It is expressed in hertz/volt.

The VCO transfer characteristic (Figure 3.11) represents the variation of the frequency of the VCO output signal based on voltage V_f applied to its input.

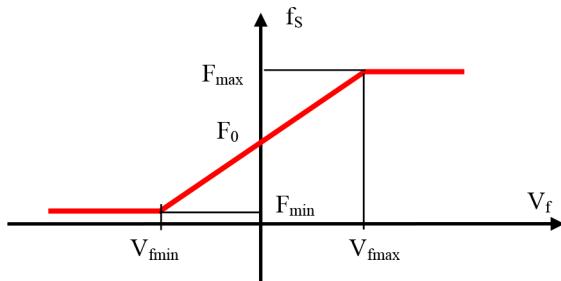


Figure 3.11. Ideal characteristic of the VCO

When the frequency f_s of the output signal is equal to frequency f_e of the input signal, it is said that the PLL is locked. The locking frequency can occupy a whole frequency range. This is referred to as the locking range of the phase-locked loop.

As long as the frequency of the signal applied to the input is within this range, the PLL remains locked and the output frequency of the voltage-controlled oscillator (VCO) will follow the changes of this frequency of the signal applied on input.

When the input frequency falls outside the locking range, the PLL will unlock. It can only initiate its locking process ($f_s = f_e$) when the frequency of the signal applied on input falls within the capture range of the PLL.

The capture range is less extended than the locking range as it is schematically presented in Figure 3.12.

The PLL locking range mainly depends on the characteristics of the voltage-controlled oscillator. This range goes from frequency F_{\max} to frequency F_{\min} .

The capture range, which is much less extensive than the locking range, mainly depends on the characteristics of the low-pass filter.

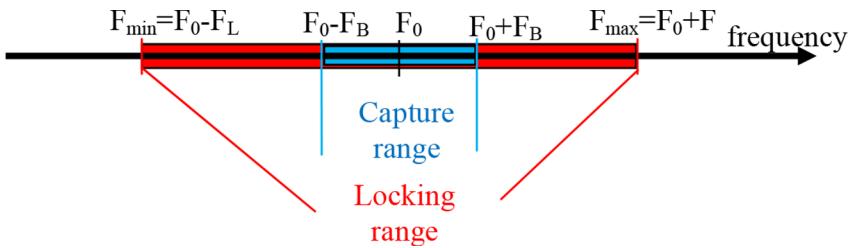


Figure 3.12. Capture range and locking range. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The capture range bandwidth is equal to $2F_B$, and the bandwidth of the locking range is equal to $2F_L$. It should be noted that $F_B < F_L$.

The capture and unhook mode (the PLL is no longer locked) of the phase-locked loop is summarized in Figure 3.13.

The analysis of this diagram allows us to observe that when a signal v_e of frequency $f_e \ll f_{\min}$ is applied to the input of the loop, the frequency of the output signal is equal to the central frequency of the VCO: $f_s = F_0$ (the loop is unlocked). The output signal frequency will remain equal to the VCO central frequency.

We increase frequency f_e of the input signal v_e . Based on the frequency F_{CL} , the frequency of the output signal f_s becomes strictly equal to the frequency f_e of the input signal. It is then said that the loop is “*tracking*” or that it is “*locked*”. This frequency F_{CL} is the low capture frequency.

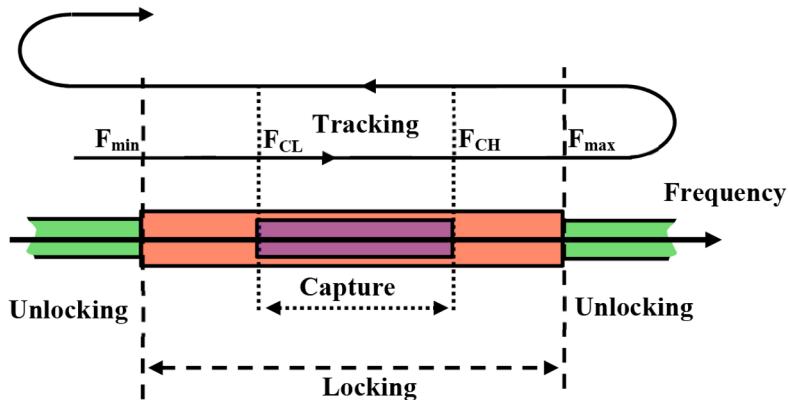


Figure 3.13. Operating mode of a PLL. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

When the frequency f_e of the input signal is continuously increased, the frequency f_s of the output signal will follow the evolution of the frequency f_e of the input signal (the loop remains locked) until the value F_{\max} is reached.

When the value of the input signal frequency f_e reaches the frequency F_{\max} (maximal possible frequency of the voltage-controlled oscillator), the PLL unlocks. The output signal frequency is no longer equal to the input signal frequency. The output signal frequency becomes equal to the VCO central frequency F_0 ($f_s = F_0$).

To relock the loop, the frequency f_e of the input signal has to be brought down to a value less than the frequency F_{CH} , the so-called high capture frequency of the PLL. It should be noted that the high capture frequency is less than the maximal locking frequency:

$$F_{CH} < F_{\max}$$

When the frequency of the input signal decreases and becomes smaller than frequency F_{\min} ($f_e < F_{\min}$), the PLL is no longer locked and $f_s = F_0$. It is able to lock only on the condition that the frequency f_e of the input or reference signal can be found within the capture range.

SUMMARY.—

Locked loop $f_e = f_s = f$ with $F_{\min} < f < F_{\max}$

Capture range = $[F_{CL} - F_{CH}]$ = frequency range within which the frequency f_e has to be brought to lock the loop if it was not so initially.

Locking range = $[F_{\min} - F_{\max}]$ = frequency range within which the loop remains locked.

These ranges are dependent on the phase comparator being used and on the characteristics of the low-pass filter.

We still virtually have:

$$f_{CH} - f_{CL} \leq f_{\max} - f_{\min}.$$

The PLL correctly operates when the input signal has the same frequency as the signal, which can be found on output ($f_e = f_s$). The voltage-controlled oscillator adjusts the frequency of the signal that is on output (f_s) to the input signal frequency (f_e) under the action of the control voltage V_f that is provided by the phase comparator and averaged by the low-pass filter. The phase comparator gives a constant phase difference when the PLL is locked.

When we have: $\phi_e(t) - \phi_s(t) = \text{constant} = \Delta\Phi_1$.

$$v_e = V_1 \sin(\phi_e); v_s = V_2 \sin(\omega_s t + \theta_s);$$

$$v_s = V_2 \sin(\phi_s); v_s = V_2 \sin(\omega_s t + \theta_s)$$

We have:

$$\frac{d(\phi_e - \phi_s)}{dt} = \frac{d(\omega_e t + \theta_e - \omega_s t - \theta_s)}{dt} = \omega_e - \omega_s = 0$$

$$f_s = f_e = f_{e1}$$

3.4.2.3. Reaction of the PLL to frequency changes in signals

First case: the frequency of the input signal increases

When the vector representation of voltages v_e and v_s is plotted as indicated in Figure 3.14, it can be observed that the phase shift between signals v_e and v_s is equal to $(\phi_e - \phi_s) = \Delta\Phi_1$. We have the equality:

$$f_s = f_e = f_{e1}$$

Now assume that the frequency of the reference or input signal increases (f_e changes from the value f_{e1} to value f_{e2}). The tip of the vector representing $v_e(t)$ will move to the left.

The phase comparator will then detect an increase of phase shift, which causes a variation in the control voltage V_f .

This variation of voltage V_f acts on the VCO to increase the frequency f_s of the output signal $v_s(t)$ to bring it to the same frequency as the input or reference signal $v_e(t)$. In these conditions, we have:

$$\phi_e - \phi_s = \Delta\Phi_2; \Delta\Phi_2 > \Delta\Phi_1$$

$$f_s = f_e = f_{e2} > f_{e1}$$

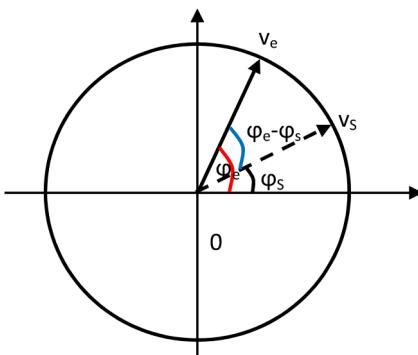


Figure 3.14. Vector representation of input and output signals. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

Second case: the frequency of the input signal decreases

When frequency f_e decreases, the phase comparator will detect a decrease in the phase shift, which causes a variation (downwards compared to the previous value) of the control voltage V_f . This variation of voltage V_f then acts on the VCO to decrease the frequency f_s of the output signal $v_s(t)$, which becomes identical to that of signal $v_e(t)$. In these conditions:

$$\phi_e - \phi_s = \Delta\Phi_3; \Delta\Phi_3 < \Delta\Phi_1$$

$$f_s = f_e = f_{e3} < f_{e1}$$

Third case: the frequency of the output signal varies

When the frequency of the signal originating from the VCO deviates from that of the input signal $v_e(t)$, the resulting phase difference will be proportional to this phase deviation. This difference of phase will generate a voltage V_f (slowly variable) that will act on the VCO to bring its frequency equal to the frequency of the input signal. The frequency of the signal provided by the VCO is thus synchronized with the frequency of signal $v_e(t)$.

$$f_s \nearrow \quad \phi_s \nearrow \quad (\phi_e - \phi_s) \searrow \quad V_f \searrow \quad f_s \searrow \quad f_s = f_e$$

3.5. Study of the elements that constitute a PLL

3.5.1. The phase comparator

3.5.1.1. The analog PLL

The phase comparator in an analog phase-locked loop consists of an analog multiplier (Figure 3.15).

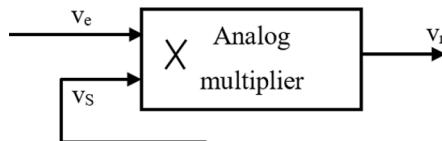


Figure 3.15. Analog multiplier phase comparator

Signals existing at the phase comparator input and at the VCO output are expressed by:

$$v_e = V_1 \sin(\phi_e); v_e = V_1 \sin(\omega_0 t + \theta_e), v_s = V_2 \sin(\phi_s); v_s = V_2 \sin(\omega_0 t + \theta_s).$$

The output voltage of the multiplier that has a transfer coefficient K is given by:

$$v_r = Kv_e v_s = V_1 V_2 \sin(\omega_0 t + \theta_e) \cdot \sin(\omega_0 t + \theta_s)$$

$$v_r = Kv_e v_s = \frac{KV_1 V_2}{2} [\cos(2\omega_0 t + \theta_e + \theta_s) + \cos(\theta_e - \theta_s)].$$

After filtering the harmonic $2\omega_0$, only the following component remains:

$$V_f = \frac{KV_1 V_2}{2} [\cos(\theta_e - \theta_s)] = \frac{KV_1 V_2}{2} \cos(\Delta\Phi)$$

$$V_f = \frac{KV_1 V_2}{2} \cos(\Delta\Phi)$$

The evolution of voltage V_f (slowly variable) according to the difference of phase between the signal applied at the input and the signal existing at the output of the VCO is shown in Figure 3.16.

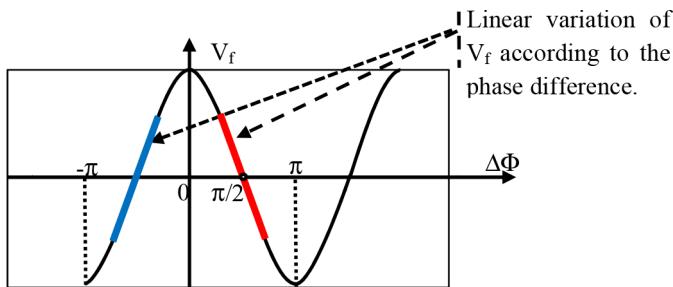


Figure 3.16. Evolution of the voltage V_f at the low-pass filter output based on the difference of phase shift $\Delta\Phi$. The variation is sinusoidal. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

To satisfy the relationship of linearity, this type of phase detector can only be used around $\pi/2$ or about $-\pi/2$. It depends on the characteristics of the voltage-controlled oscillator (VCO).

3.5.1.2. Digital PLL

Phase comparators in digital PLLs can be of two kinds: those that use combinational logic circuits and those that make use of sequential logic circuits.

Within this context, we present two simple examples to aid the understanding of phenomena. There are obviously other types of circuits, but they generally adopt the principles that are outlined in this manual.

3.5.1.2.1. Logic gate-based phase comparator

The phase comparator in the case of a digital signal consists of an “XOR” gate, as shown in Figure 3.17. The input signal (v_e) and the output signal (v_s) are square signals; they present a 50% duty cycle (the duration of the high state is equal to the duration of the low state).

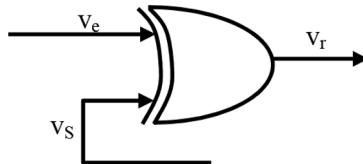


Figure 3.17. Digital signal phase comparator

The truth table of the “exclusive-or (XOR)” gate is presented in Table 3.1.

Logic state (v_e)	Logic state (v_s)	Logic state v_r
0	0	0
0	1	1
1	0	1
1	1	0

Table 3.1. “Exclusive-or” truth table

Signals that may be present at the inputs and output of a phase comparator in a digital PLL can be represented as shown in Figure 3.18.

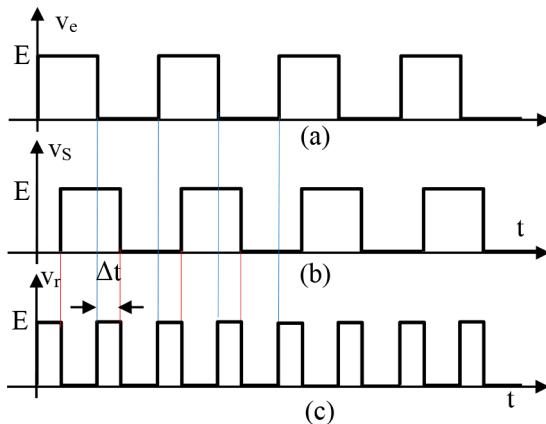


Figure 3.18. Various existing signals in a digital PLL. (a) reference signal v_e ; (b) signal v_s that can be found at the VCO output. (c) signal v_r that is found at the phase comparator output. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

When analyzing the state of signals of Figure 3.18, it can be seen that there is an offset between the reference signal (v_e) and the signal (v_s), which is provided by the voltage-controlled oscillator (VCO).

This offset represents a phase shift between v_e and v_s .

This phase shift is expressed by:

$$\Delta\Phi = \phi_e - \phi_s$$

In this context, we have to consider two separate cases:

$$- 0 < \Delta\Phi < \pi$$

$$- \pi < \Delta\Phi < 2\pi$$

First case: $0 < \Delta\Phi < \pi$

Reference and VCO output signals have similar frequencies of repetitions.

The offset between signals injected at the phase comparator input is smaller than the half-period of the reference signal or of the signal delivered by the VCO, as shown in Figure 3.19.

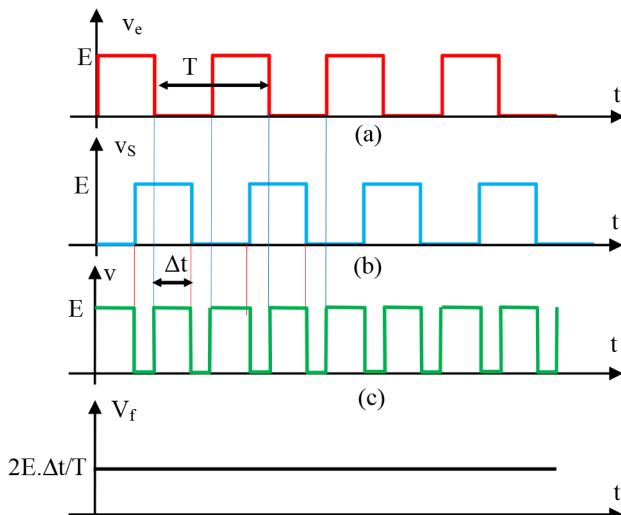


Figure 3.19. Different existing signals at the phase comparator input and output and the output of the low-pass filter ($0 < \Delta\Phi < \pi$). For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

The signal v_r located at the phase comparator output is a periodic signal. Its frequency is twice the frequency of the signal v_e or that of signal v_s . The phase shift between signals v_e and v_s is equal to $\Delta\Phi$.

The phase shift $\Delta\Phi$ is proportional to Δt .

$$\Delta\Phi = \frac{\Delta t}{T} 2\pi$$

The average value V_f of signal v_r (obtained through low-pass filtering following the phase comparator) is equal to:

$$V_f = E \frac{\Delta t}{(T/2)} = E \frac{2\Delta t}{T} = E \frac{\Delta\Phi}{\pi}$$

It can be observed that the voltage found at the output of the low-pass filter and which is directly applied to the input of the voltage-controlled oscillator is proportional to the phase shift between v_e and v_s .

Second case: $\pi < \Delta\Phi < 2\pi$

In this case, the offset between signals (v_e) and (v_s) that are applied to the phase comparator is greater than the half-period, as shown in Figure 3.20.

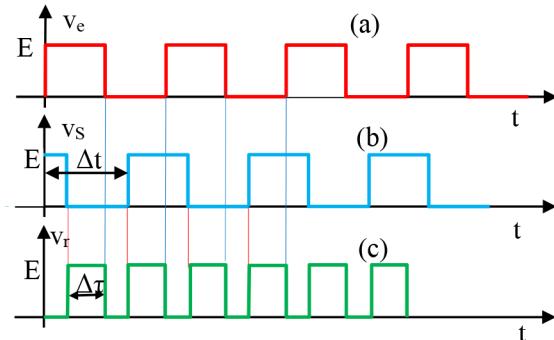


Figure 3.20. Signals at the phase comparator input and output when the phase shift is greater than π . For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

In this case, it can be seen that:

$$\Delta\tau = T - \Delta t$$

The signal (v_r) at the phase comparator output is injected through a low-pass filter, which will filter all high-frequency harmonics to only let through the slowly varying component (average value).

The expression of this average value is as follows:

$$V_{\text{avg}} = V_f = E \frac{\Delta\tau}{(T/2)} = E \frac{T - \Delta t}{(T/2)}$$

$$V_f = 2.E.(1 - \frac{\Delta t}{T})$$

The phase shift between the voltages v_e and v_s has already been defined. It can then be inferred that:

$$V_f = 2.E.(1 - \frac{\Delta\Phi}{2\pi})$$

SUMMARY.—

For: $0 < \Delta\Phi < \pi$, we have:

$$V_f = E \frac{\Delta\Phi}{\pi}$$

For: $\pi < \Delta\Phi < 2\pi$, we have:

$$V_f = 2.E.(1 - \frac{\Delta\Phi}{2\pi})$$

The variation of voltage (V_f) at the filter output with respect to the phase difference $\Delta\Phi$ between v_e and v_s is shown in Figure 3.21.

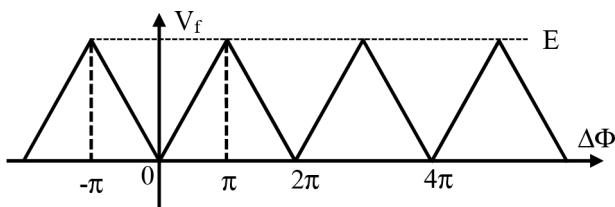


Figure 3.21. Variation of the VCO control voltage according to the phase difference between the signals applied at the phase comparator input

3.5.1.2.2. Sequential circuit-based phase comparator

These phase comparators operate on the rising or falling edges of the signals applied to them. These comparators generally make use of RS-, D- or JK-type flip-flops.

a) RS flip-flops

The representative circuit of the phase comparator is shown in Figure 3.22.

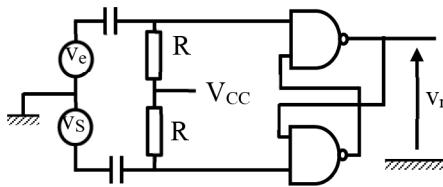


Figure 3.22. RS flip-flop phase comparator

The two inputs of the RS flip-flop are triggered on the falling edges of the reference signal (v_e) and of the signal (v_s) originating from the output of the voltage-controlled oscillator (VCO). The signals involved in this type of phase comparator are shown in Figure 3.23

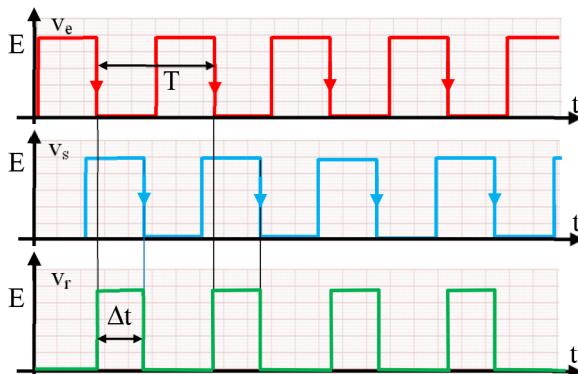


Figure 3.23. Evolution of signals at the RS flip-flop input and output of the phase comparator. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

The output voltage (v_r) of the phase comparator is then filtered using the low-pass filter, which is included in the processing chain of the phase-locked loop (PLL) to obtain the slowly varying component V_f .

The relation that links this slowly variable voltage V_f to the phase difference between the reference signal (v_e) and the signal (v_s) provided by the VCO is linear over a range that goes from zero to 2π .

The expression of this relation is:

$$V_f = E \frac{\Delta\Phi}{2\pi}$$

By inserting a low-pass filter to the phase comparator output, as indicated in Figure 3.24a, and then varying the phase difference between signals v_e and v_s , a voltage V_f is obtained at the low-pass filter output, which varies according to the curve of Figure 3.24b.

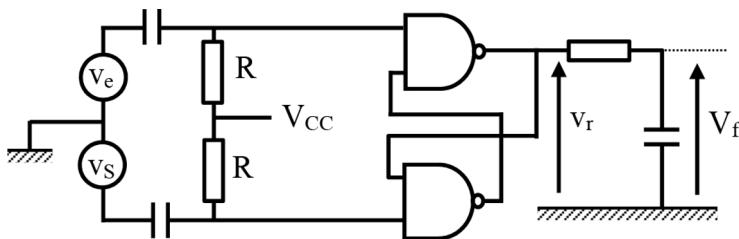


Figure 3.24a. RS flip-flop phase comparator and filtering

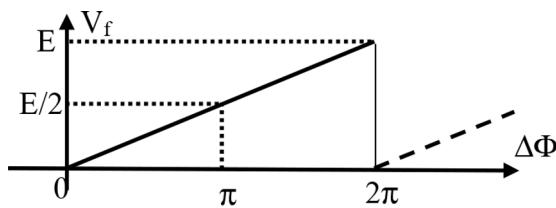


Figure 3.24b. Evolution of the filter output voltage according to the phase shift between the signals applied to the input of the “RS” flip-flop phase comparator

A very interesting case is presented in Figure 3.25. Signals v_s and v_e are in phase opposition, and the average value of signal v_r is indeed equal to $E/2$.

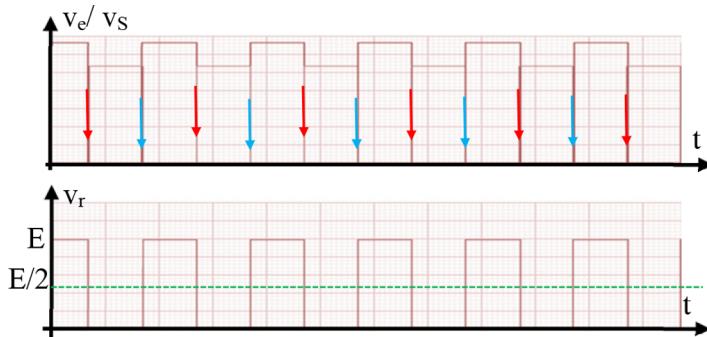


Figure 3.25. Phase comparator input and output signals. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

Switching on falling edges causes the phase comparator to no longer respond to the duty cycle of the signals.

3.5.1.2.3. Phase/frequency comparator

This type of comparison is also known as a “three-state comparator”. The name “phase-frequency” comes from the fact that this circuit operates as a frequency comparator, before the locking occurs, and operates as a phase comparator once the PLL is locked.

In general, phase/frequency comparators or three-state comparators are integrated, as will be covered when we will address a particular integrated circuit, the MOSFET 4046 circuit.

This type of phase comparator can have two outputs: one delivers a voltage that is dependent on the frequency difference relative to the signals applied to the input of the phase/frequency comparator and the other delivers a signal whose value depends on the phase difference of the two signals applied to the input of the phase/frequency comparator.

The principle of the “phase frequency” comparator is schematically presented in Figure 3.26.

It is important to remember at this level that the frequency or instantaneous pulse is the derivative of the instantaneous phase.

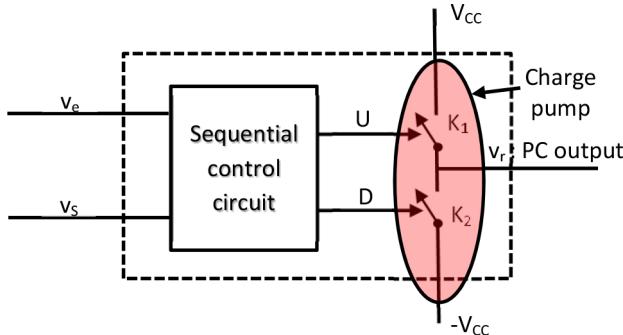


Figure 3.26. Phase/frequency comparator

The sequential control logic ensures the closing or opening of electronic switches K_1 and K_2 .

The sequential logic circuit that provides the control of the two electronic switches is schematically presented in Figure 3.27.

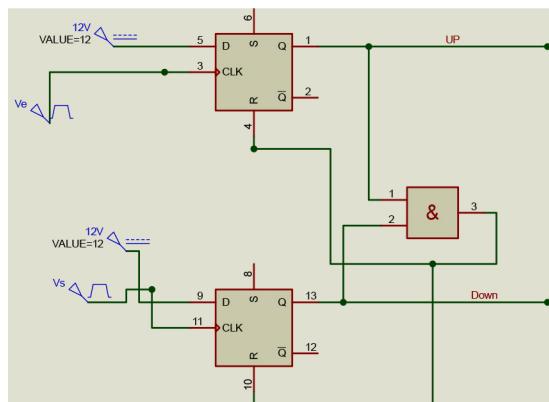


Figure 3.27. Sequential control logic in a three-state phase comparator or “phase/frequency” comparator

The evolution of the signal UP according to the phase shift that may exist between the reference signal (signal v_r) and the signal (v_s) delivered by the voltage-controlled oscillator (VCO) is presented in Figure 3.28(a–c).

The reference signal $v_e(t)$ has a leading phase difference compared to signal $v_s(t)$ provided by the VCO output.

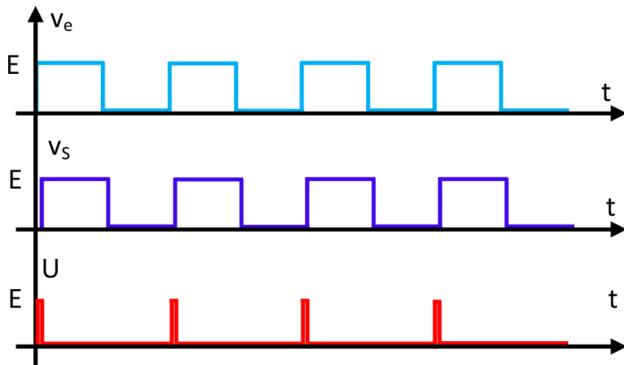


Figure 3.28a. Near-zero phase shift between v_e and v_s . For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The triggering is achieved on rising edges. The representations of Figure 3.28 show the evolution of signal UP and the duration of its high state depending on the phase shift existing between the reference signal $v_e(t)$ and the signal $v_s(t)$.

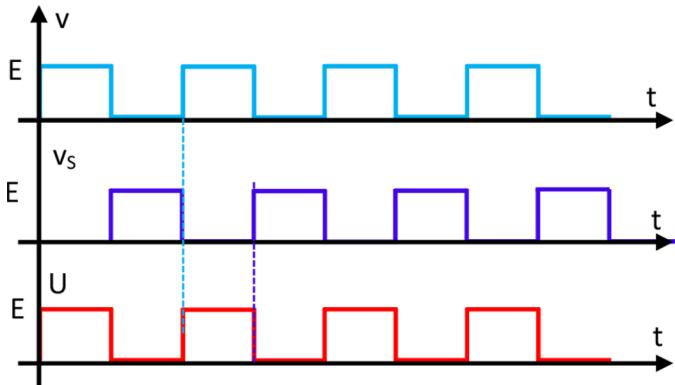


Figure 3.28b. Phase shift close to π between v_e and v_s . For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The case with the phase-shift between voltages v_e and v_s is approximately equal to 2π , as presented in Figure 3.28c.

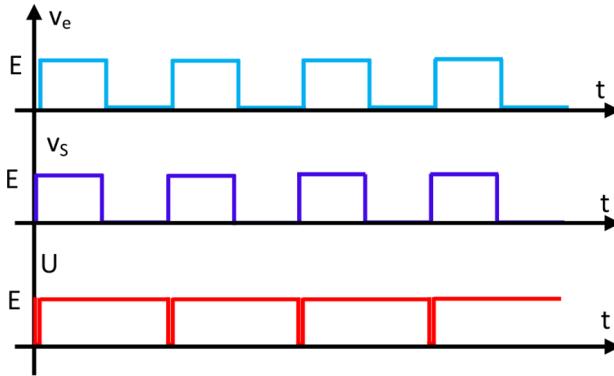


Figure 3.28c. Phase shift close to 2π between v_e and v_s . For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

It can be observed that in the three cases represented in Figure 3.28, the rising edge of the reference signal $v_e(t)$ precedes the rising edge of the signal $v_s(t)$ originating from the VCO output. In this case, only the signal denoted by U (UP) is active. The signal Down is inactive. When signal $v_e(t)$ is lagging compared to signal $v_s(t)$, signal D (Down) is active and signal Up is inactive (see Figure 3.29).

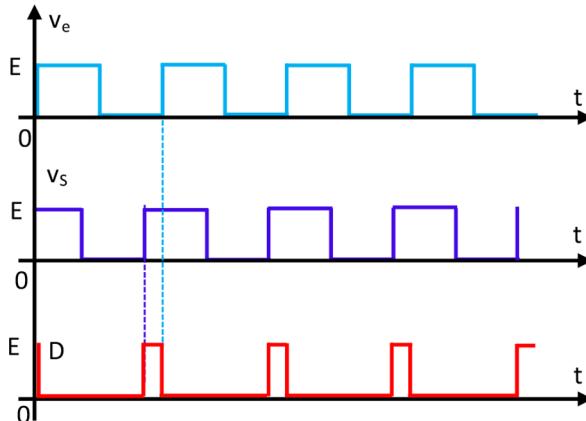


Figure 3.29. Signal $v_e(t)$ is lagging compared to signal $v_s(t)$. Signal D (Down) is active. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The frequencies of signals v_e and v_s are practically equal. The phase/frequency detector provides information not only on phase but also on frequency. As it is

known, the frequency or instantaneous pulse is the derivative of the instantaneous phase:

$$\omega_1(t) = \frac{d\phi_1(t)}{dt} = 2\pi f$$

The phase/frequency comparator PFD compares the reference signal $v_e(t)$ of frequency f_e with the signal $v_s(t)$ originating from the VCO output, which has a frequency f_s . We will thus have the activation of signals U (UP) and D (Down) according to the state and the phase difference that may occur between signals $v_e(t)$ and $v_s(t)$.

When the phase difference is greater than 2π , the circuit is in frequency detection mode, and the output current then delivers a constant value (e.g. for a charge pump). The loop filter integrates this value and the PFD continues to operate until the error between two input signals falls below 2π . From the moment when the phase shift between $v_e(t)$ and $v_s(t)$ is less than 2π , the “phase/frequency” comparator circuit will provide information related to the phase difference between the reference signal $v_e(t)$ and signal $v_s(t)$ that originates from the VCO output. When the phase difference is near zero, the circuit initiates a locking state. The full diagram of the “phase/frequency” comparator circuit is presented in Figure 3.30.

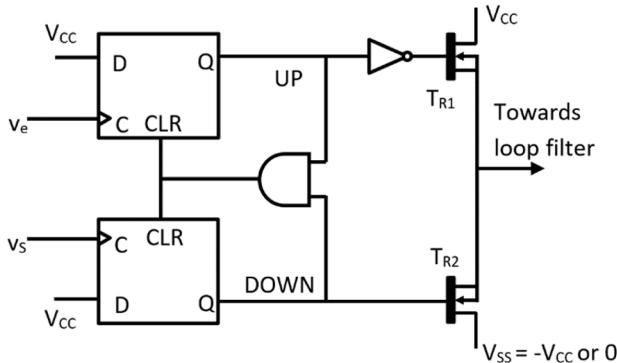


Figure 3.30. Phase/frequency comparator diagram

The functioning of this circuit can be established as follows:

When the reference signal is in leading phase compared to signal $v_s(t)$, the signal U (UP) is active and signal D (Down) is inactive. Thereby, the field-effect transistor T_{R1} is active and the voltage v_r at the “phase/frequency” comparator output is equal to $+V_{CC}$ (logic 1).

When the reference signal $v_e(t)$ is in lagging phase compared to signal $v_s(t)$, signal D (Down) is active and thereby transistor T_{R2} is active. There will be at the “phase/frequency” comparator output a voltage $v_r = 0$ (0 logic). Similarly, when the frequency f_s of the signal delivered by the VCO is higher than the frequency f_e of the input reference signal, the comparator output voltage is equal to $+V_{CC}$. On the other hand, when frequency f_s of the signal delivered by the VCO output is lower than frequency f_e of the reference signal, the voltage output of the comparator is zero.

Field-effect transistors T_{R1} and T_{R2} form the “charge pump”. The charge pump is used to convert logic signals U and D into a single signal that will be filtered to control the VCO, as indicated in Figure 3.31. The loop filter is associated with the charge pump, and its role is to filter noise components. The charge pump associated with the loop filter can be implemented in different ways. A charge pump consists of a three-position switch that is controlled by the sequential circuit. When the switch is in position U or D (K_1 or K_2 are closed), it delivers a voltage $\pm V_{CC}$ or current $\pm I$. In position N, the switches K_1 and K_2 are open. The loop low-pass filter is isolated from the charge pump.

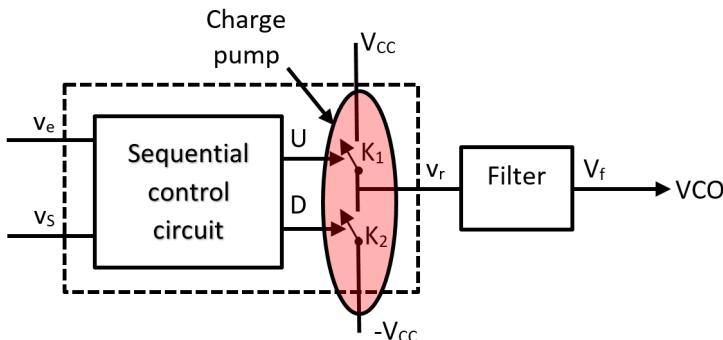


Figure 3.31. Acquisition of the VCO control signal within a PLL with a phase/frequency comparator

3.5.1.2.4. Case study application: the three-state phase comparator employed in the CMOS 4046 integrated circuit

a) Introduction

The CMOS 4046 integrated circuit (Figure 3.32) contains all the elements needed to design and implement a full phase-locked loop (PLL). The only element that is not integrated is the low-pass filter that has to be externally associated with the phase comparator to be able to control the VCO.

It can be noted that this integrated circuit comprises two phase comparators: one is based on an “exclusive-OR” and the second is a type-2 phase comparator. The first XOR-gate comparator is presented in detail in section 3.5.1.2.1.

For this case, we will focus on the study of the second-phase comparator, which is in fact a three-state comparator.

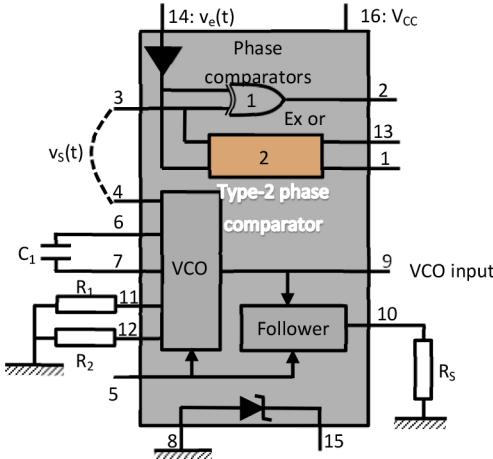


Figure 3.32. Synoptic diagram of the CMOS 4046 integrated circuit. Source: Texas Instruments Application Report

The schematic diagram of the type-2 phase comparator of the CMOS 4046 IC is shown in Figure 3.33.

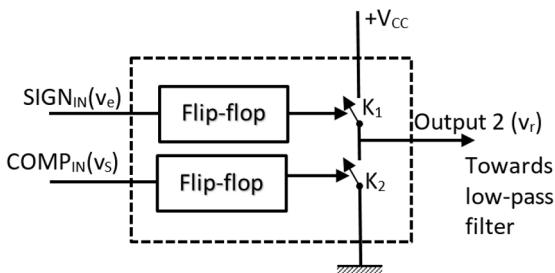


Figure 3.33. Schematic diagram of the type-2 phase comparator of the 4046 circuit

The phase comparator is only responsive to rising or descending edges of logical signals. The duty cycle of existing signals at its input has no influence.

The two flip-flops control electronic switches K_1 and K_2 . The two switches can in no case be closed at the same time.

To this end, there will be three states:

State 1: K_1 closed and K_2 open. In these conditions, we have a high logic level at the phase comparator output:

$$v_r = +V_{CC}$$

State 2: K_1 open and K_2 closed. In these conditions, we have a low logic level at the phase comparator output:

$$v_r = 0.$$

State 3: K_1 open and K_2 open. In these conditions, output 2 is disconnected. No current can flow in the load. There will be a high impedance output.

b) Schematic diagram of the phase comparator and operating principle

The internal synoptic diagram of the type-2 phase comparator integrated in the 4046 circuit is schematically presented in Figure 3.34.

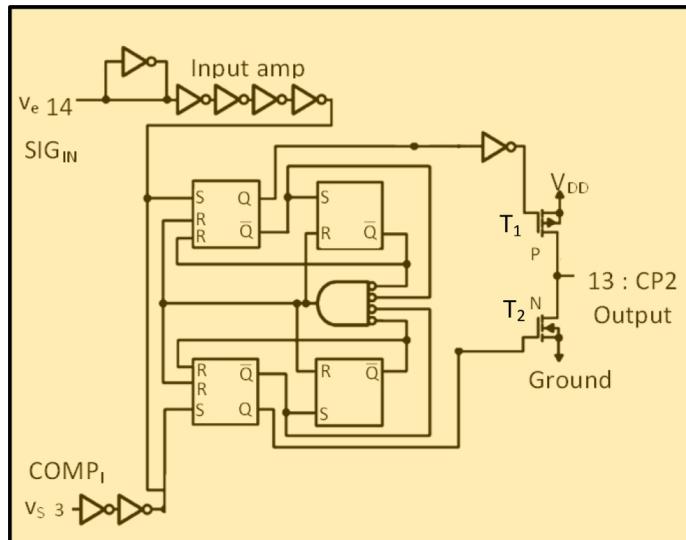


Figure 3.34. Synoptic diagram of the type-2 phase comparator integrated into the 4046 circuit. Source: Texas Instruments Application Report

The operation of this phase comparator is established as follows:

In a first step, it is assumed that the signal reference v_e and signal v_s arriving from the output of the voltage controlled oscillator have frequencies almost equal but out of phase.

In these conditions, when a rising edge of the reference signal (v_e) is applied to input SIG_{in} , the output shifts to a high state. A rising edge at input $COMP_{in}$ causes the output to fall to a low level. The activities of transistors T_1 (conducting) and T_2 (blocking) make it possible to obtain this signal at the phase comparator output. This is true when the input or reference voltage is in leading phase compared with the voltage that originates from the VCO output.

The various signals implemented in the phase comparator are schematically presented in Figure 3.35.

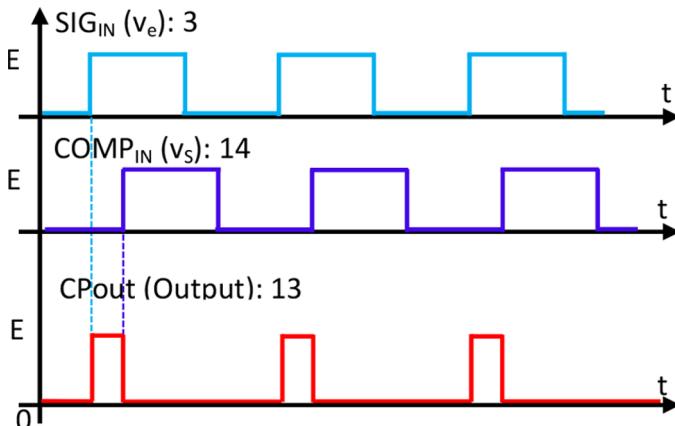


Figure 3.35. Input and output signals of the type-2 phase comparator of the 4046 IC (signal v_e is in leading phase compared to signal v_s). For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

Conversely, (v_s is in leading phase compared to v_e) transistor T_2 is conducting and transistor T_1 is blocking. Thereby, the output will be connected to ground. This poses a problem since the signal obtained on output is similar to the signal that can be obtained if the two transistors were not conducting (high-impedance output case). This aspect is summarized in Figure 3.36.

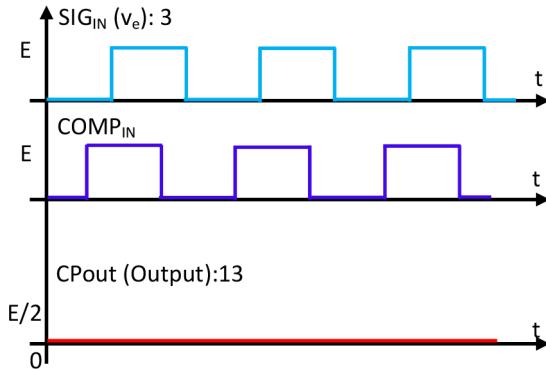


Figure 3.36. Input and output signals of the type-2 phase comparator of the 4046 IC (signal v_e is in lagging phase compared to signal v_s). For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

SUMMARY.—

When the signals have the same frequency but are out of phase, the output is periodic with a “high” level between rising edges of signals “ v_e ” and “ v_s ” if “ v_e ” is leading with respect to “ v_s .”

On the other hand, the output is at a “low” level between the rising edges of “ v_e ” and “ v_s ” when “ v_e ” is lagging with respect to “ v_s ”.

In contrast to the phase comparator based on “exclusive-OR” gates, with this kind of type-2 phase comparator, the signal that is applied to the input will always be captured, because the capture range will be almost equal to the locking range $\Delta f_{capt} = \Delta F_{mant}$.

When the frequencies of reference signals (v_e) and of the signal delivered from the VCO output are equal ($f_s = f_e$), any dephasing will result in a sequence of pulses.

With this sort of type-2 phase comparator, the input signal may not have a duty cycle equal to 0.5.

Signals at the phase comparator output related to a high-impedance state and related to the comparison of the phase shift between v_e and v_s when the reference voltage (v_e) is lagging with respect to output voltage (v_s) are similar.

To be able to establish the difference between the high-impedance output state (the two non-conducting transistors T_1 and T_2) and the state of the output connected to ground due to the fact that voltage v_e is in lagging phase compared to v_s (transistor T_1 is not conducting and transistor T_2 is conducting), a reference voltage V_0 can be added at the phase comparator output. As a result, we can easily establish the difference between a high-impedance state and a state where the signals at the input of the phase comparator are out of phase (the reference signal v_e is lagging compared to signal v_s).

3.5.2. Low-pass filter

3.5.2.1. Filtering positioning

The phase comparator output signal is formed by a signal rich in harmonics. This signal is the result of the comparison of the reference signal v_e and signal v_s provided by the output of the VCO. The signal at the phase comparator output also contains a slowly varying component that is retrieved at the output of the low-pass filter. This slowly varying component provides information on the phase difference between the reference voltage “ v_e ” and voltage v_s applied to the phase comparator input.

The low-pass filter has a very significant influence on the transient state and the proper functioning of the PLL. The calculation of the low-pass filter must take into account the speed of the signal that is applied on input and also provide some stability to enable the locking of the PLL. The low-pass cutoff filter frequency must meet specific conditions. It cannot be too small or too high. Compromises must therefore be adopted for the calculation of the low-pass filter.

The type of filter that has to be chosen can be passive or active. It is generally of the first order, but it can be of a higher order.

When, for example, a first-order low-pass filter has been chosen, the filter cutoff frequency “ F_C ” must be low compared to the minimal frequency of the voltage-controlled oscillator (VCO) to ensure a correct operation of the PLL.

3.5.2.2. Examples of low-pass filters

A first example of passive low-pass “RC” filter is schematically presented in Figure 3.37. This type of filter is very simple. It is widely used in PLLs in applications such as frequency synthesis.

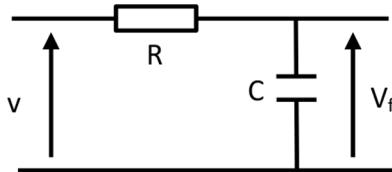


Figure 3.37. First-order low-pass “RC” filter

The transfer function of this filter is given by:

$$H(p) = \frac{V_f}{V_r} = \frac{1}{1+RCp}$$

where p is the Laplace variable, $p = j\omega$ (with sinusoidal waves) and j is an imaginary number.

In this case, it can be written that:

$$\frac{V_f}{V_r} = \frac{1}{1+jRC\omega}$$

$$\left| \frac{V_f}{V_r} \right| = \frac{1}{1+(RC\omega)^2}$$

$$\varphi = -\text{Arctg}(RC\omega)$$

The use of a first-order low-pass filter gives a second-order PLL. This will be clarified when aspects related to modeling the PLL are addressed in their general form. The utilization of the low-pass RC filter is a means to obtain at the VCO output a signal that has a frequency exactly identical to the frequency of the input signal when the PLL is locked.

A Bode plot (modulus and phase) for this type of loop filter is shown in Figure 3.38.

The first-order low-pass filter that utilizes a single resistance and a single capacitor can only be employed for closed-loop wide-bandwidth applications. For narrow-bandwidth applications, this filter may not be an element sufficient for the stability of the PLL.

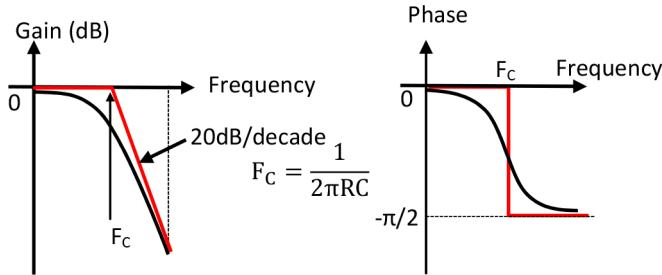


Figure 3.38. Bode plot of the first-order low-pass filter

Thereby, to solve this issue, a second type of low-pass filter is used, known as a phase delay filter, whose diagram is presented in Figure 3.39.

This filter obviously has a dual function. Its function is to obtain on output the slowly varying voltage, which is related to the phase difference between signals that are applied at the phase comparator input and also contributes to the performance of the phase-locked loop especially with regard to stability aspects.

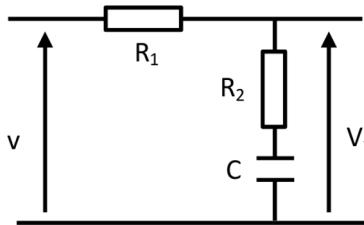


Figure 3.39. Second type of low-pass filter employed in a PLL

Furthermore, the circuit transfer function is given by:

$$H(p) = \frac{V_f}{V_r} = \frac{1+R_2Cp}{1+R_1Cp+R_2Cp}$$

$$H(p) = \frac{1+\tau_2 p}{1+\tau_1 p+\tau_2 p}$$

$$\tau_1 = R_1 C \text{ et } \tau_2 = R_2 C$$

Two time constants can be identified, τ_1 and τ_2 , in contrast to the low-pass filter simply comprising a resistor and a capacitor. This is designed to meet two criteria:

- to only obtain the slowly varying signal at the filter output;
- to provide good stability to the loop.

The Bode plot is presented in Figure 3.40.

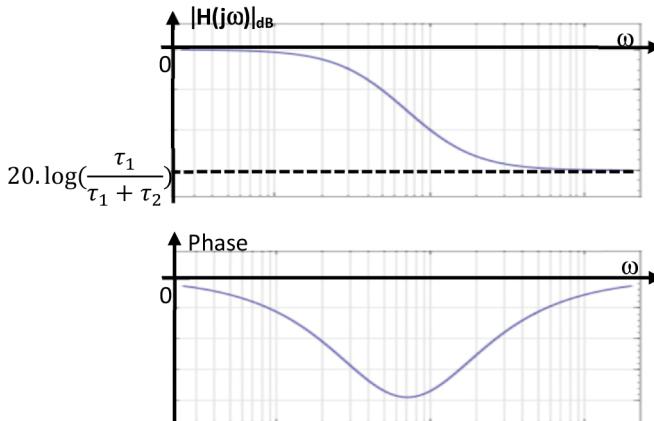


Figure 3.40. Bode plot for the second type of low-pass filter

When analyzing the Bode plot of this second low-pass filter (see Figure 3.40), it can be observed that high-frequency components (unwanted components) are not sufficiently attenuated. It is therefore important to address this by adding an additional capacitance on output (see Figure 3.41) to strengthen the attenuation power of the circuit such that only the slowly varying component of the VCO control is allowed to pass through.

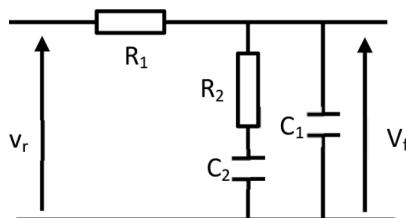


Figure 3.41. Improvement of the second type of low-pass loop filter for rejecting high frequencies

As we have already pointed out, it is also possible to use active low-pass filters. The most widely utilized is that which is schematically presented in Figure 3.42. For this purpose, two operational amplifiers are used. The function of the second op-amp circuit A_2 is only to ensure a phase rotation equal to π to compensate for the phase inversion introduced by circuit A_1 .

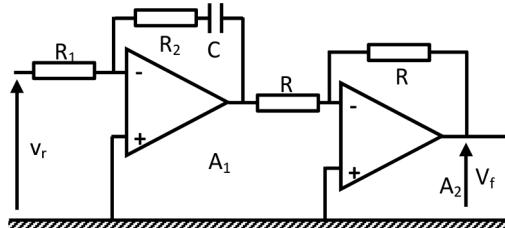


Figure 3.42. Low-pass filter employed in a PLL

The transfer function of this circuit is given by:

$$\frac{V_f}{V_r} = \frac{1+R_2Cp}{R_1Cp}; \quad \frac{V_f}{V_r} = \frac{1+\tau_2 p}{\tau_1 p}$$

It can also be observed that there are time constants τ_1 and τ_2 . The goal is the same: to detect the slowly varying wave and to ensure optimal stability for the PLL. The Bode plot of this active filter is shown in Figure 3.43.

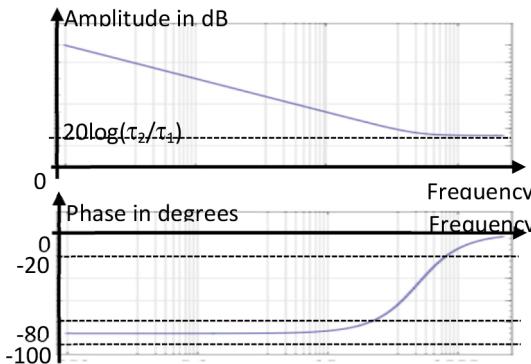


Figure 3.43. Bode plot of the active low-pass filter

It should be noted that the active low-pass filter cannot filter high frequencies with efficiency. This problem is corrected by inserting after the active filter a first-order passive filter (see Figure 3.44).

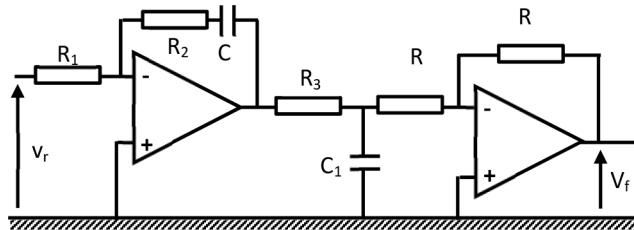


Figure 3.44. Improved active filter for filtering high frequencies

3.5.3. Voltage-controlled oscillator (VCO)

3.5.3.1. General information

A VCO generates an output signal whose frequency f_s can be modified by means of a control voltage V_f as indicated in Figure 3.45.

The control law f_s as a function of V_f is called a characteristic of the VCO.



Figure 3.45. VCO operating principle

The VCO transfer characteristic is presented in Figure 3.46.

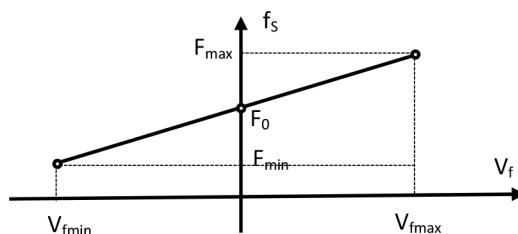


Figure 3.46. Transfer characteristic of a VCO

The VCO will operate around the central frequency or natural frequency F_0 . The slope of the transfer characteristic represents the parameter K_{VCO} . It is expressed in rad/s.V or Hz/V.

The voltage-controlled oscillator (VCO) can be represented by its block diagram, as shown in Figure 3.47.

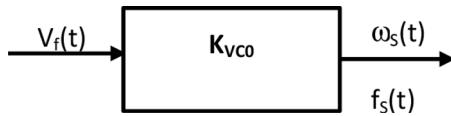


Figure 3.47. VCO block diagram

The frequency interval $[F_{\min} - F_{\max}]$ usable is called the oscillator frequency range. The central frequency or natural frequency is expressed by:

$$F_0 = (F_{\min} + F_{\max})/2$$

Two main families of VCOs can be distinguished:

- relaxation oscillators;
- quasi-sinusoidal oscillators.

Relaxation or astable oscillators can be used up to about 10 MHz and are able to deliver square or triangular waveforms (or even sine waves with a distortion of a few percents). They are simple in their implementation. At high frequencies, quasi-sinusoidal oscillators (varicap diode-based systems) or specialized integrated circuits making use, for example, of ECL (Emitter-Coupled Logic) technology are employed instead.

Variable frequency oscillators based on discrete components or VCOs in integrated form can be utilized. The two concepts will be presented. However, more emphasis will be given to the concept of integrated circuits due to the fact that existing PLLs are in most cases in integrated form.

3.5.3.2. Discrete component-based VCO

For the calculation of a voltage-controlled oscillator, it is necessary to know the range of the frequency bandwidth that is to be covered. The choice of elements for the feedback circuit (circuit that sets the oscillation frequency and its variation range) is very important. For high frequencies, an “LC”-type resonant circuit is used as feedback circuit in oscillators. In general, the variable element to vary the frequency of the oscillator is the capacitor that will be represented by a variable capacitance diode (varicap) or a set of varicap (or varactor) diodes properly assembled. It is also important to know the relative gain variation of the VCO that expresses the change in frequency according to the value of the control voltage.

The shape of the function $f_s = F(V_f)$ is very important for the integration of the VCO in a PLL.

For low frequencies, we will use integrated circuits including feedback circuits built around resistors and capacitors.

For high frequencies, there are several types of VCOs existing based on known structures such as Colpitts, Clapp or Hartley oscillators.

For the discrete component, a bipolar transistor or a field-effect transistor could be used, which would be suitable for the frequency bandwidth that the VCO is supposed to cover.

In the example, we will present a field-effect transistor Colpitts oscillator. The study of a Hartley or Clapp oscillator remains similar.

A simple diagram of a Colpitts oscillator using a field-effect transistor is schematically presented in Figure 3.48.

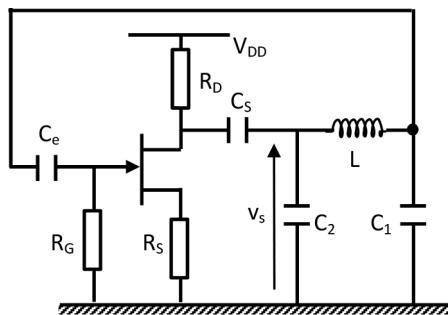


Figure 3.48. Field-effect transistor Colpitts oscillator

Resistors R_D , R_S and R_G are polarization resistors. Capacitors C_e and C_S are coupling capacitors. They present negligible impedances to the operating frequency of the oscillator. Their main function is to block continuous components required for the polarization of the field-effect transistor.

The feedback network of the oscillator is formed by the circuit composed of capacitors C_1 and C_2 and the self-inductance L . Unlike bipolar transistors, field-effect transistors (FET) present a very high input resistance. They consume a

relatively low amount of power. The function of the feedback circuit is to determine the oscillation frequency of the oscillator. This frequency is given by the relation:

$$f = \frac{1}{2\pi\sqrt{\frac{LC_1C_2}{C_1+C_2}}}$$

In order to have a variable frequency controlled by an external voltage, a means should be found to vary capacitances C_1 or C_2 or both at the same time based on a voltage that is externally applied. For this purpose, we use a component that allows us to obtain a variation of capacitance according to a voltage; this is the variable capacitance diode (varactor). In fact, this type of diode (see Figure 3.49a) has the characteristic (see Figure 3.49b) of having between its terminals a capacitance that varies according to the reverse voltage that is applied to it. Therefore, the insertion of a diode with variable capacity in parallel or in series with one of the capacitors C_1 and C_2 or both at the same time will make it possible to have an equivalent capacitor whose capacitance will vary depending on the reverse bias voltage applied to the varicap diode.

The variation of the junction capacitance of the variable capacitance diode that uses, for example, planar technology obeys the relation:

$$C_j = \frac{C_{j0}}{\sqrt{\left(1 + \frac{V_R}{V_0}\right)}}$$

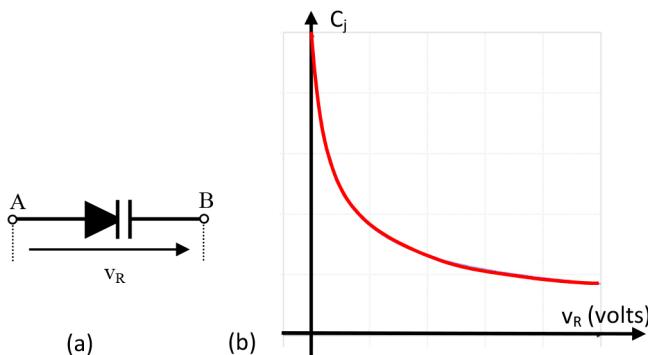


Figure 3.49. Variable capacitance diode (a) and variation direction in its junction capacitance according to the reverse voltage applied thereto (b)

When the varactor diode is integrated into the feedback network of the Colpitts oscillator, it is very important to pay attention to how the reverse voltage v_R is applied to vary the varactor capacitance.

This voltage must in no way disrupt the polarization of the active element.

The operating diagram of a voltage-controlled oscillator is shown in Figure 3.50. The capacitor C_L prevents the bias voltage v_R of the variable capacitance diode to disrupt the bias of the field-effect transistor.

The choke coil L_{choc} is included to prevent high-frequency signals to disrupt the bias voltage of the varactor diode. It also works as a linking circuit between the varactor diode and control voltage V_R .

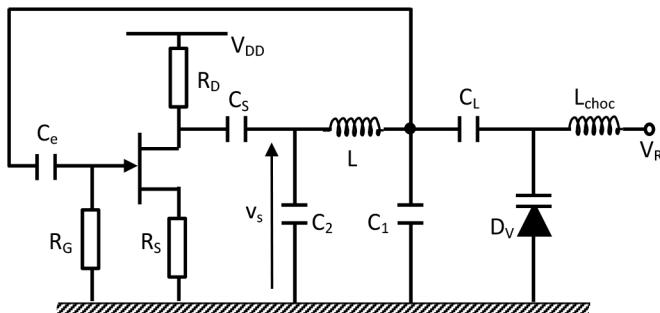


Figure 3.50. Operating diagram of the voltage-controlled oscillator (VCO)

3.5.3.3. IC-based VCO

An IC-based voltage-controlled oscillator is generally utilized with low frequency, or more generally with frequencies below a few tens of MHz. There are nonetheless a few integrated circuits that operate as voltage-controlled oscillators (VCO) that can reach and even exceed 100 MHz. There are a multitude of ICs that can operate as VCOs. In the following, we will present some integrated circuits that seem to respond to the educational and training objectives expected by this manual. The types of VCOs that are directly integrated into PLLs will not be addressed. They will be covered in a dedicated paragraph and that will focus on integrated PLL circuits. The issue of VCOs that are predestined to specific applications will also not be covered.

a) The XR-2206 circuit

The XR-2206 circuit is not new. It is usually no longer employed nowadays. Its main interest is particularly educational for the production of a variable-frequency signal by varying a control voltage.

It can be used for a variety of applications and integrated into a phase-locked loop. It consists of a 16-pin DIL casing (dual in-line) (see Figure 3.51).

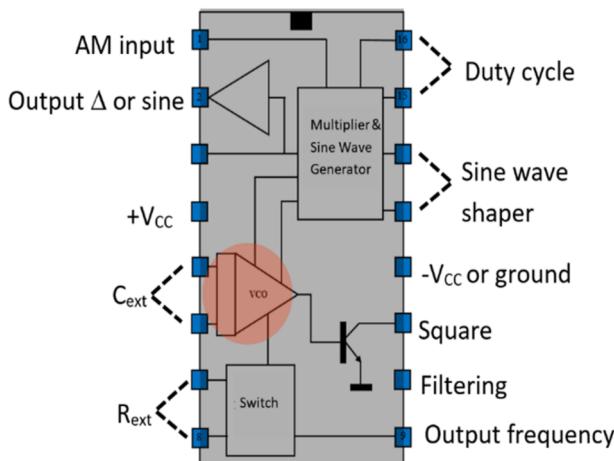


Figure 3.51. Internal diagram of the XR 2206 circuit. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

The XR 2206 essentially contains a power switch, a multiplier, a shaping circuit, a bipolar open-collector transistor, a follower stage and a voltage-controlled oscillator (VCO) whose frequency is determined by external components C_{ext} and R_{ext} .

The frequency variation of the output signal is provided by the injection of a signal at the sweeping input of the voltage-controlled oscillator (VCO) circuit, as indicated in Figure 3.52.

The input 7 of the current switch is a low-impedance input. It has a constant voltage that is virtually equal to 3 volts.

The frequency of the output signal is given by the relation:

$$f(\text{Hz}) = \frac{320I_F \cdot 10^3}{C}$$

When we take $R = R_C$, it leads to the relation

$$f(\text{Hz}) = \frac{32 \cdot 10^4}{RC} V_f = KV_f$$

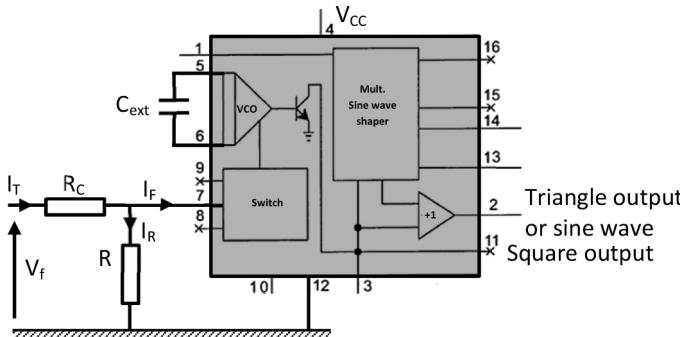


Figure 3.52. XR 2206 IC VCO operation

b) The LTC6990 circuit

There are much more recent circuits than the XR 2206 that can also operate as VCOs in low-frequency ranges with very interesting frequency/voltage linearity. This is the case, for example, for the LTC 6990 circuit (see Figure 3.53). The operation principle of the LTC 6990 integrated circuit as an oscillator is very simple. In order to have a signal on output that has a fixed frequency, a fixed resistance is inserted between the input "SET" of the circuit and the ground. The frequency of the output signal is proportional to that resistance. In reality, the frequency is proportional to the current found at this "SET" input. The value of the resistance will allow the current intensity to be modulated. When the objective is to implement a voltage-controlled oscillator using the LTC 6990 circuit, we can implement the diagram presented in Figure 3.54.

The injection of a control voltage through the network R_{VCO} , R_{SET} will allow the frequency of the output signal to be controlled (see Figure 3.54).

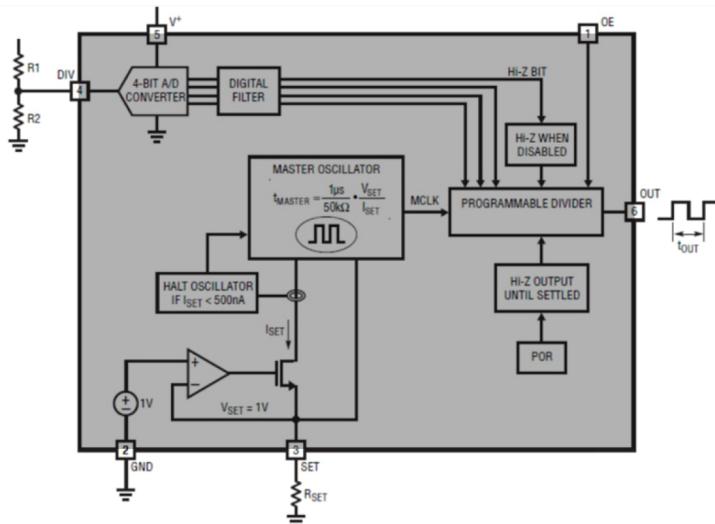


Figure 3.53. Block diagram of the LTC6990 IC/Source: Analog Devices data sheet

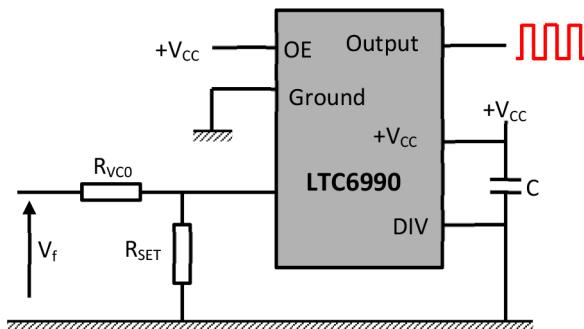


Figure 3.54. Operating principle of the LTC6990/Source: Analog Devices data sheet

The output signal frequency is expressed as:

$$f_{\text{OUT}} = f_{\text{MASTER}} - 0.5 \cdot V_f / R_{\text{SET}}$$

It is clearly visible that there is a relationship of linearity between the frequency of the output signal and the control voltage V_f.

This relationship is confirmed by the “manufacturer’s” curve which provides the variation of the frequency according to the control voltage (see Figure 3.55). The slope of the curve is negative. The frequency F_0 for zero control voltage is equal to 1 MHz.

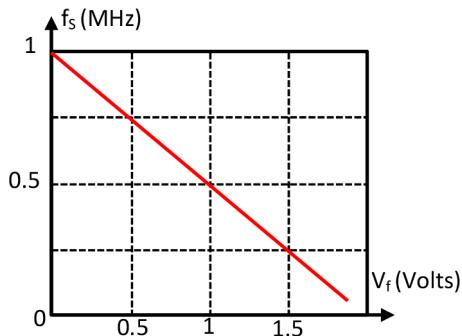


Figure 3.55. LTC1990 IC-based VCO transfer function

c) Motorola MC100EL1648 (1648) integrated circuit

The MC1648 and MC100EL1648 circuits are practically similar. They have been designed according to the same topology, except that the MC100EL1648 circuit can operate at much higher frequencies.

The MC1648 circuit can operate up to 200 MHz and the MC100EL1648 circuit can reach and exceed 1 GHz.

The MC 1648 circuit is implemented in a 14-pin DIL (dual in-line) casing (see Figure 3.56a) and makes use of an external tank circuit to operate as an oscillator (see Figure 3.56b).

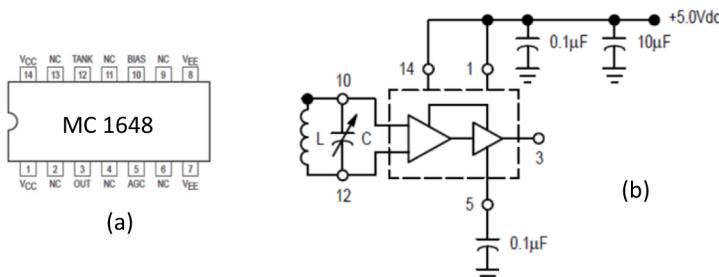


Figure 3.56. (a) DIL case regarding MC1648 IC; (b) MC1648-based oscillator design. Source: Motorola data sheet

This circuit uses bipolar transistors and ECL (Emitter-Coupled Logic) technology. This enables it to cover a frequency bandwidth that ranges from 1 MHz up to 200 MHz.

The MC100EL1648 circuit uses the same principles as the 1648. It however uses technology related to bipolar transistors much more advanced than that employed for the MC1648 circuit. This technology is specific to the firm that manufactures the circuit. This enables the MC100EL1648 circuit to have lower consumption and a spectral range that can cover from a few KHz up to 1.1 GHz. Square- or sinusoidal-shaped output signals can be obtained with this circuit. The MC100EL1648 circuit is a circuit implemented with two different casings. There is an 8-pin DIL case and a 14-pin DIL case (see Figures 3.57(a) and (b)).

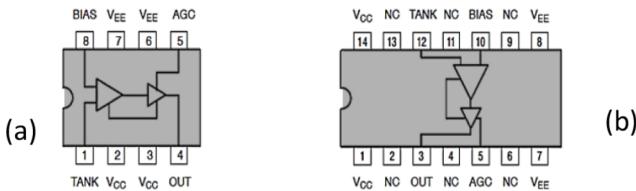


Figure 3.57. (a) MC100EL1648 circuit in 8-pin DIL case and (b) MC100EL1648 circuit in 14-pin DIL case

To operate the MC 100EL1648 as oscillator, a high-quality parallel LC circuit just needs to be added (see Figure 3.58).

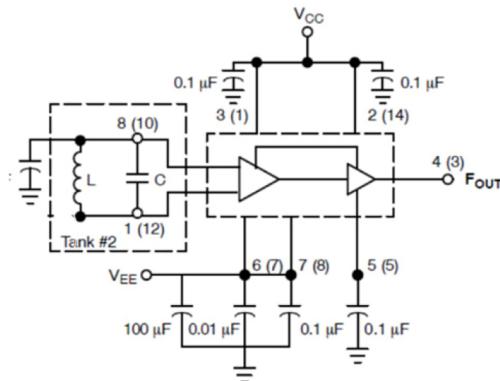


Figure 3.58. Design of an MC100EL1648 IC-based oscillator. Source: Motorola data sheet

To operate these circuits as voltage-controlled oscillators, the capacitance C of the “LC” tuning circuit simply needs to be replaced, either by a diode with variable capacitance or by two varactor diodes assembled in an antiparallel fashion and biased by a voltage external, as indicated in Figure 3.59.

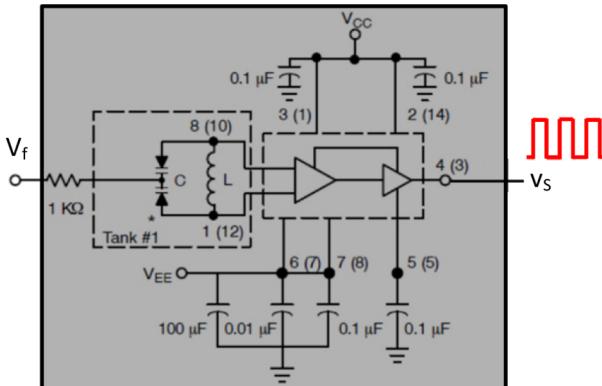


Figure 3.59. MC100EL1648-based VCO. Source: Motorola data sheet

3.6. Examples of integrated PLL

3.6.1. 4046 IC-based PLL

3.6.1.1. Overview

As we have seen, the PLL contains different kinds of circuits such as the phase comparator, the VCO and low-pass filter. Designing each circuit on their own and building a PLL by interconnecting the whole is a daunting task. Currently, there are phase-locked loops that virtually cover most of all useful frequency bandwidths that are in the form of integrated circuits. One of the most famous of these circuits is probably the 4046 integrated circuit. This circuit is widely used for educational purposes. The block diagram of the CMOS 4046 circuit (Figure 3.60) contains:

- a voltage-controlled oscillator (VCO);
- an exclusive-OR gate-based phase comparator (type-1);
- a type-2 phase comparator;
- a voltage follower and a Zener diode.

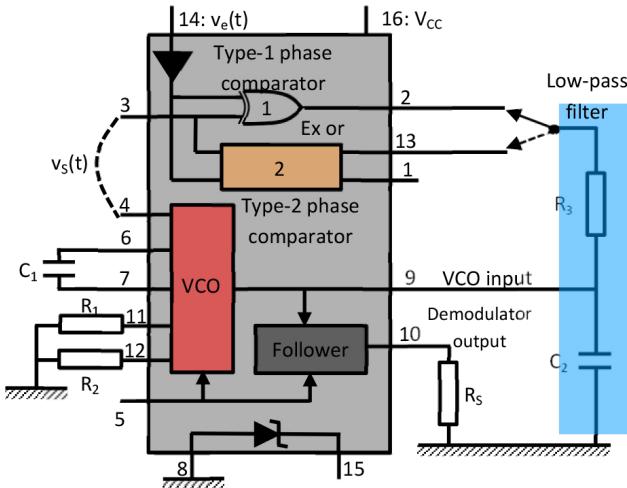


Figure 3.60. The 4046 IC and its block diagram. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

3.6.1.2. 4046 operation

a) The VCO

The frequency range of the output signal of the integrated VCO is imposed by the values of resistors R_1 and R_2 , capacitance C and voltage V_f applied to input “9” of the VCO. The voltage-controlled oscillator in the 4046 circuit is quite complex (see Figure 3.61).

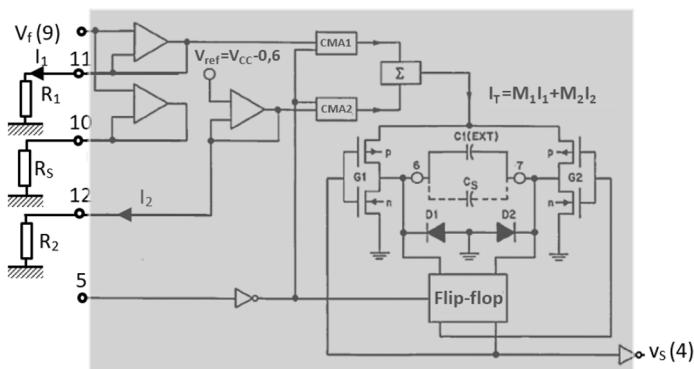


Figure 3.61. Schematic diagram of the voltage-controlled oscillator in the PLL based on the 4046 IC

Through the analysis of this circuit, it can be seen that resistors R_1 and R_2 produce currents I_1 and I_2 respectively. Current I_1 is proportional to voltage V_f that is applied to the VCO input (pin 9 of the 4046 and at the low-pass filter output). Current I_2 is proportional to V_{ref} .

$$V_{ref} = V_{CC} - 0.6 \text{ V}$$

After amplification by two differential current mirror amplifiers, currents I_1 and I_2 are added together to generate current I_T . This current I_T will charge capacitor C_{ext} through the conduction resistances of the MOS transistors. The voltage V_C at the terminals of capacitor C_{ext} can be written as follows:

$$V_C = \frac{1}{C_{ext}} \int_0^t I_T dt$$

The current I_T is constant at a certain time. As a result, the capacitor C_{ext} is charged by a constant current and the voltage at its terminals is a ramp:

$$V_C = \frac{1}{C_{ext}} I_T t$$

After a charging time T_1 (see Figure 3.62), the capacitor is instantly reset to start a new cycle.

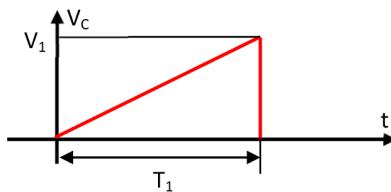


Figure 3.62. Voltage changes at the terminals of capacitor C_{ext} inserted at terminals 6 and 7 of the VCO integrated into the 4046 circuit

At the end of time T_1 , the voltage at the terminals of capacitor C_{ext} will have the value:

$$V_1 = \frac{1}{C_{ext}} I_T T_1$$

The VCO oscillation frequency is defined by

$$f_{osc} = \frac{1}{T_{osc}} \cong \frac{1}{2T_1}$$

It is obvious why the output frequency will depend on R_1 , R_2 and the capacitance value of capacitor C_{ext} . A number of disruptive parameters such as parasitic capacitances and propagation time have been omitted to simplify the explanation.

The calculation of T_1 requires a given number of steps and certain considerations. There is a certain complexity in detailing all of the calculation procedures that do not contribute with essential elements to the understanding of the subject being addressed. To avoid making this part even more cumbersome, we ignore these steps and introduce a number of practical equations to quickly and approximately define frequencies relatively to the VCO integrated into the 4046 circuit.

The minimal VCO frequency depends on resistor R_2 .

$$f_{min} \cong \frac{K_a}{R_2 C}$$

Since the current flowing through R_2 depends on the supply voltage V_{CC} , coefficient K_a also necessarily will.

The maximal VCO frequency is a function of the two resistors R_1 and R_2 .

$$f_{max} \cong \frac{K_a}{C} \left(\frac{1}{R_1} + \frac{1}{R_2} \right)$$

The output frequency of the VCO is a linear function of V_f :

$$f_s = f_{osc} \cong \frac{f_{max} - f_{min}}{K_b} V_f + f_{min}$$

Parameters K_a and K_b depend on the supply voltage. When choosing a power supply $V_{CC} = 6$ volts, it follows that:

$$K_a = 10$$

$$K_b = 5.4$$

The VCO output frequency can be expressed using the relation:

$$f_s = K_{VCO} \cdot V_f + f_{min}$$

For values of external components:

$$R_1 = 16 \text{ k}\Omega, R_2 = 35 \text{ k}\Omega \text{ and } C_{\text{ext}} = 2 \text{ nF}.$$

For the VCO coefficient transfer, the following estimate is obtained:

$$K_{\text{VCO}} = 9.6 \text{ kHz/volt}$$

b) Phase comparators

As we have already pointed out, the 4046 integrated circuit contains two types of phase comparators (see Figure 3.63).

Again, we can find the phase comparator based on “exclusive-OR” gates and the three-state and charge pump flip-flop phase comparator.

These two types of comparators have been respectively studied in sections 3.5.1.2.1 and 3.5.1.2.4.

In the “exclusive-OR” gate-based phase comparator, there is a certain ambiguity in the phase detection.

In effect, it is not possible to know whether the voltage at the output of the low-pass filter is relative to a phase variation smaller than π or if this phase variation is comprised between π and 2π . This ambiguity does not exist when using the type-2 phase detector of the 4046 circuit. Its dynamic ranges from 0 to 2π . This is possible because the triggering is carried out on rising or falling edges only.

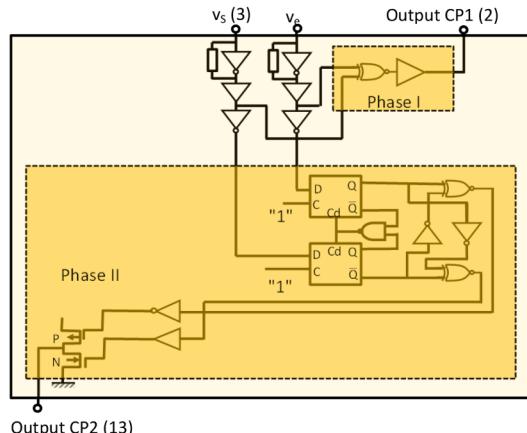


Figure 3.63. Schematic diagram of the two types of 4046 phase comparators.
For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

3.6.2. The 565 and 567 IC-based PLL

3.6.2.1. Overview

The 565 and 567 PLL circuits belong to the same series. These circuits differ only in the frequency range that they cover. We will more particularly focus on the 565 PLL circuit because it is the most popular and most widely used of the series.

The 565 integrated circuit is available in two different casings. The 14-pin DIL (dual in-line) type of casing is presented in Figure 3.64a. The cylindrical-shaped metal case with 10 pins is presented in Figure 3.64b.

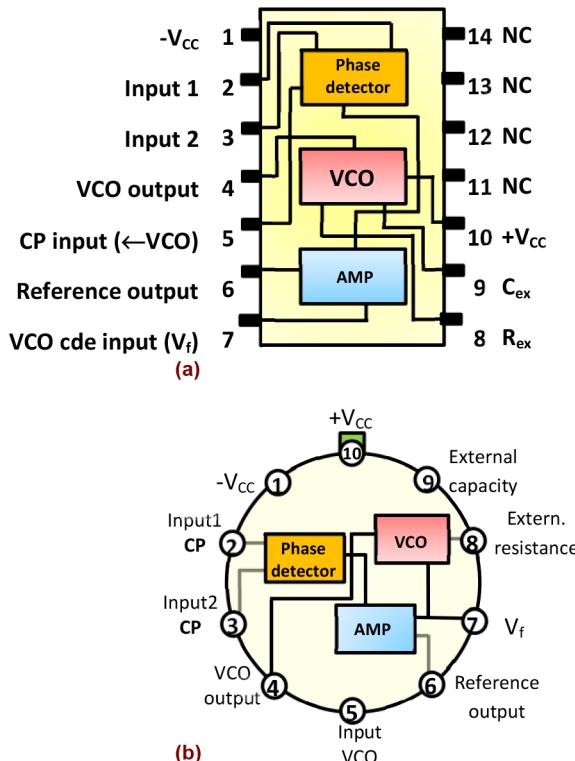


Figure 3.64. 565 PLL circuit in 14-pin DIL casing (a) and in 10-pin cylindrical-shape metal case (b). For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

The analysis of the block diagram of the 565 PLL circuit of Figure 3.65 shows the presence of a phase detector, a voltage-controlled oscillator and an amplifier. The amplifier and the voltage-controlled oscillator are partially internally connected.

The 565 integrated PLL has a very stable natural frequency f_0 . This phase-locked loop can be used over a wide frequency range from a few tens of hertz up to more than 500 kHz. The VCO output generates a square-shaped voltage and may be TTL (transistor-transistor-logic) compatible. This circuit makes use of a dual power supply but can also operate with a simple power supply.

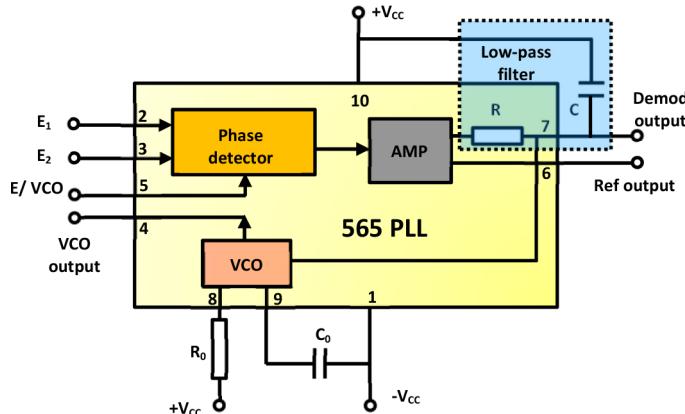


Figure 3.65. Block diagram of the 565 integrated PLL. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

Phase comparator inputs are referenced (2), (3) and (5). When pins (4) and (5) are short-circuited, the VCO output is directly connected to the input of the phase comparator. The phase comparator output is amplified by the integrated amplifier inside the PLL. The output voltage of this amplifier is either present at pin (6) or pin (7) via an integrated resistance $R = 3.6 \text{ k}\Omega$.

To implement the low-pass filter for the average value of the signal delivered from the output of the phase comparator after amplification, a capacitor C just needs to be connected between pins (7) and (10). This capacitor C will form with resistance R the necessary low-pass filter.

The filtered voltage that can be found at pin (7) is internally connected to the input of the voltage-controlled oscillator (VCO) integrated at the 565 circuit-based PLL level.

The natural free operating frequency of the VCO (lack of control voltage) linked to the 565 PLL is determined by the relation:

$$f_0 = \frac{0.3}{R_0 C_0} \text{ (Hz)}$$

Resistance R_0 and capacitor C_0 are external components that are respectively connected to pins (8) and (9) in order to set the idle frequency of the VCO. To properly operate, it would be necessary that resistance R_0 be not too large and not too small either. A compromise consists of choosing a value in general between 2 and 20 k Ω for R_0 .

The VCO frequency variation of the 565 PLL is obtained by means of injecting a signal V_f at input 7. In reality, this voltage V_f comes from the low-pass filtering of the signal originating from the phase comparator. The transfer function of the VCO integrated into the 565 PLL circuit is schematically presented in Figure 3.66

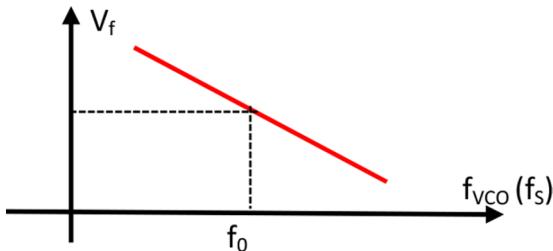


Figure 3.66. 565 PLL circuit VCO transfer characteristic

It can be seen that the slope K_{VCO} of the VCO transfer curve is negative. This has implications on how to use the phase comparator. The output frequency can be defined using the expression:

$$f_s = f_0 + K_{VCO}(V_f - V_{VCO})$$

The frequency variation of the output signal can also be obtained by adjusting the value of components R_0 and C_0 .

The phase comparator of the 565 IC-based PLL is designed around an exclusive-OR logic gate. Let us recall that the transfer function of the phase comparator is shown in Figure 3.67.

To compensate for the negative sign introduced in the VCO transfer function, we use the response curve of the phase comparator in the portion where its slope is negative as shown in Figure 3.67. This will provide the transfer coefficient K_D of the phase comparator, which will be negative.

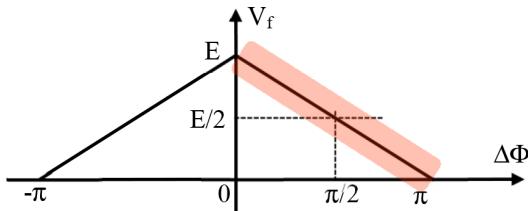


Figure 3.67. The phase comparator transfer characteristic being used in the portion where its slope is negative

In fact, we have the loop gain:

$$K = K_D \cdot K_{VCO} > 0$$

The coefficient K_D is expressed in volts/radian:

$$K_D = \frac{V_r}{\varphi_e(t) - \varphi_s(t)}$$

and K_{VCO} is expressed in (radians/second).volts.

In general, the loop gain is a function of the VCO natural frequency and the global supply voltage V_{CC} of the 565 PLL circuit.

$$K = \frac{33,6f_0}{V_{CC}}$$

The locking range of the 565 PLL is in relation to the idle VCO frequency. It is generally estimated by the relation:

$$\Delta f_{ver} = \frac{16f_0}{V_{CC}}$$

3.7. PLL block diagram

It should be noted that the PLL is a loop system. With a view to identifying the performance of this device, we represent it in the form of a block diagram. It is important to remember that the PLL is a nonlinear system. Nevertheless, solutions can be found to study the PLL using a block diagram, assuming that the PLL is already locked (quasi-stationary state) and by adopting a number of compromises regarding the phase comparator. Therefore, a PLL can be schematically presented by the block diagram in Figure 3.68 and using phase quantities.

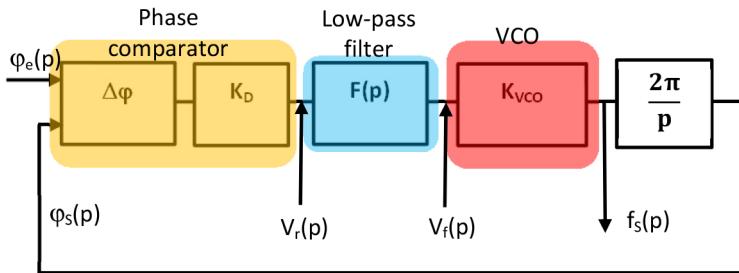


Figure 3.68. Block diagram of a PLL in terms of phase. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

Since we are working with phases and given that the VCO output is a signal whose variable element is a frequency, it is necessary to add the $2\pi/p$ block because we must remember that the frequency is derived from a phase. Hence, there is the need to add a $2\pi/p$ block for shifting from frequency processing to phase processing. In effect, we have:

$$\varphi_s(t) = \int_0^t \omega_s(t) dt$$

$$\varphi_s(p) = \frac{\omega_s(p)}{p} = \frac{2\pi}{p} f_s(p)$$

The low-pass filter is a passive linear system in general which has a transfer function $F(p)$.

With:

$$F(p) = \frac{V_f(p)}{V_r(p)}$$

The slope K_{VCO} of the VCO is expressed in Hz/Volt. It is defined by means of the following expression:

$$K_{VCO} = \frac{df_s(p)}{dV_f} = \frac{F_{\max} - F_{\min}}{V_{f\max} - V_{f\min}}$$

K_D is the transfer coefficient of the phase comparator. It is expressed in V/rads

$$K_D = \frac{dV_r}{d\varphi}$$

When the PLL is to be represented as a block diagram in terms of frequencies as indicated in Figure 3.69, a few changes are introduced with regard to the block diagram in terms of phase.

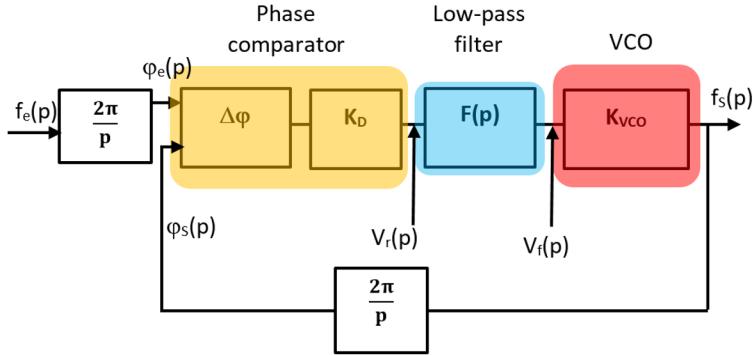


Figure 3.69. PLL block diagram; the input and output quantities are frequencies.
For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The block diagram in Figure 3.69 can be transformed into a somewhat simpler diagram by introducing a unity feedback loop (see Figure 3.70).

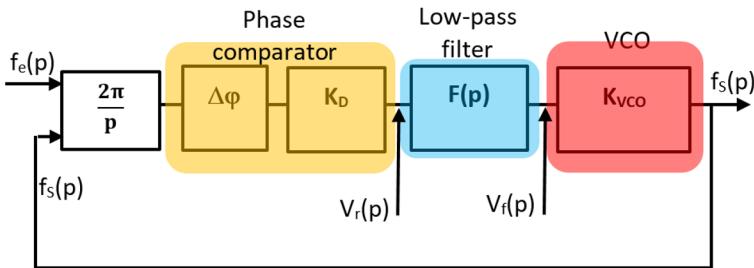


Figure 3.70. PLL block diagram in terms of frequency with unity feedback.
For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

3.8. Study of the behavior of a PLL

3.8.1. PLL transfer function

Based on the block diagram, it is possible to carry out the study of the behavior of a PLL as a controlled (servo) system. The behavior of the PLL can thus be predicted for a given excitation.

For this purpose, it is important to determine the transfer function of the PLL and analyze existing situations (nature of the excitement, nature of the filter and nature of the phase comparator).

As we have previously demonstrated, several types of transfer functions can be defined relatively to a PLL.

In the cases that we are focusing on, we only address the transfer function related to the relation between input and output phases or related to the relation between input and output frequencies.

For the study of the behavior of the PLL, most will be reduced to one of these two transfer functions.

It should be reminded that the transfer function of a negative feedback loop system is given by the relation:

$$H(p) = \frac{H_0(p).B(p)}{1+H_0(p).B(p)}$$

For simplification purposes, we will address a unity-feedback phase-locked loop, which gives:

$$B(p) = 1$$

The PLL transfer function is thus reduced to the relation:

$$H(p) = \frac{H_0(p)}{1+H_0(p)}$$

It should also be recalled that $H_0(p)$ is the transfer function of the direct channel or open-loop transfer function.

When analyzing the diagrams in Figure 3.71, it can be inferred that the PLL open-loop transfer function is none other than:

$$H_0(p) = 2\pi.K_D.K_{VC0}.F(p)/p$$

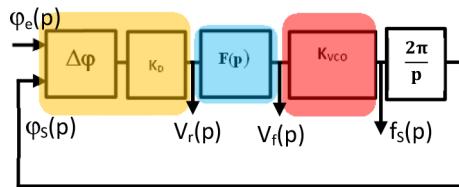


Figure 3.71. Diagram for the determination of the transfer function. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The PLL closed-loop transfer function is defined by:

$$H(p) = \frac{2\pi K_D K_{VCO} F(p)}{p + 2\pi K_D K_{VCO} F(p)}$$

3.8.2. Behavior of the PLL according to filter type

3.8.2.1. Passive low-pass RC filter

The low-pass filter used for this first study is presented in Figure 3.72. The transfer function of this filter is given by:

$$F(p) = \frac{1}{1 + RCp} = \frac{1}{1 + \tau p}$$

It should be noted that this filter only has a single pole.

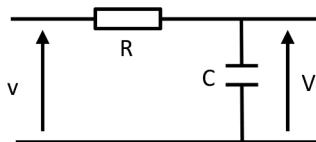


Figure 3.72. Low-pass filter utilized in the phase-locked loop

When integrating the low-pass filter transfer function into the transfer function of the closed-loop PLL, the following relation is obtained:

$$H(p) = \frac{2\pi K_D K_{VCO} \left(\frac{1}{1 + \tau p} \right)}{p + 2\pi K_D K_{VCO} \frac{1}{1 + \tau p}}$$

Finally:

$$H(p) = \frac{2\pi K_D K_{VCO}}{\tau p^2 + p + 2\pi K_D K_{VCO}}$$

It can be noted that when utilizing a first-order low-pass filter in the loop, the closed-loop transfer function of the PLL is that of a second-order system.

In the study of this particular case, the behavior and characteristics of the PLL, such as stability, response time and bandwidth, will depend on the choice of low-pass filter, which is inserted in the loop. To show this, we study the parameters involved in the transfer function. Therefore, we rewrite the transfer function in the following form:

$$H(p) = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

By identification, it can be deduced that:

$$2\zeta\omega_n = \frac{1}{\tau}; \omega_n^2 = \frac{2\pi K_D K_{VCO}}{\tau} \text{ and } \zeta = \frac{1}{2\sqrt{2\pi K_D K_{VCO}\tau}}$$

We use the transfer function $H(p)$ to analyze the behavior of the PLL. We have the parameter ζ that represents the damping and ω_n that represents the bandwidth or critical frequency. For a phase-locked loop, we obviously look for the stability of the loop and also a quick response (a minimal response time).

3.8.2.2. Stability and phase margin

When using an R-C-type of low-pass filter, the time constant τ will be chosen to have a suitable damping factor such that the overflow is minimal and thus to have a good phase margin to ensure the stability of the phase-locked loop (PLL). It is recalled here that a loop system is stable when we have a positive phase margin M_ϕ . The principle of the calculation of the phase margin can be established as follows:

The expression is defined in the Laplace domain of the open-loop transfer function of the PLL $H_0(p)$. We then replace p by $j\omega$. We plot the modulus and phase Bode diagram. The equation $|H_0(j\omega)| = 1$ is either analytically or graphically solved to find the solution of this equation represented by the pulse $\omega = \omega_\phi$. The phase margin is expressed using the relation:

$$M_\phi = 180^\circ + \text{Arg}(H_0(j\omega_\phi))$$

We remember that the filter cutoff frequency is:

$$F_C = \frac{\omega_C}{2\pi} = \frac{1}{2\pi\tau}$$

The parameter “ τ ” affects the capture range. It is important that the cutoff frequency “ F_C ” of the filter be able to maintain the capture range of the PLL lower than the locking range. Without this point, the PLL will not be capable of tracking. To provide further details about the study of the behavior of the PLL, it is necessary to draw the Bode diagram of the transfer function of the open-loop PLL. For this purpose, it should be recalled that the open-loop transfer function is given by:

$$H_0(p) = 2\pi K_D K_{VCO} F(p)/p$$

$$H_0(p) = \frac{2\pi K_D K_{VCO}}{p(1 + \tau p)}$$

With sinusoidal waves, we have:

$$H_0(j\omega) = \frac{2\pi K_D K_{VCO}}{j\omega(1 + j\omega\tau)} \Rightarrow |H_0(j\omega)| = 2\pi \sqrt{\frac{(K_D K_{VCO})^2}{\omega^2(1 + (\omega\tau)^2)}}$$

$$|H_0(j\omega)| = 2\pi \sqrt{\frac{\tau^2 (K_D K_{VCO})^2}{\tau^2 \omega^2 (1 + (\omega\tau)^2)}} = 2\pi \frac{K_D K_{VCO} \tau}{\sqrt{\frac{\omega^2}{\omega_C^2} \left[1 + \frac{\omega^2}{\omega_C^2} \right]}}$$

$$|H_0(j\omega)|_{dB} = 20 \cdot \log(2\pi K_D K_{VCO} \tau) - 20 \log\left(\frac{\omega}{\omega_C}\right) - 10 \log\left(1 + \frac{\omega^2}{\omega_C^2}\right)$$

For the phase, it follows that:

$$\text{Arg}(H_0(j\omega)) = \frac{-\pi}{2} - \text{Arctg}\left(\frac{\omega}{\omega_C}\right)$$

The asymptotic representation of the Bode plot yields:

$$\omega \ll \omega_C :$$

$$|H_0(j\omega)|_{dB} = 20 \cdot \log(2\pi K_D K_{VCO} \tau) - 20 \log\left(\frac{\omega}{\omega_C}\right)$$

$$\text{Arg}(H_0(j\omega)) = \frac{-\pi}{2}$$

$\omega >> \omega_C$:

$$|H_0(j\omega)|_{\text{dB}} = 20 \cdot \log(2\pi K_D K_{VCO} \tau) - 40 \log\left(\frac{\omega}{\omega_C}\right)$$

$$\text{Arg}(H_0(j\omega)) = \pi$$

The graph that represents the Bode plot (modulus and phase) of the open-loop transfer function is schematically presented in Figure 3.73.

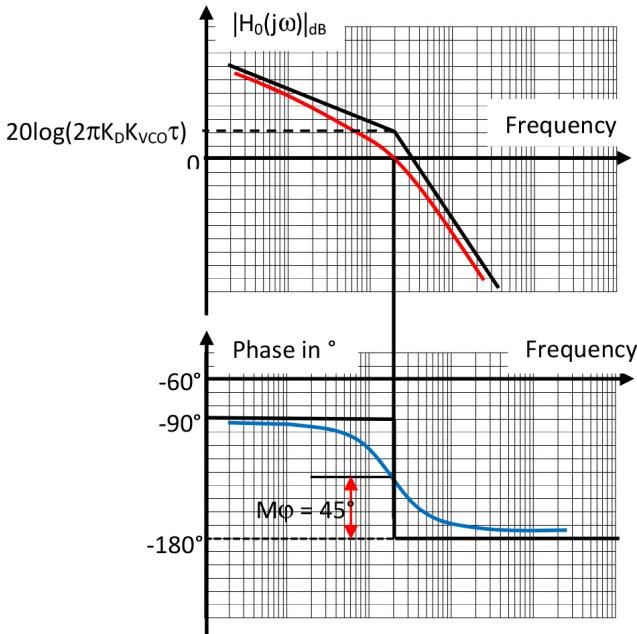


Figure 3.73. Bode plot of the open-loop transfer function of the PLL with a first-order low-pass RC-type loop filter. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The modulus of the open-loop gain is equal to 1 for a specific pulse ω_ϕ :

$$\omega_\phi^2 = \frac{\sqrt{1 + (4\pi^2 \tau^2 K_D^2 K_{VCO}^2)} - 1}{2\tau^2}$$

The negative solution is to be rejected.

The phase margin is 45° when the product “ $2\pi K_D K_{VCO} \tau$ ” is equal to 1. The phase margin changes with the product $K_D K_{VCO} \tau$ (see Figures 3.74(a–c)).

In order for the phase margin to be above 45° to ensure a very good stability to the phase-locked loop (phase margin greater than 45°), it would be necessary that the term $2\pi K_D K_{VCO} \tau < 1$.

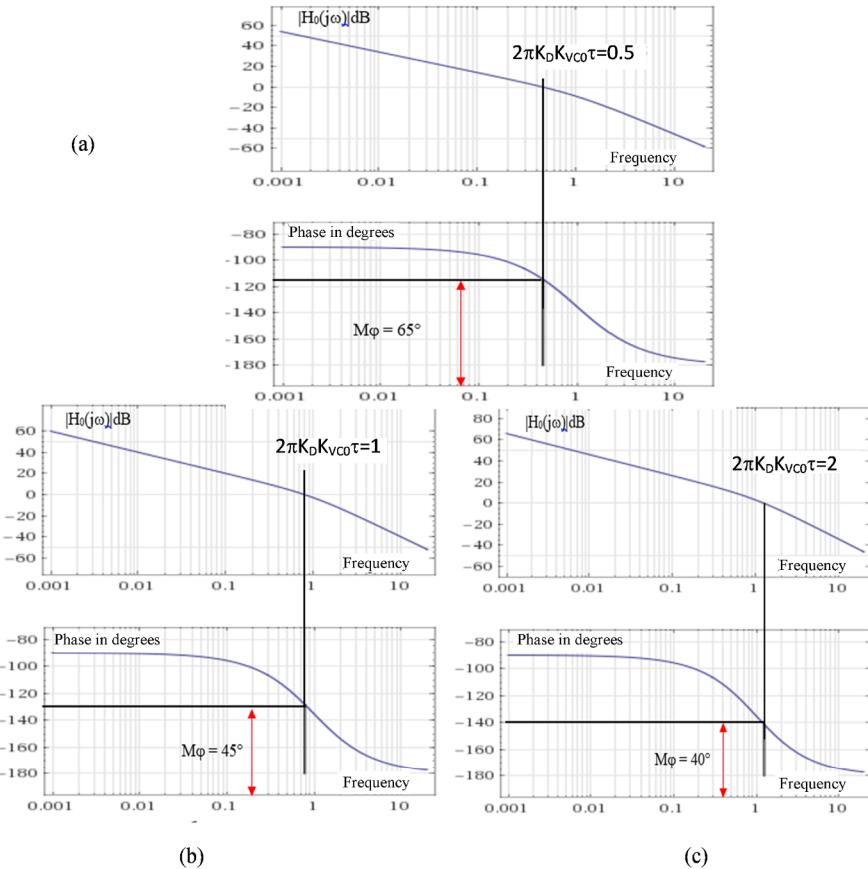


Figure 3.74. Evolution of the phase margin according to the parameter $K_D K_{VCO} \tau$

However, despite the fact that the PLL has a positive phase margin, it has a poor degree of stability.

3.8.2.3. PLL stability and step response

The step response of a PLL consists of injecting a frequency step $f_e(p) = \Delta F_e/p$. The choice of the filter is important in the study of the stability.

To understand this aspect of excitation, consider the case of an FSK demodulation (for frequency shift keying demodulation). More precisely, the frequency of an FSK-modulated signal abruptly changes from a frequency f_{e1} (logic level “0”) to a frequency f_{e2} (logic level “1”). Normally, the frequency of the VCO output signal must follow the frequency of the input signal and we will have the frequency of the output signal that will shift from a frequency $f_{s1} = f_{e1}$ to a frequency $f_{s2} = f_{e2}$. This can only be achieved on the condition that specific constraints are followed.

It should be noted that the transfer function of the phase-locked loop, when utilizing a first-order low-pass filter, which has the transfer function $F(p) = (1/(1+\tau p))$, is given by:

$$H(p) = \frac{f_s(p)}{f_e(p)} = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

$$2\zeta\omega_n = \frac{1}{\tau}$$

$$\omega_n^2 = \frac{2\pi K_D K_{VCO}}{\tau}$$

$$\zeta = \frac{1}{2\sqrt{2\pi K_D K_{VCO}\tau}}$$

$$\tau = RC.$$

The expression in the Laplace domain of the output signal frequency is:

$$f_s(p) = f_e(p) \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}; f_e(p) = \Delta F_e/p$$

$$f_s(p) = \Delta F_e(p) \frac{\omega_n^2}{p(p^2 + 2\zeta\omega_n p + \omega_n^2)}$$

When $\zeta > 1$, an aperiodic answer will be obtained, and this response from the PLL may happen to be too slow. This means that the output of the phase-locked loop might not be able to follow the variations that occur at the input of the PLL.

We thus consider the case where $\zeta < 1$ to obtain a phase-locked loop fast enough such that the output signal is able to follow changes relative to the PLL input signal.

The expression in the time domain of the output signal frequency when $\zeta < 1$ is oscillating is:

$$f_s(t) = \Delta F_e \left[1 + \frac{1}{(1-\zeta^2)^{\frac{1}{2}}} e^{-\zeta \omega_n t} \sin(\omega_n ((1-\zeta^2)^{\frac{1}{2}}) t + \phi) \right]$$

$$\phi = \arctg\left(\frac{(1+\zeta^2)^{\frac{1}{2}}}{-\zeta}\right)$$

The significance of this oscillation will depend on the damping factor (Figure 3.75).

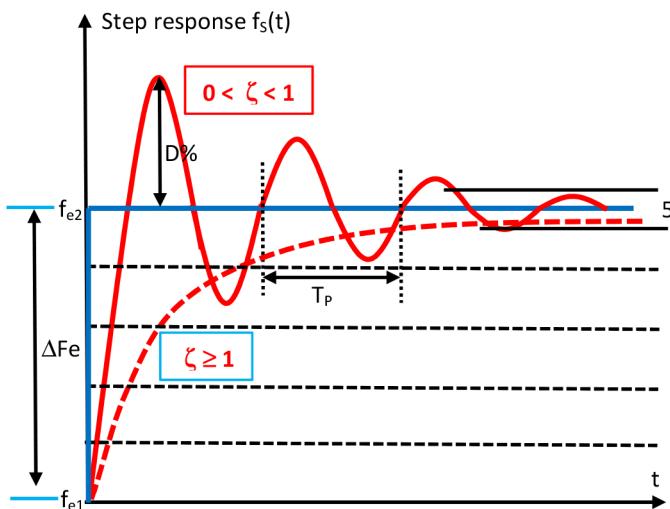


Figure 3.75. Second-order system step response. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

When the damping factor is less than 1, it is clearly visible that we have an oscillatory response. The overshoot is a function of the damping coefficient.

If ζ tends to 0, the overshoot tends towards 100%, the 5% response time tends to infinity and the loop is completely unstable.

If $\zeta \geq 1$, the overshoot is zero but the 5% response time is long.

The goal is to have a stable loop and also minimal response time. For this purpose in most cases, we choose a damping coefficient ζ usually comprised between 0.4 and 0.7. This is indeed a good compromise:

$$0.4 < \zeta < 0.7 \Rightarrow 4.6\% < D < 25.8\%$$

The response time is minimal for $\zeta = 0.7$ (see graph of Figure 3.76). There is however a rather significant overshoot ($D \cong 25\%$).

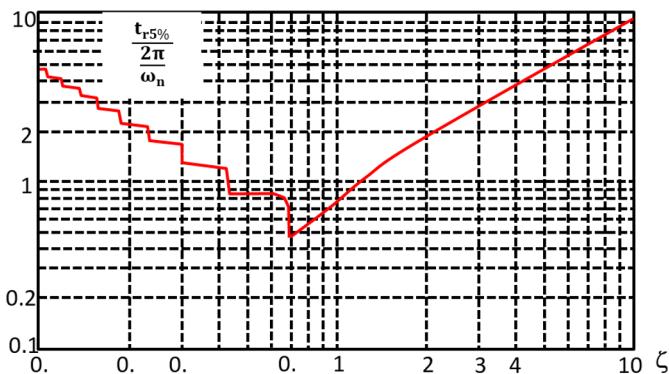


Figure 3.76. Response time of a second-order system according to the damping factor

There is obviously a relation between the phase margin and the amortization factor. To increase the influence of the phase margin on stability and the behavior of a phase-locked loop and its interaction with the damping factor, the step response of the PLL simply has to be analyzed for different values of phase margin (see Figure 3.77). It can be clearly seen that when the phase margin is less than 15° , there are risks that the PLL will become unstable. Therefore, there is a high risk of dropping out of lock.

On the other hand, if the phase margin is too significant ($M\varphi > 100^\circ$), the PLL is too slow. There is a risk that it will not track and lock. Thereby, a compromise is necessary. A good compromise situates the phase margin between 15° and 50° .

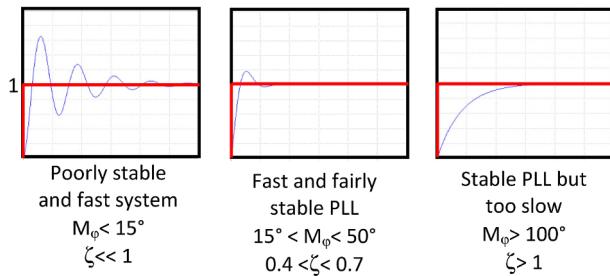


Figure 3.77. Evolution of a PLL step response according to the phase margin M_ϕ and the damping coefficient. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

3.9. Applications for PLLs

The development of the phase-locked loop (PLL) is, as we have seen, related to the issue of amplitude modulation and demodulation. In fact, in 1932, Henri de Bellescize, an engineer, wanted to reconstitute a synchronous signal from the modulated signal. He implemented a loop system that ensured frequency or phase servo control. This aspect would allow us to lock a signal to a certain input frequency.

This thus helped to implement the process that is the phase-locked loop and whose applications have enormously diversified. Two main categories of applications can be distinguished:

- the usage of the PLL in the field of very narrow bandpass filtering, for instance, for recovering a carrier signal hidden in noise;
- utilization of the phase-locked loop as a frequency multiplier.

It is important to point out that the PLL makes it possible to produce signals of very stable frequencies, varying by steps, which are necessary in telecommunications systems. It can provide on output a signal having the stability of quartz but the frequency can be varied according to the user's choice.

The best-known and most interesting applications include:

- frequency multiplication;
- frequency synthesis;
- frequency modulation;
- amplitude and frequency demodulation.

3.9.1. Frequency multiplication

3.9.1.1. Principle

It is very easy to divide the frequency of a signal using digital circuits. However, it proves very difficult to multiply the frequency of a signal. The use of flip-flops as in the division case does not contribute any solution. In order to be able to increase the frequency of a signal, it has to be distorted and filtered to only allow the harmonic “n” that we intend to keep. This signal should then be amplified. This is not an easy task, especially in the presence of high-frequency signals.

With a PLL, the problem is greatly simplified. The synoptic diagram of the circuit for frequency multiplication is shown in Figure 3.78.

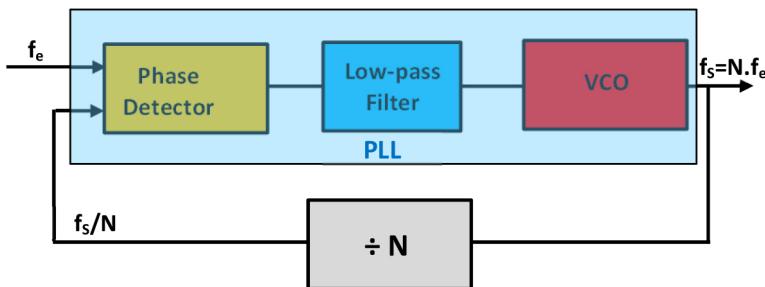


Figure 3.78. Principle of PLL-based frequency multiplying. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

A frequency divider is inserted between the voltage-controlled oscillator (VCO) and the phase comparator. As a result, the output frequency of the VCO is divided using integer-N division.

The signals that are applied at the phase comparator input are f_e and f_s/N .

When the loop is locked, it will follow that:

$$f_e = \frac{f_s}{N}$$

$$f_s = N \cdot f_e$$

The output signal frequency is N times the frequency of the input signal.

3.9.1.2. Frequency multiplier practical example

A practical example of a frequency multiplier based on the 565 IC PLL circuit is presented in Figure 3.79.

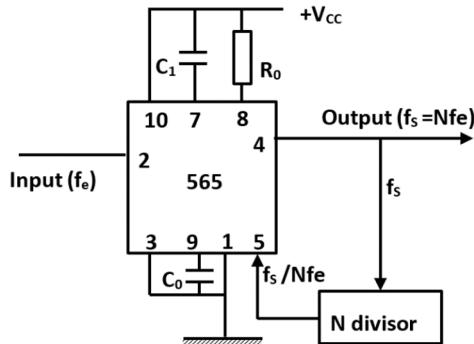


Figure 3.79. Implementation example of a frequency multiplication circuit based on an integrated PLL

The divider-by-N can be a preset or programmable divider. Within this context, a counter can be used to perform this division such as, for example, the CMOS 4020, 4040 or 4060 circuits with which N ratios can be obtained ranging from 2 up to 32. TTL circuits can also be used, such as, for instance, the 7490 counter, which can enable ratios ranging from 2 to 10.

The operation of this 565 PLL circuit-based frequency multiplier is explained as follows.

The input signal is applied to one of the inputs of the phase comparator integrated in the 565 (input 2). The output of the VCO signal is applied after amplification and division at the second input. The VCO natural frequency is imposed by the circuit composed of the external resistance R_0 and capacitor C_0 . It is clearly visible that resistance R_0 is connected to the power supply and capacitor C_0 is connected to ground. Capacitor C_1 and the internal resistance of the 565 circuit will operate as a low-pass filter for the output signal of the phase comparator. The value of the internal resistance is equal to $3.6\text{ k}\Omega$.

The VCO output frequency will be variable depending on the value of the filtered voltage that is internally applied to the 565 PLL. This filtered voltage may be available at the level of pin (7) of the 565. When locking, we thus have $f_s = Nf_e$. When the frequency of the input signal varies in the proportions of the PLL locking band, the output frequency will follow it but with a multiplication factor equal to N .

3.9.2. Frequency synthesis

From a reference signal, frequency synthesis allows us to generate a signal that can have a variable frequency over a wide range. The need to generate a signal with a frequency different from that of the reference signal is very important at the telecommunication or signal transmission levels, for example.

The PLL is widely used to meet this need. It should be noted that it is very difficult to achieve a variable frequency oscillator with a satisfactory stability. There are always drifts related to various problems. The main source of these drifts is undoubtedly temperature. The utilization of servo systems (PLL) making use of a stable reference (e.g. a quartz oscillator) makes it possible to effectively solve the issues related to drifts that occur. Frequency synthesis derives from frequency multiplication except that the divisor that is inserted between the VCO and the phase comparator is programmable according to the user's will. To obtain more manageability, it is also possible to insert another frequency divider between the reference signal and the comparator phase, as indicated in Figure 3.80.

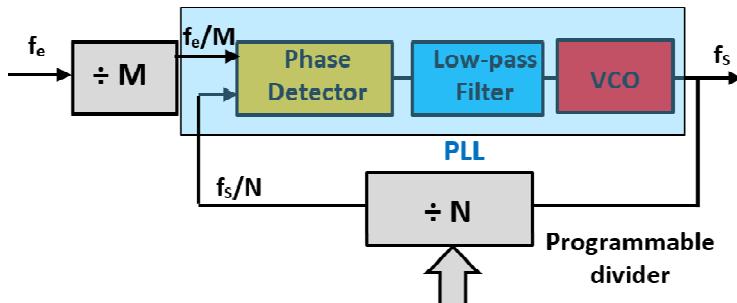


Figure 3.80. Principle of frequency synthesis using a PLL. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The phase comparator receives at its respective inputs signals of frequencies f_e/M and f_s/N , with the numbers N and M being integers. N is a programmable coefficient.

When the PLL is locked, we have:

$$\frac{f_e}{M} = \frac{f_s}{N}$$

The result is an output frequency, which will have the expression:

$$f_s = N \cdot \frac{f_e}{M}$$

To show the interest of this application, it is assumed that a reference frequency $f_e = 10$ MHz is available and that we want to produce on output all the frequencies ranging from 88 to 108 MHz. To this end, we simply define the coefficient $M = 10$ and need to have a coefficient N programmable in increments of 1 ranging from 88 to 108. This will enable on output all frequencies: $f_{s1} = 88$ MHz, $f_{s2} = 89$ MHz up to $f_{s21} = 108$ MHz.

3.9.3. Frequency modulation and demodulation

3.9.3.1. Frequency modulation principle

In general, in signal transmission, the useful signal $s(t)$ to be transmitted is a low-frequency signal (modulating signal). To transmit this signal, we resort to a carrier signal, which has a high frequency. When the useful information is carried by variations in the carrier frequency, this is referred to as frequency modulation. The carrier is a sinusoidal signal. It is expressed using the relation:

$$v_p(t) = V_0 \cdot \cos(\theta)$$

with V_0 : carrier amplitude.

$$\theta = \int_0^t \omega_p dt \text{ and } \omega_p = 2\pi f_p$$

For frequency modulation, the frequency f (or angular frequency ω) of the modulated signal linearly varies with the amplitude of the modulating signal $s(t)$.

$$\omega = \omega_p + 2k\pi s(t)$$

The expression of the frequency-modulated (FM) signal is given by:

$$v_{FM}(t) = V_0 \cdot \cos(\theta_1)$$

with:

$$\theta_1 = \int_0^t \omega(t) dt = \int_0^t (\omega_p + 2k\pi s(t)) dt$$

Finally, the FM signal will have the general expression:

$$v_{FM} = V_0 \cos \left[\int_0^t (\omega_p + 2k\pi s(t)) dt \right]$$

The carrier frequency f_p ($\omega_p = 2\pi f_p$) is constant:

$$v_{FM} = V_0 \cos \left[\omega_p t + \int_0^t 2k\pi s(t) dt \right]$$

3.9.3.2. Frequency modulation circuit based on a PLL

The circuit that is to be designed from a PLL must produce a frequency-modulated output signal (see the synoptic diagram in Figure 3.81).

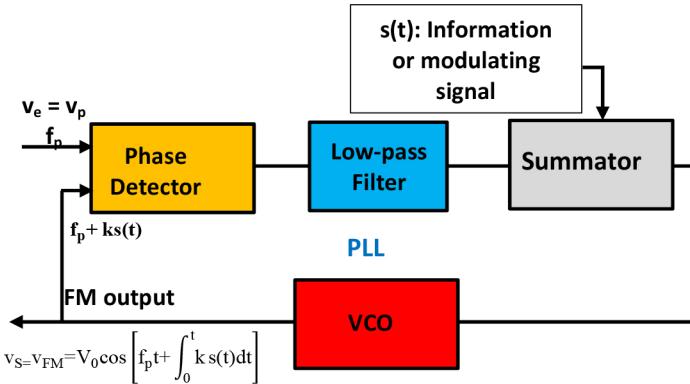


Figure 3.81. Frequency modulation using a PLL circuit. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

The use of a PLL and adding a summator circuit enables a frequency-modulated signal to be obtained. When the carrier frequency falls within the capture range of the PLL, the latter is locked and the output frequency in the absence of a modulating signal will be equal to the carrier frequency.

When the signal modulator is added to the signal related to the phase error, the output of the voltage-controlled oscillator will vary at the rate of this modulating signal around the carrier frequency.

As we have pointed out, the modulating signal is a low-frequency signal. The PLL is very effective to ensure frequency modulation provided that the modulating signal is not too fast. Conversely, the PLL may not follow.

3.9.3.3. Frequency demodulation

Frequency demodulation consists of recovering the signal that carries the information or modulating signal that is carried by the variations of the carrier frequency. To this end, we make use of the synoptic diagram, based on a PLL, in Figure 3.82.

In a transmission, the FM signal picked by the receiver is applied to the PLL input. It then locks up and follows changes in frequency due to modulation.

The low-pass filter is calculated to let through the frequencies of the modulating signal. As such, the signal $s(t)$ is collected (low-pass filter output), which is the image of the initial modulating signal.

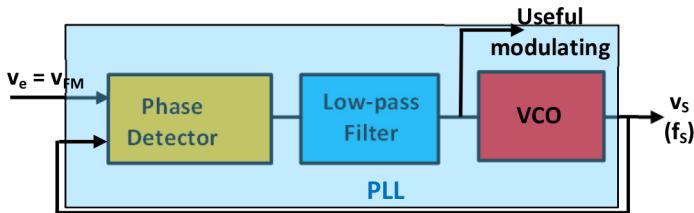


Figure 3.82. Frequency demodulation principle. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

It should be noted here that there are other methods to ensure frequency demodulation that naturally do not rely on PLL circuits. Their effectiveness is nevertheless reduced.

3.9.4. Frequency hopping-based or FSK (frequency shift keying) demodulation

3.9.4.1. FSK modulation principle

Frequency hopping-based modulation can be considered to be a special case of frequency modulation. In analog frequency modulation, the variation of frequency of the modulated signal is continuous at the rate of the analog signal. In frequency-hopping modulation, the modulating signal is a digital signal. The carrier is a high-frequency sinusoidal signal. Its frequency will vary by hops according to the binary value of the digital signal.

When, for example, considering a dual-state digital signal of the NRZ-type (no return to zero), the modulated signal will have a frequency f_1 for the high state and frequency f_2 for the low state.

An example of dual-state FSK modulation is presented in Figure 3.83a.

There are many possibilities to achieve this type of modulation. It is, for example, possible to use two oscillators that can be alternately switched by a control responsive to the bit levels of the digital signal.

A more attractive alternative is the use of a VCO (Figure 3.83b) that will be controlled by the modulating signal.

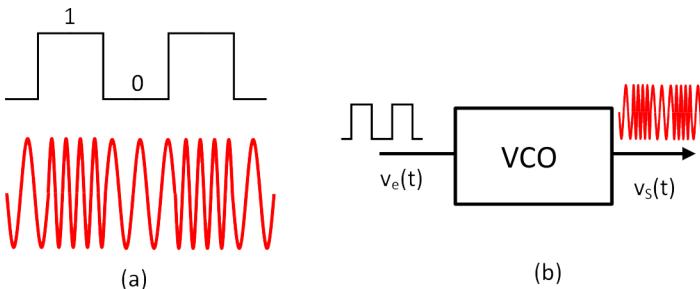


Figure 3.83. (a) Principle of FSK modulation; (b) production of an FSK-modulated wave

The signal at the VCO output will have the expression:

$$v_s(t) = V_0 \cos(2\pi f_1 t) \text{ when the input is in high state}$$

with $f_1 = f_p + \Delta f$, where f_p and V_0 are respectively the carrier frequency and amplitude and $+\Delta f$ represents the deviation of the frequency with respect to the carrier relative to the presence of a high state at the VCO input.

$$v_s(t) = V_0 \cos(2\pi f_2 t) \text{ when the input is in low state}$$

with $f_2 = f_p - \Delta f$ and $-\Delta f$ represents the negative frequency deviation with respect to the carrier that represents the presence of a low state at the VCO input.

To present FSK modulation, we chose the binary version or BFSK. There are of course more extensive modulations such as the 4FSK with which it will be necessary to code 4 symbols (00, 01, 10 and 11).

BFSK and 4FSK are variants of MFSK modulation in which M symbols will have to be coded.

3.9.4.2. FSK demodulation

The principle of FSK demodulation is presented in Figure 3.84. The FSK signal is applied to one of the two phase comparator inputs. The second input is driven by the VCO output signal. At the phase comparator output, a signal proportional to the frequency hop of the FSK signal is retrieved.

Amplification is necessary for boosting the digital signal for proper use.

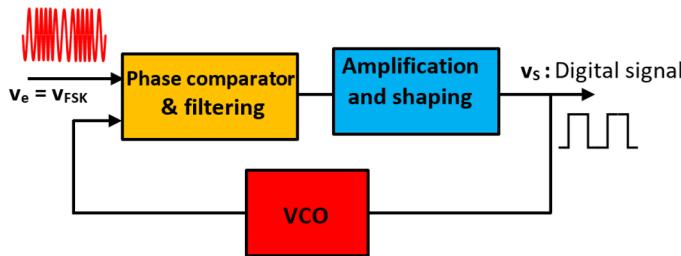


Figure 3.84. FSK demodulation principle. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

3.9.4.3. 4046 PLL-based FSK demodulation and modulation

The analysis of the synoptic diagram in Figure 3.85 shows that the phase-locked loop (PLL) based on the 4046 integrated circuit only needs an external low-pass filter to achieve the desirable operations of FSK modulation and demodulation.

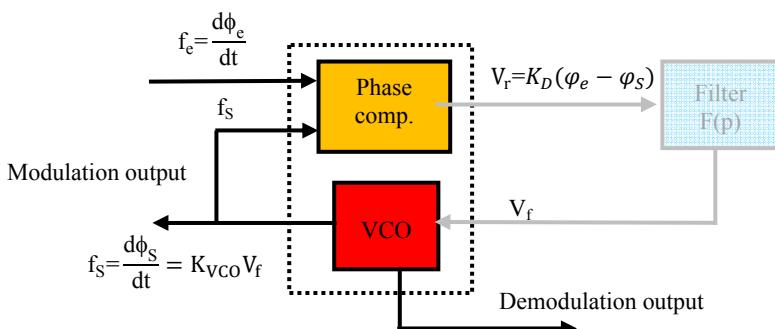


Figure 3.85. 4046 IC-based FSK modulation and demodulation. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

For FSK modulation, only the VCO is used. The VCO natural frequency is imposed by external components. The VCO frequency variation range for FSK modulation ($f_0 + \Delta f$ and $f_0 - \Delta f$) is related to the digital modulating signal. A simplified diagram of an FSK modulator based on the 4046 PLL circuit is shown in Figure 3.86.

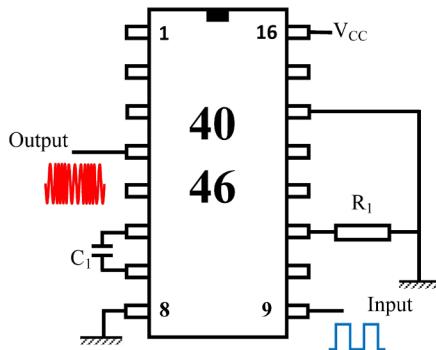


Figure 3.86. 4046 circuit-based FSK modulator

For the FSK demodulation, all the elements of the PLL are required, including the low-pass filter external to the 4046 IC. The capture range of the PLL operating in closed loop will depend on the characteristics of the external low-pass filter when utilizing the type-1 phase comparator (based on an exclusive-OR logical gate).

When utilizing the type-2 phase comparator, integrated into the 4046 PLL circuit, the capture range does not depend on the characteristics of the low-pass filter. In this case, the capture range can match the locking range.

It should be recalled that the type-2 phase comparator integrated into the 4046 circuit employs sequential logic and presents more interesting performances than the type-1 comparator.

The practical diagram of the 4046 PLL circuit-based FSK demodulator is shown in Figure 3.87. To optimize the operation of the demodulator, a resistance R ($50 \text{ k}\Omega < R < 300 \text{ k}\Omega$) could be connected between the output and the ground.

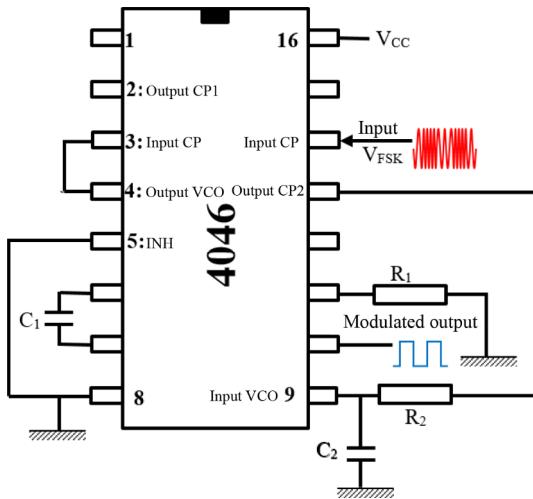


Figure 3.87. 4046-based FSK demodulator circuit

3.10. Exercises on PLLs

EXERCISE 1

Consider a PLL in which frequency f_e is that of the input signal, frequency f_s is the frequency of the VCO output signal and frequency f_0 is the natural frequency of the VCO. Indicate the right answer among propositions a, b, c and d.

1) When a signal of frequency f_e close to f_0 is injected into the loop:

- (a) the PLL is locked and $f_s = f_e$,
- (b) the loop leaves the capture range and $f_s = f_0$,
- (c) the loop is in an unstable state and $f_s = f_e$ and
- (d) the loop enters a stable state and $f_s = f_e$.

2) Once the loop is locked or tracking, the input frequency can vary without unlocking this loop within:

- (a) the capture range and $f_s = f_e$,
- (b) the capture range and $f_s = f_0$,
- (c) the locking range and $f_s = f_e$ and
- (d) the locking range and $f_s = f_0$.

SOLUTIONS TO EXERCISE 1

1) When a signal of frequency f_e close to f_0 is injected into the loop:

- (a) the PLL locks up and $f_s = f_e$;
- (d) the loop enters a stable state and $f_s = f_e$.

2) Once the loop is locked or tracking, the input frequency can vary without unlocking this loop within:

- (a) the capture range and $f_s = f_e$;
- (c) the locking range and $f_s = f_e$.

EXERCISE 2

Give the answer to the various following questions and justify the answer given each time.

1) Does a voltage-controlled oscillator have a transfer coefficient K_{VCO} that has V/Hz as unit?

2) A PLL has a locking range that extends from 500 kHz to 3 MHz and a capture range that extends from 1 to 2 MHz. The PLL is unlocked. The input signal frequency of the PLL is 750 kHz. Will the PLL lock? Justify the answer given.

3) A PLL has a locking range that extends from 500 kHz to 3 MHz and a capture range that extends from 1 to 2 MHz. The PLL is unlocked. The PLL input signal frequency is 1500 kHz. Will the PLL lock? Why?

4) A PLL has a locking range that extends from 500 kHz to 3 MHz and a capture range that extends from 1 to 2 MHz. The PLL is locked. The input signal frequency of the PLL is 2,500 kHz. Will the PLL unlock? Why?

5) Can a voltage-controlled oscillator (VCO) use varicap diodes in the feedback circuit? Why?

6) The signal that is applied to the PLL input (Figure E2.1) has a frequency of the form $f_e = f_0 + ks(t)$ (k is a constant, $s(t)$ is a low-frequency signal, f_0 is a very high frequency compared to the cutoff frequency of the first-order low-pass filter).

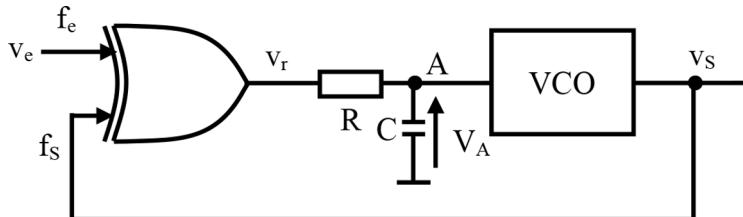


Figure E2.1. PLL circuit

The maximal frequency of the low-frequency signal $s(t)$ is within the passband of the low-pass filter.

6.1) What is the nature of the signal that is applied on input?

6.2) What is the function of the circuit when the output is taken at point A? Explain.

SOLUTIONS TO EXERCISE 2

1) The transfer coefficient K_{VCO} of a voltage-controlled oscillator is expressed in (Hz/V) because on input a variable tension is applied to obtain an output signal of variable frequency.

2) The PLL is not yet locked. The frequency of the signal falls outside the capture range. The PLL will not lock.

3) The PLL is not yet locked. The frequency of the signal processed is within the capture range. The PLL will lock.

4) The PLL will not unlock. The PLL is already locked and the processed signal has a frequency that does not fall outside the locking range.

5) A voltage-controlled oscillator (VCO) may use varicap diodes in its feedback circuit. It should be remembered that the feedback circuit sets the oscillation frequency of any oscillator. Given that the frequency of a signal originating from a VCO is variable according to a control voltage, it would be necessary that in the feedback circuit, a component would be included that has characteristics that vary according to a voltage that is applied to it and that this component has some action on the frequency of the output signal. The varicap diode presents all these characteristics. The varicap diode has a variable capacitance depending on the reverse bias that is applied thereto.

6) Nature of signal v_e applied on input and circuit function when the output is taken at point A and explanation:

6.1) Nature of the signal v_e applied on input:

The frequency of the signal that is applied on input varies according to variations in the signal $s(t)$ up to coefficient k . Signal v_e that is applied on input is a frequency-modulated signal.

6.2) Circuit function when the output is taken at point A and explanation:

The frequency spectrum of signal $s(t)$ is within the passband of the low-pass filter. The frequency of the input signal is of the form: $f_e = f_0 + ks(t)$. It is known that

frequency f_0 is very large compared to the cutoff frequency of the low-pass filter. The XOR gate-based phase comparator will detect the phase variation between the reference signal v_e and signal v_s at the output of the voltage-controlled oscillator. We will have at the output of the low-pass filter: $V_A = k' \cdot s(t)$

The function performed is frequency demodulation.

EXERCISE 3

Consider the circuit shown in Figure E3.1. An “Exclusive-OR” (XOR) gate is associated with a low-pass filter is employed.

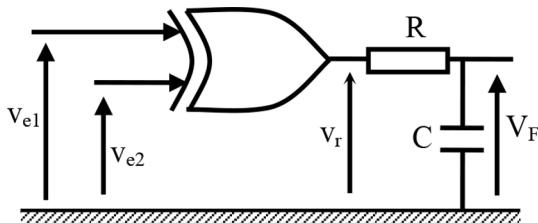


Figure E3.1. Study circuit based on an “XOR” gate and a first-order low-pass filter

Voltages v_{e1} and v_{e2} are square signals of frequency $f = 1/T$ and amplitude varying from 0 V to $V = 10$ V. The “Exclusive-OR” gate is in CMOS technology and it is powered by a voltage equal to V . The signal v_{e2} is lagging compared to signal v_{e1} by time “ t_d ”. We want to know:

- 1) What is the expression of the output voltage V_F as a function of time “ t_d ”? Calculate the value of V_F for $t_d = T/3$. What is the maximal value of V_F ?
- 2) The signal v_{e2} is lagging with respect to signal v_{e1} by $T/4$. Represent corresponding signals v_{e1} , v_{e2} , v_r and V_F . Give the expression and the value of the phase shift $\Delta\phi$ between v_{e1} and v_{e2} .
- 3) Deduce therefrom the expression of V_F according to the phase shift between v_{e1} and v_{e2} when $0 < t_d < T/2$.
- 4) Represent the characteristic of this circuit $V_F = f(\Delta\phi)$. Deduce therefrom the expression and the value of the transfer coefficient associated with this circuit.

SOLUTIONS TO EXERCISE 3

1) Expression of V_F according to t_d , values of V_F :

1.1) V_F expression:

$$V_F = \frac{2}{T} \int_0^{t_d} v_r(t) dt, \quad V_F = \frac{2V}{T} t_d$$

1.2) Value of V_F for $t_d = T/3$ and maximal value of V_F :

When we have $t_d = T/3$, it can be seen that: $V_F = \frac{2V}{3}$

The maximal value for V_F is obtained when voltage v_{e1} is in antiphase with respect to voltage v_{e2} . The offset is equal to $T/2$: $V_f = V$.

2) Representation of corresponding signals v_{e1} , v_{e2} , v_r and V_F . Expression and value of the phase shift $\Delta\phi$ between v_{e1} and v_{e2} when signal v_{e2} is lagging with respect to signal v_{e1} by a period equal to $T/4$:

2.1) Representation of signals v_{e1} , v_{e2} , v_r and V_F (see Figure E3.2):

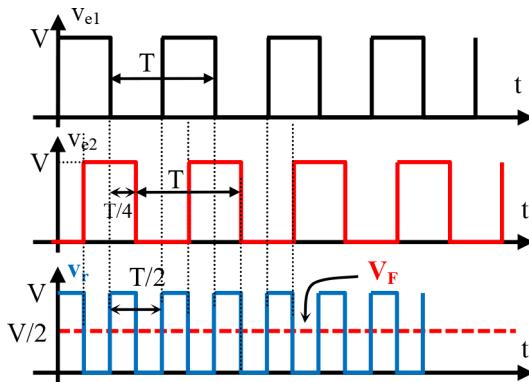


Figure E3.2. Representation of signals v_{e1} , v_{e2} , v_r and V_F . For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

2.2) Phase shift expression and value for $t_d = (T/4)$:

As long as the phase shift is less than π , it can be written that:

$$\Delta\phi = 2\pi \cdot \frac{t_d}{T}$$

$$\Delta\varphi = \frac{\pi}{2}$$

For $t_d = (T/4)$:

3) Expression of V_F according to the phase shift between v_{e1} and v_{e2} :

As long as time t_d is between zero and half-period ($0 < t_d < T/2$), it can be written that:

$$V_F = \frac{2V}{T} \int_0^{t_d} dt = \frac{2V}{T} t_d ;$$

$$\Delta\varphi = 2\pi \cdot \frac{t_d}{T} = \pi \cdot \frac{V_F}{V}$$

4) Representation of the characteristic of the circuit $V_F = f(\Delta\varphi)$ and expression and value of the transfer coefficient associated with this circuit:

4.1) Representation of $V_F = f(\Delta\varphi)$:

The voltage V_F variation at the low-pass filter output according to the phase difference is linear (see Figure E3.3).

$$V_F = V \frac{\Delta\varphi}{\pi}$$

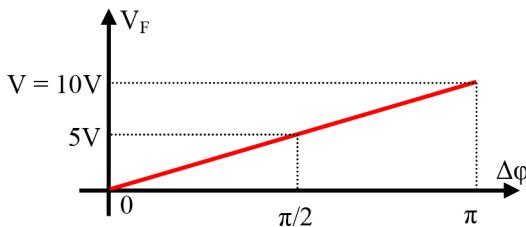


Figure E3.3. Evolution of V_F according to the phase difference

4.2) Expression and value of the transfer coefficient:

$$K = \frac{V}{\pi} = 3.18V / rad$$

EXERCISE 4

It is proposed to study the analog phase-locked loop (PLL) whose synoptic diagram is shown in Figure E4.1.

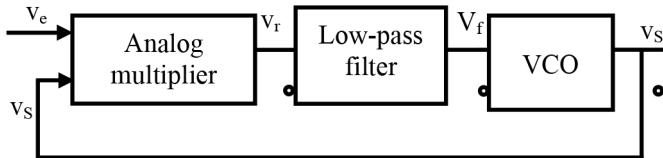


Figure E4.1. PLL device under study

The input signal v_e (reference signal) and output signal v_s are given by the following expressions:

$$v_e = V_1 \cos(\omega t + \varphi_e)$$

$$v_s = V_2 \sin(\omega t + \varphi_s)$$

It is assumed that the frequencies of the input and output signals are virtually equal and that their phases are close enough.

The multiplier transfer coefficient is equal to K_1 ($v_r = K_1 v_e \cdot v_s$).

- 1) What is the expression of signal $v_r(t)$ that is at the output of the analog multiplier?
- 2) What is the expression of signal V_f at the output of the low-pass filter?
- 3) The voltage V_f is a function of the phase difference between the phase relative to the input signal and the output signal phase. The VCO output frequency linearly varies with respect to V_f ($f_s = K_{VCO} \cdot V_f$). What is the VCO transmittance (φ_s/V_f)?

SOLUTIONS TO EXERCISE 4

- 1) Expression of signal $v_r(t)$ that can be found at the analog multiplier output:

$$v_r = v_e \cdot v_s = K_1 V_1 \cos(\omega t + \varphi_e) \cdot V_2 \sin(\omega t + \varphi_s)$$

$$v_r = K_1 V_1 \cdot V_2 \cdot \cos(\omega t + \varphi_e) \cdot \sin(\omega t + \varphi_s)$$

$$v_r = \frac{K_1 V_1 \cdot V_2}{2} \cdot (\sin(2\omega t + \varphi_e + \varphi_s) + \sin(\varphi_s - \varphi_e))$$

2) Expression of signal V_f at the low-pass filter output:

The role of the low-pass filter is to eliminate high frequencies that are represented by pulse 2ω . Therefore, at the low-pass filter output, signal V_f is obtained, which has the signal expression then defined by:

$$V_f = \frac{K_1 V_1 \cdot V_2}{2} \cdot \sin(\varphi_s - \varphi_e)$$

The phases φ_s and φ_e are close enough to one another. Their difference is small. Under these conditions, it can be written that:

$$V_f = \frac{K_1 V_1 \cdot V_2}{2} (\varphi_s - \varphi_e)$$

3) VCO transmittance (φ_s/V_f):

The VCO output is a signal of variable frequency f_s . It is known that:

$$f_s = \frac{1}{2\pi} \frac{d\varphi_s}{dt}$$

It is also known that the variation of the output signal frequency is proportional to the voltage that is applied at the VCO input.

$$f_s = K_{VCO} \cdot V_F$$

This leads to the following expression for the transmittance:

$$\frac{\varphi_s(p)}{V_f(p)} = \frac{2\pi K_{VCO}}{p}$$

EXERCISE 5

We want to achieve a frequency synthesizer (Figure E5.1) built around a phase-locked loop (PLL). It is required to:

- 1) Give the expression of the frequency f_s of the output signal based on f_x , N and M .
- 2) The factor N determines the synthesis step, while the value of M is fixed (N and M are integers). What is the expression of the minimal value of f_s ? Digital application $M = 20$ and $f_x = 10$ MHz.

3) Using synthesis, we want to generate signals that have frequencies ranging from 1 to 100 MHz. It is required to determine the extreme values that must be injected at the programmable divider level.

4) The phase comparator is an “Exclusive-OR” logic gate. It is required to find the signal frequency at the “Exclusive-OR” output when the signal output frequency of the VCO is equal to 60 MHz.

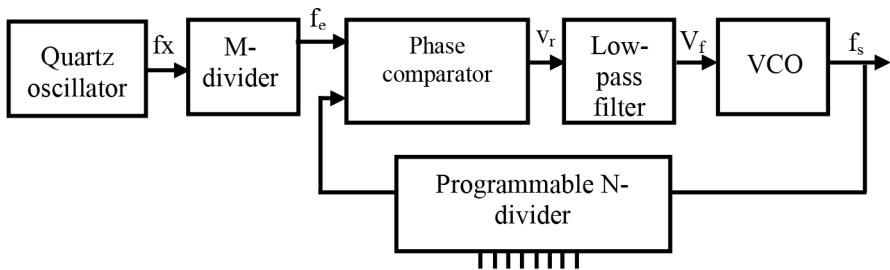


Figure E5.1. Frequency synthesizer

SOLUTIONS TO EXERCISE 5

1) Expression of frequency f_s of the output signal according to frequency f_x , to N and M :

$$f_s = f_x \frac{N}{M}$$

2) Expression of the minimal value of f_s and digital application:

2.1) Expression of the minimal value:

$$f_{s\min} = \frac{f_x}{M}$$

2.2) Numerical application: $f_{s\min} = 500$ kHz.

3) Determination of extreme values that have to be injected at the programmable divider level to cover the entire band ranging from 1 to 100 MHz:

$$f_s = f_x \frac{N}{M}$$

The band to be covered extends from 1 to 100 MHz. The extreme values of the synthesized frequency are respectively:

$$f_{S1} = 1 \text{ MHz}$$

$$f_{S2} = 100 \text{ MHz}$$

The values of N needed to achieve these extreme frequencies are respectively:

$$N_1 = 2 \text{ and } N_2 = 200$$

4) Frequency of the “Exclusive-OR” output signal when the VCO output signal frequency is equal to 60 MHz:

When the PLL is locked and a digital phase comparator is employed in the form of an “Exclusive-OR” gate, the latter will present an output signal with twice the repetition frequency with respect to the signal frequency that is found at its output. The input frequency of the phase comparator, which corresponds to 60 MHz (VCO output frequency) is:

$$f_e = \frac{f_s}{N} = 500 \text{ kHz}$$

The frequency at the output of the “Exclusive-OR” phase comparator is:

$$f_r = 2.f_e = 1 \text{ MHz.}$$

EXERCISE 6

The proposed phase-locked loop (PLL) circuit under study is schematically presented in Figure E6.1. Input and output signals are of square forms, period T and amplitude 5 V (see Figure E6.2).

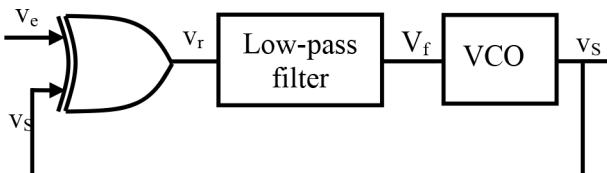


Figure E6.1. Circuit under study

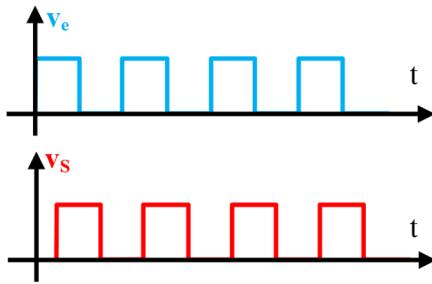


Figure E6.2. Input and output signal

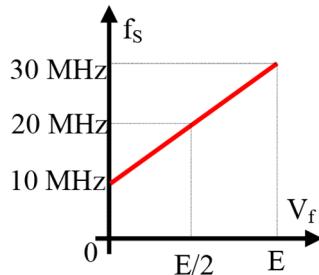


Figure E6.3. VCO transfer characteristic

1) The low-pass filter is of the first order and consists of a resistor and a capacitor. Give the diagram of this filter. What is its cut-off frequency at -3 dB? Numerical application $R = 50 \text{ k}\Omega$ and $C = 0.2 \mu\text{F}$.

2) The voltage-controlled oscillator (VCO) has the frequency of its output signal, which varies based on a control voltage. The VCO transfer function is presented in Figure E6.3. It is assumed that the PLL is locked. It is required to represent voltage variations of v_e , v_S , v_i and V_f when voltages v_e and v_S are out of phase by an angle φ , with: a) $\varphi = 0$, b) $\varphi = (\pi/8)$, c) $\varphi = (\pi/4)$ and d) $\varphi = (\pi/2)$. In each case, what is the value of voltage V_f and the operating frequency of the PLL?

3) It is assumed that the phase shift between reference voltage v_e and the feedback voltage that originates from the VCO output is variable. Under these

conditions, represent the variation of control voltage V_F based on the variation of phase.

4) Provide the block diagram of the PLL with phases ϕ_e and ϕ_S as input and output quantities respectively.

SOLUTIONS TO EXERCISE 6

1) Diagram of the low-pass filter, cutoff frequency at -3 dB:

The diagram of the first-order low-pass RC filter is schematically presented in Figure E6.4.

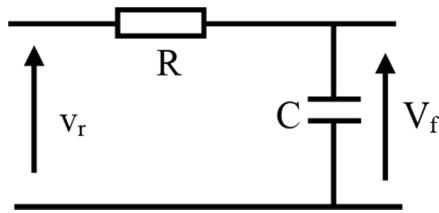


Figure E6.4. Diagram of the RC-type low-pass filter

The transfer function of this filter is given by:

$$H(j\omega) = \frac{V_f}{V_r} = \frac{1}{1+jRC\omega}$$

To calculate the cutoff frequency at -3 dB, the modulus of the transfer function has first to be calculated.

$$|H(j\omega)| = \left| \frac{V_f}{V_r} \right| = \frac{1}{\sqrt{(1+(RC\omega)^2)}}$$

The cutoff frequency f_c is defined when we have:

$$|H(j\omega)| = \frac{1}{\sqrt{2}} \Rightarrow (RC\omega_c) = 1$$

The cutoff frequency is defined based on the following relation:

$$f_c = \frac{1}{2\pi RC}$$

Numerical application: $R = 50 \text{ k}\Omega$, $C = 0.2 \mu\text{F}$; $f_c = 16 \text{ Hz}$

2) Representation of voltage variations of v_e , v_s , v_r and V_f when voltages v_e and v_s are out of phase by an angle φ . The different values of voltage V_f and operating frequency:

2.1) Representation of voltage variations v_e , v_s , v_r and V_f .

The representations of v_e , v_s , v_r and V_f for a zero phase shift and a phase shift equal to $(\pi/8)$ are given in Figure E6.5.

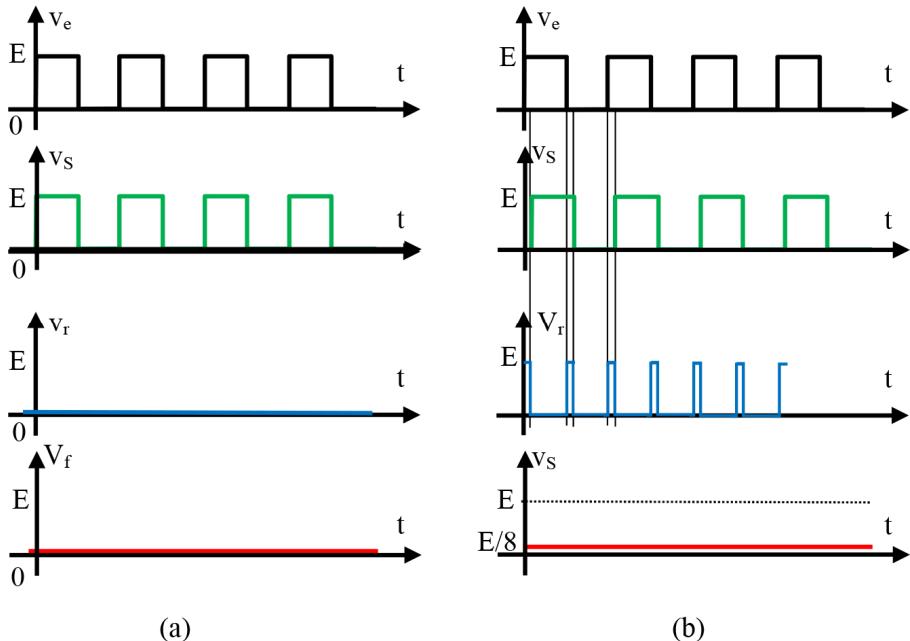


Figure E6.5. Voltage evolution of v_e , v_s , v_r and V_f for a) $\varphi = 0$ and b) $\varphi = (\pi/8)$

The representations of signals for the cases in which $\varphi = (\pi/4)$ and $\varphi = (\pi/2)$ are given in Figure E6.6.

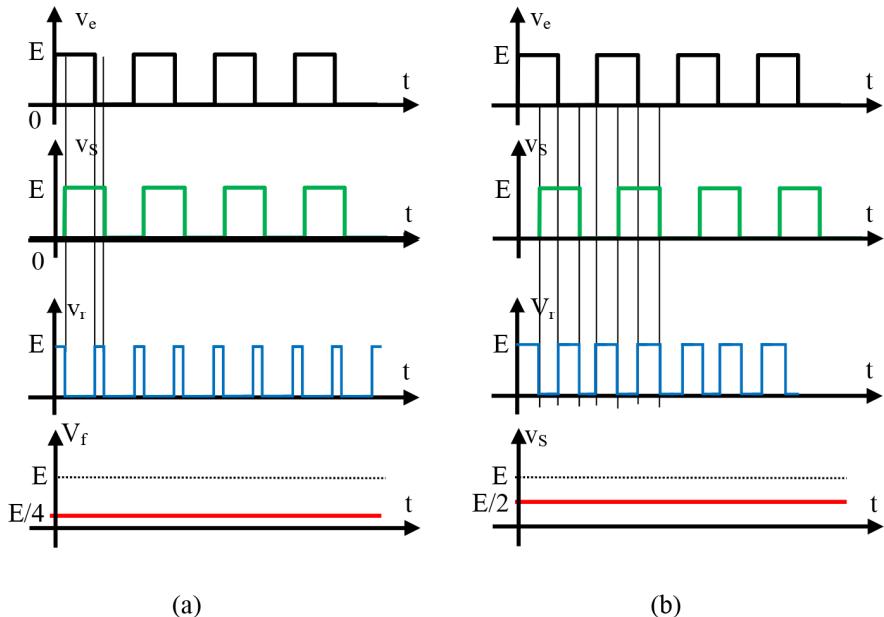


Figure E6.6. Voltage evolution of v_e , v_s , v_r and V_f for a) $\varphi = (\pi/4)$ and b) $\varphi = (\pi/2)$

2.2) Value of the control voltage V_f for different phase values φ :

It should be noted that the frequency of the output signal of the logic gate “Exclusive-OR” is twice the frequency of the reference signal applied on input.

On output, the low-pass filter will only keep the average value of voltage v_r :

$$V_f = \frac{2}{T} \int_0^{T/2} v_r \cdot dt = \frac{2}{T} \int_0^{\Delta t} E \cdot dt = \frac{2\Delta t \cdot E}{T}$$

The time offset Δt is a function of the phase shift φ between the input reference voltage v_e and the output voltage v_s .

When analyzing the graph relatively to voltages v_e and v_s , it can be seen that for a phase shift equal to π , the time offset Δt is equal to $T/2$.

This allows us to deduce:

$$\Delta t = \frac{T\phi}{2\pi}$$

$$V_f = \frac{2\Delta t \cdot E}{T} = \frac{E\phi}{\pi}$$

There is a relation of proportionality between the control voltage and the phase difference ϕ between input and output signals.

For $\phi = 0$; $V_f = 0$;

$$\phi = (\pi/8); V_f = E/8$$

$$\phi = (\pi/4); V_f = E/4;$$

$$\phi = (\pi/2); V_f = E/2$$

2.3) Value of the operating frequency of the PLL:

The PLL is locked. The output signal frequency of the VCO is equal to the frequency of the input reference signal.

According to the VCO transfer characteristic, it can be observed that there is also a relation of proportionality between the frequency f_s and control voltage V_f .

$$f_s = aV_f + b$$

The parameters a and b are both constants that are respectively defined by:

$$a = 20.10^6/E \text{ in Hz/V and } b = 10^6 \text{ Hz}$$

$$f_s(\text{MHz}) = 10\left(\frac{2V_f}{E} + 1\right)$$

For $\phi = 0$; $V_f = 0$; $f_s = 10 \text{ MHz}$

$$\phi = (\pi/8); V_f = E/8; f_s = 12.5 \text{ MHz}$$

$$\varphi = (\pi/4); V_f = E/4; f_s = 15 \text{ MHz}$$

$$\varphi = (\pi/2); V_f = E/2; f_s = 20 \text{ MHz}$$

3) Representation of the variation of the control voltage V_f according to the variation of phase (see Figure E6.7):

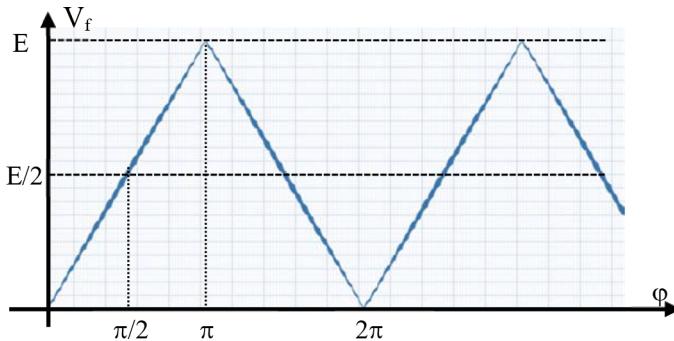


Figure E6.7. Evolution of voltage V_f when the phase shift φ between v_e and v_s varies

4) Block diagram of the PLL having phases φ_e and φ_s as input and output quantities respectively:

It should be remembered that the relation that links phase and frequency in the time domain is given by:

$$f(t) = \frac{1}{2\pi} \cdot \frac{d\varphi(t)}{dt}$$

When input and output quantities are phase variations, the block diagram of the PLL is presented in Figure E6.8.

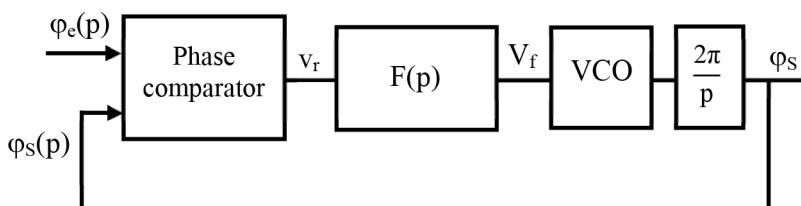


Figure E6.8. Block diagram of the PLL with phase variations as input and output quantities

EXERCISE 7

We want to study the phase comparator schematically presented in Figure E7.1. The two generators each provide a constant current equal to I .

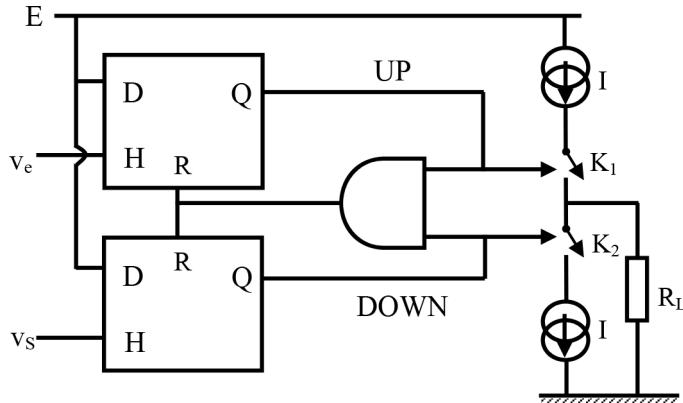


Figure E7.1. Phase comparator under study

- 1) Give the truth table of the D flip-flop that is inserted in the diagram of the phase comparator.
- 2) Study the operation of the circuit by representing UP and DOWN signals and the voltage at the terminals of resistance R_L .
- 3) What is the average value of the voltage at the terminals of R_L and what is the relation that relates this average value to the phase shift between voltages v_e and v_s ?
- 4) What is the transfer function of the phase comparator knowing that at the output, the average value of the voltage at the terminals of resistance R_L , is recovered?
- 5) The load R_L is replaced by a capacitor C . What is the expression of voltage V_C at the terminals of capacitor C ?
- 6) It is assumed that the phase difference between voltages v_e and v_s is variable. Under these conditions, plot the evolution of the variation of voltage V_C based on the phase difference.

SOLUTIONS TO EXERCISE 7

- 1) Truth table of a D flip-flop including a Reset input:

This is in fact an asynchronous-type D flip-flop. Only the “RESET” input is used.

The diagram of the flip-flop that is used in the phase comparator, which we are focusing on, as well as its truth table are given in Figure E7.2.

The input D of the flip-flop is always in a high state ($V_D = E$).

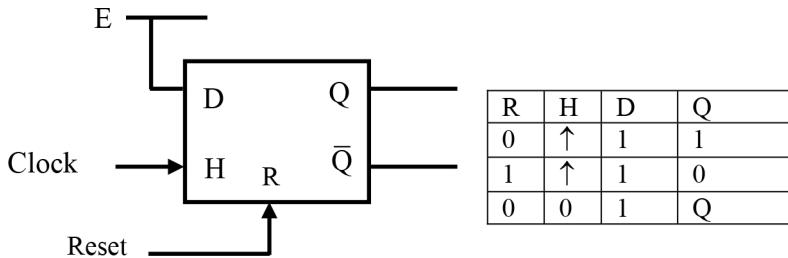


Figure E7.2. D flip-flop and its truth table

- 2) Circuit operation, representation of UP and DOWN signals and of the signal at the terminals of resistance R_L :

Signals v_e and v_s are out of phase with an angle φ . They operate as clock signals for both D flip-flops that are present in the phase comparator. The analysis of the behavior of the two D flip-flop when applying v_e and v_s makes it possible to deduce UP and DOWN signals.

In the absence of feedback signal to the reset due to the combination of UP and DOWN signals through the “AND” gate, the outputs of the two D flip-flops are in the high state.

However, there is an offset between the occurrences of these high levels. This is related to the phase shift that may exist between the voltages that are applied to the clock inputs of the two flip-flops.

This shift is used to generate the signals UP and DOWN, as shown in Figure E7.3.

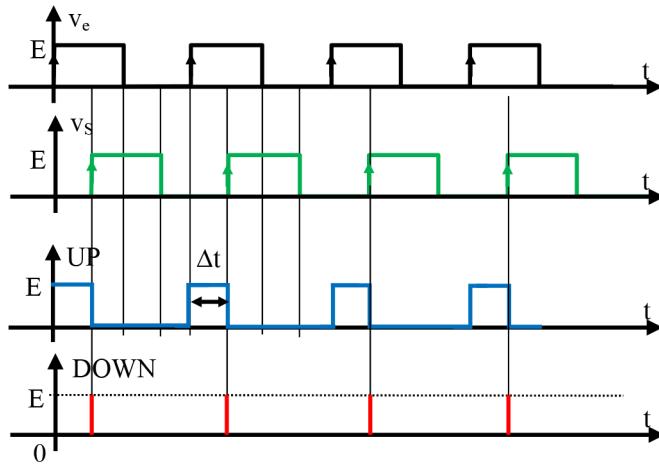


Figure E7.3. Phase comparator UP and DOWN signals

To find the voltage at the terminals of resistance R_L , we just have to see that switch K_1 is closed during duration Δt . This means that:

$$v_{RL} = R_L I \text{ for } 0 < t < \Delta t$$

Current I is constant. The representation of voltage variations at R_L is given in Figure E7.4.

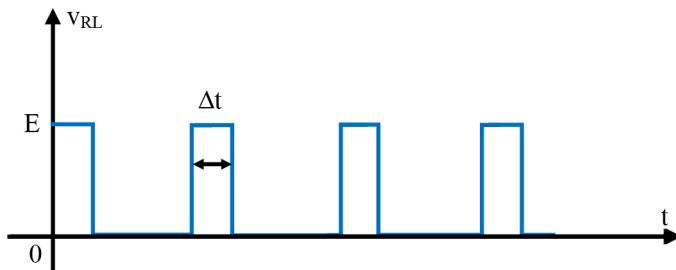


Figure E7.4. Voltage evolution at the terminals of resistance R_L

3) Voltage average value (V_{ave}) at the terminals of resistance R_L and relation of V_{ave} with the phase shift between signals v_e and v_s :

3.1) Voltage average value at the terminals of resistance R_L :

The expression of the average value of the voltage at the terminals of resistance R_L can be defined as follows:

$$V_{ave} = \frac{1}{T} \int_T V_{RL} dt = \frac{1}{T} \int_0^{\Delta t} R_L I dt$$

where T is the period of one of the signals v_e or v_s .

The computation yields:

$$V_{ave} = \frac{R_L I \cdot \Delta t}{T}$$

When the time offset is equal to the period, the phase shift $\varphi = \varphi_e - \varphi_s$ between signals v_e and v_s is equal to 2π . For a time offset equal to Δt , the phase shift can be expressed as follows:

$$\varphi = \varphi_e - \varphi_s = \frac{2\pi \cdot \Delta t}{T}$$

Finally:

$$V_{ave}(p) = \frac{R_L I}{2\pi} (\varphi_e(p) - \varphi_s(p))$$

4) Transfer function of the phase comparator:

The phase comparator is shown by the block diagram in Figure E7.5.

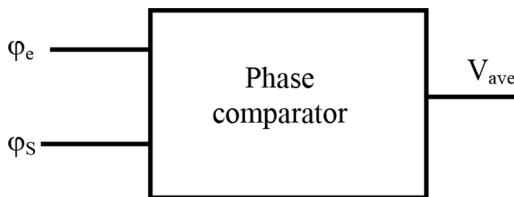


Figure E7.5. Phase comparator block diagram

The transfer function of the phase comparator (K_{CP}) can be expressed by:

$$K_{CP} = \frac{V_{ave}(p)}{(\varphi_e(p) - \varphi_S(p))}$$

$$K_{CP} = \frac{R_L I}{2\pi}$$

5) Expression of the voltage at the terminals of capacitor C:

When resistance R_L is replaced by a capacitor with capacitance C, it will charge with a constant current during time Δt .

This time Δt is proportional to the phase shift between voltage v_e and voltage v_S .

When the UP output is in a high state and the DOWN output is at the low state, switch K_1 is closed. The expression of voltage (V_C) at the terminals of capacitor "C" is then given by:

$$V_C = \frac{1}{C} \int_0^{\Delta t} I \cdot dt$$

Current I is constant:

$$V_C = \frac{I \cdot \Delta t}{C}$$

$$V_C = \frac{I \cdot (\varphi_e - \varphi_S) T}{2\pi C}$$

$$V_C = K \cdot \frac{(\varphi_e - \varphi_S)}{2\pi}$$

$$K = \frac{I \cdot T}{C}$$

6) Evolution of voltage V_C at the terminals of capacitor C according to the phase difference. The phase difference between voltages v_e and v_S is variable:

When the phase difference is variable, the duration of the pulse UP will also be variable.

The D flip-flop is triggered by rising edges. The phase difference varies from zero to 2π .

For a zero phase variation, voltage V_C is zero. For a maximal phase variation equal to 2π , we have:

$$V_C = K = \frac{IT}{C}$$

The variation of voltage V_C based on the variation of phase difference φ between v_e and v_s is linear. It is presented in Figure E7.6.

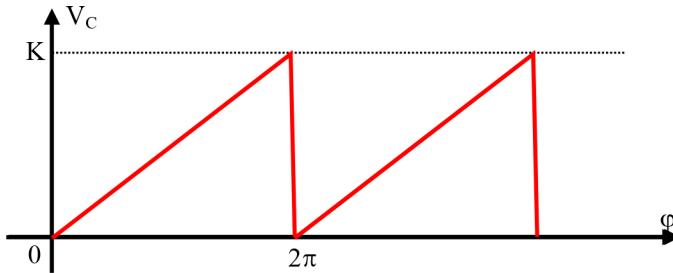
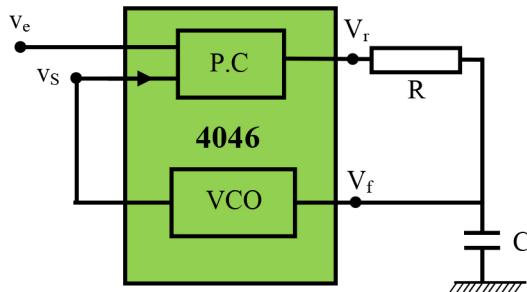


Figure E7.6. Voltage variation at the terminals of capacitor C according to the phase difference between v_e and v_s

EXERCISE 8

Consider the CMOS 4046 integrated circuit connected as shown in Figure E8.1. The frequency variation of the VCO output signal according to control voltage V_f that is applied to its input is shown in Figure E8.2.



P.C: phase comparator

VCO: voltage-controlled oscillator

Figure E8.1. Diagram of the circuit under study

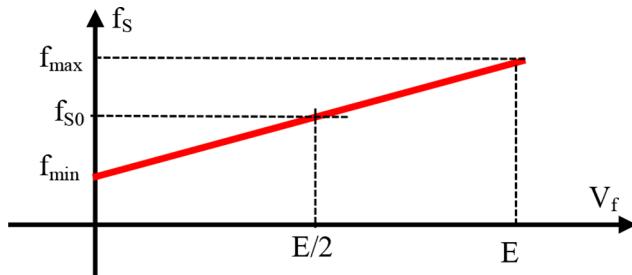


Figure E8.2. Evolution of the frequency of the VCO output signal according to the control voltage

1) Voltages $v_e(t)$ and $v_s(t)$ have a square shape, a single pole and amplitude equal to E . We use the type-1 phase comparator (XOR gate) of the 4046 circuit. It is required to find the expression of voltage V_f according to the variation of phase between voltages $v_e(t)$ and $v_s(t)$.

2) Signal V_f represents the VCO control. What is the expression of the output frequency $f_S(t)$ according to the control voltage?

3) We have the block diagram that is presented by the synoptic of Figure E8.3. It is required to find the expressions of the missing functions $h_1(t)$ and $h_2(t)$ in the block diagram while providing the necessary explanation. Give a simplified representation of Figure E8.3 by combining the action of $h_1(t)$ and $h_2(t)$.

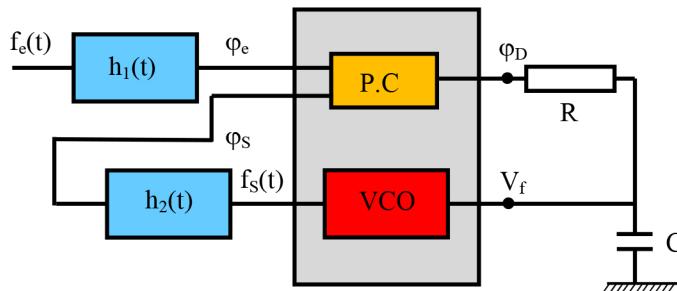


Figure E8.3. Block diagram under study. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

SOLUTIONS TO EXERCISE 8

1) Expression of voltage V_f according to the phase variation between voltages $v_e(t)$ and $v_s(t)$:

Signals $v_e(t)$ and $v_s(t)$ are square signals. The measurement of the phase offset is tantamount to measuring a time offset. The expression of voltage V_f at the output of the low-pass filter according to the phase difference is given by:

$$V_f = E \frac{\Delta\varphi}{\pi} = E \frac{\varphi_e - \varphi_s}{\pi} \text{ for } 0 < \Delta\varphi < \pi$$

$$V_f = 2E\left(1 - \frac{\Delta\varphi}{2\pi}\right) \text{ for } \pi < \Delta\varphi < 2\pi$$

2) Expression of the output frequency based on the control voltage V_f .

The evolution of the output frequency f_s according to the control voltage V_f is a linear function:

$$f_s = aV_f + b$$

When $V_f = 0$, the output frequency is equal to f_{\min} : $b = f_{\min}$. When $V_f = E$, the VCO output frequency f_s is equal to f_{\max} .

$$f_{\max} = aE + b$$

It then yields:

$$a = \frac{f_{\max} - f_{\min}}{E}$$

$$f_s = \frac{f_{\max} - f_{\min}}{E} V_f + f_{\min}$$

3) Expressions of missing functions $h_1(t)$ and $h_2(t)$ in the block diagram and simplified diagram:

3.1) Expressions of $h_1(t)$ and $h_2(t)$:

It should be remembered that shifting from a frequency to a phase requires integration and that frequency derives from phase.

As a result, it can be inferred that:

$$h_1(t) = 2\pi \int_0^t f_e(t).dt$$

$$h_2(t) = 2\pi \int_0^t f_s(t).dt$$

3.2) Simplified schematic:

The simplified synoptic diagram consists of finding the possibility of integrating the two blocks $h_1(t)$ and $h_2(t)$ into a single one. The phase comparator will have f_e and f_s as input frequencies, and thereby, it is required under these conditions to represent the diagram of the PLL by the diagram shown in Figure E8.4.

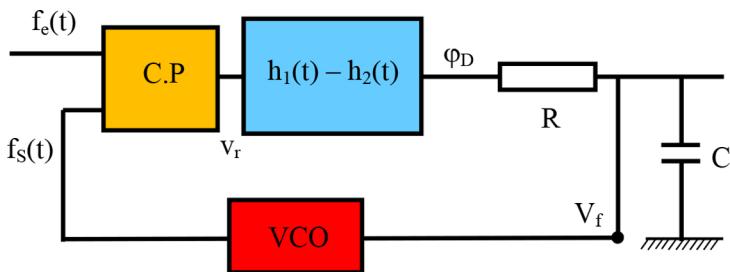


Figure E8.4. Simplified diagram of the PLL. For a color version of this figure, see www.iste.co.uk/haraouibia/nonlinear2.zip

EXERCISE 9

Consider the synoptic diagram of the phase-locked loop (PLL) of Figure E9.1. With:

$$f_s = \frac{K_{VCO}}{2\pi} V_f + f_0$$

$$v_e = V_1 \cdot \sin(\phi_1(t)); v_s = V_2 \cdot \sin(\phi_2(t))$$

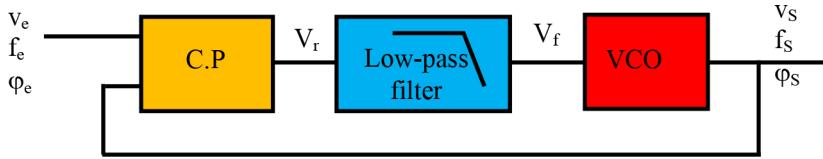


Figure E9.1. PLL circuit. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

1) It is required to express $\phi_1(t)$ and $\phi_2(t)$ according to the frequencies of signals $v_e(t)$ and $v_s(t)$ as well as according to initial phases $\phi_1(0) = \phi_1$ and $\phi_2(0) = \phi_2$. What is the expression of the phase difference and what can we say if initial phases are zero?

2) It is assumed that we are working in the Laplace domain. The block diagram of the PLL is shown in Figure E9.2. In these circumstances, find the expressions of functions $H_1(p)$ and $H_2(p)$.

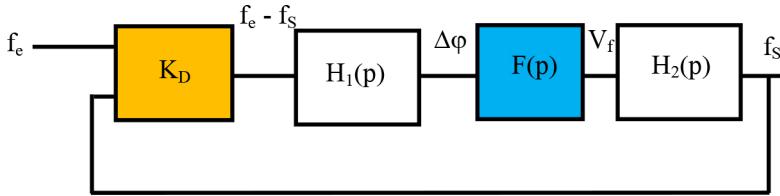


Figure E9.2. PLL block diagram. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

3) We want to find the expression of the open-loop transfer function $H_{B0}(p)$ and of the closed-loop transfer function $H_{BF}(p)$. The parameter K_D is the transfer coefficient of the phase comparator and $F(p)$ is the transfer function of the low-pass filter.

4) We want to study the stability of the phase-locked loop, knowing that the PLL utilizes a low-pass filter, which has a transfer function of the form:

$$F(p) = \frac{1}{RCp}$$

5) The low-pass type filter studied in question 4 is replaced by a second type of low-pass filter (see Figure E9.3). What is the transfer function $F(p)$ of this filter? Study the stability of the PLL with this type of filter and draw a conclusion.

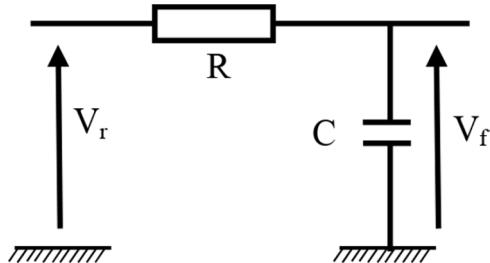


Figure E9.3. Second type of low-pass filter

6) The second type of filter studied in question 5 is replaced by a third type of low-pass filter as in Figure E9.4.

6.1) What is the transfer function $F'(p)$ of this filter? Deduce therefrom the transfer function $F'(p)$ according to $F(p)$ of the circuit of Figure E9.3 knowing that $R_2 = aR$, with $0 < a < 1$ and $(R_1 + R_2) = R$.

6.2) Study the stability of the phase-locked loop including the low-pass filter that is schematically presented in Figure E9.4. Compare with results found in 5 and draw a conclusion.

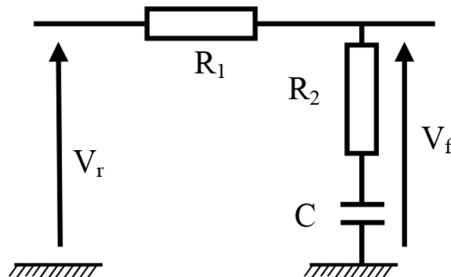


Figure E9.4. Third type of low-pass filter

SOLUTIONS TO EXERCISE 9

1) Expressions of $\phi_1(t)$ and $\phi_2(t)$ according to the frequencies of signals $v_e(t)$ and $v_s(t)$ with initial phases $\phi_1(0) = \phi_1$ and $\phi_2(0) = \phi_2$ and expression of the phase difference:

1.1) Expressions of $\phi_1(t)$ and $\phi_2(t)$:

The phases are expressed based on the following relations:

$$\phi_1(t) = 2\pi \int_t f_e dt = 2\pi f_e t + \phi_1$$

$$\phi_2(t) = 2\pi \int_t f_s dt = 2\pi f_s t + \phi_2$$

1.2) Expression of the phase difference:

$$\Delta\phi = (\phi_1(t) - \phi_2(t)) = 2\pi(f_e - f_s)t + (\phi_1 - \phi_2)$$

When initial phases are zero, we have:

$$\Delta\phi = (\phi_1(t) - \phi_2(t)) = 2\pi(f_e - f_s)t$$

The phase variation varies to the rate of the difference ($f_e - f_s$). When the phase difference is zero, then frequencies f_e and f_s are equal.

$$\Delta\phi = 0; f_e = f_s$$

2) Expressions of functions $H_1(p)$ and $H_2(p)$:

In order to shift from the frequency domain to the phase domain, a transfer function $H_1(p)$ has to be introduced.

$$H_1(p) = \frac{2\pi}{p}$$

Function $H_2(p)$ is the transfer function of the VCO.

$$H_2(p) = K_{VCO}$$

The block diagram of the phase-locked loop (PLL) is shown in Figure E9.5.

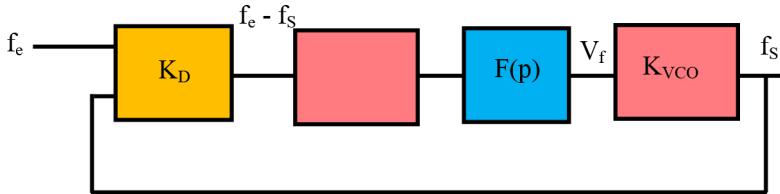


Figure E9.5. PLL block diagram with the definition of each block. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

3) Expression of the open-loop transfer function $H_{BO}(p)$ and the closed-loop transfer function $H_{BF}(p)$. The open-loop transfer function is given by the relation:

$$H_{BO} = \frac{2\pi F(p) \cdot K_D \cdot K_{VCO}}{p}$$

In a general framework, the closed-loop transfer function is given by:

$$H_{BF} = \frac{H_{BO}(p)}{1 + H_{BO}(p)}$$

This makes it possible to deduce the transfer function of the closed-loop phase-locked loop.

$$H_{BF}(p) = \frac{2\pi \frac{F(p) \cdot K_D \cdot K_{VCO}}{p}}{1 + 2\pi \frac{F(p) \cdot K_D \cdot K_{VCO}}{p}}$$

$$H_{BF}(p) = \frac{2\pi F(p) \cdot K_D \cdot K_{VCO}}{p + 2\pi F(p) \cdot K_D \cdot K_{VCO}}$$

4) Study of the stability of the phase-locked loop:

When the transfer function of the low-pass filter is of the form:

$$F(p) = \frac{1}{RCp}$$

the transfer functions of the open-loop and closed-loop PLLs are expressed by the following relations:

Open loop:

$$H_{BO} = \frac{2\pi F(p) \cdot K_D K_{VCO}}{p}$$

$$H_{BO} = \frac{2\pi K_D K_{VCO}}{R C p^2}$$

Closed loop:

$$H_{BF} = \frac{2\pi K_D K_{VCO}}{R C p^2 + 2\pi K_D K_{VCO}}$$

The stability of the phase-locked loop can be studied using either the PLL open-loop transfer function or the closed-loop transfer function. If the open-loop transfer function is employed, we have to find what the phase margin is and see if this phase margin is significant or not.

$$H_{BO}(j\omega) = -\frac{2\pi K_D K_{VCO}}{R C \omega^2}$$

The phase margin for this type of device is zero ($M\phi = 0$). This shows that the system is unstable. When using the closed-loop transfer function, the step response according to the damping factor, for example, will be studied. To this end, let us recall that the closed-loop transfer function of a phase-locked loop can be written in the form:

$$H(p) = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

For the present case, it follows that:

$$H_{BF} = \frac{2\pi K_D K_{VCO}}{R C p^2 + 2\pi K_D K_{VCO}} = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

$$H_{BF} = \frac{\frac{2\pi K_D K_{VCO}}{RC}}{p^2 + \frac{2\pi K_D K_{VCO}}{RC}} = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

It is easy to see that for this case that we are focusing on, the damping factor is zero. It is known that when the damping factor is less than 1, we have an oscillatory response. The overshoot is a function of the damping coefficient. If ζ tends to 0, the overshoot tends to 100%, the 5% response time tends to infinity and the loop is completely unstable.

5) Filter transfer function and stability of the PLL with the type of filter under study and conclusion:

5.1) Function of the low-pass filter (see Figure E9.3):

$$F(p) = \frac{1}{1+RCp}$$

5.2) Stability study:

When using the low-pass filter that has the transfer function described above, we obtain for the PLL the open-loop and closed-loop transfer functions that will provide us with information about the stability of the PLL. For the open-loop PLL, the phase margin will be the main point of interest and for the closed loop, we will look into how the damping factor evolves.

Open loop

$$H_{BO} = \frac{\frac{2\pi}{1+RCp} \cdot K_D K_{VCO}}{p}$$

$$H_{BO} = \frac{2\pi K_D K_{VCO}}{p + RCp^2}$$

With sinusoidal waves, we have:

$$H_{BO}(j\omega) = \frac{2\pi K_D K_{VCO}}{-RC\omega^2 - j\omega}$$

The Bode diagram relating to this transfer function is given by representations of Figure E9.6 (a) and (b).

The analysis of the Bode plot of Figure E9.6a shows that it is possible to have phase margins large enough (larger than 30°) on the condition that we have:

$$2\pi K_D K_{VCO} \tau < 1.$$

The product $2\pi K_D K_{VCO} \tau$ affects the characteristics of the phase comparator. This product is related to the cutoff frequency of the low-pass filter. When this product is equal to 0.4, the phase margin is of the order of 55° . This allows us to state that the PLL is stable enough.

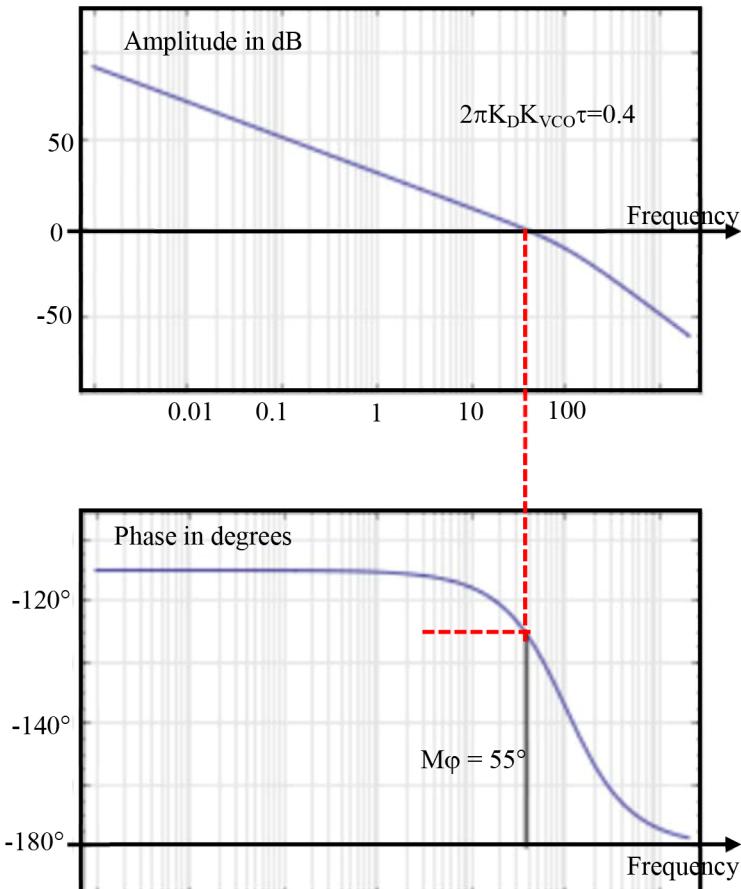


Figure E9.6a. PLL phase margin and stability for a product $K_D K_{VCO} \tau = 0.4$

When we plot the Bode diagram for a product $K_D K_{VCO} \tau$, greater than 1, we obtain the curves shown in Figure E9.6b. It can be noted that the margin phase $M\varphi = 25^\circ$ is smaller. Its value is significant for the stability of the PLL. In this case, the PLL is less stable than in the case of $M\varphi = 55^\circ$.

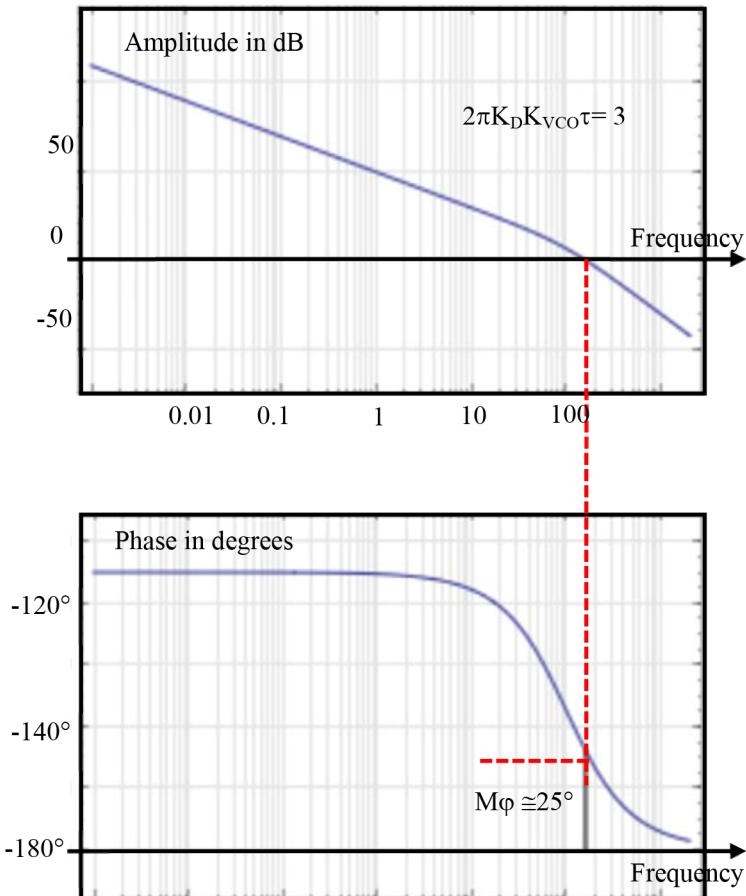


Figure E9.6b. PLL phase margin and stability for a product $K_D \cdot K_{VCO} \cdot \tau = 3$

It should be noted that the parameter τ characterizes the low-pass filter inserted into the phase-locked loop. It affects the loop stability.

When the coefficient $2\pi K_D \cdot K_{VCO} \cdot \tau$ increases, the phase margin decreases and therefore the stability of the PLL decreases. It therefore proves advantageous that this coefficient be less than 1 to keep a phase margin large enough in order to have a sufficiently stable phase-locked loop.

This coefficient $2\pi K_D \cdot K_{VCO} \cdot \tau$ should not be too small at the risk of making the system too slow.

The closed loop: it is reminded that the transfer function of the PLL loop under study is of the form:

$$H_{BF}(p) = \frac{2\pi F(p) \cdot K_D K_{VCO}}{p + 2\pi F(p) \cdot K_D K_{VCO}}$$

With:

$$F(p) = \frac{1}{1+RCp} \text{ and } \tau = RC$$

$$H_{BF}(p) = \frac{\frac{2\pi}{1+RCp} \cdot K_D K_{VCO}}{p + \frac{2\pi}{1+RCp} \cdot K_D K_{VCO}} = \frac{\frac{2\pi K_D K_{VCO}}{\tau}}{p^2 + \frac{1}{\tau} p + \frac{2\pi K_D K_{VCO}}{\tau}}$$

$$H_{BF}(p) = \frac{\frac{2\pi K_D K_{VCO}}{\tau}}{p^2 + \frac{1}{\tau} p + \frac{2\pi K_D K_{VCO}}{\tau}} = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

The transfer function can be written in the following form:

$$H_{BF}(p) = \frac{\frac{2\pi K_D K_{VCO}}{\tau}}{p^2 + 2\tau(\sqrt{\frac{K_D K_{VCO}}{\tau}})p + \frac{2\pi K_D K_{VCO}}{\tau}} = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

The damping factor is defined by:

$$\zeta = \frac{1}{2\sqrt{2\pi K_D K_{VCO} \tau}}$$

To have a correct stability, it is compulsory to adjust the damping factor with values between 0.4 and 0.7. Under these conditions, it follows that:

$$0.51 < 2\pi K_D K_{VCO} \tau < 1.56$$

6) Transfer function of the third type of low-pass filter and study about the stability of the PLL:

6.1) Third type of low-pass filter transfer function:

The transfer function of the filter is defined as follows:

$$F'(p) = \frac{V_f}{V_r} = \frac{1+R_2Cp}{1+(R_1+R_2)Cp}$$

When we have the following equalities:

$$R_2 = aR,$$

$$(R_1 + R_2) = R,$$

with: $0 < a < 1$,

the transfer function $F'(p)$ can be defined by the relation:

$$F'(p) = \frac{1+aR.Cp}{1+R.Cp}$$

6.2) Study of the phase-locked loop stability and conclusion:

We remember that the transfer function that has been used in question 5 (transfer equation of the circuit shown in Figure E9.3) is defined by:

$$F(p) = \frac{1}{1+RCp}$$

The new transfer function $F'(p)$ can be written as:

$$F'(p) = \frac{1+aR.Cp}{1+R.Cp}$$

$$F'(p) = F(p).(1+aR.Cp).$$

Based on the definition of the new transfer function of the low-pass filter, we can determine the new block diagram of the PLL (see Figure E9.3).

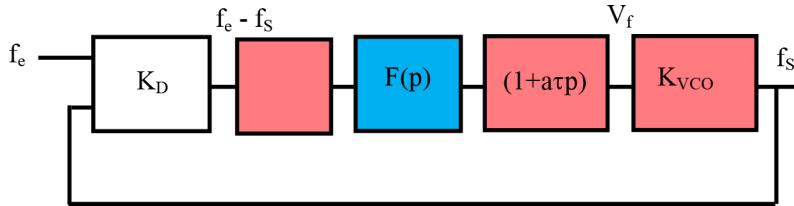


Figure E9.7. PLL block diagram with the low-pass filter of Figure E9.4. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

Here, we find again the action of a corrector with proportional and derivative action. This makes it possible to improve the stability and speed of the PLL.

EXERCISE 10

Consider the phase comparator based on sequential logic circuits. The phase comparator is charged by a low-pass filter, which delivers the control voltage of the voltage-controlled oscillator (Figure E10.1).

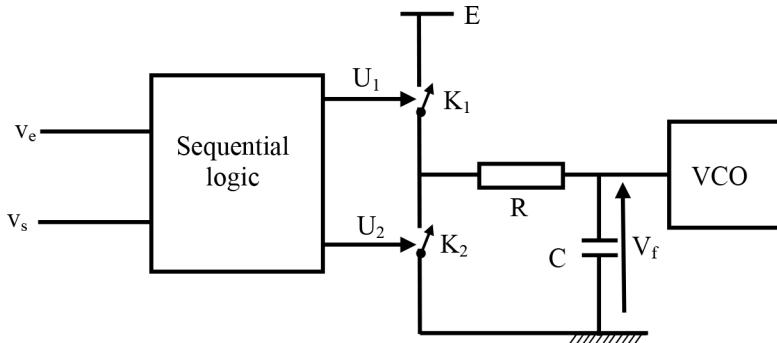


Figure E10.1. Phase comparator under study

It is assumed that at time $t = 0$, the voltage at the terminals of capacitor C is equal to: $V_f = (E/2)$.

From signals v_e and v_s , the sequential logic provides two voltages U_1 and U_2 . These two voltages U_1 and U_2 will control switching on and off switches K_1 and K_2 respectively.

For this purpose, voltages (v_e and v_s) applied to the input of the phase comparator and voltages U_1 and U_2 are schematically presented in Figure E10.2.

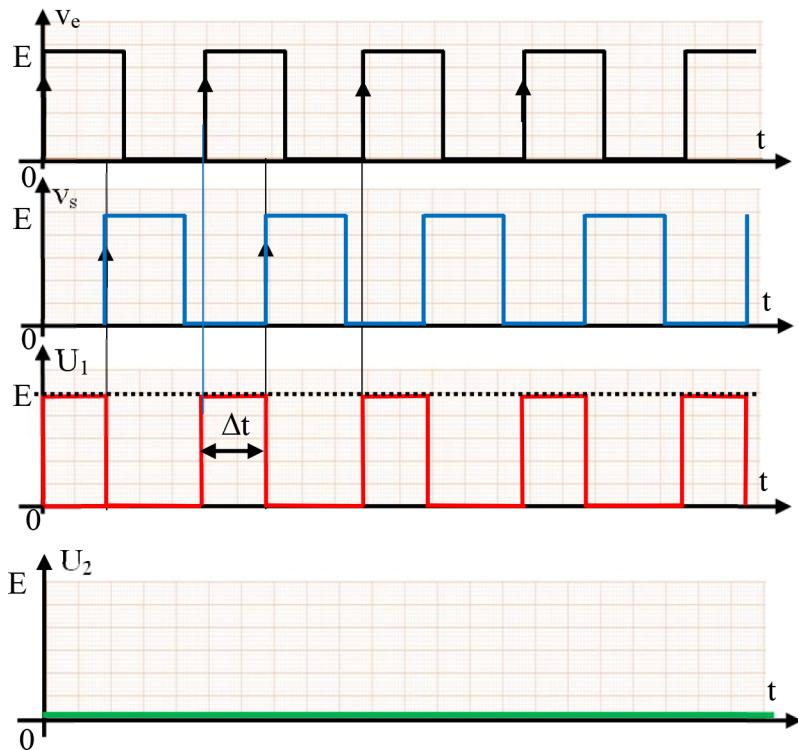


Figure E10.2. Signals at the input of the phase comparator and at the output of the sequential logic

- 1) What is the expression of current i that flows through capacitor C at the initial time $t = 0$?
- 2) It is assumed that the time constant RC is chosen to be very large compared to the period T of signal v_e . It is also assumed that signals v_e and v_s have the same frequency. What is the expression over time of the voltage (V_f) at the terminals of the capacitor?
- 3) What is the expression of the variation ΔV_f of the voltage (V_f) at the capacitor terminals during time Δt ? It is required to represent variations of voltage V_f over at least one period. What is the value of the amplitude of the variation ΔV_f ?

4) The time offset Δt is due to the fact that voltages v_e and v_s are out of phase. What is the relation that links the phase difference ($\Delta\varphi = \varphi_e - \varphi_s$) between v_e and v_s to the amplitude of the variation ΔV_f ?

Numerical application: $E = 12$ V, $R = 68$ k Ω , $C = 2$ μ F, $\Delta t = 0.1$ ms

SOLUTIONS TO EXERCISE 10

1) Expression of current i that flows through capacitor C at time $t = 0$:

At the initial time, switch K_1 switches off as a result of the pulse of voltage U_1 . We thus have:

$$i(t=0) = \frac{E - \frac{E}{2}}{R} = \frac{E}{2R}$$

2) Expression over time of voltage V_f at the terminals of capacitor C:

The expression of the voltage evolution at the capacitor terminals is written as follows:

$$V_f = A e^{\frac{-t}{RC}} + B$$

For $t = 0$, we have $V_f = E/2$ and for $t \rightarrow \infty$, $V_f = E$

$$V_f = E \left(1 - \frac{1}{2} e^{\frac{-t}{RC}}\right)$$

3) Voltage variation (V_f) at the capacitor terminals during the time interval Δt , representation and value of the amplitude of the variation ΔV_f :

3.1) Variation of V_f during the time interval Δt :

It is known that at time $t = 0$, the initial voltage at the terminals of capacitor C has the value:

$$V_f = E/2.$$

The voltage at the capacitor terminals is changing exponentially. After a time equal to Δt , it will have the value:

$$V_f(t = \Delta t) = E \left(1 - \frac{1}{2} e^{\frac{-\Delta t}{RC}}\right)$$

It is also known that the constant load RC is very large compared to the period of signal v_e or of signal v_s . This leads to saying that $\Delta t \ll RC$.

In this situation, the following approximation can be adopted:

$$V_f(t = \Delta t) = E\left(1 - \frac{1}{2}\left(1 - \frac{\Delta t}{RC}\right)\right)$$

$$V_f(t = \Delta t) = \frac{E}{2} \left(1 + \frac{\Delta t}{RC}\right)$$

The variation of the voltage at the capacitor terminals during period Δt :

$$\Delta V_f = V_f(t = \Delta t) - \frac{E}{2}$$

$$\Delta V_f = \frac{E \cdot \Delta t}{2RC}$$

3.2) Representation of variations V_f changes over a period:

It can be noted that voltage V_f starts from an initial voltage equal to $(E/2)$ and linearly varies over time Δt .

The evolution of voltage V_f at the capacitor terminals is presented by the graph in Figure E10.3.

Voltage V_f is the VCO control voltage. It affects the output frequency of this latter.

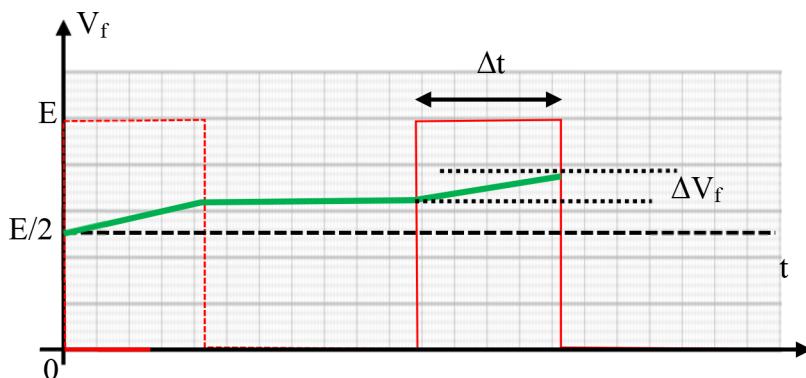


Figure E10.3. Evolution of voltage V_f at the capacitor terminals. For a color version of this figure, see www.iste.co.uk/haraoubia/nonlinear2.zip

3.3) Value of the amplitude of the variation ΔV_f :

We have: $E = 12 \text{ V}$, $R = 68 \text{ k}\Omega$, $C = 2 \mu\text{F}$, $\Delta t = 0.2 \text{ ms}$

$$\Delta V_f = \frac{E \cdot \Delta t}{2RC} = \frac{12.0, 1.10^{-3}}{2.68.0, 2.10^{-3}} = 44 \text{ mV}$$

4) Relation linking the phase difference ($\Delta\varphi = \varphi_e - \varphi_s$) between v_e and v_s to the amplitude of the variation ΔV_f .

The relation between the time offset Δt and the phase difference $\Delta\varphi$ is given by:

$$\Delta\varphi = \frac{2\pi \cdot \Delta t}{T}$$

$$\Delta V_f = \frac{E \cdot \Delta t}{2RC} = \frac{E \cdot \Delta\varphi \cdot T}{4\pi RC}$$

$$\Delta\varphi = \frac{4\pi \cdot \Delta V_f \cdot RC}{E \cdot T}$$