Hardware & Architecture HW #6 – 100 Pts

1. (8 Pts) For a $\overline{S} - \overline{R}$ Flip-Flop
    - **a.** Construct the basic un-clocked Logic Diagram for the circuit functionality
    - **b.** Draw the State Transition Diagram
    - **c.** Create the State Transition Table
    - **d.** Derive the characteristic (next-state) equation

2. (8 Pts) For a $S - R$ Flip-Flop
    - **a.** Construct the Logic Diagram for the circuit functionality
    - **b.** Draw the State Transition Diagram
    - **c.** Create the State Transition Table
    - **d.** Derive the characteristic (next-state) equation

3. (8 Pts) For a Negative-Edge Triggered $J - K$ Flip-Flop with Active-Low Preset and Clear
    - **a.** Draw the State Transition Diagram
    - **b.** Create the State Transition Table
    - **c.** Derive the characteristic (next state) equation
    - **d.** Draw the Block Diagram

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4. (8 Pts) A Positive-Edge Triggered T Flip-Flop toggles the output when the T-Input is high
- **a.** Draw the State Transition Diagram
- **b.** Create the State Transition Table
- **c.** Derive the characteristic (next state) equation
- **d.** Draw the Block Diagram

5. (4 Pts) Create a T Flip-Flop using
- **a.** J-K Flip Flop and basic logic gates, if needed
- **b.** Using a D Flip Flop and basic logic gates, if needed

6. (2 Pt) Design a gated D-latch using only NAND gates and one inverter.

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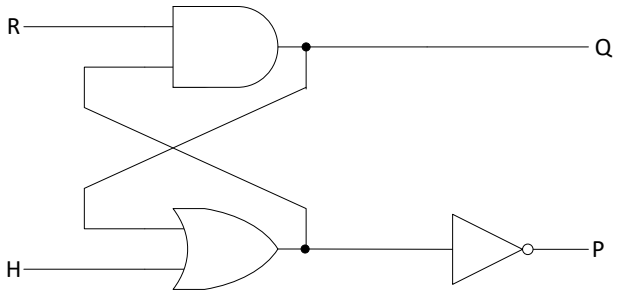
7. (8 Pts) A latch can be constructed from an OR gate, an AND gate, and an Inverter as follows:



- **a.** What restriction must be placed on R and H so that P will always equal Q' (under steady-state conditions)?
- **b.** Draw the State Transition Diagram
- **c.** Construct the State Transition Table
- **d.** Derive the characteristic (next state) equation

8. (16 Pts) A Reset-Dominant Flip-Flop behaves like an S-R Flip-Flop, except that the input S=R=1 is allowed and will cause the Latch to Reset

- **a.** Draw the State Transition Diagram
- **b.** Construct the State Transition Table
- **c.** Derive the characteristic (next state) equation
- **d.** Show how a Reset-Dominant latch can be constructed by adding gate(s) to an S-R latch.
- **e.** Repeat a – d for a Set-Dominant Flip-Flop, where S=R=1 is allowed and will Set the Latch.

9. (6 Pts) Design the following conversions by adding external gates

- **a.** D Flip-Flop to a J-K Flip-Flop
- **b.** T Flip-Flop to a D Flip-Flop
- **c.** T Flip-Flop to a D flip-Flop with Clock Enable

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10. (4 Pts) Design a 4-bit register with Data, Load, Clock, and Clear Inputs using D-Flip-Flops. Draw the circuit and explain the function of the design.

11. (4 Pts) Design a Synchronous Serial–In / Serial–Out clocked 8–bit Shift Register using S–R Flip–Flops and an Inverter. Draw the circuit and explain the function of the design.

12. (24 Pts) A stoplight is basically a 3-State Shift Register that shifts from the "Green" state to the "Yellow" state to the "Red", and back to "Green" state based on a Transition input.

- **a.** Derive the logic equation for the Transition Input.
- **b.** Is the equations for the Transition Input, combinatorial, sequential, or both. Explain
- **c.** Draw the State Transition Diagram for the Stoplight with the Transition Input
- **d.** Derive the State Transition Table for the Stoplight with the Transition Input
- **e.** Derive the characteristic (next state) equations for the Stoplight with the Transition Input