Description	Instruction																			Fla	gs	
1 1 1 2 1 2 1 2	1.01.0		Operandes	_	15	14	13			10	9	8	_	6		3	2 1	0	N	Z	С	V
Logical Shift left	LSLS	Rd	Rm	imm5	0	0	0	0	0			imm5			Rm		Rd		х	х	Х	
Logical Shift right	LSRS	Rd	Rm	imm6	0	0	0	0	1			imm5			Rm		Rd		Х	х	Х	
Arithmetic Shift Right	ASRS	Rd	Rm	imm7	0	0	0	0	0	_	_	imm5			Rm		Rd		Х	Х	Х	
Shift,add,sub,mov ADD rergister	ADDS	Dd	D-	Dm	0	C	C	4	1	0	C		Rm		Rn		Rd		v	V	V	v
SUB rergister	SUBS	Rd Rd	Rn Rn	Rm Rm	0	0	0	1	1	0	0		Rm		Rn		Rd		x	x x	X X	x
ADD-immediate	ADDS	Rd	Rn	imm3	0	0	0	1	1	1	0		imm3		Rn		Rd		x	x	x	x
SUB-immediate	SUBS	Rd	Rm	imm3	0	0	0	1	1	1	0		imm		Rn		Rd		X	X	x	×
MOV-immediate	MOVS	Rd	Kill	IIIIII	0	0	1	0	0	Ė	U	Rd		,	- 10		nm8		x	x	^	
CMP-immediate	CMP	Rd			0	0	0	0	0			Rd					nm8		x	x	х	х
ADD-immediate 8bits	ADDS	Rd			0	0	1	1	0			Rd					nm8		x	x	х	x
SUB-immediate 8bits	SUBS	Rd			0	0	1	1	1			Rd					nm8		x	x	х	x
Data processing																						
AND Bitwise	AND	Rdn	Rm		0	1	0	0	0	0	0	0	0	0	Rn	n	Rdn		x	х	x	
EXCLUSIVE OR	EOR	Rdn	Rm		0	1	0	0	0	0	0	0	0	1	Rn	n	Rdn		x	х	x	
Logical-Shift-Left	LSL	Rdn	Rm		0	1	0	0	0	0	0	0	1	0	Rn		Rdn		x	х	х	
Logical-Shift-Right	LSR	Rdn	Rm		0	1	0	0	0	0	0	0	1	1	Rn		Rdn		x	х	х	
Arithmetic-Shift-Right	ASR	Rdn	Rm		0	1	0	0	0	0	0	1	0	0	Rn		Rdn		x	х	х	
ADD with Carry	ADC	Rdn	Rm		0	1	0	0	0	0	0	1	0	1	Rn		Rdn		x	х	х	
Substract with Carry	SBC	Rdn	Rm		0	1	0	0	0	0	0	1	1	0	Rn		Rdn		Х	Х	Х	x
Rotate Right	ROR	Rdn	Rm		0	1	0	0	0	0	0	1	1	1	Rn		Rdn		Х	Х	Х	
Set Flags on Bitwise AND	TST	Rn	Rm		0	1	0	0	0	0	0	0	0	0	Rn		Rn		X	Χ	X	
Reverse Substract from 0 Compare Registres	RSB CMP	Rd Rn	Rn		0	1	0	0	0	0	1	0	0	0	Rn Rn		Rd Rn		X	X	X	×
Compare Registres Compare Negative	CMN	Rn Rdn	Rm Rm		0	1	0	0	0	0	1	0	1	1	Rn		Rn Rn		x	x x	X X	x
Logical OR	ORR	Rdn	Rm		0	1	0	0	0	0	1	1	0	0	Rn		Rdn		x	x	x	^
Multiply two registres	MUL	Rdm	Rn		0	1	0	0	0	0	1	0	0	0	Rn		Rdm		X	X	^	
Bit Clear	BIC	Rdn	Rm		0	1	0	0	0	0	1	1	1	0	Rn		Rdn		x	x	x	
Bitwise NOT	MVN	Rd	Rm		0	1	0	0	0	0	1	1	1	1	Rn		Rd		x	x	х	