ISPD 2019 Initial Detailed Routing Contest and Benchmark with Advanced Routing Rules

Wen-Hao Liu, Stefanus Mantik, Wing-Kai Chow, Yixiao Ding,
Amin Farshidi, Gracieli Posser
Cadence Design Systems, USA
{ whliu, smantik, wkchow, yxding, afarshid, gposser }@cadence.com

ABSTRACT

Detailed routing becomes the most complicated and runtime consuming stage in the physical design flow as technology nodes advance. Due to the inaccessibility of advanced routing rules and industrial designs, it is hard to conduct detailed routing academic researches using the modern real-world designs. ISPD18 hosts the first detailed routing contest [1] and releases a set of benchmarks synthesized by industrial tools with practical routing rules. ISPD18 contest spurs detailed routing researches and provides students the opportunity to become familiar with the industrial designs and rules. On top of ISPD18 detailed routing contest, we host another detailed routing contest in ISPD19 [2] to consider several advanced routing rules and make the contest problem one step closer to the real-world routing challenges in advanced technology nodes. ISPD19 detailed routing contest encourages participants to use double-cut vias to improve yield and result quality. In addition, in order to drive the development of efficient routing frameworks, the deterministic multithreading feature is encouraged but optional in this contest.

ACM Reference Format:

Wen-Hao Liu, Stefanus Mantik, Wing-Kai Chow, Yixiao Ding, Amin Farshidi, Gracieli Posser. 2019. ISPD 2019 Initial Detailed Routing Contest and Benchmarks with Advanced Routing Rules. In ISPD '19: 2019 International Symposium on Physical Design, April 14–17, 2019, San Francisco, CA, USA. ACM, New York, NY, USA, 5 pages.

https://doi.org/10.1145/3299902.3311067

1 INTRODUCTION

When technology node advances with more complex design rules, routing problem becomes more and more challenging. Particularly, detailed routing plays a very important role for new node enablement. If detailed routing is not able to find solutions satisfying all design rules, new node enablement will be delayed. Therefore, industry invests a lot of resources on improving detailed routing engines to pursue the routing solutions with better timing, lower power and lower design-rule-checking violations (DRVs). However, due the lack of real-world testcases and the design rule information, it is hard to conduct the up-to-date academic research to tackle the modern detailed routing challenges.

To spur detailed routing research from academia, Cadence hosts the first ISPD contest on detailed routing problem in 2018 [1]. In this contest, the benchmarks synthesized by industrial tools are released, which consider the practical routing rules like spacing table, cut spacing, end-of-line spacing, and min-area rules. In addition, the global routing guide associated with each benchmark is provided, and detailed routers are required to honor the routing guides as much as possible while minimizing DRVs.

ISPD18 contest leads to development of several academic detailed routers [3-5]. The work in [3] proposes a negotiation-based rip-up-and-rerouting scheme with via-aware track assignment; TritonRoute [4] presents a mixed integer-linear programing based routing framework; and the router presented in [5] adopts a minimum-area-captured path search algorithm to find the routing paths obeying routing rules. The routers presented in [3-5] all have multithreading features and are able to obtain deterministic routing results. They have also discussed how to efficiently use memory to handle large-scale designs. With these innovations, the academic detailed routers become more practical to handle real-world designs. Accordingly, the DATC Robust Design Flow (RDF) project [6] can integrate these routers to enable an academic flow from logic synthesis to detailed routing, which builds a foundation for future EDA researches.

On top of ISPD18 initial detailed routing contest, we host another detailed routing contest in ISPD19 to consider several advanced routing rules and objectives to make the contest problem one step closer to the real-world routing challenges faced in advanced nodes. The extensions of this year's contest are listed below:

(1) This contest considers the advanced routing rules including parallel run spacing, adjacent cut spacing, and corner-to-corner spacing, which are common to see in sub-16nm designs.

ISPD '19, April 14–17, 2019, San Francisco, CA, USA

ACM ISBN 978-1-4503-6253-5/19/04…$15.00
https://doi.org/10.1145/3299902.3311067

(2) To improve yield, reality, and timing, double-cut vias are widely used in industrial designs. In this contest, we provide double-cut via library and encourage contest participants to use double-cut vias.
(3) The benchmarks used in this contest have power and ground (PG) structures. The PG structure may occupy a lot of routing resources and make the routing problem more difficult. Detailed routers need to efficiently handle the required spacing between routing wires and PGs; otherwise they may easily trigger spacing violations.
(4) This contest generates diverse benchmarks from either commercial place-and-route tool Innovus [7] or academic DATC RDF flow [6].
(5) During contest evaluation process, we set tighter runtime limit for each benchmark based on its design size. We try to encourage the development of more efficient and scalable routing framework.

The remaining sections are organized as follows. Section 2 gives the overview of ISPD18 contest problem. Section 3 introduces the new rules and extensions considered in ISPD19 contest. In Section 4, the evaluation metrics used in this contest are detailed. Section 5 describes how the benchmarks are generated. Finally, acknowledgement is presented in Section 6.

2 OVERVIEW OF ISPD18 CONTEST

ISPD18 initial detailed routing contest assumes that a given global routing result is already well optimized for certain metrics (e.g., congestion and timing). Then, a detailed router needs to honor the global routing result in order to keep the optimized metrics and meanwhile avoid DRVs. In addition, the following connectivity constraints, routing rules, and detailed routing metrics are considered in ISPD18 contest:

- Open
- Short
- Spacing Table
- End-of-line spacing
- Cut spacing
- Min area rule
- Global routing guide honoring
- Wrong-way routing minimization
- Off-track routing minimization
- Wirelength and via minimization
- Multithreading determinism

For more details of these rules and metrics, please refer to the ISPD18 contest paper [1]. Also, the details of rule representation can be found in the LEF/DEF document [8]. Note that different technology nodes, different foundries, or different designs may have different routing rules. ISPD18 contest only consider the most common and major routing rules.

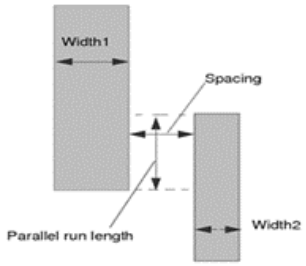

Fig. 1. Example of parallel run spacing

3 NEW RULES AND OBJECTIVES CONSIDERED IN ISPD19 CONTEST

A detailed router is subject to various design rules to satisfy manufacturing requirements from the foundries. In various technology nodes, the design rules are usually different. In ISPD19 contest, we further consider several advanced spacing rules which are very common and critical to handle during the initial detailed routing. In addition, we consider double-cut via insertion as one of our objectives. We believe the contest will be more practical and challenging by applying the rules and objective described in this section.

3.1 Advanced Spacing Rules

The new routing rules considered in this year's contest include parallel run spacing, adjacent cut spacing, and corner-to-corner spacing rules. The violations triggered by these rules cannot be easily detected just based on the distances between two objects. The required spacing values from these rules are *dynamic*, which may be affected by the routing length, other objects, or the routing directions. Accordingly, the difficulty of detailed routing increases dramatically after those advanced spacing rules emerge.

3.1.1 Parallel Run Spacing

Spacing table in LEF file specifies the required spacing between two objects according to the parallel-run length between two objects and the widths of the objects. Parallel-run length is the projection length between two objects. Figure 1 illustrates how the width, parallel-run length, and the required spacing are defined in the spacing table. In general, the spacing table contains multiple length thresholds. Once the parallel-run length is over a bigger length threshold, larger required spacing will be triggered.

3.1.2 Adjacent Cut Spacing

The adjacent cut rule specifies the minimum spacing allowed between via cuts on the same net or different nets when the cut has two, three, or four via cuts that are

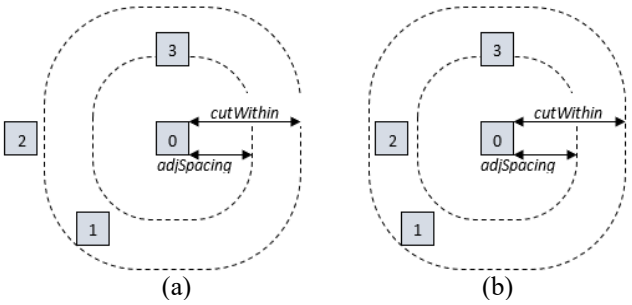

Fig. 2. Example of adjacent cut spacing rule

less than *cutWithin* distance, in microns, from each other as illustrated in Figure 2. A cut is considered adjacent if it is within *cutWithin* distance of another cut in any direction (including a 45-degree angle). Figure 2(a) shows cut #0 has only two neighboring cuts, which satisfy adjacent-cut-3 rule, while Figure 2(b) shows the same cut but with three neighboring cuts, which will violate the adjacent-cut-3 rule.

3.1.3 Corner-to-corner Spacing

The rule specifies the required spacing between a convex corner and any edge. The spacing value is calculated in MAXXY method. Specifically, given two rectangular objects R1(lx, ly, ux, uy) and R2(lx, ly, ux, uy). Let dX be the corner-to-corner distance between two objects in X direction. Then, dX = max((R1.lx - R2.ux), (R2.lx - R1.ux)). Similarly, let dY be the corner-to-corner distance between two objects in Y direction. Then, dY = max((R1.ly - R2.uy), (R2.ly - R1.uy)) Then, the MAXXY distance between the two objects is: max(dX, dY). The rule is only triggered when the parallel run length between two objects is less than or equal to 0. In addition, if the width of the object containing the corner is greater than width value specified in the table, then the corresponding spacing is applied. The optional keyword EXCEPTEOL specifies that the corner-to-corner spacing rule does not apply to a corner which is an end-of-line (EOL) edge with width less than a predefined width *eolWidth*.

Figure 3 shows three different routing configurations. Figure 3(a) shows the routing configuration that needs to meet the corner-to-corner spacing rule where the spacing required is governed by the width of the wide metal (width = 0.15) and the spacing is measured in MAXXY fashion. Configuration in Figure 3(b) will not have corner spacing violation if the rule has the EXCEPTEOL 0.080 keyword where the rule is exempted due to end-of-line edge less than 0.080 that is adjacent to the corner (which applies to both the lower metal and the upper metal). Figure 3(c) shows a routing configuration that does not have any corner spacing violation. In this case, the parallel run length between the convex corner of the wide metal and the nearby wire is greater than 0, thus the corner spacing rule does not apply.

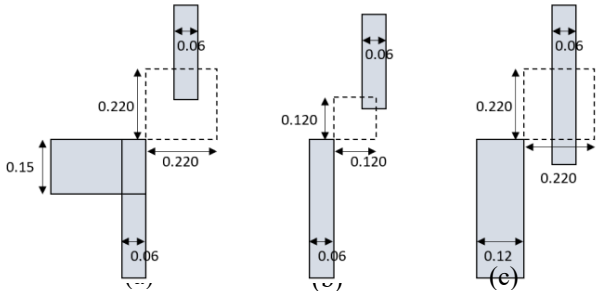

Fig. 3. Example of corner-to-corner spacing rule

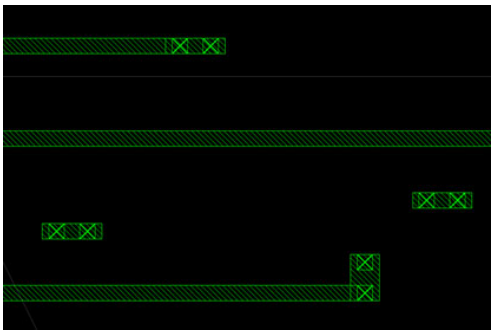

Fig. 4. Example of using double-cut vias

3.2 Double-Cut Via Insertion

For reality and performance concerns, detailed routers prefer to use double-cut/multi-cut vias rather than single-cut vias [9, 10]. This contest will provide both double-cut and single-cut vias in the via library. During solution evaluation, single-cut vias will be more expansive than double-cut vias in order to encourage the usage of double-cut vias. In addition, for some situations, min-area rule can be satisfied by using double-cut vias carefully. Figure 4 shows an example of using double-cut vias.

4 EVALUATION METRICS

In this contest, we have set a 64GB restriction on memory usage for the routers. Each benchmark has a specific runtime limit ranging between 1 hour and 12 hours, depending on the routing difficulty. A routing solution is considered as valid if the solution output is in the correct DEF format and there is no open net.

The solution quality is measured with Eq. (1). A router which produces a routing solution with lower *scaled_score* is considered as better in this contest.

$$scaled\_score = original\_score * (1 + np + rf) \quad (1)$$

TABLE 1 EVALUATION METRICS

Metric	Weight
Shorted metal / cut area	500
Number of shorted metal / cut	500
Number of min-area violations	500
Number of parallel run length violations	500
Number of EOL spacing violations	500
Number of cut spacing violations	500
Number of corner spacing violations	500
Total length of out-of-guide wires	1
Total number of out-of-guide vias	1
Total length of off-track wires	0.5
Total number of off-track vias	1
Total length of wrong-way wires	1
Total number of multi-cut vias	2
Total number of single-cut vias	4
Total length of wires	0.5

where *original_score* represents the result quality of a given detailed routing solution, *np* denotes the non-deterministic penalty, and *rf* denotes a runtime factor.

- The *original_score* is measured by the weighted sum of the metrics shown in Table 1, which is computed by the released evaluator [2], and Cadence P&R tool Innovus [7] is used to verify DRC violations. Note that the lengths in Table 1 use one M2 pitch size as one unit.
- The non-deterministic penalty score reflects the debugging and maintenance difficulty for a non-deterministic router. We run a router multiple times for each benchmark. If we observe different results among different runs, the median *scaled_score* will be chosen and 3% of non-deterministic penalty score will be added to the final score for the benchmark. Otherwise, if the results are consistent among different runs, no non-deterministic penalty will apply. Namely, *np* in Eq. (1) will be zero.
- The runtime factor *rf* is defined in Eqs. (2) and (3), where *rwt*(*b*) represents the wall time of a detailed router for benchmark *b*, and *mwt*(*b*) represents the median wall time of all submitted detailed routers from contestants for the benchmark *b*. The runtime factor is limited between -0.1 and +0.1.

$$rf = \min(0.1, \max(-0.1, f)) \quad (2),$$

$$f = 0.02 * \log_2(rwt(b) / mwt(b)) \quad (3).$$

5 BENCHMARKS

The testcases used for the contest benchmarks are derived from three real-world designs, a single-core 32-bit processor with four memory cores, a quad-core 32-bit processor with 16 on-chip memory blocks, and a dual-tone multi-frequency encoder/decoder. The original sizes for the designs are 37k nets, 147k nets, and 9k nets, respectively. The designs are synthesized using generic 28nm cell libraries. Cadence Genus [11] and Innovus [7] are used to perform logic synthesis, floorplanning, and placement on the designs. In addition, two designs are adapted from the 2015 ISPD Blockage-Aware Detailed Routing-Driven Placement Contest Benchmarks [12] with 65nm cell libraries. These two designs are placed using the placement engine from DATC RDF [6]. In order to be used as benchmarks for the contest, we simplify the designs, so they pertain to the core essence of the contest while still maintaining the accuracy of the initial design intent. The followings are the simplification steps done on the designs:

- Non-default rules are removed to reduce the additional complexity introduced by wide wires.
- Since the primary goal for this contest is DRC cleanliness and wirelength, timing related information is removed.
- Only design rules listed in previous section are kept and the remaining is removed.

TABLE 2 BENCHAMRK INFORMATION

	#std	#blk	#net	#pin	#layer
ispd19_sample	22	0	11	0	9
ispd19_sample2	22	1	16	0	9
ispd19_sample3	5	1	7	5	16
Ispd19_sample4	67	0	22	0	9
ispd19_test1	8879	0	3153	0	9
ispd19_test2	72094	4	72410	1211	9
ispd19_test3	8283	4	8953	57	9
ispd19_test4	146442	7	151612	4802	5
ispd19_test5	28914	6	29416	360	5
ispd19_test6	179881	16	179863	1211	9
ispd19_test7	359746	16	358720	2216	9
ispd19_test8	539611	16	537577	3221	9
ispd19_test9	899341	16	895253	3221	9
ispd19_test10	899404	0	895253	3221	9

Table 2 shows the benchmark information, where #std, #blk, #net, #pin, and #layer denote the number of standard cells, macro blockages, nets, IO pins, and metal layers, respectively. The sample benchmarks (ispd19_sample*) are derived from the original single-core design. The nets are selected randomly. A placement run is called for the selected instances that are connected to those selected nets to produce a compact floorplan. These testcases will be used as a sample for the contestants to make sure their binary is able to read the design data correctly and perform the initial detailed routing process. These sample tests will not be used for evaluation purpose. On the other hand, "ispd19_test*" are the official benchmarks used to evaluate and rank the detailed routers developed by the contestants.

6 ACKNOWLEDGEMENT

We would like to thank the following people: Patrick Haspel, Cheryl Mendenhall, Anton Klotz, Sai Durga Dasu, Tracy Zhu, Shraddha Susarla and Kira Jones from Cadence Academic Network for the great support on the Innovus licenses and also on the contest and ISPD promotion; Neal Chang from Chip Implement Center (CIC) in Taiwan for helping universities to setup Cadence licenses; Yufeng Luo, Mehmet C. Yildiz, Zhuo Li, Chuck Alpert, Jing Chen, and Ismail S. Bustany for their insight and help on this contest; Jinwook Jung and Iris Hui-Ru Jiang for helping creating two benchmarks using DATC RDF; Guilherme A. Flach, Jucemar Monteiro and Mateus Fogaça for the adjustments on Rsyn academic tool to support the requirements for this contest and help students get the setup easily.

REFERENCES

[1] Stefanus Mantik, Gracieli Posser, Wing-Kai Chow, Yixiao Ding, Wen-Hao Liu, ISPD 2018 Initial Detailed Routing Contest and Benchmarks, In Proc. of the International Symposium on Physical Design (ISPD), p.140-143, March 25-28, 2018, Monterey, California, USA.

[2] ISPD19 Contest website: http://www.ispd.cc/contests/19/index.htm

[3] Fan-Keng Sun, Hao Chen, Ching-Yu Chen, Chen-Hao Hsu, Yao-Wen Chang, A multithreaded initial detailed routing algorithm considering global routing guides, In Proc. of the International Conference on Computer-Aided Design (ICCAD), p.1-7, November 05-08, 2018, San Diego, California, USA.

[4] Andrew B. Kahng, Lutong Wang, Bangqi Xu, TritonRoute: an initial detailed router for advanced VLSI technologies, In Proc. of the International Conference on Computer-Aided Design (ICCAD), p.1-8, November 05-08, 2018, San Diego, California, USA.

[5] Gengjie Chen, Chak-Wa Pui, Haocheng Li, Jingsong Chen, Bentian Jiang, Evangeline F. Y. Young. Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search, In Proc. of the Asia and South Pacific Design Automation Conference (ASPDAC), p.754-760, January 21-24, 2019, Tokyo, Japan.

[6] Jinwook Jung, Iris Hui-Ru Jiang, Jianli Chen, Shih-Ting Lin, Yih-Lang Li, Victor N. Kravets, Gi-Joon Nam, DATC RDF: an academic flow from logic synthesis to detailed routing, In Proc. of the International Conference on Computer-Aided Design (ICCAD), p.1-4, November 05-08, 2018, San Diego, California, USA.

[7] Cadence P&R Tool Innovus: https://www.cadence.com/content/cadence-www/global/en_US/home/tools/digital-design-and-signoff/hierarchical-design-and-floorplanning/innovus-implementation-system.h

[8] Cadence, Inc. LEF/DEF 5.3 to 5.8 exchange format: www.si2.org/openeda.si2.org/projects/lefdef

[9] Yixiao Ding, Chris Chu and Wai-Kei Mak, Self-Aligned Double Patterning-Aware Detailed Routing With Double Via Insertion and Via Manufacturability Consideration, In IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 37, no. 3, p.657-668, March 2018.

[10] Youngsoo Song, Jinwook Jung, Daijoon Hyun, and Youngsoo Shin, Timing optimization in SADP process through wire widening and double via insertion, In Proc. of Design-Process-Technology Co-optimization for Manufacturability XII (SPIE 10588), 105880R, March 20, 2018, San Jose, California, US.

[11] Cadence logic synthesis tool: https://www.cadence.com/content/cadence-www/global/en_US/home/tools/digital-design-and-signoff/synthesis/genus-synthesis-solution.html

[12] Ismail S. Bustany, David Chinnery, Joseph R. Shinnerl, Vladimir Yutsis, ISPD 2015 Benchmarks with Fence Regions and Routing Blockages for Detailed-Routing-Driven Placement, In Proc. of the International Symposium on Physical Design (ISPD), p.157-164, March 29 – April 01, 2015, Monterey, California, USA.