ISPD 2018 Initial Detailed Routing Contest and Benchmarks

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ABSTRACT

In advanced technology nodes, detailed routing becomes the most complicated and runtime consuming stage. To spur detailed routing research, ISPD 2018 initial detailed routing contest is hosted and it is the first ISPD contest on detailed routing problem. In this contest, the benchmarks synthesized by industrial tool and library are released, which consider the design rules like spacing table, cut spacing, end-of-line spacing, and min-area rules. In addition, the global routing guide is provided associated to each benchmark, and detailed routers are required to honor the routing guides as much as possible meanwhile minimize design-rule-checking (DRC) violations. The biggest benchmark released in this contest has near-millions of nets, so the runtime and memory scalability for detailed routers need to be well addressed. To reduce routers' runtime, the deterministic multithreading framework is encouraged but optional in this contest.

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1 INTRODUCTION

Every new technology node comes with more complex design rules making the routing stage become more and more challenging, and so the routability awareness becomes more critical in the physical design flow [1-5]. Due to the enormous computational complexity, routing typically is divided into two stages: global routing and detailed routing.

In global routing, the entire routing region is divided into regular global cells and routing is performed based on these global cells. The obtained global routing results are used to generate detailed routing solution considering exact metal shapes and positions in the detailed routing stage.

The detailed routing stage can be further divided into two steps. First, an initial detailed routing step implements physical wires and vias from the global routing result while handling the major routing rules. Then, a detailed routing refinement step is performed to fix the remaining complicated DRC violations. The ISPD contest of this year focuses on the initial detailed routing step.

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Assuming that a global routing result is already well optimized for certain metrics (e.g., congestion and timing [6, 7]), a detailed router needs to honor the global routing result in order to keep the optimized metrics. In addition, to minimize the net topology disturbance contributed by the later detailed routing refinement step, the initial detailed routing step needs to consider the major routing rules. If the initial detailed routing solution can meet the most common routing rules even it is not fully DRC clean, the later detailed routing refinement step will have less chance to largely disturb the routing solution. Therefore, the initial detailed routing need to obey the "guide" from global routing as much as possible and at the same time minimize DRC violations [8, 9, 10].

Although detailed routing has been studied extensively in the literature, there are still various challenges that make it difficult to apply the existing academic algorithms to modern industrial designs. The ISPD contest of this year aims at exposing some of the industrial detailed routing challenges to the academic community, while keeping the problem complexity reasonable to drive practical detailed routing researches. The contributions of this contest are listed below:

(1) Currently the detailed-routing researches take different objectives and test cases making hard to compare the performance of different routers [11-16]. This contest provides realistic industrial benchmarks with the common design rules as a standard to more fairly evaluate the effectiveness of the detailed-routing researches.
(2) This contest provides contestants the license of Cadence P&R tool Innovus [17] to evaluate and debug their routing solutions, which gives them the opportunity to combine their academic researches with industrial tool, producing more realistic results.
(3) In the physical design flow, detailed routing is one of the most complicated and time-consuming stages. Although the works [11-16] attempt to address the advanced routing issues, the problem instances adopted in these works are much smaller than the real industrial designs. By releasing the benchmarks with near millions of nets, this contest aims to drive detailed routing researches to have practical scalability in terms of runtime and memory.
(4) In this contest, the comprehensive routing issues and the common routing rules are considered. In order to obtain good routing solutions, contestants need to co-optimize routing strategy, pin access, DRC handling, routing guide honoring, and multithreading scheduling. Handling all of these constraints gives contestants a better understanding of the routing challenges on industrial designs.

The remaining sections are organized as follows. Section 2 describes the problem for the initial detailed routing contest. In Section 3, the evaluation metrics used in the contest are detailed. Section 4 introduces the benchmark information. Finally, acknowledgement is presented in Section 5.

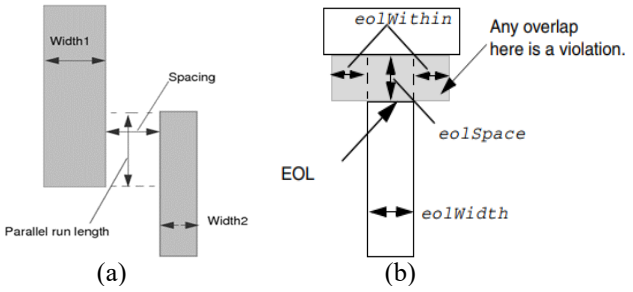

Fig. 1. (a) Example of spacing table; (b) Example of end-of-line (EOL) spacing.

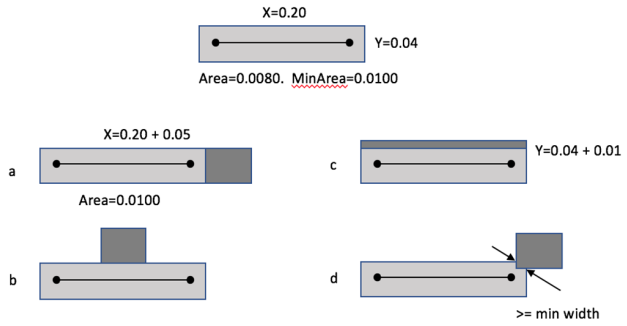

Fig. 2. Example of adding patch metal to satisfy min-area rule. (a), (b), and (c) are valid patch metal insertion solution, while (d) is an invalid solution.

2 PROBLEM DESCRIPTION

This contest evaluates the quality of detailed routing solutions from the following aspects:

(1) Connectivity constraints
(2) LEF routing rules
(3) Routing preference metrics

According to these constraints/rules/metrics, we will come out a score for a given detailed routing solution, and ranking of each participated team for the contest will be based on the scores. The details of these constraints/rules/metrics will be introduced in this section, and scoring method will be introduced in Section 3. Because this contest uses LEF/DEF format to represent the problem instances, the details of rule representation can be found in [18].

2.1 Connectivity Constraints

The connectivity constraints have to be satisfied in order to guarantee the valid signal and the routing wires that are able to be implemented. Therefore, the connectivity constraints have the highest priority to be obeyed.

2.1.1 Open

The pins of each net defined in DEF file need to be fully connected. If any pin in a net is disconnected, the net will be considered as an open net and the routing solution is invalid.

2.1.2 Short

A short violation will happen when either a via metal or wire metal overlaps with another object like via metal, wire metal, blockages, or pin shapes. The intersection part between two objects is the short area.

2.2 LEF Routing Rules

A detailed router need to consider many routing results defined in LEF files in order to meet the manufacturing requirements from foundries. Different technology nodes, different foundries, or different designs may have different routing rules. In this contest, we only consider the most common and major routing rules.

2.2.1 Spacing Table

Spacing table in LEF file specifies the required spacing between two objects according to the parallel-run length between two objects and the widths of the objects. Parallel-run length is the projection length between two objects. Figure 1(a) illustrates how the width, parallel-run length, and the required spacing are defined in the spacing table. In general, the spacing table contains multiple length thresholds. Once the parallel-run length is over a bigger length threshold, larger required spacing will be triggered. For the simplicity of the contest, we reduce the number of length thresholds into one. Thus, the spacing value remain the same regardless of the parallel-run length as long as it is greater than zero. Namely, in this contest, the spacing value defined in the spacing table only depends on the width of the objects.

2.2.2 End-of-line Spacing

The end-of-line (EOL) spacing rule indicates that an edge that is shorter than *eolWidth*, noted as end-of-line edge requires spacing greater than or equal to *eolSpace* beyond the EOL anywhere within (that is, less than) *eolWithin* distance (see Figure 1(b)). Typically, *eolSpace* is slightly larger than the minimum allowed spacing on the layer. The *eolWithin* value must be less than the minimum allowed spacing.

2.2.3 Cut Spacing

The cut spacing rule specifies the minimum spacing allowed between via cuts on the same net or different nets.

2.2.4 Min Area Rule

The min area rule specifies the minimum metal area required for polygons on each layer. All polygons must have an area that is greater than or equal to the specified area value.

When a routed metal segment is small such that the whole polygon area does not satisfy the min area rule, a patch metal can be added to increase the area for the polygon. See Figure 2(a) to 2(c) for possible patch solution added to the existing metal routing to satisfy min area rule. However, the location and the size of the patch metal must be decided carefully so it will not cause any spacing or short violation. In addition, the overlapping region between patch and the existing metal routing must be greater or equal to the minimum *width* of the current routing layer (see Figure 2(d)).

2.3 Routing Preference Metrics

There are several metrics generally used to evaluate the quality of a detailed routing solution. Although they are not hard rules, the quality of a routing solution usually could be better in terms of timing, routability, and manufacturability if the detailed router considers these metrics.

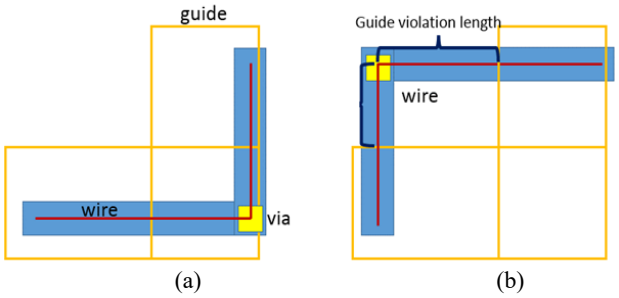

Fig. 3. (a) guide-violation-free routing solution; (b) guide-violation routing solution.

2.3.1 Routing Guide Honoring

In the typical routing flow, global routing performs followed by detailed routing. A global routing result is usually well optimized for certain metrics, a detailed router needs to honor the global routing result as much as possible in order to minimize the disturbance to these metrics. In this contest, each benchmark has a guide file in which every net associates to a list of rectangles. The list of rectangles is called global routing guide (yellow rectangles in Fig. 3) to represent the regions passed by the global routing result of the associated net, and the global routing guide guarantees to contain at least a fully connected detailed routing solution for the net. If the center lines (red lines in Fig. 3) of wires or the coordinate of vias route outside of the guide, they will be considered as a guide violation; if wires or vias route inside or just on the boundaries of the rectangles, there is no guide violation. For example, Fig. 3(a) shows a routing solution without guide violations, while Fig. 3(b) shows a routing solution with guide violations for both via and wires. The score penalty will be applied based on the number of vias and the length of wires are routed out of guides. Note that, routing guide honoring does not consider patch metals. Namely, patch metals can put out of guides without the penalty.

2.3.2 Wrong-way Routing

Each metal layer has a preferred routing direction defined in LEF file, which is either horizontal or vertical. If a wire routes horizontally (vertically) on a vertical (horizontal) layer, the wire is considered as a wrong-way wire. The length of wrong-way wires will contribute as a penalty to the scoring function.

2.3.3 Off-track Routing

Each metal layer has a track structure defined in DEF files. The routing wires that align with tracks is so called on-track wires; otherwise, the wires are off-track wires. Also, a via is considered as an on-track via when the coordinate of the via aligns with the tracks on its both bottom and top layers. The length of off-track wires and the number of off-track vias will be considered as a penalty in the scoring function.

2.3.4 Multithreading Determinism

When design scale increases, the multithreading technique becomes an important feature to a detailed router. In this contest, we will evaluate the detailed routers on a machine with 8 CPUs, so multithreading technique is encouraged but optional. However, multithreading technique is easier to cause nondeterministic issue. Because nondeterministic behavior will increase the maintenance effort largely for a detailed router, it is better to be avoided.

TABLE 1 EVALUATION METRICS

Metric	Weight
Short metal area	500
Number of spacing violations	500
Number of min-area violations	500
Total length of the wires outside of the routing guides	1
Total number of the vias outside of routing guides	1
Total length of off-track wires	0.5
Total number of off-track vias	1
Total length of wrong-way wires	1
Total number of vias	2
Total length of wires	0.5

3 EVALUATION METRICS

In this contest, a routing solution is treated as a valid solution only when the memory and runtime usage of the proposed router is respectively under 64G and 12 hours, and the solution has no open net. The quality of a valid routing solution is measured by Eq. (1). A router which can obtain a solution with a smaller scaled_score is considered as a better router in this contest.

$$\text{scaled\_score} = \text{original\_score} * (1 + np + rf), \quad (1),$$

where original_score represents the result quality of a given detailed routing solution, *np* denotes the nondeterministic penalty, and *rf* denotes a runtime factor.

- The original score is measured by the weighted sum of the metrics shown in Table 1, which is computed by the released evaluator [19], and Cadence P&R tool Innovus [17] is used to verify DRC violations. Note that, the length unit used in Table 1 is the number of M2 pitches.
- The nondeterministic penalty is to reflect the debugging and maintenance difficulty for a nondeterministic router. We will run multiple times of a router for a benchmark, and pick the median scaled_score as the final score for the benchmark. If we observe nondeterministic results, nondeterministic penalty will be set to 3%; otherwise, it will be 0.
- The runtime factor *rf* is defined in Eqs. (2) and (3), where *rwt*(*b*) represents the wall time of a detailed router for benchmark *b*, and *mwt*(*b*) represents the median wall time of all submitted detailed routers from contestants for the benchmark *b*. The runtime factor is limited within 0.1 and -0.1.

$$rf = \min(0.1, \max(-0.1, f)) \quad (2),$$
$$f = 0.02 * \log_2(\text{rwt}(b) / \text{mwt}(b)) \quad (3),$$

4 BENCHMARKS

The test cases used for the benchmark are derived from two real designs, a single-core 32-bit processor with four memory cores and a quad-core 32-bit processors with 16 on-chip memory blocks. The original size for the designs are 37k nets and 147k nets respectively. The designs are synthesized using generic 45nm and 32nm technology and cell libraries. Cadence Genus [20] and Innovus [17] are used to perform logic synthesis, floorplan, and placement on the designs. In order to be used as benchmarks for the contest, we simplify the designs so they pertain to the core essence of the contest while still maintaining

TABLE 2 BENCHAMRK INFORMATION

	#std	#blk	#net	#pin	#layer
ispd18_sample	22	0	11	0	9
ispd18_sample2	22	1	16	0	9
ispd18_sample3	5	1	7	5	16
ispd18_test1	8879	0	3153	0	9
ispd18_test2	35913	0	36834	1211	9
ispd18_test3	35973	4	36700	1211	9
ispd18_test4	72090	4	72410	1211	9
ispd18_test5	71946	8	72394	1211	9
ispd18_test6	107919	0	107701	1211	9
ispd18_test7	179865	16	179863	1211	9
ispd18_test8	191987	16	179863	1211	9
ispd18_test9	192911	0	178858	1211	9
ispd18_test10	290386	0	182000	1211	9

the accuracy of the initial design intent. The followings are the simplification steps done on the designs.

- Power and ground nets are removed due to the complexity of the special nets representation in DEF.
- Non-default rules are removed to reduce the additional complexity introduced by wide wires.
- Since the primary goal for this contest is DRC cleanliness and wirelength, timing related information are removed.
- For the purpose of the initial detailed routing contest, some design rules are also simplified into a regular spacing rule and an EOL spacing rule for the metal layers, and a simple cut-to-cut spacing rule for the cut layers.

Table 2 shows the benchmark information, where #std, #blk, #net, #pin, and #layer denote the number of standard cells, macro blockages, nets, IO pins, and metal layers, respectively. The sample benchmarks (ispd18_sample*) are derived from the original single-core design. The nets are selected randomly. A placement run is called for the selected instances that are connected to those selected nets to produce a compact floorplan. These test cases will be used as a sample for the contestants to make sure their binary is able to read the design data correctly and perform the initial detailed routing process. These sample tests will not be used for evaluation purpose. On the other hand, "ispd18_test*" are the official benchmarks used to evaluate and rank the detailed routers developed by the contestants.

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