SERGIO CHACON

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EDUCATION

University of Texas at Austin Aug. 2017 - Dec. 2020
B.S. Electrical and Computer Engineering, December 2020 GPA : 3.77
Enrolled in Integrated BSEE/MSE Degree Program
Technical Cores: Integrated Circuits and Systems, Academic Enrichment

EMPLOYMENT

Test Engineering Intern, *Texas Instruments Inc.* June 2020 - Aug. 2020
- Implemented C++ code for characterization test programs for family of logic devices to be run on ETS-88 automated tester.
- Developed PCBs for ATE hardware setup using Cadence PCB Editor. Led design reviews and worked alongside external layout engineer.
- Wrote python scripts and presented Spotfire report to identify risk in removing probe from production for logic translator.

Product/Validation Engineering Intern, *Texas Instruments Inc.* May 2019 - Aug. 2019
- Operated and debugged automated lab bench with LabVIEW and NI Test Stand code to validate I2C performance of translator.
- Designed PCB test boards for Validation team using Altium. Led design reviews with Validation team and worked with external layout engineer.
- Enabled qualification of commercial device by submitting reliability tests, collecting characterization data on ETS-88, and presenting data in Spotfire to cross-functional team.

Undergraduate TA - EE316, EE411, *University of Texas at Austin ECE Department* Aug. 2019 - Current
- Provided assistance to engineering students in office hours for Digital Logic Design and Circuit Theory
- Collaborated with Graduate TA's to lead weekly recitation and lab sessions and grade class assignments

Undergraduate Tutor - EE302, EE411, *University of Texas at Austin ECE Department* Aug. 2018 - May 2019
- Held weekly open tutoring for engineering students in Intro to Electrical Engineering and Circuit Theory
- Tutored students in a one-on-one setting and in a group setting in tandem with another tutor

PERSONAL PROJECTS

ALU Schematic Design - EE460R Fall 2019
- Designed 16-bit ALU in Cadence Virtuoso with Kogge-Stone adder, magnitude comparator, and shift capability
- Tested functionality with NC Verilog and ran static timing analysis with Synopsys Primetime
- Utilized Cadence Encounter for Automatic Place and Route layout stage

SSP UART Verification - EE382M-11 Spring 2020
- Worked with graduate team to verify Synchronous Serial Port with UART communication
- Formally verified design with assertion properties written in System Verilog and proven with Cadence Jaspergold
- Contributed to writing UVM testbench and FPGA prototype verification

FPGA Based Deep Learning Accelerator - Capstone Senior Design Spring 2020 - Current
- Implementing a Convolutional Neural Network onto a PYNQ FPGA board using TVM compiler and VTA Accelerator
- Writing Python code to optimize accelerator architecture performance and tune operator scheduling

Op-Amp Based Transceiver Chain - EE438K Spring 2020
- Designed op-amp signal chain of 1st Order Delta Sigma Modulation, LED driver, photodiode receiver, amplifier, and active filter stages
- Simulated in LTspice by inputting and recovering .wav file and built transmit and receive chains separately on a breadboard

SKILLS

SOFTWARE: C/C++, SystemVerilog, Python, LabVIEW, Cadence Virtuoso, LTspice, Altium PCB Design, Cadence Allegro
HARDWARE: Teradyne ETS-88, TM4C Microcontroller, Basys3 FPGA, NI myDAQ, Oscilloscope, Function Generator, Thermostream

RELEVANT COURSEWORK

EE382M-11: Verification of Digital Systems EE438K: Analog Electronics EE460R: Intro to VLSI Design EE460N Computer Architecture (F20) EE382M-14: Analog IC Design (F20)