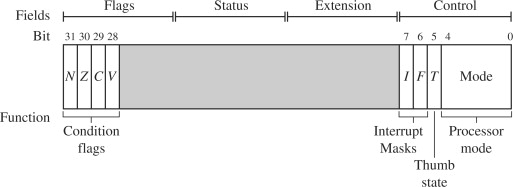
CURRENT PROGRAM STATUS REGISTER

The ARM core uses the *cpsr* to monitor and control internal operations. The *cpsr* is a dedicated 32-bit register and resides in the register file. Figure 2.3 shows the basic layout of a generic program status register. Note that the shaded parts are reserved for future expansion.



The *cpsr* is divided into four fields, each 8 bits wide: flags, status, extension, and control. In current designs the extension and status fields are reserved for future use. The control field contains the processor mode, state, and interrupt mask bits. The flags field contains the condition flags.

The CPSR can be broken down into four main fields:

1. Flags (bits 31–28): These are condition flags used for conditional instructions.

N (Negative)

Z (Zero)

C (Carry)

V (Overflow)

2. Reserved bits (27–8): These are not used typically and should remain unchanged.

3. Control bits (7–0):

Q (Saturation flag – bit 27)

I (IRQ disable – bit 7)

F (FIQ disable – bit 6)

T (Thumb state – bit 5)

4.Mode bits (4–0): Indicates the processor mode like User, FIQ, IRQ, SVC, etc.

Now, based on the conditions mentioned:

Zero flag is set, so Z = 1

Other flags N, C, V, Q are clear, so N = 0, C = 0, V = 0, Q = 0

Thumb state is active, so T = 1

IRQ interrupts are enabled, so I = 0

Processor is in SVC mode, which is 10011 in binary (for mode bits)

Here’s how the CPSR layout would look (only the relevant bits are shown for clarity):

| N | Z | C | V | Q | ... | I | F | T | Mode |

| 0 | 1 | 0 | 0 | 0 | ... | 0 | x | 1 | 10011 |

N,C,V,Q = 0

Z = 1

I = 0 (enabled)

T = 1 (Thumb state)

Mode = 10011 (SVC mode)

This register is super useful during debugging and context switching because it tells us the exact state the processor is in.