Name: Sachin Mahadev Jadhav
Address: At Itti, Post-Poharegaon, Tal: Renapur,
Dist: Latur, Pin - 413512.
Contact NO:9850823263
E-mail: jadhavsa996@gmail.com

---

1 Career Objective:

Utilization of knowledge and Technical skills along with design abilities to promote growth and development of the organization and self by implementing my innovative ideas, skills and creativity.

---

2 Academic Details:

Sr No:	Class	Year of Passing	institute	Grades
1.	TY B.Tech	2017-18		9.3
2.	SY B.Tech	2016-17	WCE,Sangli	9.12
3.	FY B.Tech	2015-16		8.78
4.	HSC	2014-15	Dayanand Science college,Latur	91.38
5.	SSC	2012-13	Renuka Vidyalay Bhokaramba	91.45

---

3 Projects Undertaken:

1. Biomorphic Hyper Redundant Snake Robot.
   - Under E-Yantra 2017 robotic competition organized by IITB.
     -Using joystick communication and 3D designing of snake and Servo actuator.
2. Line following based multipurpose system for hospitals.
   - India innovation challenge design contest by Texas Instruments and IIM Bangalore.
   - Idea is to make clone for doing multiple tasks such as sweeping,cleaning,dustbin collection,medicine delivery
3. Pocket DSO
   - Third year sem 2 miniproject
   - Cost and Power efficient portable DSO using GLCD with MSP430.

4. Anti-pilferage and anti-adulteration system for fuel road tankers.
    - Smart India Hackthon 2018
    - Solution to the pilferage and adulteration of fuel tanks en-route from terminals to retailer by continuous monitoring of location ,level, pressure and temperature parameters with cloud connectivity also ensuring emergency management.
5. Digital Trekking Watch.
    - TY BTech sem 1 Mini project
    - OLED based compass and location tracking using magnetometer and GPS.
6. Modeling 3D terrain in blender
    - EYantra 2016 robotic championship by IITB
    - 3D modelling of a terrain in Blender using X-bee comm. with Firebird V.

4 Training and Workshop:

1. Successfully completed the online course on Hardware Modelling Using Verilog conducted by **IIT KHARAGPUR** under NPTEL.
2. Successfully compeleted workshop on **"Analog VLSI Design with Emphasis on OP-Amp Design"**.