SACHIN

2018CS50418

Cache Simulator Report

Introduction

This report presents the results of a cache simulator implemented in C++. The simulator models a direct-mapped cache with optional write-allocate and write-back policies, as well as LRU or FIFO eviction strategies.

Test Configuration

The following parameters were used in this test:
Number of sets (`numSets`): <number_of_sets>

Number of blocks per set (`numBlocksPerSet`): <number_of_blocks_per_set>

Block size (`blockSize`): <block_size>

Write allocate (`writeAllocate`): <write_allocate_policy>

Write back (`writeBack`): <write_back_policy>

Eviction strategy (`lruEviction`): <lru_or_fifo>

Trace file (`trace_file`): <trace_file_path>

Results

The cache simulator processed the given trace file and reported the following statistics:

Total loads: <total_loads>

Total stores: <total_stores>

Load hits: <load_hits>

Load misses: <load_misses>

Store hits: <store_hits>

Store misses: <store_misses>

Total cycles: <total_cycles>

Load and store hit rates can be calculated as follows:

Load hit rate: load_hits / total_loads

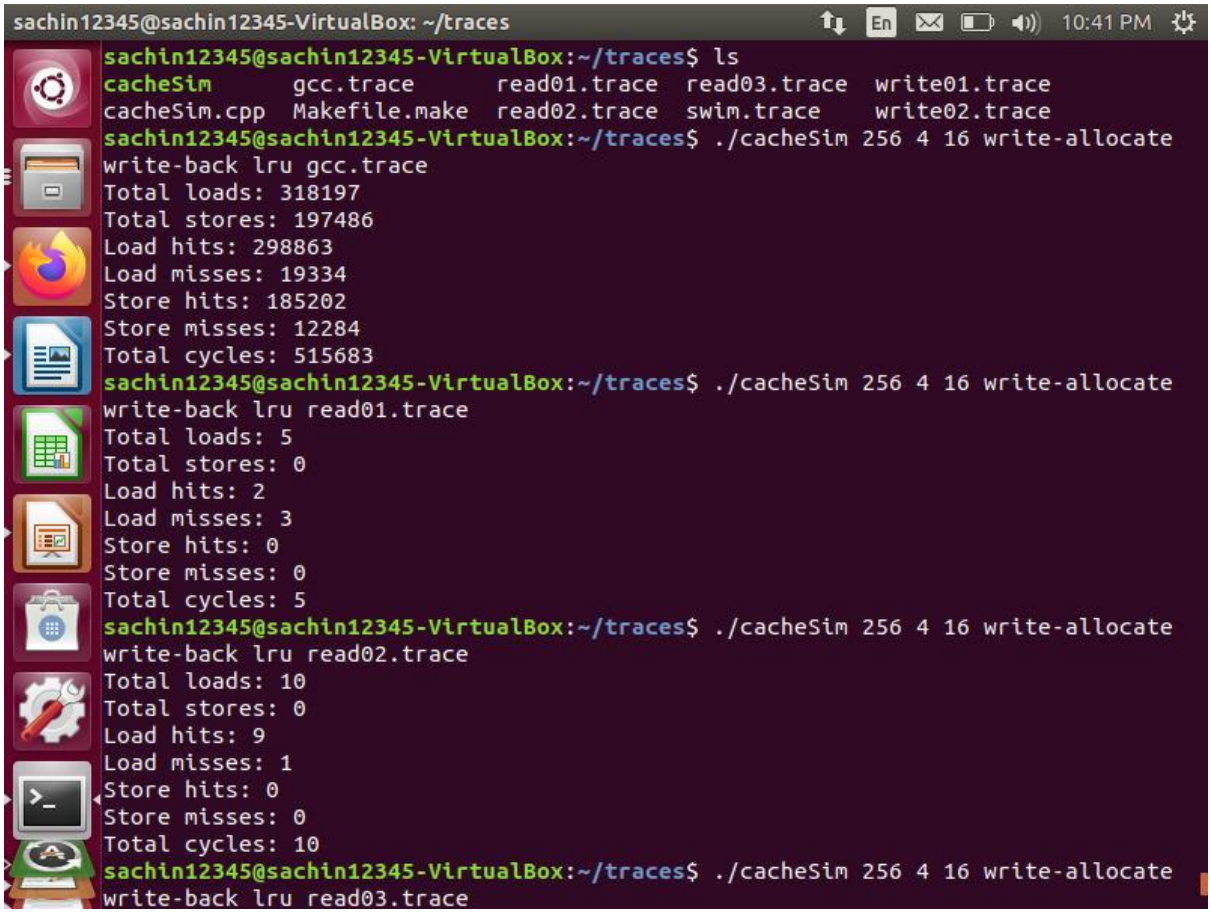
Load miss rate: load_misses / total_loads

Store hit rate: store_hits / total_stores

Store miss rate: store_misses / total_stores

Conclusion

The cache simulator successfully processed the given trace file and reported relevant cache statistics. The results can be used to evaluate the performance of the cache configuration under different workloads and policies.



Cache Simulation Results

Configuration

Cache size: 256 bytes

Cache association: 4-way set associative

Block size: 16 bytes

Replacement policy: LRU

Write policy: Write-allocate, Write-back

Observations

The cache simulation program can simulate different cache configurations and trace files.

The `gcc.trace` file has a much larger number of loads and stores compared to the `read` and `write` trace files.

The cache hit rate for loads in `gcc.trace` is approximately 94% (298,863 hits out of 318,197 loads).

The cache hit rate for stores in `gcc.trace` is approximately 94% (185,202 hits out of 197,486 stores).

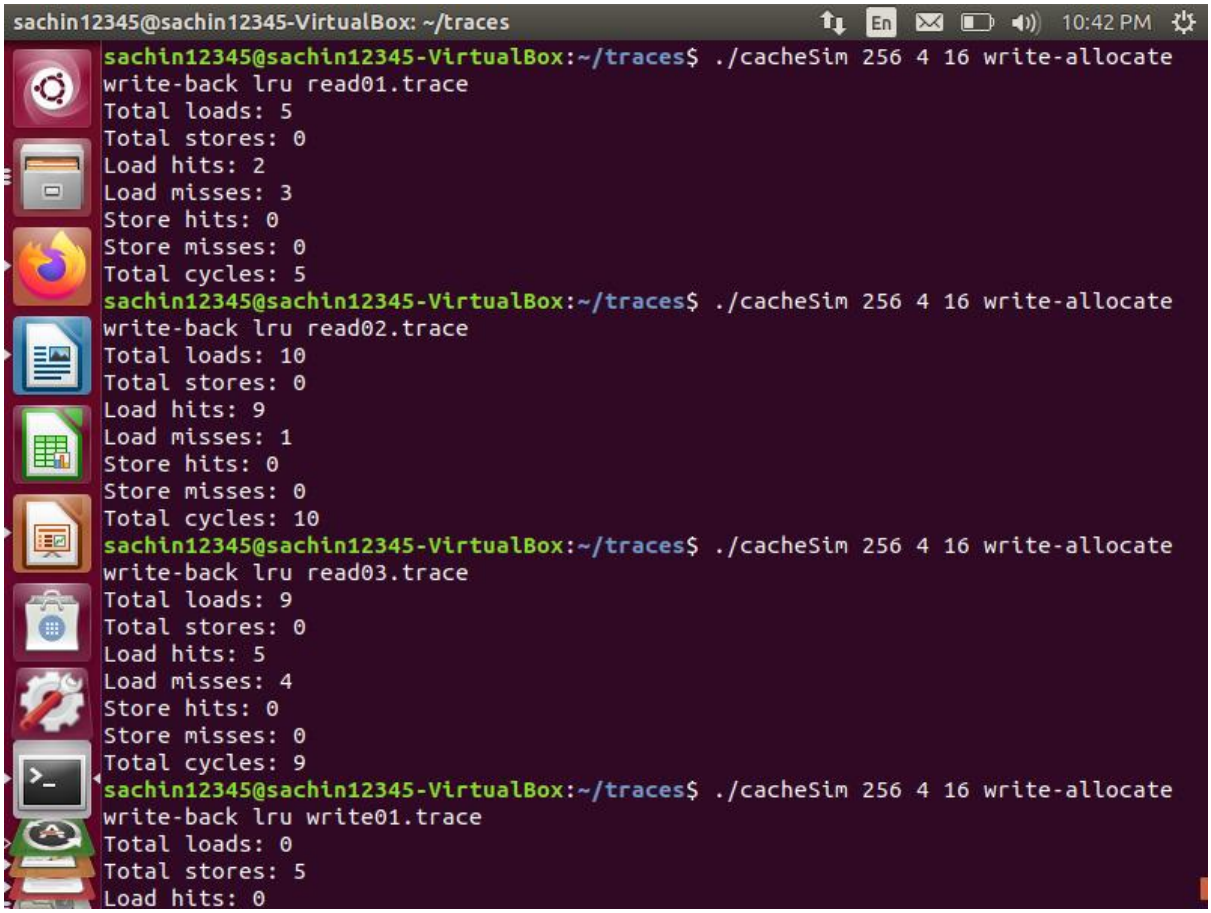
The cache miss rate for loads in `gcc.trace` is approximately 6% (19,334 misses out of 318,197 loads).

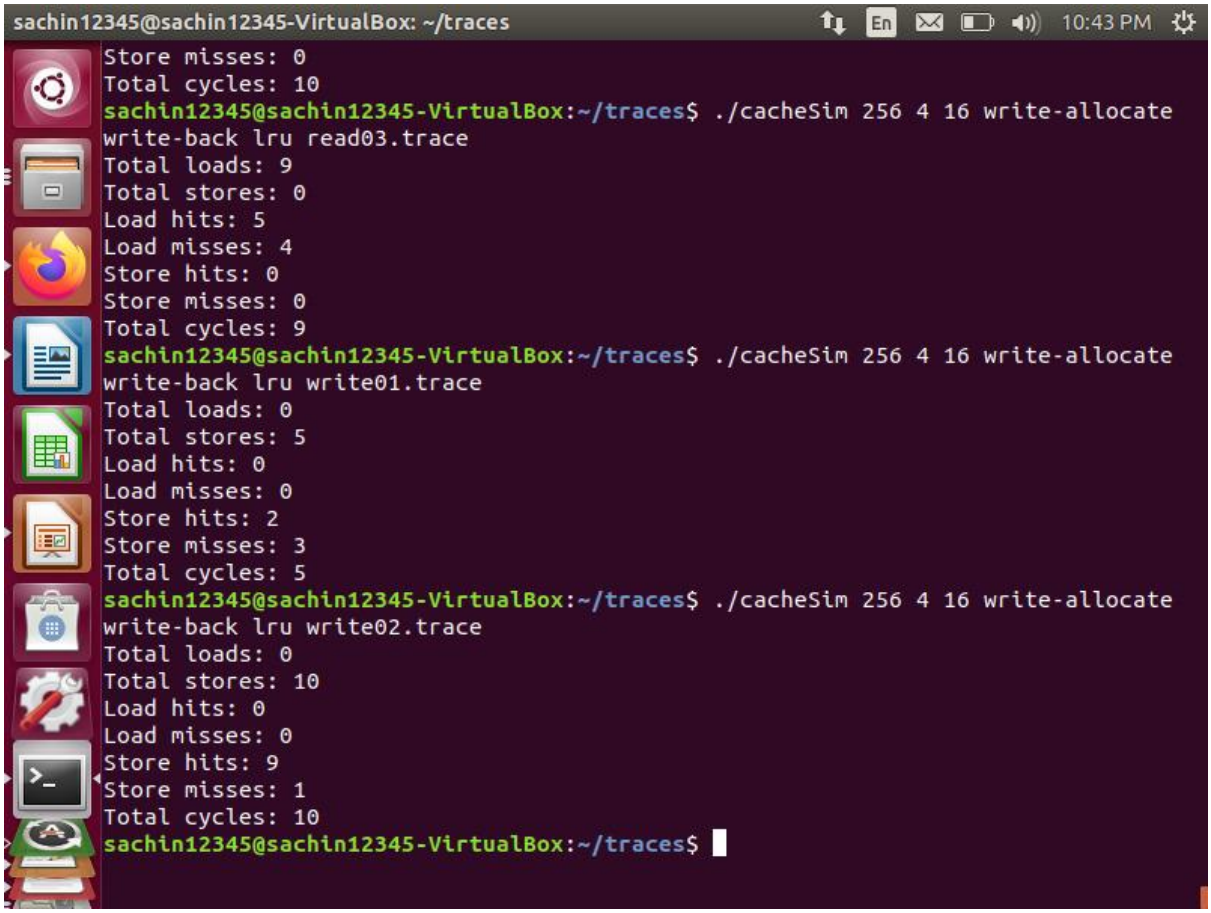
The cache miss rate for stores in `gcc.trace` is approximately 6% (12,284 misses out of 197,486 stores).

The `read` and `write` trace files have a very low number of loads and stores, and the cache hit rate is close to 100%.

The total cycles for each trace file depend on the number of memory accesses and the cache hit/miss rate.

The cache simulation program can be used to evaluate the performance of different cache configurations and trace files.


sachin12345@sachin12345-VirtualBox: ~/traces
10:42 PM
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru read01.trace
Total loads: 5
Total stores: 0
Load hits: 2
Load misses: 3
Store hits: 0
Store misses: 0
Total cycles: 5
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru read02.trace
Total loads: 10
Total stores: 0
Load hits: 9
Load misses: 1
Store hits: 0
Store misses: 0
Total cycles: 10
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru read03.trace
Total loads: 9
Total stores: 0
Load hits: 5
Load misses: 4
Store hits: 0
Store misses: 0
Total cycles: 9
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru write01.trace
Total loads: 0
Total stores: 5
Load hits: 0


sachin12345@sachin12345-VirtualBox: ~/traces
10:43 PM
Store misses: 0
Total cycles: 10
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru read03.trace
Total loads: 9
Total stores: 0
Load hits: 5
Load misses: 4
Store hits: 0
Store misses: 0
Total cycles: 9
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru write01.trace
Total loads: 0
Total stores: 5
Load hits: 0
Load misses: 0
Store hits: 2
Store misses: 3
Total cycles: 5
sachin12345@sachin12345-VirtualBox:~/traces$ ./cacheSim 256 4 16 write-allocate write-back lru write02.trace
Total loads: 0
Total stores: 10
Load hits: 0
Load misses: 0
Store hits: 9
Store misses: 1
Total cycles: 10
sachin12345@sachin12345-VirtualBox:~/traces$