

Assignment 1

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Download all codes from

https://github.com/sachinomdubey/FPGA_Lab/Assignment1/codes

and latex-tikz codes from

https://github.com/sachinomdubey/FPGA_Lab/Assignment1

1 PROBLEM

(CBSE/CS/2019/6.c) Derive a Canonical POS expression for a Boolean function F , represented by the following TABLE 0:

X	Y	Z	$F(X, Y, Z)$
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

TABLE 0: Truth table for Function F

2 SOLUTION

Here, the output F is '0' for four combinations of inputs. The corresponding Max terms are $(X+Y+\bar{Z})$, $(X+\bar{Y}+\bar{Z})$, $(\bar{X}+\bar{Y}+Z)$, $(\bar{X}+\bar{Y}+\bar{Z})$. By doing logical AND of these four Max terms, we will get the Boolean function F ,

$$F = (X + Y + \bar{Z}) \cdot (X + \bar{Y} + \bar{Z}) \cdot (\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + \bar{Y} + \bar{Z}) \quad (2.0.1)$$

This is the canonical POS form for the Boolean function F . We can also represent this function in following two notations.

$$F = M_1 \cdot M_3 \cdot M_6 \cdot M_7 \quad (2.0.2)$$

$$F = \prod M(1, 3, 5, 7) \quad (2.0.3)$$

Implementation using two input NAND gates

Minimizing the function using K-maps,

		BC			
		00	01	11	10
A	0	1	0	0	1
	1	1	1	0	0

We get the following minimized POS form,

$$F = (A + \bar{C}) \cdot (\bar{A} + \bar{B}) \quad (2.0.4)$$

Using Demorgan's law, we can write :

$$F = \overline{(\bar{A} \cdot C)} \cdot \overline{(A \cdot B)} \quad (2.0.5)$$

$$= \overline{(\bar{A} \cdot C)} \cdot \overline{(A \cdot B)} \quad (2.0.6)$$

Implementing using two input NAND gate :

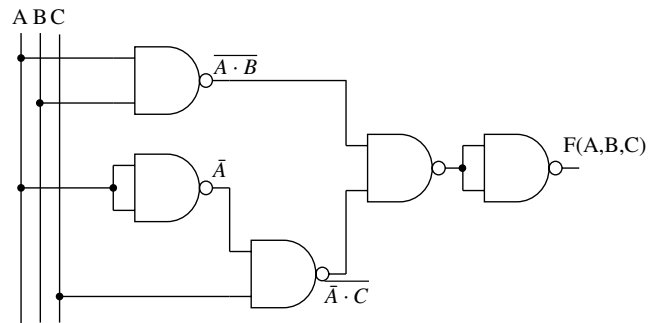


Fig. 0: Implementation using two input NAND gates