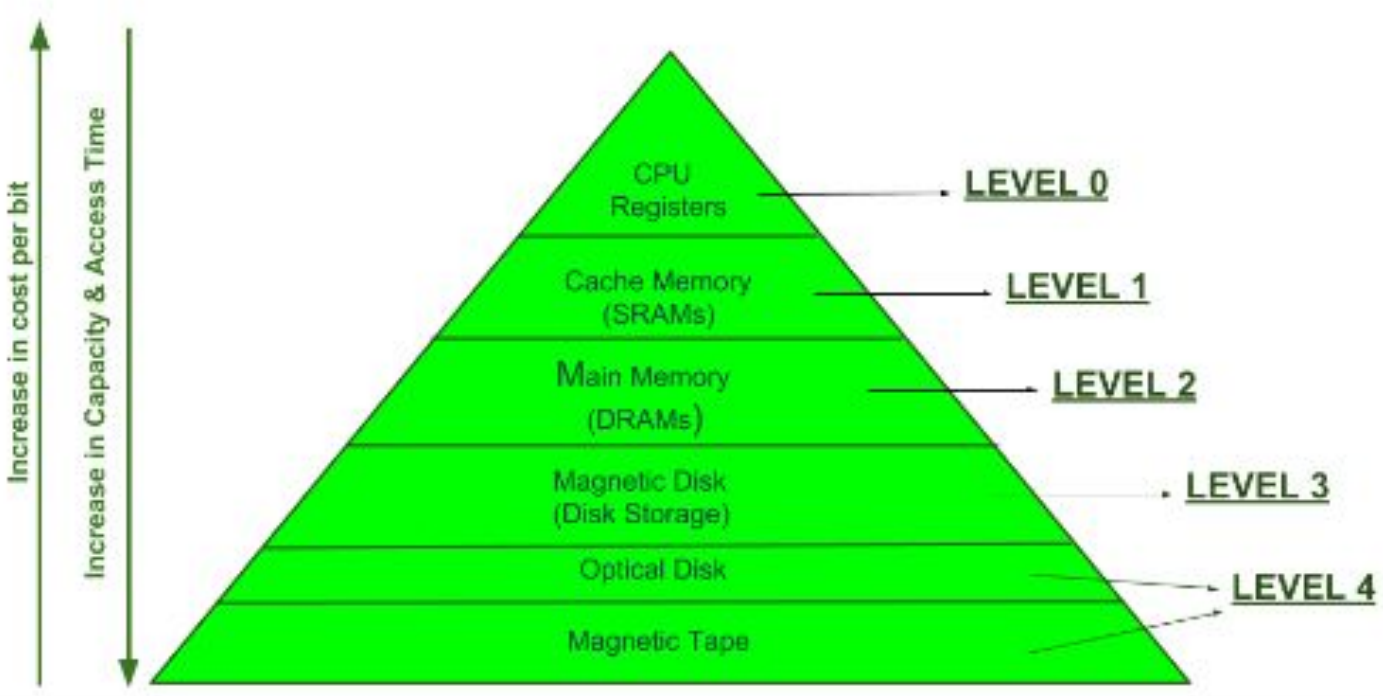
Division algorithm

Floating point representation

BCD adder

Memory Organization



Main Memory

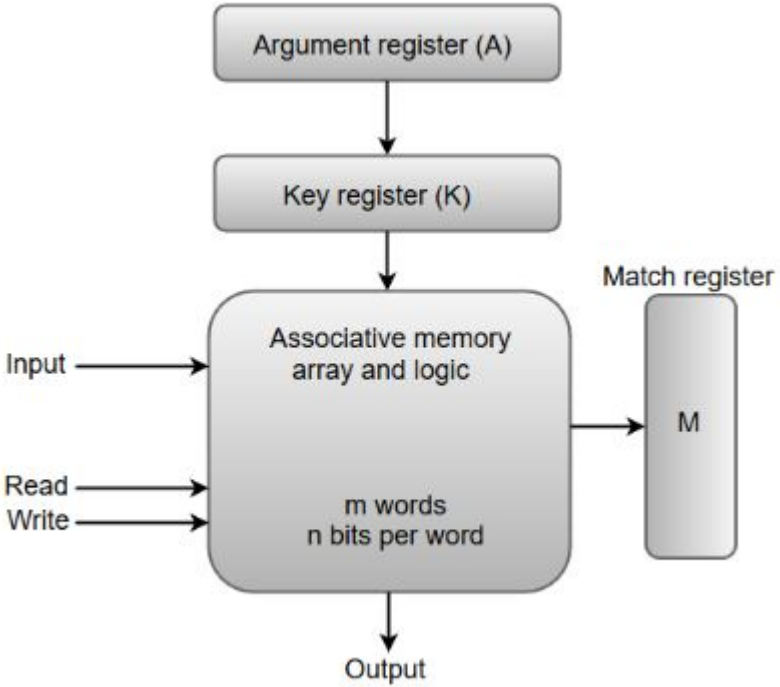
1. RAM: Random Access Memory (volatile memory)
    - DRAM- Dynamic RAM, is made of capacitors and transistors, and must be refreshed every 10~100 ms. It is slower and cheaper than SRAM.
    - SRAM: Static RAM, has a six transistor circuit in each cell and retains data, until powered off.
    - NVRAM: Non-Volatile RAM, retains its data, even when turned off.
2. ROM:Read Only Memory (non volatile memory)
    - PROM(Programmable ROM)
    - EPROM(Erasable PROM)
    - EEPROM(Electrically Erasable PROM)

Auxiliary Memory

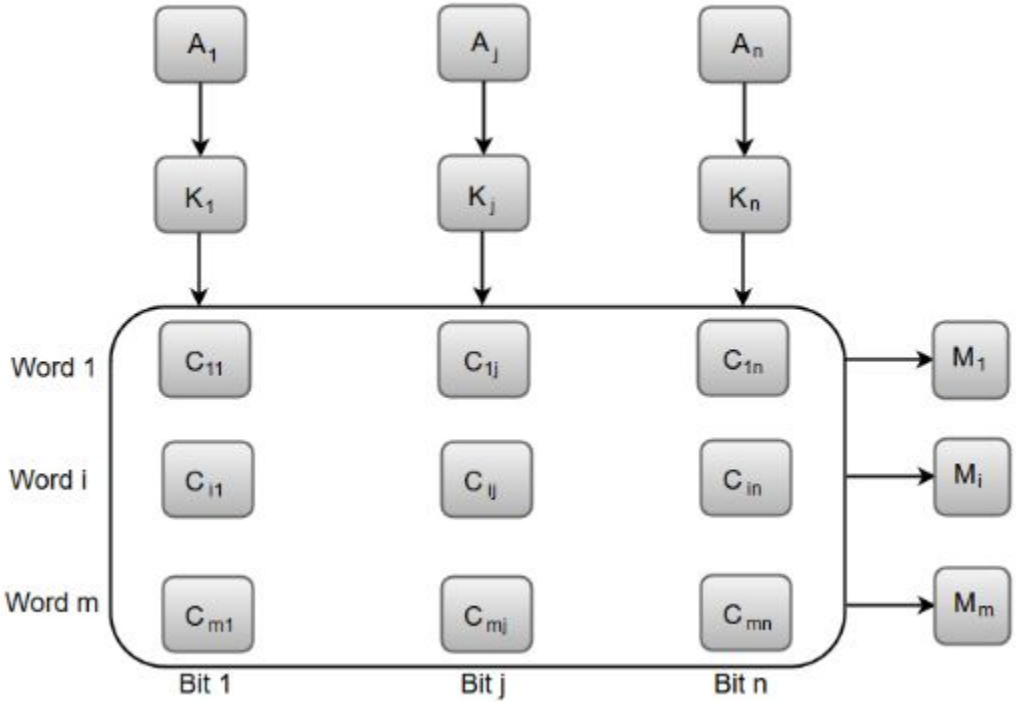
- Magnetic Disks

- Magnetic tapes

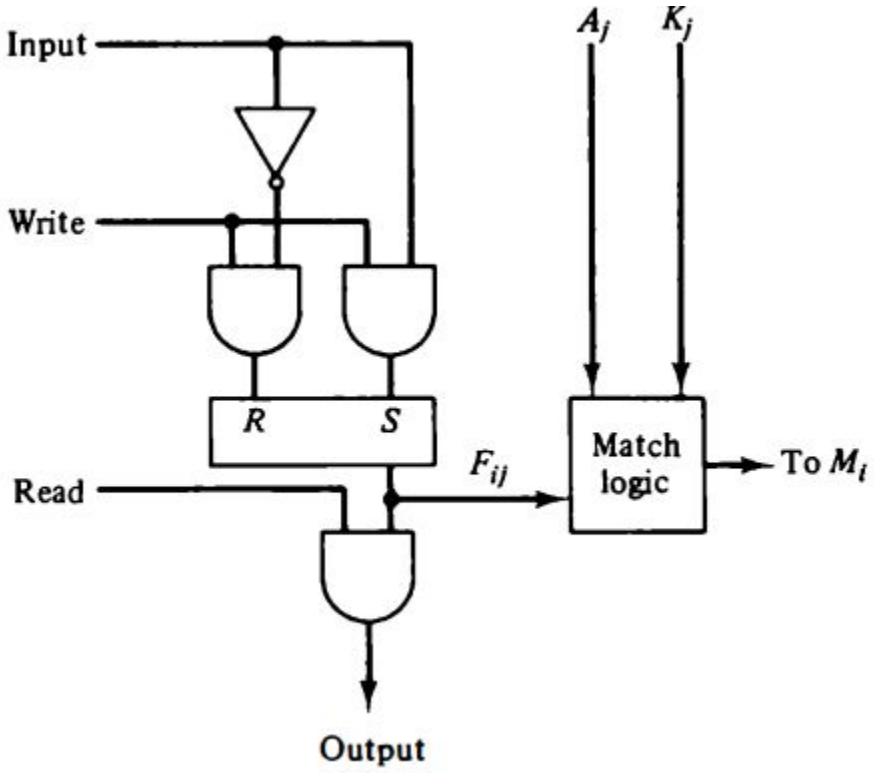
Associate Memory



Associative memory of m word, n cells per word:



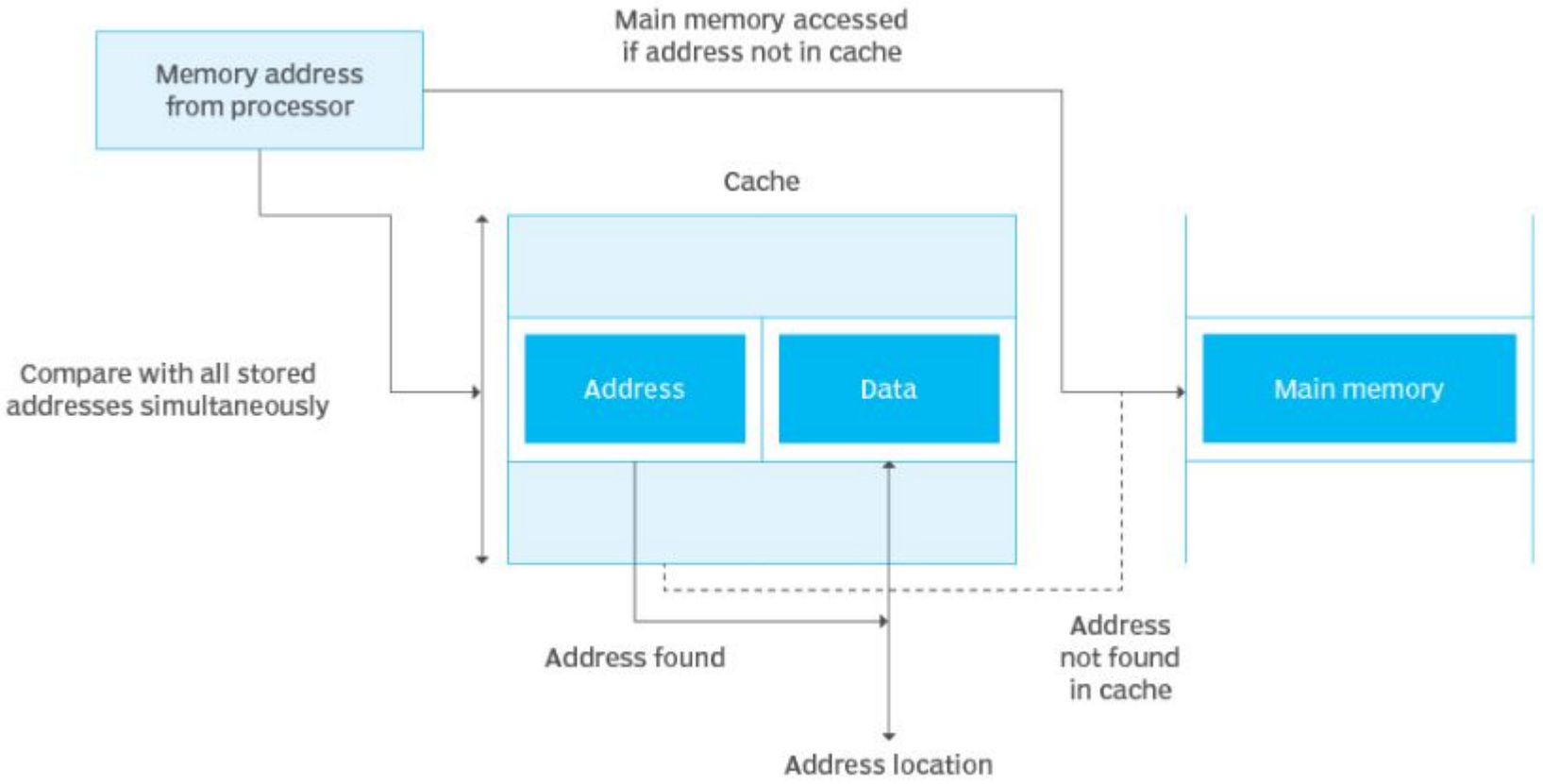
One cell associative memory

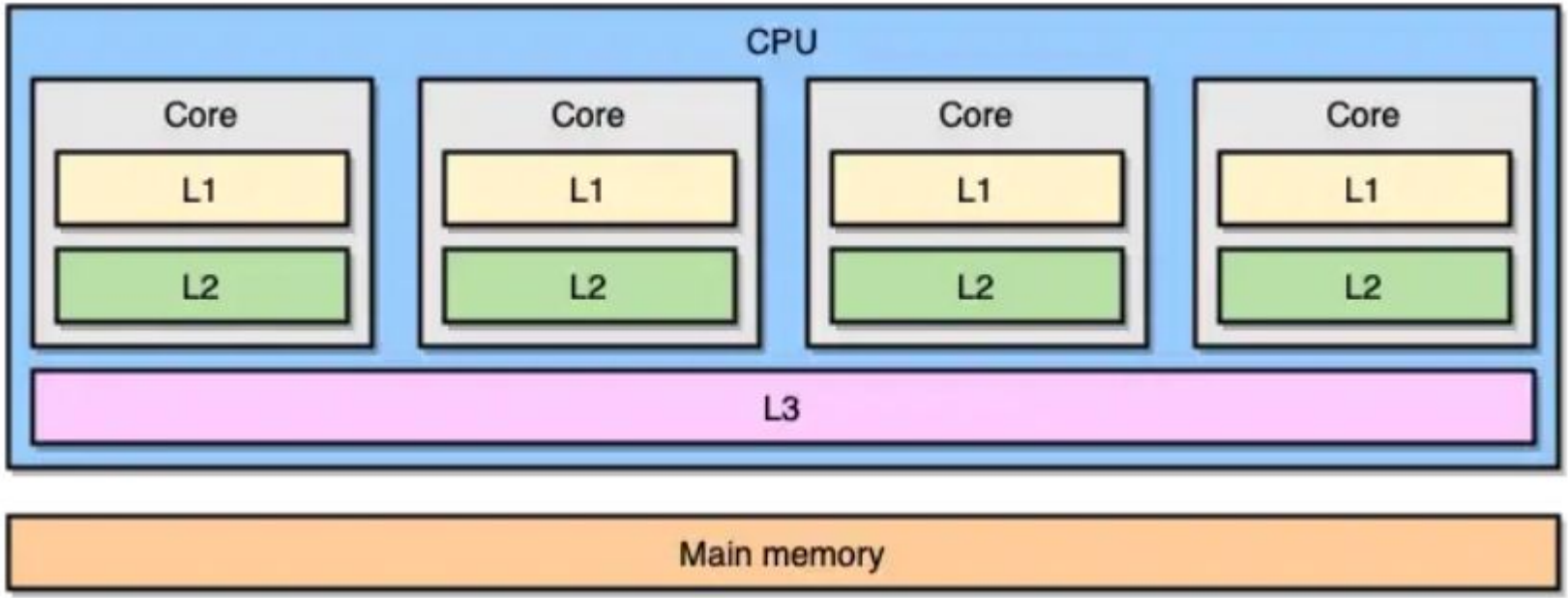


Memory Address map

Component	Hexadecimal address	Address bus									
		10	9	8	7	6	5	4	3	2	1
RAM 1	0000–007F	0	0	0	x	x	x	x	x	x	x
RAM 2	0080–00FF	0	0	1	x	x	x	x	x	x	x
RAM 3	0100–017F	0	1	0	x	x	x	x	x	x	x
RAM 4	0180–01FF	0	1	1	x	x	x	x	x	x	x
ROM	0200–03FF	1	x	x	x	x	x	x	x	x	x

Cache Memory




CPU
Core
L1
L2
Core
L1
L2
Core
L1
L2
Core
L1
L2
L3
Main memory

- Cache hit
- Cache miss
- Page fault
- Page hit

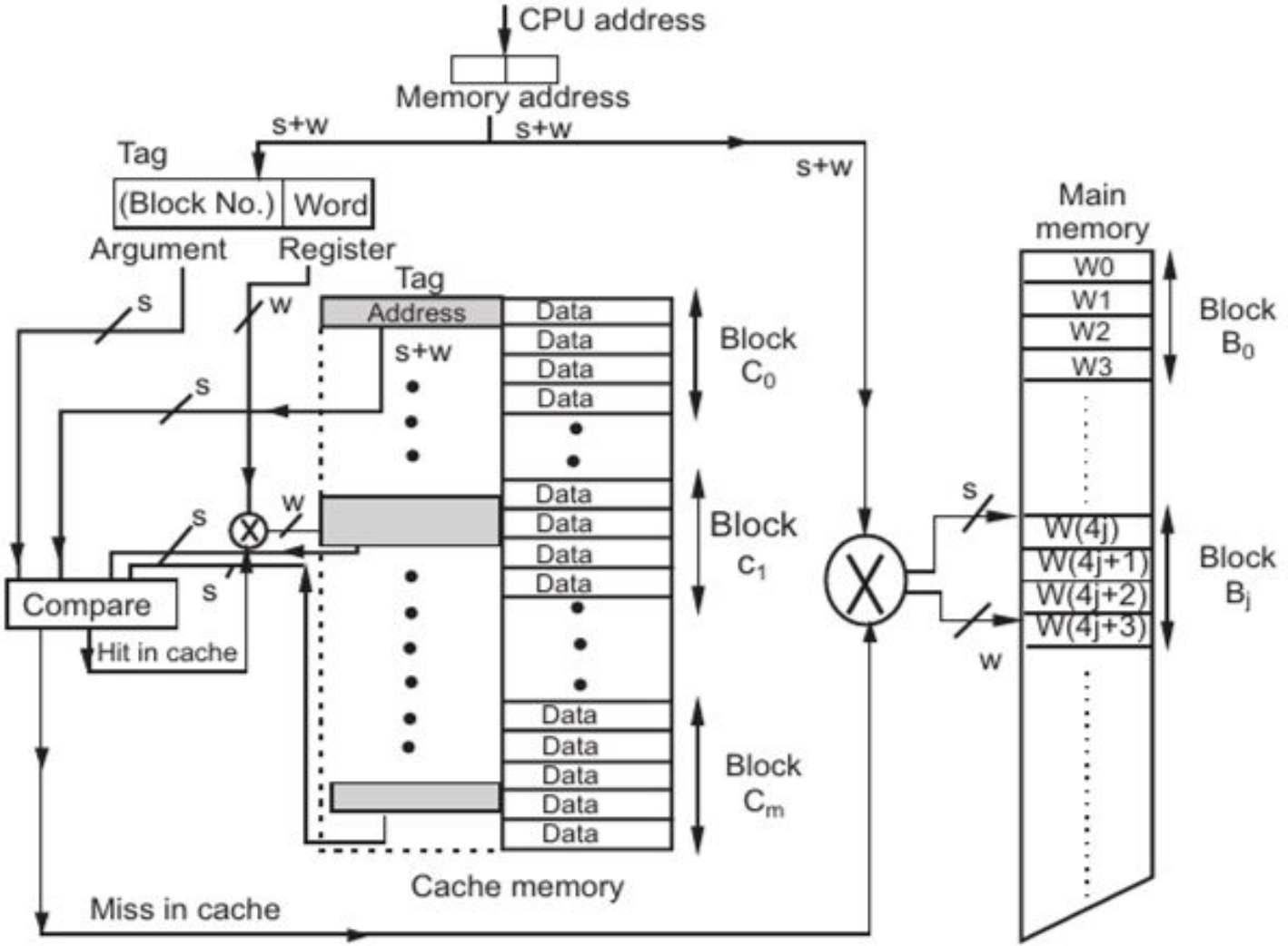
Cache Performance

Hit ratio = hit / (hit + miss) = no. of hits/total accesses

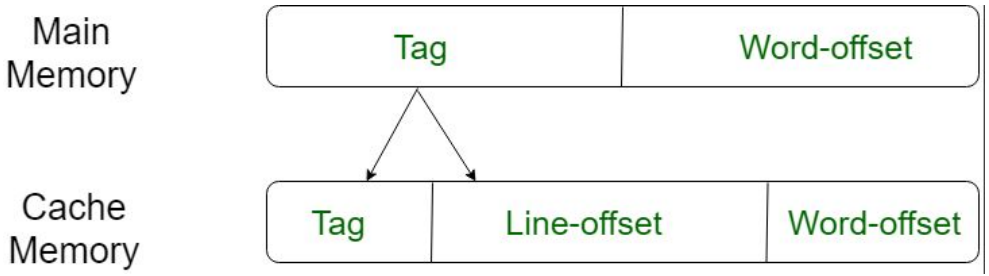
Cache Mapping

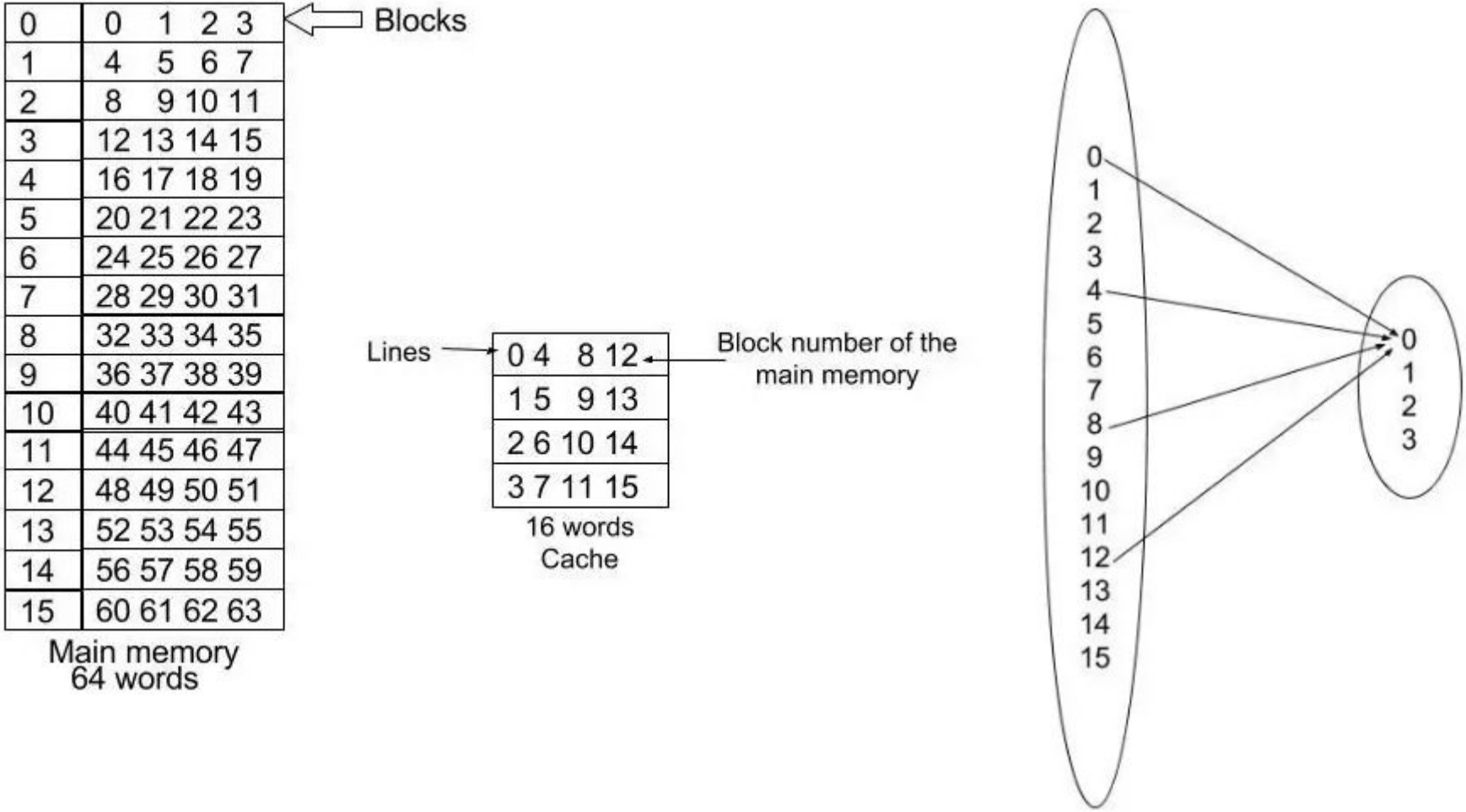
Associative

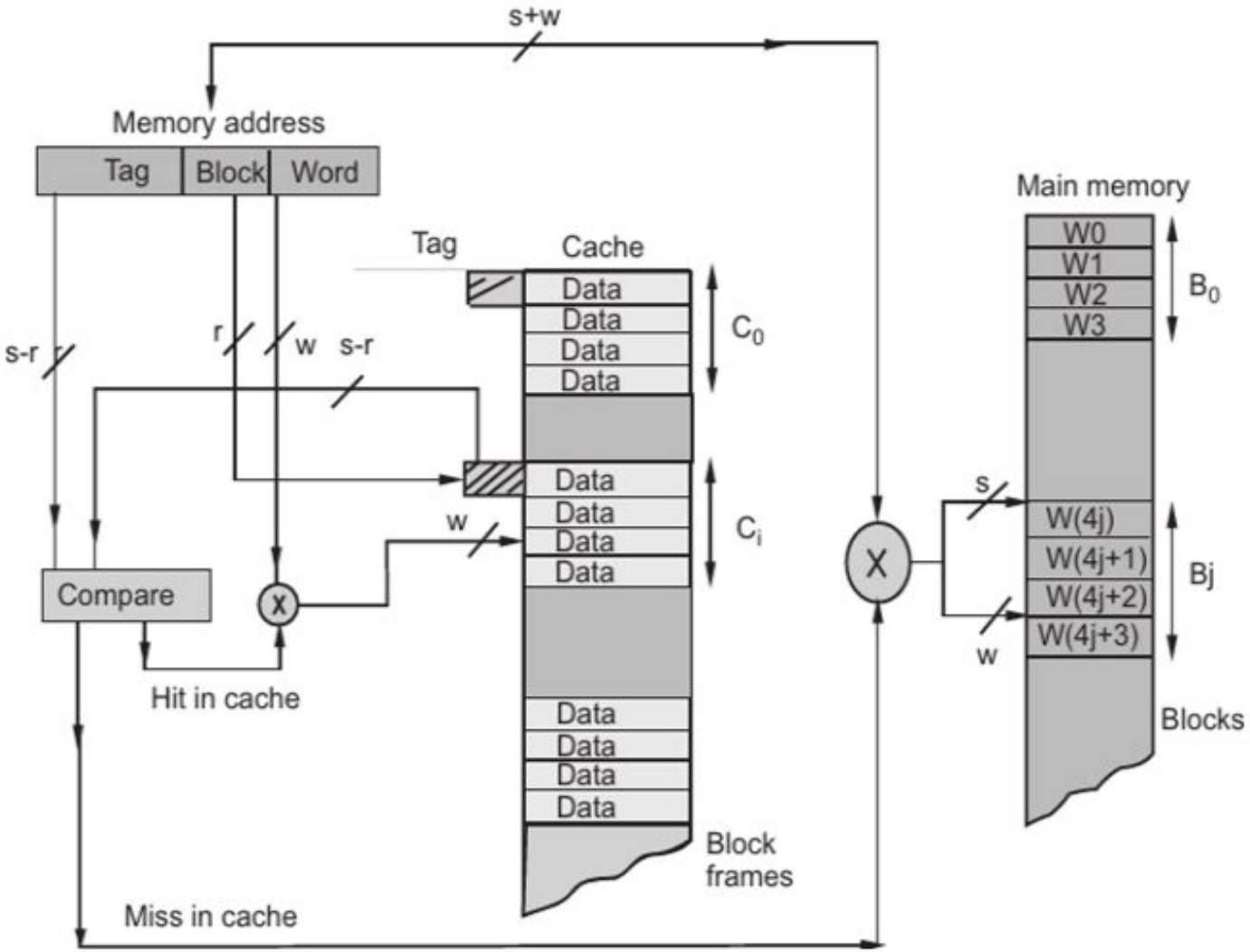
Mapping



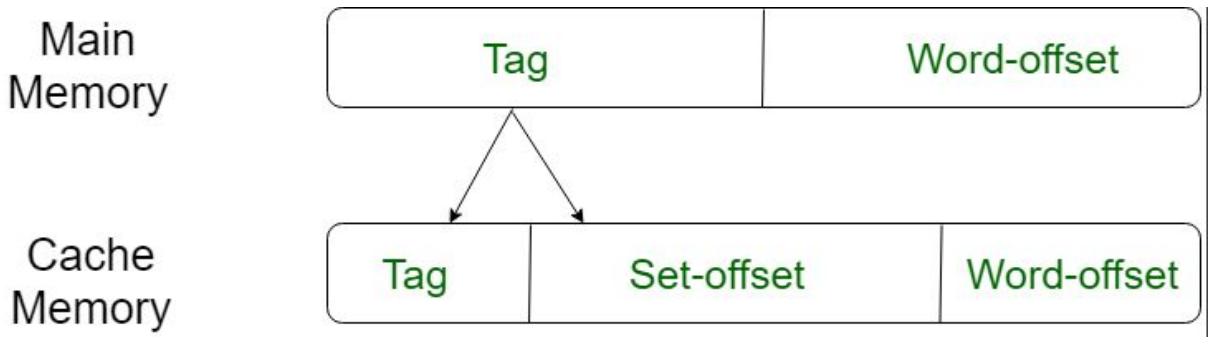
Direct Mapping

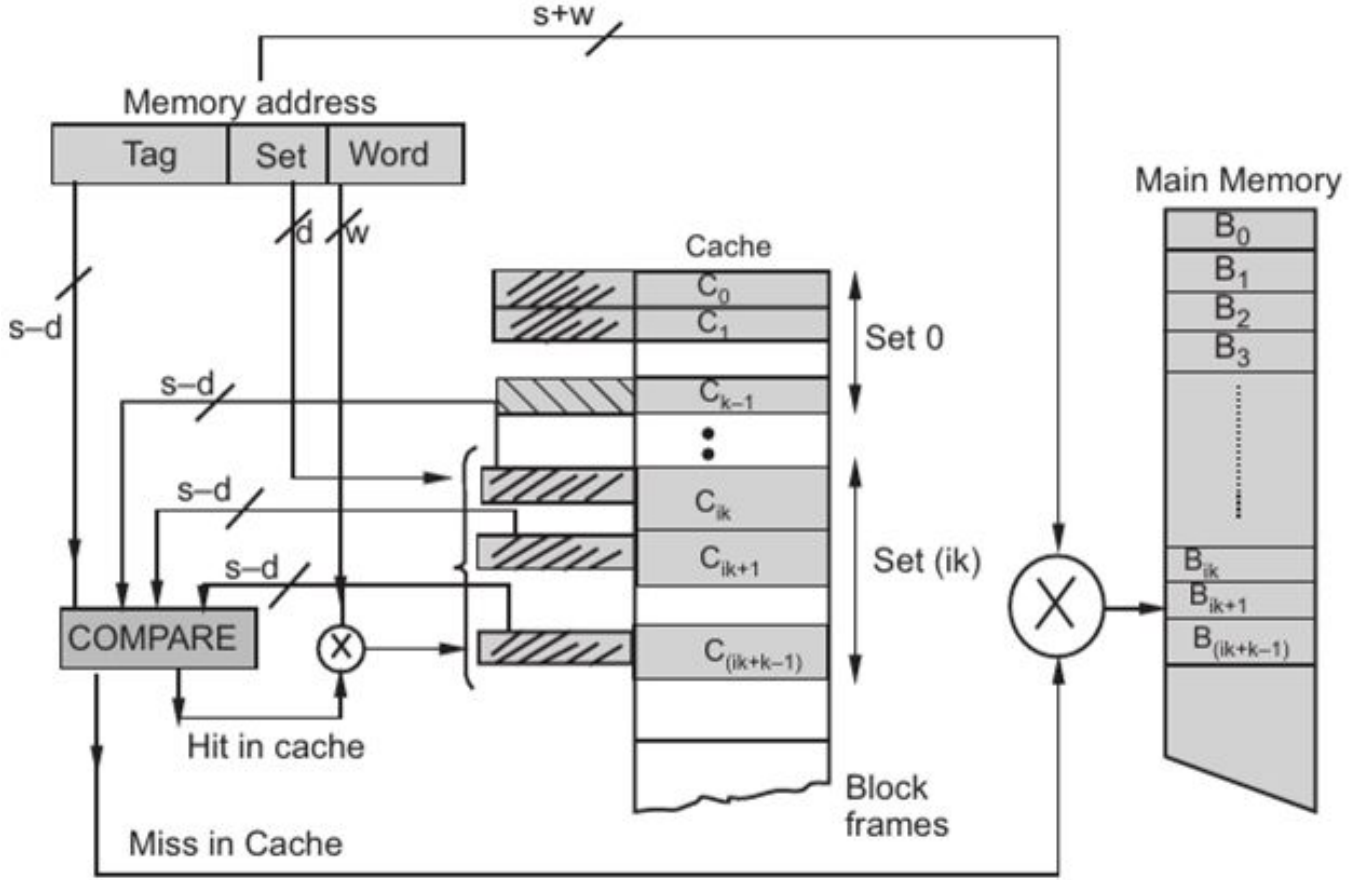



0 0 1 2 3
1 4 5 6 7
2 8 9 10 11
3 12 13 14 15
4 16 17 18 19
5 20 21 22 23
6 24 25 26 27
7 28 29 30 31
8 32 33 34 35
9 36 37 38 39
10 40 41 42 43
11 44 45 46 47
12 48 49 50 51
13 52 53 54 55
14 56 57 58 59
15 60 61 62 63
Blocks
Main memory
64 words
Lines
0 4 8 12
1 5 9 13
2 6 10 14
3 7 11 15
16 words
Cache
Block number of the
main memory
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
0
1
2
3


s+w
Memory address
Tag
Block
Word
Tag
Cache
Data
Data
Data
Data
C_0
s-r
r
w
s-r
Data
Data
Data
Data
C_i
w
Compare
X
Hit in cache
Data
Data
Data
Data
Block
frames
Miss in cache
Main memory
W0
W1
W2
W3
B_0
s
W(4j)
W(4j+1)
W(4j+2)
W(4j+3)
Bj
w
Blocks
X

Set associative mapping




s+w
Memory address
Tag
Set
Word
d
w
s–d
s–d
s–d
s–d
Cache
C_0
C_1
C_{k-1}
C_{ik}
C_{ik+1}
$C_{(ik+k-1)}$
Set 0
Set (ik)
Block frames
Main Memory
B_0
B_1
B_2
B_3
B_{ik}
B_{ik+1}
$B_{(ik+k-1)}$
COMPARE
Hit in cache
Miss in Cache

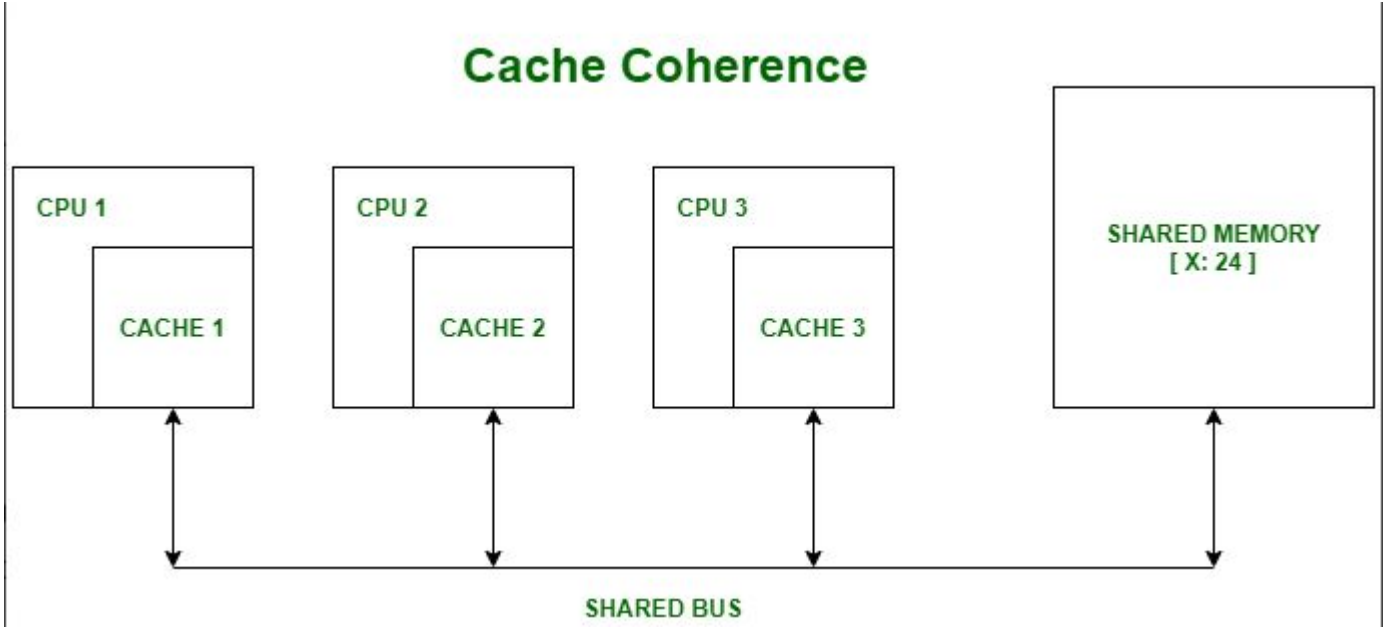
Cache Initialization

- The cache is initialized when the computer is switched on, or the computer is reset, or when the main memory is loaded with a set of programs from secondary memory.
- When the cache is initialized, all the valid bits are set to 0.
- When a word is loaded into cache from main memory, its corresponding valid bit is set to 1

Writing into Cache

- Write-Through (Store Through)
- Write-Back (Copy Back)

Cache Coherence



- **Modified –** It means that the value in the cache is dirty, that is the value in current cache is different from the main memory.
- **Exclusive –** It means that the value present in the cache is same as that present in the main memory, that is the value is clean.
- **Shared –** It means that the cache value holds the most recent data copy and that is what shared among all the cache and main memory as well.
- **Owned –** It means that the current cache holds the block and is now the owner of that block, that is having all rights on that particular blocks.
- **Invalid –** This states that the current cache block itself is invalid and is required to be fetched from other cache or main memory.

Cache Coherence Protocols in multiprocessor system

- MSI protocol (Modified, Shared, Invalid)
- MOSI protocol (Modified, Owned, Shared, Invalid)
- MESI protocol (Modified, Exclusive, Shared, Invalid)
- MOESI protocol (Modified, Owned, Exclusive, Shared, Invalid)

Coherency mechanisms