DEPARTMENT OF INFORMATION TECHNOLOGY, NITK SURATHKAL
MID-SEMESTER EXAMINATION, NOVEMBER 2022

IT201: Computer Organization And Architecture

Class: B.Tech(IT)
Date: 29/11/2022

Time: 1.5 Hrs.
Marks: 50

Register No: 2 1 1 0 0 9 3

NOTE: 1. Answer all questions.

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1. With a diagram explaining, design Full- adder using two Half-adder addresses and external logic gates if necessary. Design and explain a logic circuit to perform addition and subtraction of two 'n' bits numbers **X** and **Y**. This circuit can be suitably modified to perform **Y - X** operation **(10M)**

2. Explain various instruction formats based on the number of address fields used in the instruction format with an example. **(8M)**

3. Define addressing modes. Explain all the addressing modes using examples. **(8M)**

4. What are applications of Logic Microoperations **(6M)**

5. A bit stream **10011101** is transmitted using the standard CRC method. The generator polynomial is $x^3+1$.

   a) What is the actual bit string transmitted?

   b) Suppose the third bit from the left is inverted during transmission. How will the receiver detect this error? **(8M)**

6. Answer the following

   a) Consider the data unit to be transmitted is **10011001 11100010 01001000 00000100** . Consider **8 bit** checksum.

   b) Construct (7,4) hamming code for the message **1010** such that **odd parity** exists **(5M+5M)**

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