DEPARTMENT OF INFORMATION TECHNOLOGY, NITK SURATHKAL
END SEMESTER EXAMINATION, JANUARY 2023

IT201 Computer Organization And Architecture

Class: B.Tech(IT)
Date: 27.01.2023

Time: 3 Hrs
Marks: 70

Register No: 2 1 1 0 0 9 3

211IT058

NOTE: 1. Answer all questions

1) Write and explain general register organization with diagram **(5M)**

2) Write and explain on CPU organization with diagram **(5M)**

3) Explain Flynn's taxonomy with diagrams **(8M)**

4) What is asynchronous data transfer? Write a note on control signals occur during asynchronous data transfer **(1M+8M=9M)**

5) a. Explain BCD adder with a diagram. **(5M+5M=10M)**

b. Explain Associative memory page table with a diagram

6) Distinguish cache mapping using only neat diagrams **(15M)**

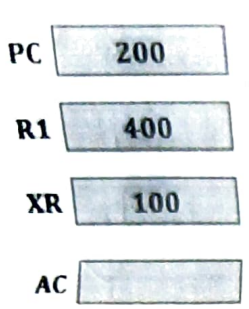
7) Consider the Pages referenced by the CPU in the order are 6, 7, 8, 9, 6, 7, 1, 6, 7, 8, 9, 1, 7, 9, 6 the number of frames in the memory is 3. Find out the number of page faults for

a. Optimal Page Replacement Algorithm,

b. FIFO Page Replacement Algorithm,

c. LRU Page Replacement Algorithm **(3*3M=9M)**

8) Apply addressing modes for the following diagram(except base addressing mode) **(9M)**



Address	Memory	
200	Load to AC	Mode
201	Address = 500	
202	Next Instruction	
399	450	
400	700	
500	800	
600	900	
702	325	
800	300	

END