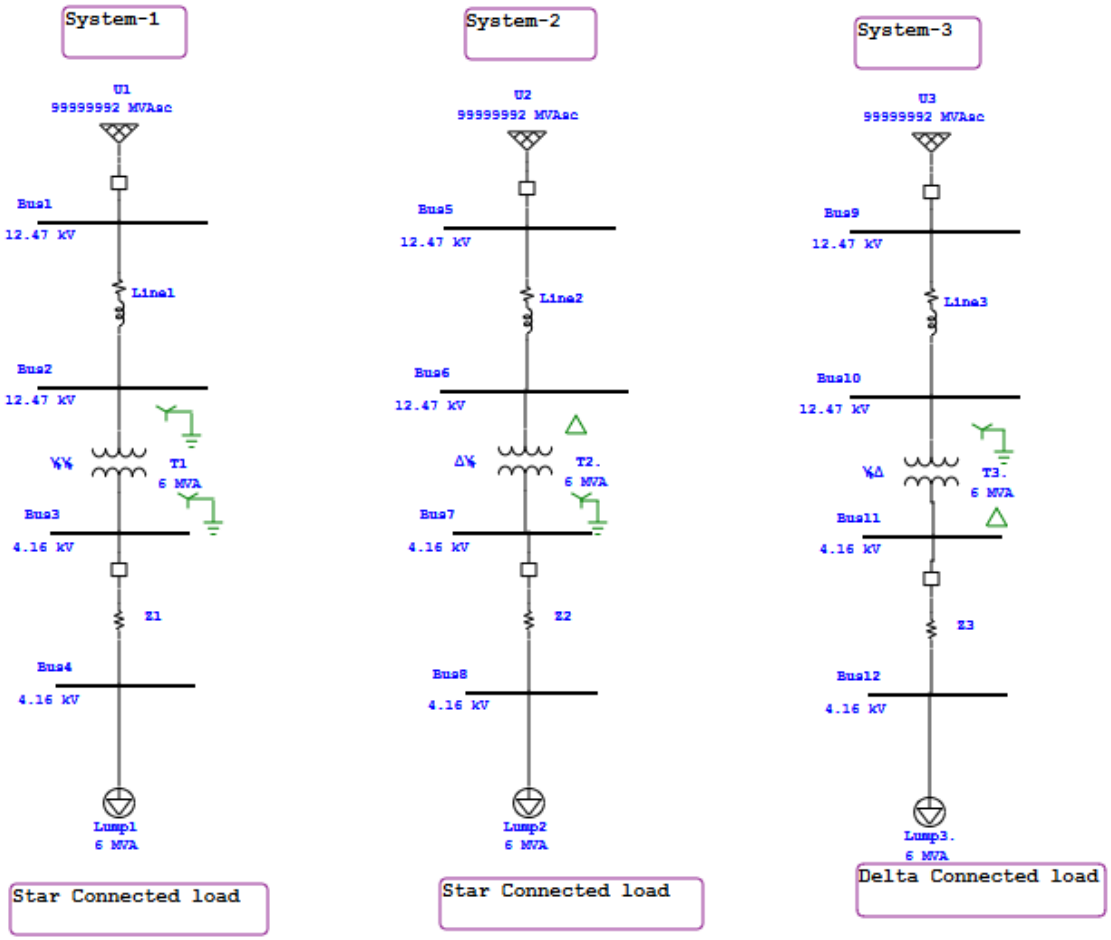
Unbalanced Load Flow

ULF-Example1

File Location:

Open the ETAP File – UNBALANCED LOAD FLOW (ULF) ->Examples->ULF_Example1

Library Location – C: -> ETAP 1610 -> lib -> etaplib1610.lib



Set Up:

3 systems have been shown in the SLD with the per phase loads same in each of them except system 1 & 2 has start connected load & system 3 has delta connected load. Also note the vector group difference of the transformers in each of these system are

Element	Primary	Secondary
XFMR -T1 (System1)	Y solid grounded	Y solid grounded
XFMR -T2 (System2)	Delta	Y solid grounded
XFMR -T3 (System3)	Y solid grounded	Delta

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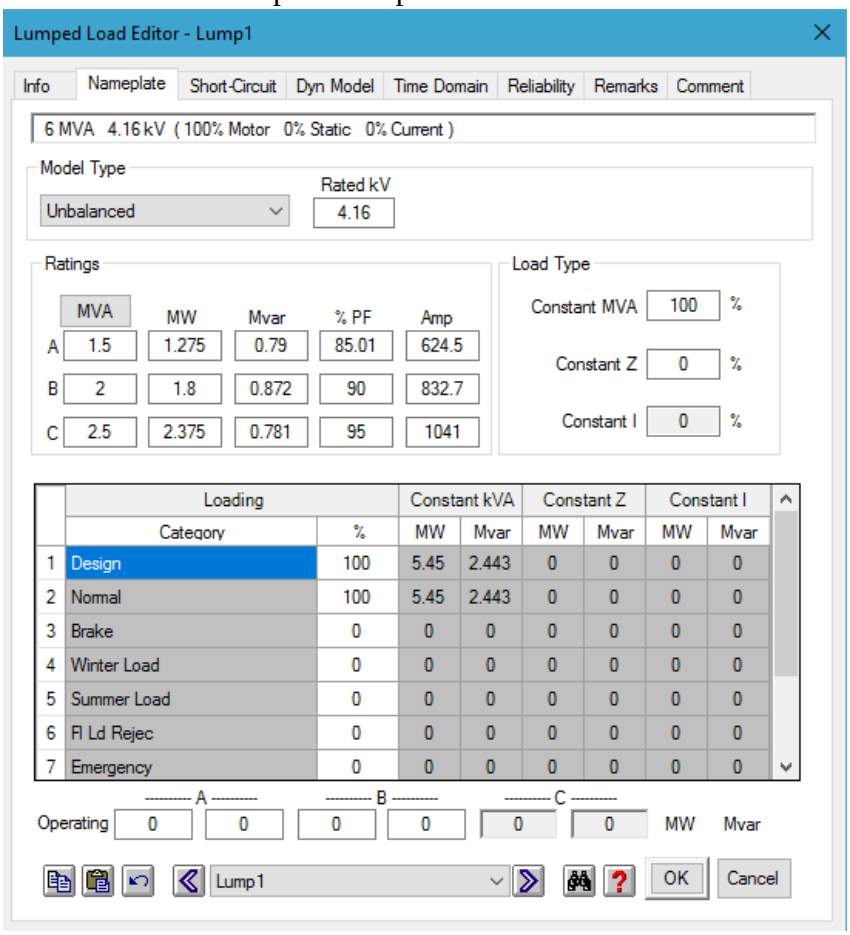
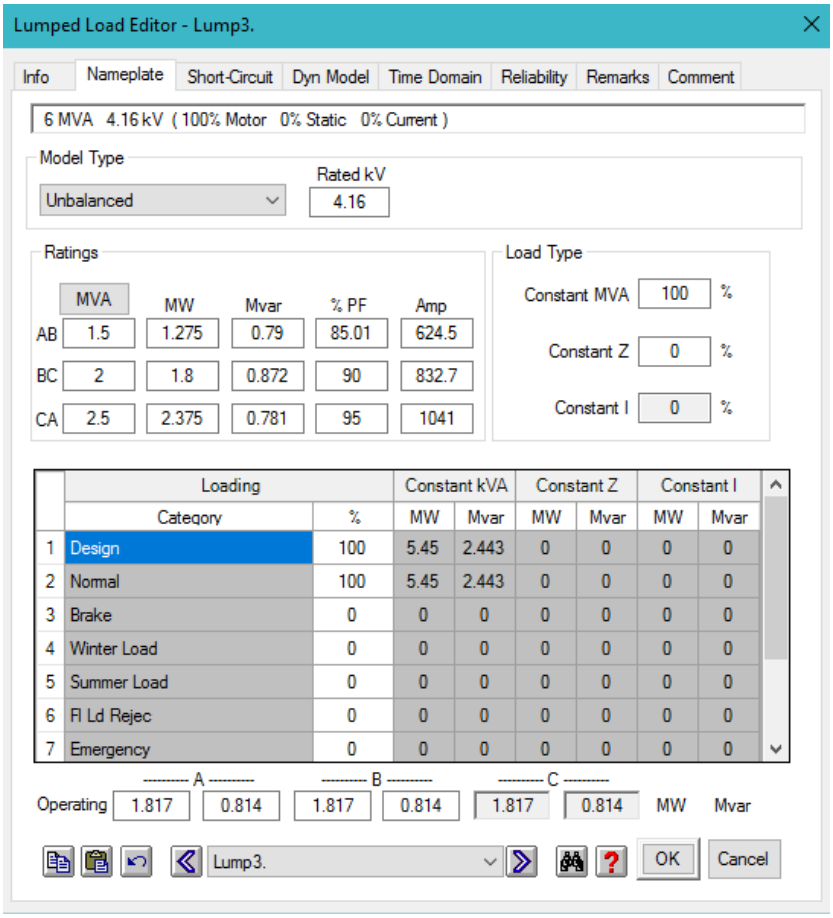
Note the lumped load details for lump1 & lump2 which are star connected are as follows:



Similarly lumped load details for lump3 which is delta connected is as follows:

Unbalanced Load Flow



Procedure:

To run 3 systems with Unbalanced & Balanced Load Flows

1. Run ULF. Check the system and check the results on the SLD. Note that, in unbalanced Load Flow each phases branch power flow & bus voltages will be displayed in the SLD results. The SLD can be set to display per phase kW+j kvar power or kVA & pf.

2. Now run LF (balanced) with the default study case. Check calculation results for all three systems.

3. Compare ULF and LF Calculation Results.

Unbalanced Load Flow

4. Note that in unbalanced load flow study case editor, there is one additional alert page called as Advanced Alert page. In this exercise the Adv. alert page is set as follows.

Type	Critical	Marginal
Bus Voltage (For each of LVUR, VUF2 & VUF0)	5%	2%
Branch Current (For each of LIUR, IUF2 & IUF0)	10%	4%
For details of terminology LVUR, VUF2 & VUF0, LIUR, IUF2 & IUF0 refer definitions given at the end of the ULF example1		

Note: The display of Unbalanced & Balanced load flow bus voltages shows that ULF takes the effect of phase loading & transformer vector group correctly in comparison to balanced LF studies of cases whose loads are unbalanced.

Observe in display option of ULF, following displays that are available on the SLD:

- Average values
- All phases
- All sequences

The alert displays are based on following alerts:

For Bus alerts:

- LVUR

  LVUR refers to unbalance ratio of line voltages. The NEMA (National Equipment Manufacturer's Association) definition of voltage unbalance, also known as the line voltage unbalance rate (LVUR) is given by:

$$LVUR = \frac{\text{Max voltage deviation from the avg line voltage}}{\text{Avg line voltage}} \times 100(\%)$$

- PVUR

  PVUR refers to use unbalance ratio of phase voltages. The IEEE definition of voltage unbalance, also known as the phase voltage unbalance rate (PVUR) is given by:

$$PVUR = \frac{\text{Max voltage deviation from the avg phase voltage}}{\text{Avg phase voltage}} \times 100(\%)$$

Unbalanced Load Flow

- VUF 2

  It is the ratio of the negative sequence voltage to the positive sequence voltage and is given by:

$$VUF_2 = \frac{V_2}{V_1} \times 100(\%)$$

- VUF 0

  The zero sequence voltage unbalance factor of phase voltages, which is given by:

$$VUF_0 = \frac{V_0}{V_1} \times 100(\%)$$

For Branch alerts:

- LIUR (IUR)

  Branch current unbalance ratio (IUR), which is given by:

$$IUR = \frac{\text{Max branch current deviation from the average}}{\text{Average of branch currents}} \times 100(\%)$$

- IUF 2

  The negative sequence branch current unbalance factor, which is given by:

$$IUF_2 = \frac{I_2}{I_1} \times 100(\%)$$

- IUF 0

  The zero sequence branch current unbalance factor, which is given by

$$IUF_0 = \frac{I_0}{I_1} \times 100(\%)$$

  Observe all these alerts after running ULF.

Unbalanced Load Flow

ULF-Example 2

File Location:
Open the ETAP File – UNBALANCED LOAD FLOW (ULF) ->Examples->ULF_Example2
Library Location – C: -> ETAP 1610 -> lib -> etaplib1610.lib

This exercise demonstrate method of connecting 2 phase cables and single phase loads. For running ULF with such types of unbalanced circuit.

In the SLD observe Bus671 and connect it to system on left side through phase adapter, based on the additional system already modelled in ETAP. The phase adapter should be connected for 2 phase CA application.

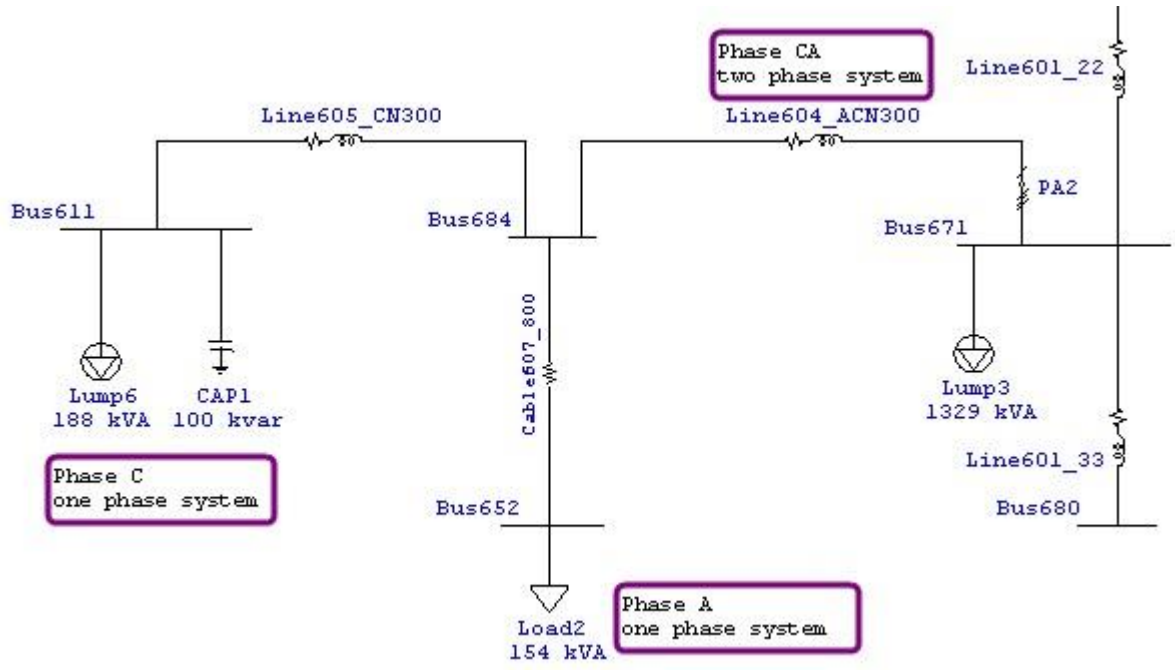
Connect main SLD Bus671 to new unbalanced circuit Bus684 through phase adapter as per line data and SLD details given in the following part of exercise:

Since new SLD is already modelled check the inputs given are correct as per sketch given below:

1. Additional System Data Entry
   - Load parameters

Entries	Lump 6	Cap1	Load2
Phase	C	C	A
kV	2.4	2.4	2.4
KVA	188	100	154
PF	90.48 %	0 %	83 %
Motor Load %	50%	N/A	N/A

Unbalanced Load Flow



- Parameters for Cable607_800 modelled as impedance:

Entries (For phase A & C)	Cable607_800
R	1.4925 %
X	0.6231%
Base kV	4.16
Base MVA	1.1

- Parameters for Line604_ACN300 and Line605_CN300

Entries	Line605_ACN300	Line605_CN300
Info Page		
Length	300 ft	300 ft
Configuration Page		
Phase A -- X	0	0 for N
Phase A -- Y	28	29 for N
Phase C -- X	7	7
Phase C -- Y	28	29
Ground Wires G1	checked	checked
G1 -- X	3.5	0
G1 -- Y	34	34
Conductor/Phase	1	1

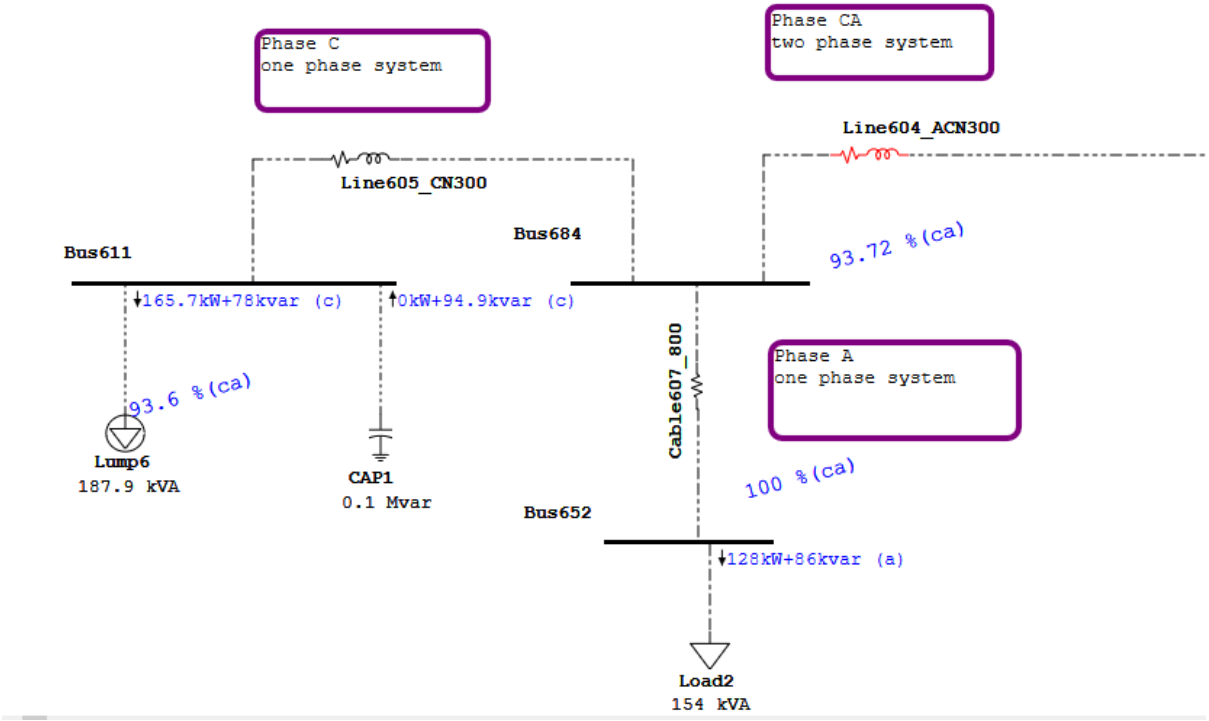
Unbalanced Load Flow

- Editor specifically designed for ULF – Bus, Transmission Line, Impedance, Lump Load

2. Use the default Study Case.

3. Run Unbalanced Load Flow.

Unbalanced Load Flow



4. Check results from report, OLV, display, and alert.