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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Major Project Report Phase - 2 on

" ANALOG BANDGAP REFERENCE DESIGN USING SKY130 "

Submitted in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics and Communication Engineering

Submitted by

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CERTIFICATE

This is Certified that the Major project work entitled **"Analog Bangap Reference design using sky130"** carried out by **Sadaf Taneem, Sneha Anantapur, Sushma Bhosale** bonafide students of **VP Dr P.G Halakatti College of Engineering and Technology, Vijayapura** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belgaum** during the year 2025-2026. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The Major project report has been approved as it satisfies the academic requirement in respect of Major project work prescribed for the said degree.

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ACKNOWLEDGEMENT

ABSTRACT

This work presents the design and implementation of a CMOS bandgap voltage reference circuit using the open-source Skywater SKY130 PDK. The objective is to develop a temperature-independent and process-variation-tolerant reference voltage suitable for integration in mixed-signal and analog systems. The proposed BGR utilizes bipolar junction transistors (BJTs) available in the SKY130 process, along with a combination of proportional to absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) voltage sources to achieve temperature compensation. The design targets a reference voltage of approximately 1.2 V, with minimal curvature error a cross a wide temperature range (-40°C to 125°C). Circuit simulations were conducted using the NG Spice environment and tools from the open-source Skywater PDK ecosystem. Post-layout simulations confirm the robustness of the design with low line sensitivity, good power supply rejection, and reduced temperature coefficient, making it suitable for low-power and precision analog applications.

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CHAPTER 1:
INTRODUCTION

1.1. Bandgap Reference Circuit (BGR) :

Bandgap reference circuit is an analog Ip block . It provides constant reference voltage irrespective of temperature , supply voltage and process variations. It is used in a number of analog and mixed circuit such as LDO , ADC, DAC.A bandgap reference circuit utilizes a combination of transistors and resistors to create a voltage that's independent of these factors as shown in Fig1.1.
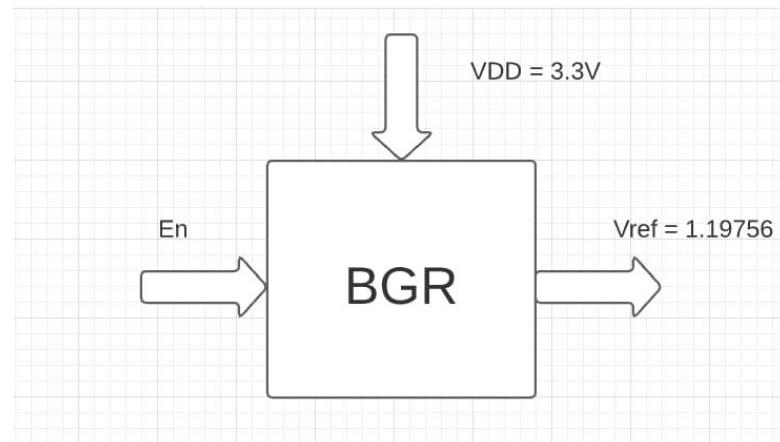
Fig 1.1.I/O of a BGR

In a BGR (Bandgap Reference) circuit, CTAT (Complementary to Absolute Temperature) and PTAT (Proportional to Absolute Temperature) circuits are combined to create a temperature-stable reference voltage as shown in Fig 1.2.

The BGR leverages the opposite temperature characteristics of CTAT and PTAT to compensate for each other, resulting in a voltage that is relatively insensitive to temperature variations.
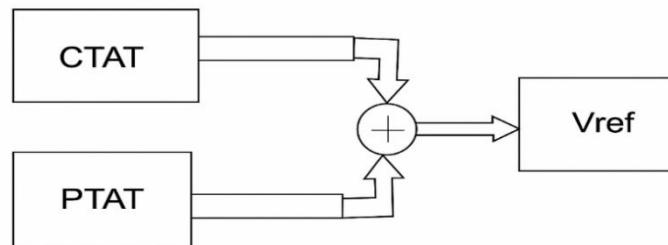
Fig 1.2. Bandgap Reference Circuit

CTAT part has negative temperature co-efficient that is decrease with increase temperature. Where as PTAT has positive temperature co-efficient that is increase with arising temperature .

1.2. Complementary To Absolute Temperature (CTAT) :
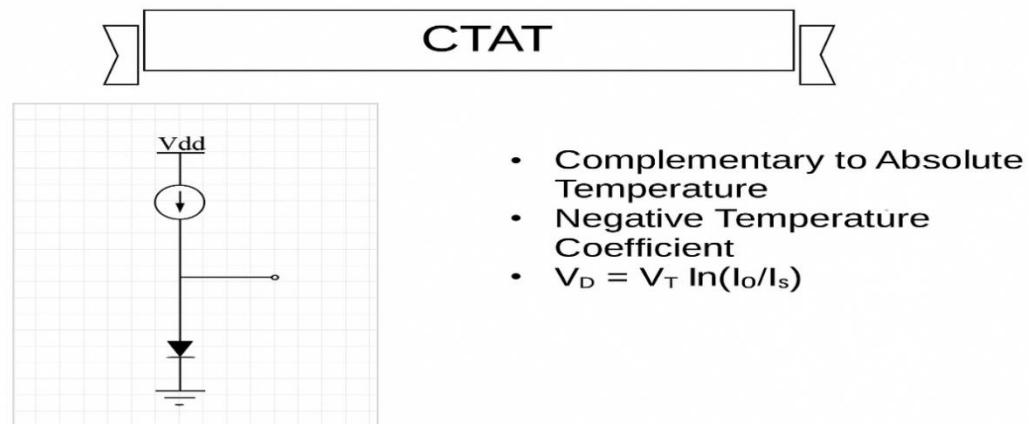
Fig 1.3. CTAT

CTAT stands complementary to absolute temperature.It consists of current source connected to Vdd and diode connected to gnd as shown in fig 1.3.

- $V_D = V_T \ln(I_0/I_s)$.

- Here V_T stands for Thermal Voltage
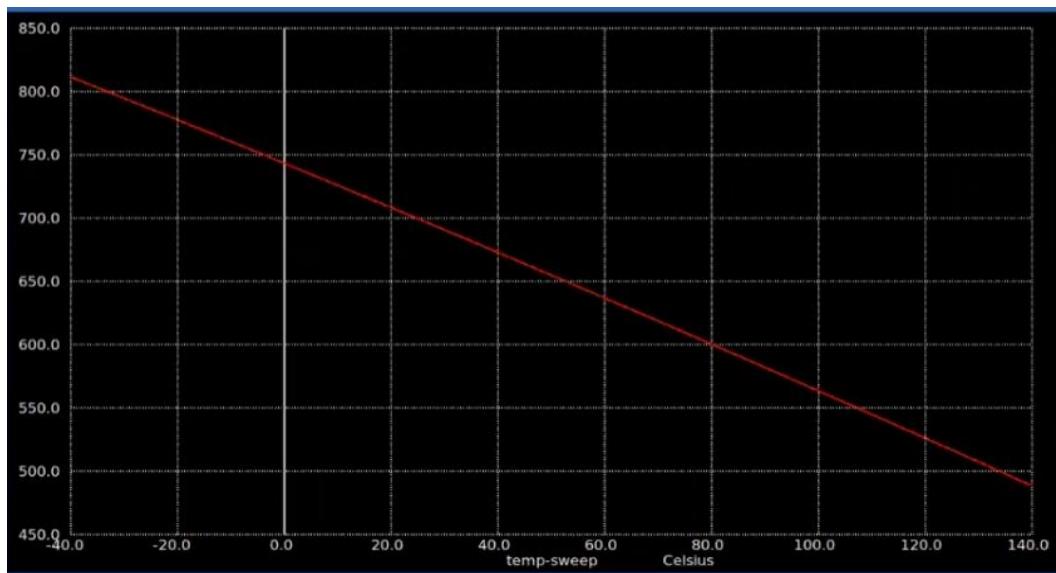
Fig 1.4. CTAT Slope

As the temperature increases the value of CTAT decreases.Fig 1.4 is a CTAT slope.

1.2. Proportional To Absolute Temperature (PTAT) :

- Proportional to Absolute Temperature
- Positive temperature coefficient
- $V_2 - V_D = V_T \ln (n)$
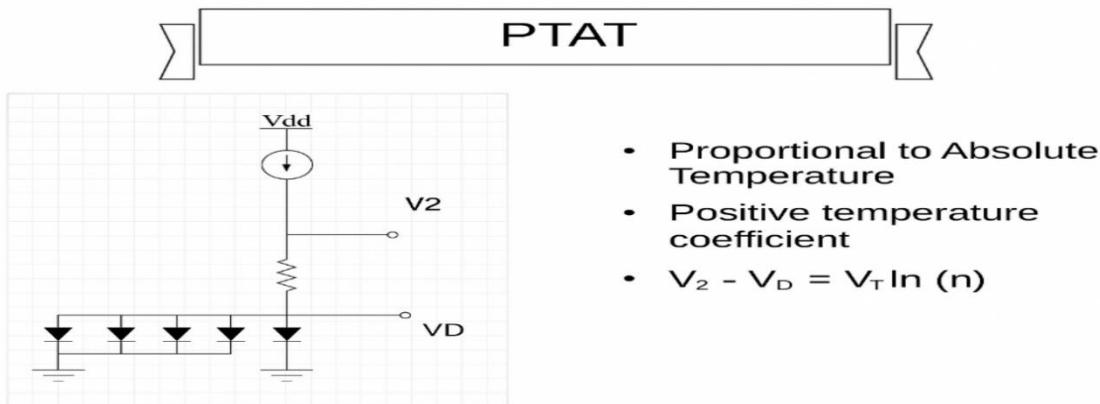
Fig.1.5. PTAT

- PTAT - stands proportional to absolute temperature .

- It is circuit current source connected to Vdd and resistor and number of Vdd connected to gnd.
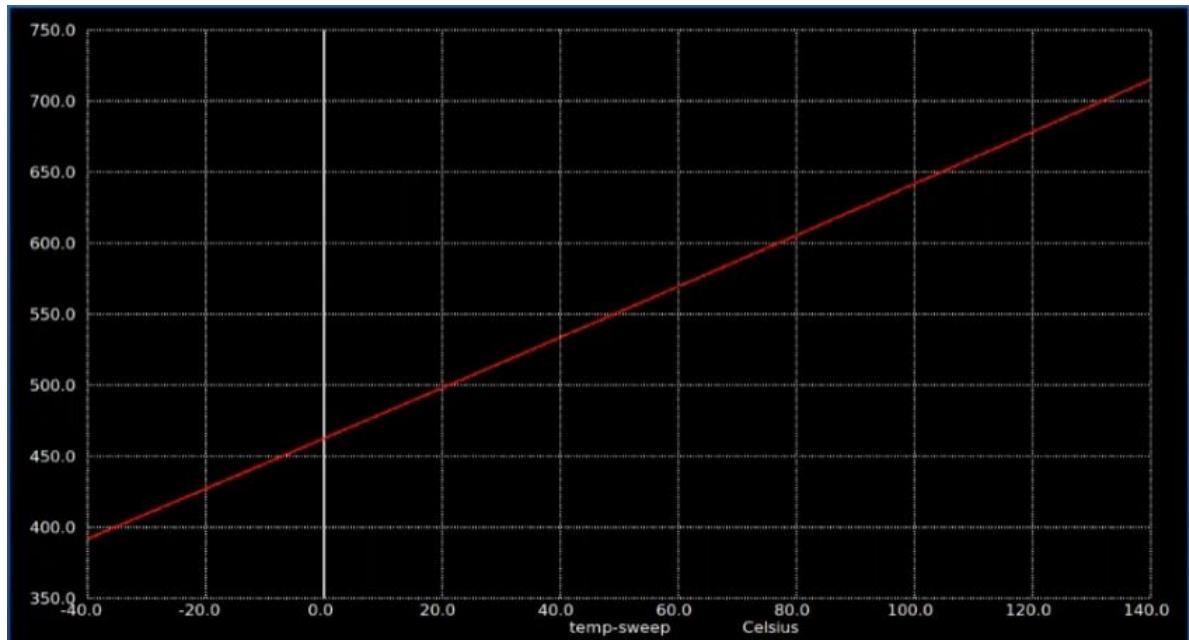
Fig 1.6. Plot of PTAT

Fig1.6 shows the graph :output vs temperature from –40°C to +140°C.Output increases linearly with temperature.This is typical of a PTAT circuit or temperature-dependent device.

- The straight red line indicates good linearity with temperature.

1.3. Traditional BGR
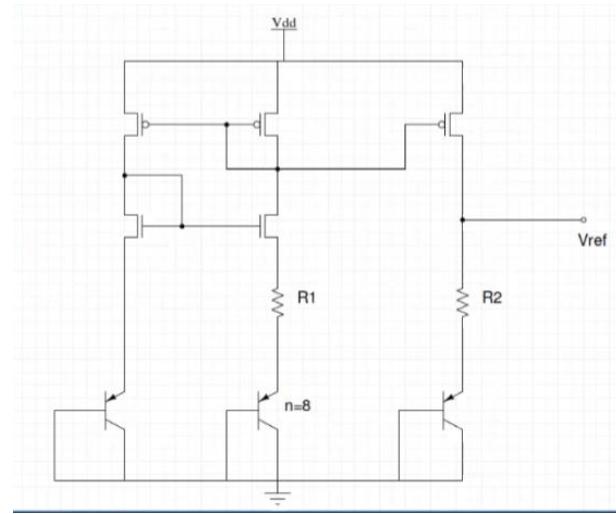
Fig 1.7. Traditional BGR Circuit

- It is a traditional BGR Which uses a current mirror for providing a constant Current source

- α1and α2 are used for adjusting values of PTAT &CTAT, so that they cancel each other perfectly.

  - α1 is kept constant as 1.
  - We make sure that α1, multiplied by Slope of PTAT plus slope of CTAT should be equal to zero to achieve a constant Vref at output.
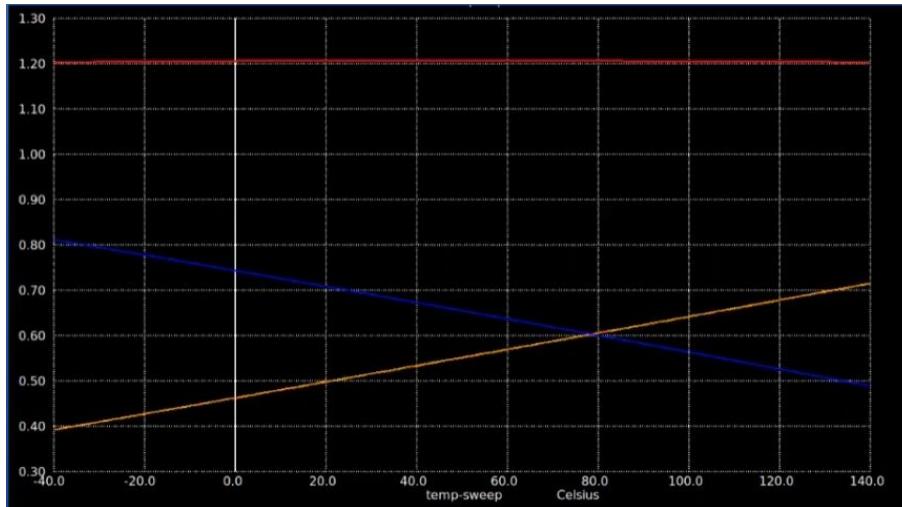
Fig 1.8.Plot of BGR

- Here the yellow line represents the PTAT.
- Blue line shows CTAT.
- We can see PTATS CTAT cancel each other perfectly.
- And the red line is Vref line which shows Vref output at BGR.

This is a **temperature-sweep plot** showing how *three different quantities* change as temperature   varies from about **–40°C to +140°C**.

Axes :

X-axis: Temperature (°C)

Y-axis: Some measured quantity (could be voltage, resistance, gain, etc.—the graph doesn't specify)

The three curves

There are **three lines**, each representing a different parameter:

1. Red Line — Flat (constant)

The red line is nearly horizontal at around **1.20**.

Interpretation:
This parameter does **not change with temperature**, or changes very little.
In engineering, this might indicate:

>   A stable voltage reference

>   A normalized constant

>   A device parameter insensitive to temperature

2. Blue Line — Decreasing with temperature

Starts near **0.80** at –40°C

Drops to about **0.48** at +140°C

Interpretation:
This parameter **decreases linearly** as temperature increases.

This is typical of:

Semiconductor mobility

Resistance with a negative temperature coefficient (NTC)

Frequency drift

Sensor sensitivity decreasing with heat

3. Orange Line — Increasing with temperature

Starts around **0.38** at –40°C

Reaches about **0.73** at +140°C

Interpretation:
This parameter **increases linearly** with temperature.

Typical causes:

Resistance with positive temperature coefficient (PTC)

Leakage currents

Amplifier offset drift

Interesting point

The **blue and orange lines intersect around ~75°C**, meaning at that temperature both
parameters have the same value (~0.60).
This is often significant because it marks:

A compensation point

A crossover temperature

Where two opposing temperature effects cancel each other

Over all Interpretation

The graph likely comes from an engineering testbench (perhaps analog IC or sensor
characterization).
It shows:

>>One stable parameter (red)

>>One that decreases with temperature (blue)

>>One that increases with temperature (orange)

This is a typical pattern in:

>>Bandgap reference circuits

>>Temperature-compensated bias circuits

>>Sensor calibration sweeps

CHAPTER 2 :

LITERATURE SURVEY

1. BGR (Bandgap Reference):

A Bandgap Reference (BGR) circuit generates a constant reference voltage that is independent of temperature, supply voltage, and transistor parameters.

It is mainly used in analog and mixed-signal ICs (like ADCs, DACs, regulators).

The output reference voltage (Vref) is usually around 1.2 V, which equals the silicon bandgap voltage at 0 K.

2. PTAT (Proportional To Absolute Temperature):

A PTAT voltage increases linearly with temperature.

It is generated by taking the difference in base–emitter voltages (ΔV_BE) of two transistors operating at different current densities.

3. CTAT (Complementary To Absolute Temperature):

A CTAT voltage decreases linearly with temperature.

It comes from the base–emitter voltage (V_BE) of a bipolar transistor, since V_BE drops by about –2 mV/°C as temperature increases.

4. Vref (Reference Voltage):

It's the final temperature-independent voltage output of the Bandgap Reference circuit.

It is made by combining PTAT and CTAT voltages such that their temperature dependencies cancel each other out.

5. Traditional Bandgap Reference Circuit :

Two BJTs (one with emitter area n× larger than the other).

Two resistors (R1, R2) for scaling voltages.

Often includes an op-amp or transistor mirror for biasing.

In modern integrated circuit (IC) design, generating a voltage reference that remains stable under varying temperature, supply voltage, and process conditions is a critical requirement. Many analog and mixed-signal systems such as ADCs, DACs, voltage regulators, and power management circuits rely heavily on a Bandgap Reference (BGR) circuit. The bandgap reference provides a constant voltage (usually around 1.2 V) derived from the physical properties of silicon.

Over the years, numerous research efforts have been made to enhance the accuracy, power efficiency, and temperature stability of the BGR circuit. The development started with the early bipolar designs and evolved to modern CMOS implementations that can operate even below 1 V supply. This section reviews some of the most influential and highly cited research papers that have contributed significantly to the development of the BGR concept.

1. The Foundational Work by R. J. Widlar (1971)

The concept of the bandgap reference was first proposed by **R. J. Widlar** in his paper "New Developments in IC Voltage Regulators" published in 1971 [1]. This work laid **the foundation of all temperature-independent voltage references** that are used today.

Widlar observed that the base-emitter voltage (V_{BE}) of a bipolar transistor decreases linearly with temperature (a CTAT – Complementary to Absolute Temperature behavior), whereas the difference between two base-emitter voltages (ΔV_{BE}) behaves as PTAT (Proportional to Absolute Temperature). By combining a CTAT voltage and a PTAT voltage in proper proportions, he achieved a voltage that was nearly constant across temperature variations — approximately 1.25 V, which corresponds to the energy bandgap of silicon at absolute zero.

The innovation in Widlar's work lies in the simple yet elegant combination of temperature-dependent parameters to cancel each other out. His design approach became the core principle for subsequent analog voltage references.

In practical applications, Widlar's bandgap structure is still considered the **classical architecture**, often called the "**Bipolar Bandgap Reference**" or "**Widlar Bandgap**." It provides excellent temperature stability, though it requires bipolar transistors and resistors, which consume more area and power.

This foundational idea is what later designs, including CMOS-based versions such as in the Sky130 process, build upon and refine to achieve low-voltage and low-power operation.

2. Low-Voltage CMOS Implementation by K. N. Leung and P. K. T. Mok (2003)

As CMOS technology advanced and supply voltages started shrinking below 1.5 V, the traditional bandgap circuits designed for bipolar technologies faced major challenges. In 2003,

K. N. Leung and P. K. T. Mok presented a paper titled "A CMOS Bandgap Reference Circuit with Sub-1-V Operation" [2], which addressed these scaling issues**.**

This work is considered one of the **most significant breakthroughs** for bandgap references in modern CMOS processes. The authors developed a **low-voltage design technique** that allowed the BGR to function reliably even at supply voltages as low as 0.9 V. This was achieved by **using CMOS transistors to emulate the bipolar behavior** and by cleverly modifying the circuit topology to reduce headroom requirements.

The paper introduced several improvements such as:

- Using **operational amplifiers** for better loop control.
- **Current mirror techniques** to replace large resistors.
- Compensation schemes to minimize line and load regulation effects.

Their design consumed very low power, making it highly suitable for **portable and battery-operated systems**, which aligns well with today's demand for energy-efficient devices.

For a project based on Sky130 technology, which supports both NMOS, PMOS, and parasitic BJT devices, the approach discussed by Leung and Mok is especially relevant. Their method shows how a **traditional bipolar concept can be adapted to CMOS technology** while maintaining stability and accuracy.

Overall, this paper represents the evolution from bipolar to CMOS implementations, marking a key transition point in the development of analog reference circuits.

3. Resistor-Less Design by A. Bakker, R. F. Wassenaar, and J. H. Huijsing (2002)

The next important milestone came from **A. Bakker, R. F. Wassenaar, and J. H. Huijsing** in their 2002 paper titled "A CMOS Bandgap Reference without Resistors" [3]. Traditional bandgap circuits required precision resistors for generating PTAT currents and voltage scaling. However, resistors consume large chip area, increase process variation, and limit circuit integration in modern SoC (System-on-Chip) designs.

This paper proposed a fully resistor-less CMOS bandgap reference, which was a remarkable innovation at that time. Instead of using resistors, they implemented **MOSFETs operating in the subthreshold region** to replace resistor behavior. This greatly reduced the area, power, and process dependency of the design.

The authors also emphasized how the resistor-less architecture improves matching and trimming accuracy, which directly affects temperature stability. Moreover, removing resistors made the circuit much more compatible with standard digital CMOS processes, eliminating the need for special analog components.

For students and engineers designing in Sky130, this paper serves as an excellent reference because the Sky130 PDK allows flexible use of MOS devices for analog emulation. Using the concepts from Bakker's work, designers can create compact and integration-friendly bandgap references that are ideal for mixed-signal VLSI systems.

The resistor-less concept has since inspired many modern low-power BGR architectures, proving that analog precision circuits can coexist efficiently with dense digital environments.

4. Optimized 1.2 V CMOS Bandgap Reference by B. Razavi (1999)

In 1999, **Behzad Razavi,** a well-known figure in analog design, presented a refined approach in his paper "Design of a 1.2 V CMOS Bandgap Reference" [4]. This design modernized the classical Widlar structure and adapted it **for low-voltage CMOS implementation** while ensuring **good line and temperature regulation**.

Razavi's design incorporated:

- Carefully matched transistor pairs for improved accuracy.
- Enhanced start-up circuits to guarantee reliable operation at power-on.
- A simplified layout that minimized offsets and mismatches.

His circuit achieved high temperature stability and better startup behavior without the complexity of trimming or calibration. The 1.2 V output corresponded to the silicon bandgap, making it ideal as a reference for ADCs and other precision analog systems.

What makes Razavi's contribution special is his practical design perspective. Unlike purely theoretical works, this paper provided clear design equations, layout strategies, and performance comparisons that can directly guide a student or engineer through the design process.

In your project using Sky130 technology, Razavi's techniques can help optimize transistor sizing, bias current selection, and temperature compensation — all of which are crucial for achieving accurate BGR performance.

5. Comparative Understanding and Evolution

The evolution of the Bandgap Reference can be seen as a **progressive journey** — from the early bipolar structures to sophisticated CMOS architectures. Widlar's original principle established the temperature-compensation concept, which remains unchanged even today. Later works by Leung, Bakker, and Razavi improved the design by addressing **power efficiency, integration, and scalability** challenges.

From Widlar's invention to the latest CMOS advancements, the Bandgap Reference circuit has evolved to meet the needs of low-voltage and high-integration technologies. Each of the four highlighted papers contributed a unique innovation — either in principle, structure, or optimization.

For the current project on Analog Bandgap Reference using Sky130, these research works provide a strong theoretical and practical foundation. Widlar's concept defines the temperature-stable mechanism, Razavi's design offers CMOS implementation guidelines, Bakker's approach enables compact integration, and Leung's work extends operation to sub-1 V domains.

Together, these references form the literature backbone of this project, guiding the design decisions, simulation strategies, and performance evaluation for the proposed BGR circuit.

The **primary objective** of this project is to design and implement a high-performance Analog Bandgap Reference (BGR) circuit using the SKY130 CMOS technology that generates a temperature-independent and stable reference voltage. The design aims to accurately combine PTAT (Proportional-To-Absolute-Temperature) and CTAT (Complementary-To-Absolute-Temperature) characteristics to achieve a well-balanced output voltage (Vref) across a wide temperature range.

This project further focuses on optimizing the BGR circuit for low power consumption, layout efficiency, and process-voltage-temperature (PVT) robustness. Using the open-source SKY130 process, the objective also includes understanding device behavior, implementing precise biasing techniques, and validating the reference voltage through schematic simulation, corner analysis, and layout-versus-schematic (LVS/DRC) checks. Ultimately, the goal is to realize a reliable, CMOS-compatible, and silicon-ready bandgap reference that meets standard analog design specifications.

CHAPTER 3 :

NECESSARY OPEN SOURCE EDA TOOLS INSTALLATION

SKY130 is an open-source Process Design Kit (PDK) developed by Skywater, Efables, and Google. It is based on SkyWater's 130nm CMOS technology and provides designers with access to chip design technology to create new and manufacturable designs. The SKY130 PDK offers several advantages, including free, open-source tools and the ability to fabricate chips at a lower cost.

3.1. Key Features and Benefits:

Open-source:

The PDK and related resources are free to use, eliminating the cost barrier to entry for chip design.

130nm Technology:

It leverages Sky Water's mature and widely used 130nm CMOS process.

Custom ASIC Design:

Allows designers to create custom ASICs with a focus on ease of use and cost effectiveness.

Open-source tools:

The PDK is supported by a community of open-source tools, including ChipIgnite, a pre designed carrier chip and automated design flow.

Access to SkyWater Foundry:

Designers can utilize SkyWater's foundry to fabricate chips designed using the SKY130 PDK.

3.2. Installation Processes required for designing of Analog BandgapReference using sky130.

Ngspice installation :

sudo apt-get install-y ngspice

Magic installation :

sudo wget "http://opencircuitdesign.com/magic/archive/magic-8.3.122.tgz"

tar-xvzf magic-8.3.122.tgz cd magic-8.3.122

sudo ./configure

sudo make

sudo make install

PDK installation :

 make a folder as pdks

 cd pdks

 git clone https://github.com/google/skywater-pdk

 cd skywater-pdk

 git submodule init libraries/sky130_fd_pr/latest

 git submodule update

 make timing

 cd ../

 git clone git://opencircuitdesign.com/open_pdks

 cd open_pdks

 sudo ./configure--enable-sky130

 pdk=/home/anmol/Desktop/webinar/pdks/skywater

 pdk/libraries--with-sky130-local-path=/home/anmol/Desktop/webinar/pdks

 sudo make

 sudo make install

CHAPTER 4 :

METHODOLOGY

The methodology for designing a bandgap reference (BGR) circuit using the SKY130 technology involves first understanding the core principles of BGR design, then choosing a suitable BGR topology, and finally, using open-source tools Ngspice , Magic and PDK for simulation and design. This includes implementing the PTAT and CTAT components, often using current mirrors and amplifiers, and then carefully simulating and optimizing the circuit for temperature and supply voltage stability.

We have designed a BGR by running a SPICE netlist.

4.1. BGR Netlist :

The netlist is written and saved in a file named Temp.cir

Using the SPICE netlist we have designed the Bandgap Reference Circuit shown in Fig .4.1.
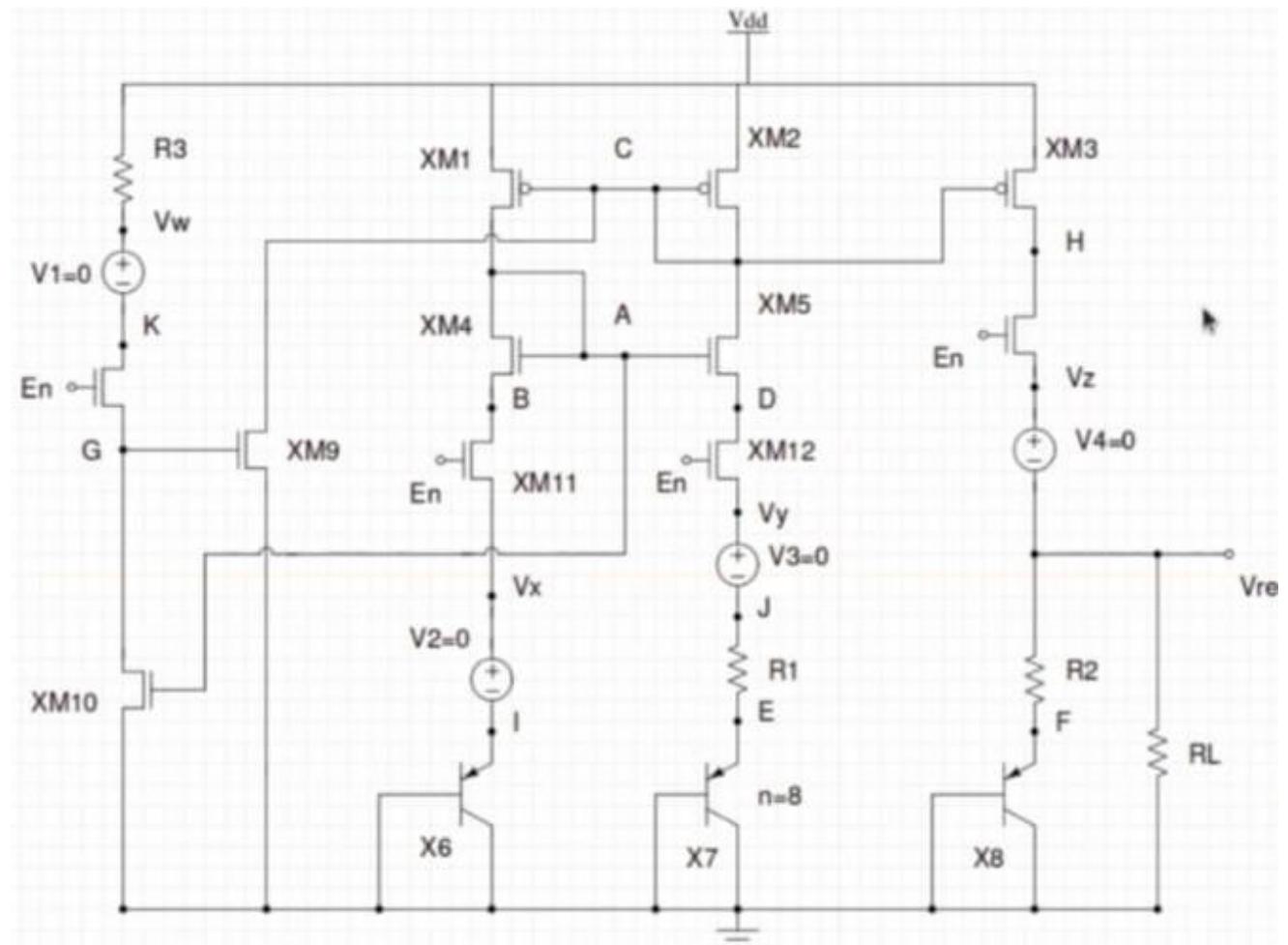

Fig 4.1.The BGR Circuit

First line is a comment line

Third line Saves the branch current

4th & 5th line gives the address of libraries which will be used for simulation

Now looking for circuit elements

For MOSFETS

- First we will write name of transistor.

- then the terminal.

Ex:XM1 A C C VDD VDD

Here XM1 is the name of Transistor

A is Drain

C is Gate

VDD is source

VDD is substrate.

For XM1 the drain terminal is connected to A node, the gate terminal is connected to C node the source and Substrate are connected to VDD. Next we write the model name of the transistor which we have used,and in the last of line we write length and width.

For BJT

Ex: X6 GND GND I GND

First GND is Collector.

Second GND is Base.

I is Emitter

Third GND is substrate

In X6 as we can see only the emitter is Connected to the node and all other In X6 as we can see only the emitter is Connected to the node and all other terminals are connected to ground, so we have written GND GND I and Ground.Next we have written the model name for the BJT.

And lastly M=1 represents the Number of BJT connected to this node.If a number of BJTS are connected to the Same terminals then we can write the number of BJTS connected to similar terminals,for the above sentence ex is X7 here we have 8 BJTS Connected to similar terminal have directly written M=8 in our code.

For Resistors

First we write Resistor name.

Then both the terminals to which it is Connected

Then it's value

Ex: RL GND Vref 100MEG

RL is the Resistor Name

GND and Vref are both the terminal to which it is connected.

100 MEG is value.

In our code we have not given the value for R1, R2, R3 because further we will give the values and take out graphs.Voltage Sources V_1, V_2, V_3 & V_4 are given so that We can measure the current flowing through the branch.

We have connected VDDA to VDD and GND and it is DC voltage of 3.3V

→VDDA VDD GND DC 3.3V

We have also connected a DC voltage of 3.3v Source to enable to make it on

→VD En GND DC 3.3V

.dc temp -40 140 0.1

↳ This line is used for DC analysis, it gives the temperature Switch from -40 to 140 °C With step size of 0.1

From line 45 to 53 are used for running the DC analysis.

All the plot are used and to plot the voltages which we want

After running the netlist we we get plots of Vref, CTAT and PTAT.

4.2. Layout Phase :

For layout design we need to start with building blocks.

So we need PMOS and NMOS of W/L ratio of With 20/5 and 20/1. and We also have to make the resistors of 30 K to 273 & 200 K

First We will create a new folder name it **Layout**

Inside the layout folder copy the Tech file.It should be under

>> Desktop >> Major Project>> Sky 130 » PDKS » Sky 130 A> > libs.tech>> magic >> Sky 130A.tech.>> Copy the Sky 130 A.tech file and paste it in Layout Folder

Now open the terminal in layout folder and type

>> magic -T Sky130A.tech

The Window of magic opens

Here we will make pmos of ratio W/L as 20/5

In magic terminal, type

>> box 0 0 500 2000 >> click enter.
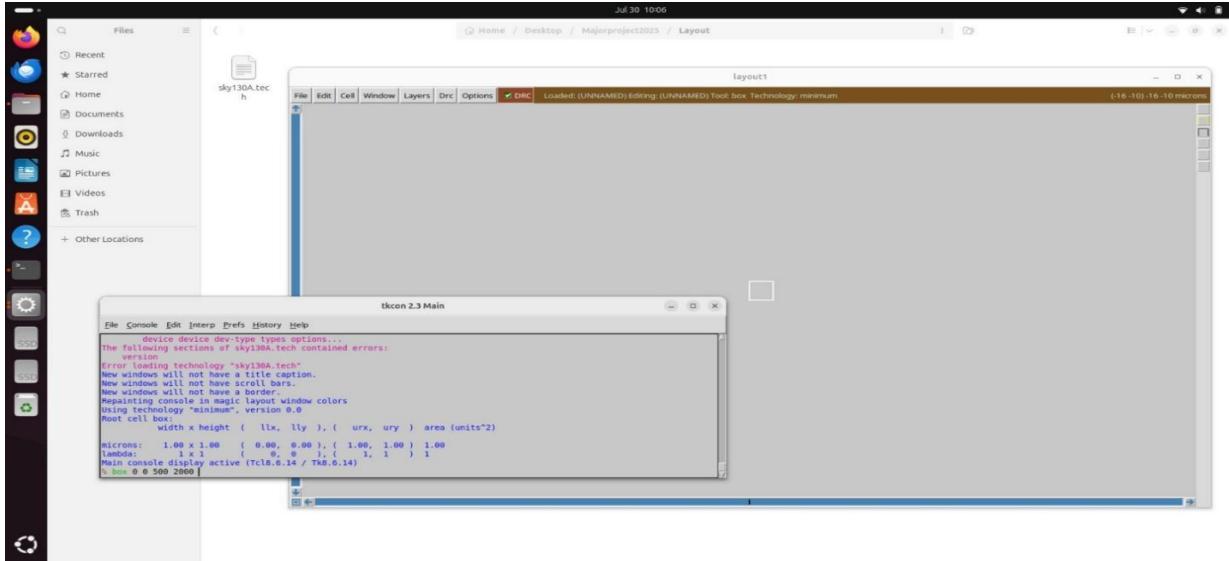
Fig.4.2.

Now fill the box which we have recieved in window with polysilicon
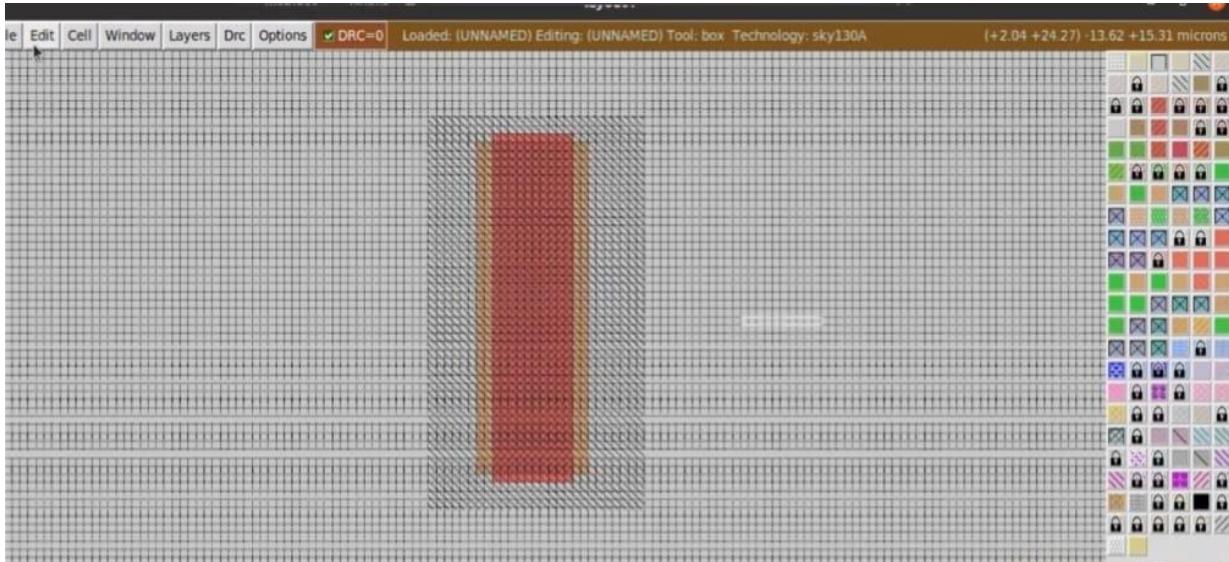
Fig.4.3.Pmos Layout

Now set the grid :Windows >> set grid 0.50um

We will fill this area with Polysilicon and we will put the grid to as now we will put left off button and other side right button and use will fill this area N diffusion now we will take area little bit bigger than and we will put over the polysilcon we extend this and lie save this as pmos 520

We will make Nmos of W/L ratio 2015 for that go to the box 0 0 500 2000 we will fill this polysilicon we will put the grid to 0.5 & we Select the area little bit danger on both Sides and we will Select MVN diffuse we extended Polysilicon both sides & we will save this file as Nmos520

We will make an Nmos of W/L.as 20/1 we go to magic terminal window type 60x 0 0 100 2000 we fill it with polysilicon & we will set the grid 2.5 & select area little bit larger than this we will extended Polysilicon layer.
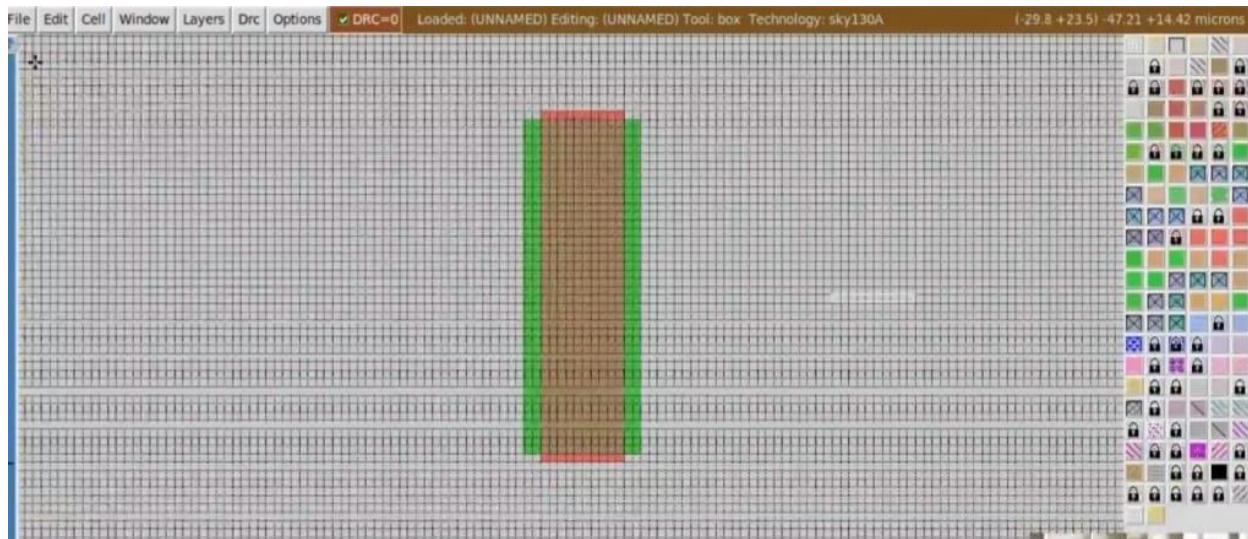

Fig.4.4.Nmos Layout

Now we save this file as NANOS12.

we have completed the layout of the pmos and nmos Now we proceed to the layout of the resistors.We need resistance of 30k, 200k, and 273k for that we are going to use poly persian resistance given by skywater pdk.

 Actually these resistance have a very high resistance of the 2000 volts/sq which is fixed 0.5 and length we can change as per our needs so by simple Calculation we find 30k resistance we require length

First we go to magic terminal and type >> box 0 0 530 35

We fill this area with polyris material by now we set the grid to 0.1 micro m and we will put the contacts The contacts we will use this for poly silicon and we save this file as resistor30k.

Similarly far 200k resistor we will require the length of 350 our 35 um so we will go to magic window to type box o 03504 35 200 fill this x polyris material & then set grid to 0.1 we fill this arca X Poly-contact and save this as resistor200K.
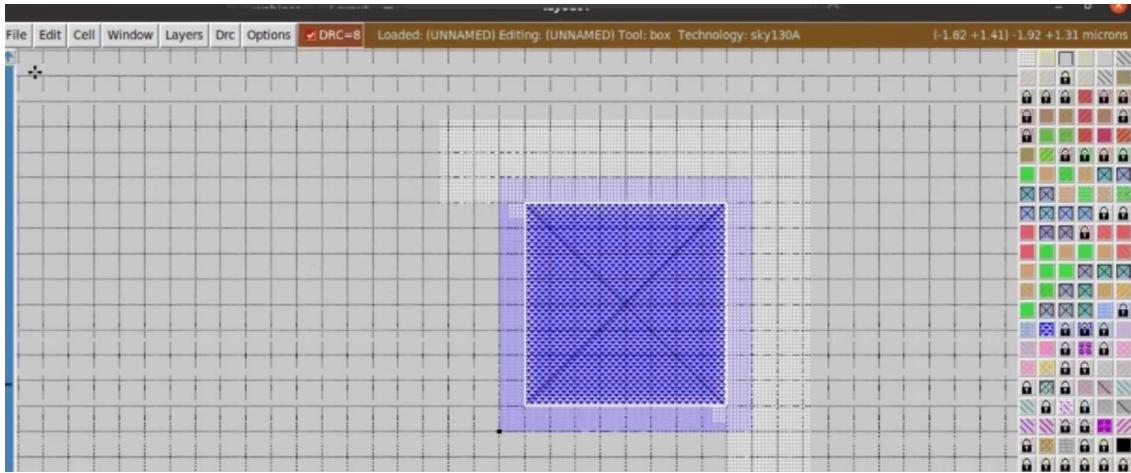
Fig.4.5. pmos metal contact.

Now we will perform the layout of resistor 273k we need the length of 95.5sum go to magic terminal type box 0 0 9559 35 we fill this area with polyris and select grid 0.1um & we fill the contact .

Save this resistor273K.

Now we have completed building blocks of the circuit.Now we proceed with the layout design of entire BGR circuit

Go to cell>> place instance>> click on pmos520.mag >>open

To see the layers we press X.according to ckt we need 3 Pmos and 8 Nmos now we will start Placing them

we go to cell>> Place instance>> PMOS520.mag.

We will make pmos substrate contact we placed the PMOS520.mag go to cell place instant Nmos120.mg, NMOS520.mag, NMOS20. mag, NMOS520.mag.

These are all **MOSFETS**
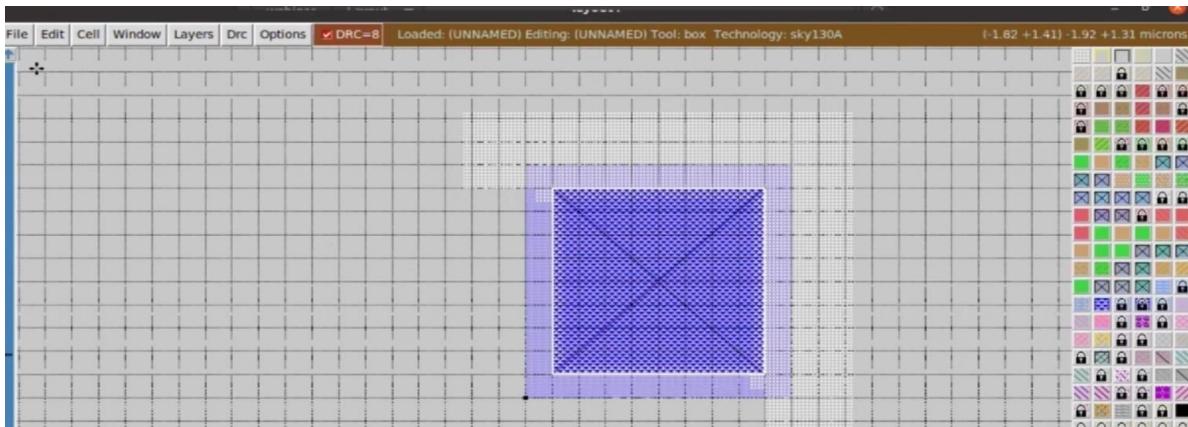
Fig.4.6. Nmos metal contact

Now we place the **BJT'S**

Go to cell>> place instance and we select the file sky130fd_pr_pnp_05us W3P4OL open this file Now according to design we need 10 BJT'S now we have to place the resistances so we put the arbitraries resistor273k.mag Now we place the 200k resistance and we place 30k resistance after this we need to see supply raise ground raise for that we will right click and then we make the supply raise metal 3 we will Name the transistor go to edit and Text and we give the Name

Text String:- XM1

Size (um):-2 of puress apply

we do similarly for all transistors save this file BLIR

Let Start with making the pmos to metal1, contact we will first set the grid 0.2um and go to magic terminal box 0 00 100 100 .Now we will put the localie layer and then Metal 1. layer & we put wire line this showing DRC error do not worry about that save this file as pmos2metal.

Now we will make nmos metal 1contact for that we go to magic terminal window.

Type >>box 0 0 100 100 Now we will put here localie layer and metal 1 layer we set the grid 0.1 and we put wire line and save this file nmos2 metal.

Go to magic terminal type>> box 0 0 200 700.

Now fill this are with M V M substrate and then we put localie layer and metal 1 layer , metal 2 layer and metal 3 layer.We set the grid to 0.1um and we put M-V-M Substrate.

Then we put via wire and we put M2 contact and then we PILE M3 contact we save this by the line pmos substrate.Proceed with making nmos contact go to magic terminal windows type box 0 0 200 700 we fill this m-v-psubstrates P-diffusion layer and localie layer metal 1 layer and now we will Set grid 2.1 and we will put the m-up substinates P contact and then we put uiadine save this nmos substrate.

Now we left with Vdd contact for that we go to magic window type box 0 0 200 700 we will fill this metal 1, metal 2, metal 3 layer fet set grid 2.1 and we put the metal 2 contact, layer and metal 3 contact we will save this Vdd contact"

we will open our design by typing >> magic-T sky130A.tech and we type file name BGR. magic

First we start the connection to the pmos to XM1,XM2, XM3 are the pmos they are connected to the Vdd we set the window grid 0.1 & we go to cell place instance we search for Pmos metal contact file & place it and we make same far all Now we place the pros Contacts.

Now we will proceed placing the Vdd contacts go to cell place instance we select udd contacts press open we repeat this par 3 times Now we select entry area Press X Now we connect this metal 1.

After this we put Pmos substrate in between Vdd contacts go to place instant and we go to pmos substrate then open repeat for 3 times here it is showing DRC error because we have forgot to do nwell layer. Now we have completed pmos Vdd contacts.

Now we will place the other contact of pmos on the downside to window select grrid 0.1 and go to cell Place instance PMOS2Metal then open we repeat for another 2 Pmos

Now we are done with pmos.

*Now we start with wnmos we will place this under the block press X according to design are need to connect XM1 and XM4, XM4 is connected to XM11

XM5 is connected to XM12 will go to cell place instance NMOSmetal we do same for XM5 also now we place the metals.
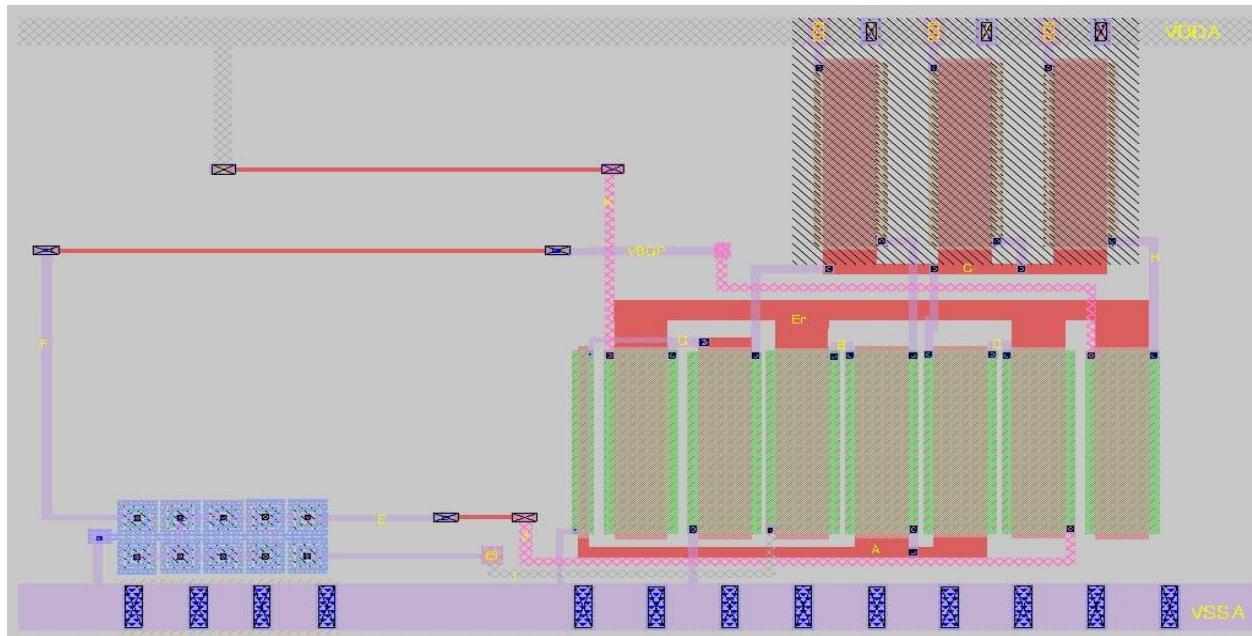

Fig 4.7. Complete Layout of a BGR Circuit

First we connect XM1 to XM4 we use metal1 layer to connect like wise we connect XM2 to XM5 we connect XM4 to XM11 and XM5 to XM12 and we need to XM3 to XM13.

Now go to cell >>place instance>> resistance 200k

Now we go to select area type "rotate 90" we press x No we will put a "Nomos contout go to cell place instant UMO metal resistance 200k is connected to Vdd to place Vdd contact we go to cell place instance

From the circuit we see gates of XM1, XM2 and XM3 are connected so we connect them using. Polysilicon layer

For nmos we connect XM4 and XM5

XM4 gate is connected to XM4 drain

we will name the nodes go to edit text

Text string:-En

size (mm) :- 1 then apply.

CHAPTER 5:

SIMULATION ANALYSIS

5.1. BGR Circuit Analysis

Now from the graph we will find the slope of CTAT and PTAT

Lets start with CTAT .we will click the left mouse button on 40. & while pressing it we will go to point 60 and then leave it.

This will give the slope CTAT :dy/dx : -0.0054054

Repeat same for PTAT (values are same)

Slope of PTAT : dx/dy = -0.000191176

Comparing the values which we have got from CTAT and PTAT, now looking into the formula

➢ slope of CTAT w e have recieved as

according to dy= -0.00154054 formula.

After running the netlist these are the graphs which we have received
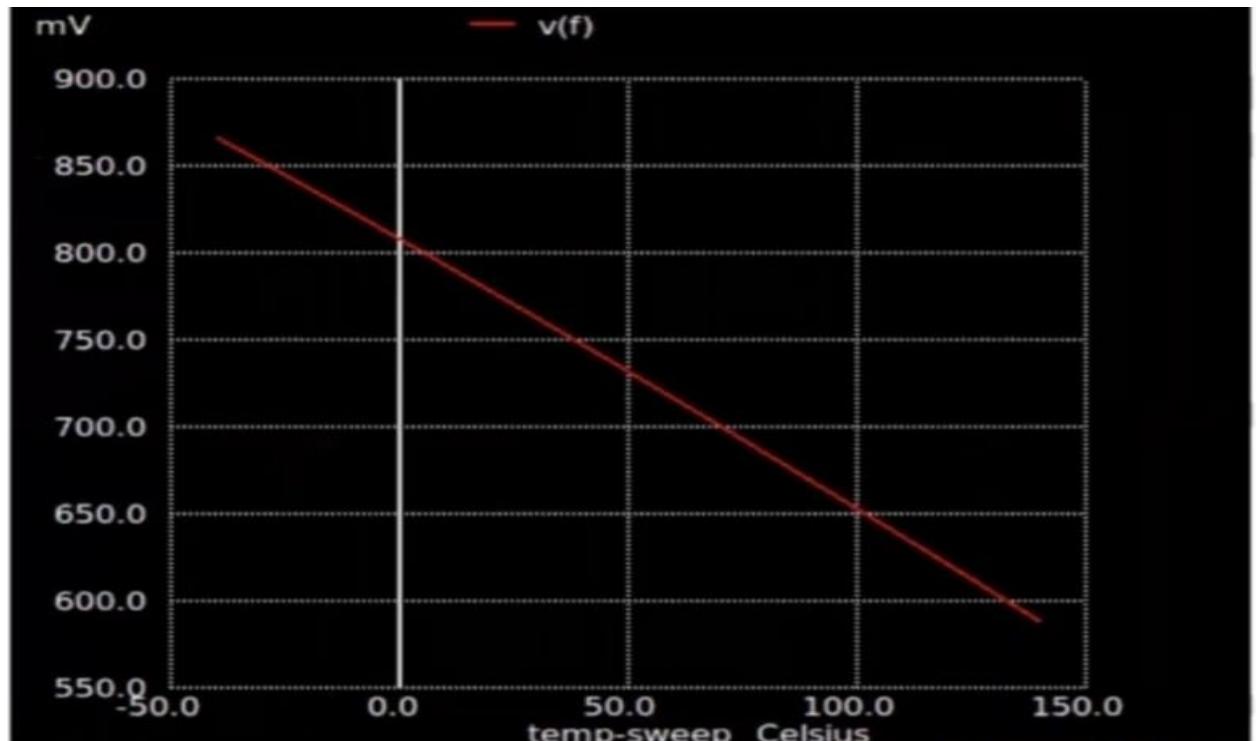

Fig.5.1.CTAT Slope
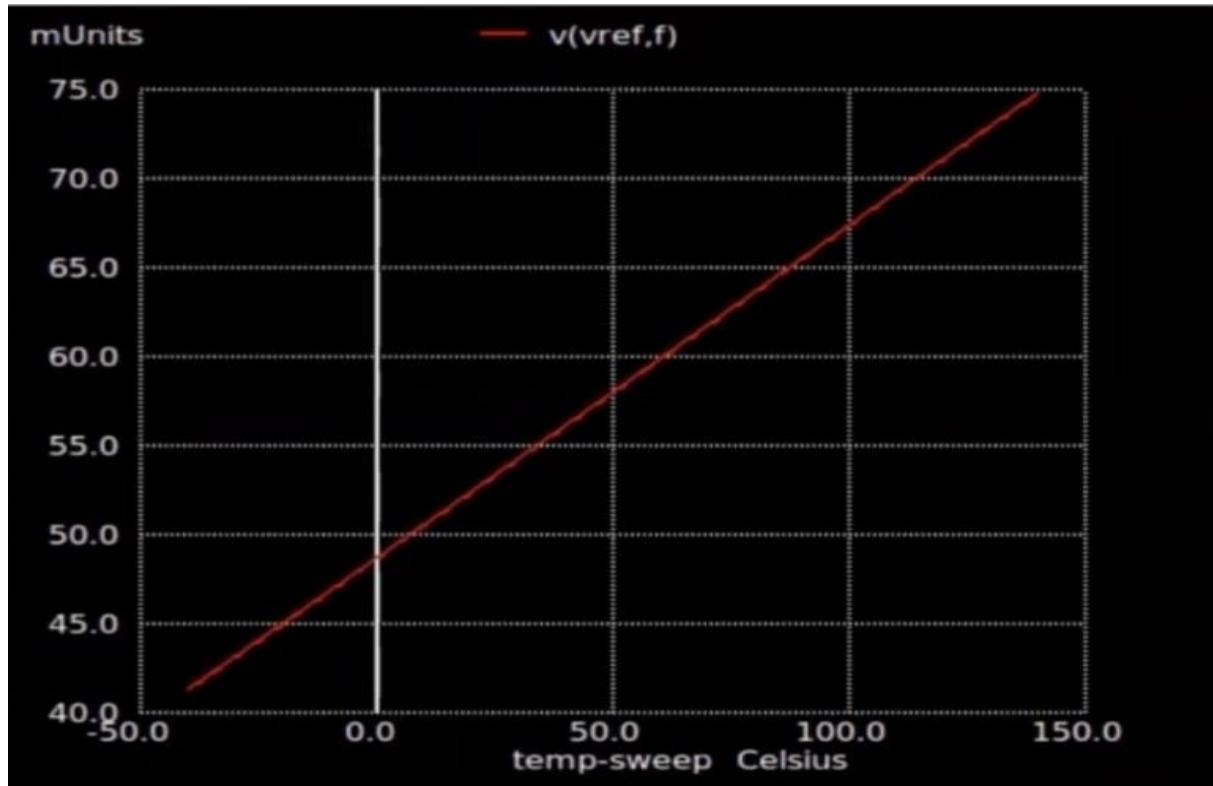
Fig.5.2. PTAT Slope

In formula value is =1 partial(PTAT) /partial T +partial (CTAT)- partial(T).For PTAT we have made R2 = R1 so it 1,but the slope of PTAT which we have found here has the value of In (n) x RF, multiplied to slope of PTAT.Now for the equation to become Zero.

Now if we try to calculate it by putting the Value of a, in this place we can find out the value of the ratio R2 / R1 which is needed for the equation to become Zero.

Now we will find out using calculator After calculating we are getting R2 / R1 as 8. something. Now we will multiply R2/R1 = 8.058

So Now to find the value of R_{2} we will multiply 8.058 with 2, we get around '16 K'.

Now we will put 16K in our netlist as the value of R2 and R3 can be similar to R2 or some what less than that So R3 = 10K.It wont affect our circuit as it is a part of startup circuit

>> Now Save the above file

In Terminal Window

Type >> clear ngspice Temp.cir

Again We have recieved 3 graphs Vref, CTAT and PTAT, but the Vref has the characteristic more like the CTAT. Fig 4.3 , 4.4 , 4.5 are those graphs.
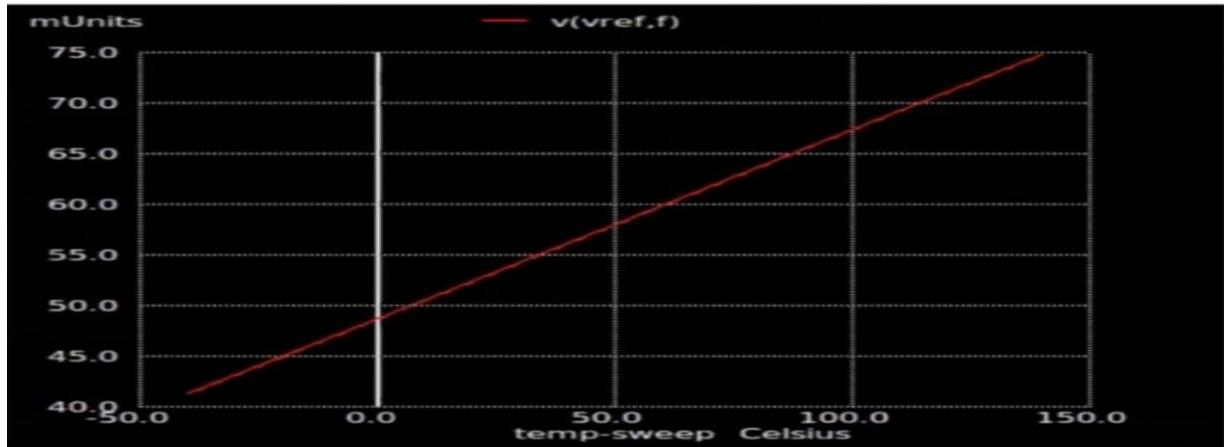
Fig.5.3.
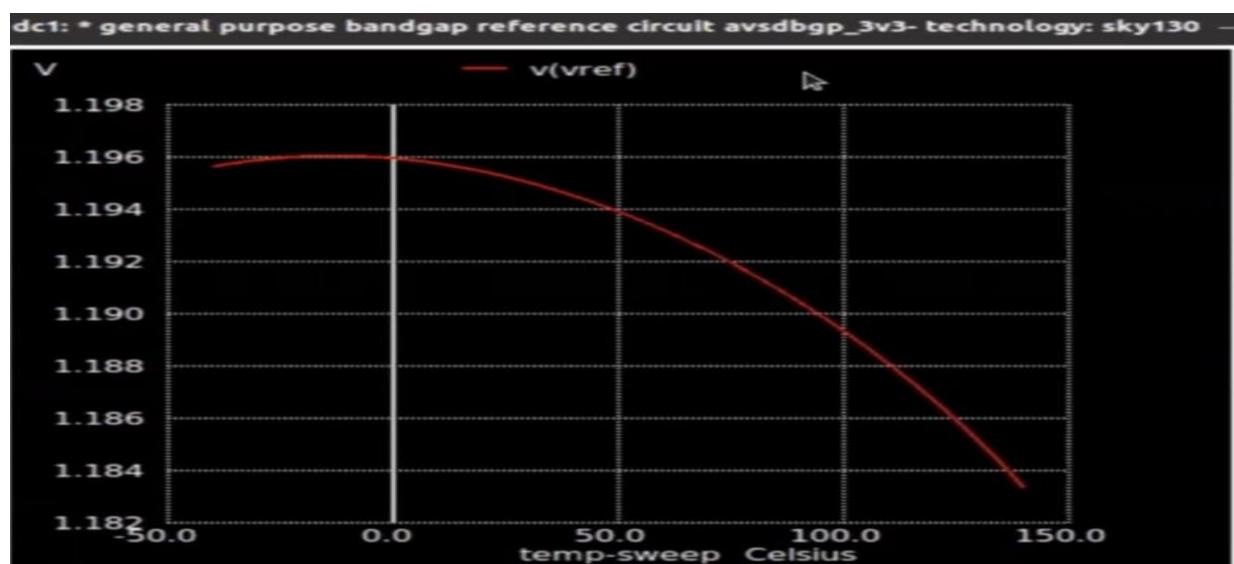
Fig.5.4.
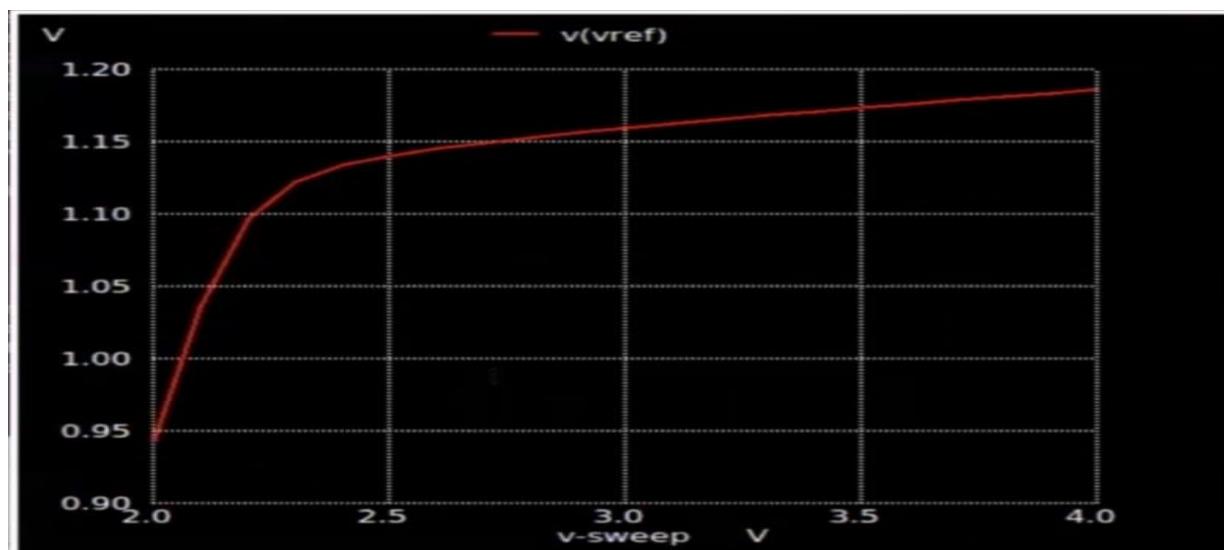
Fig.5.5.

Actually the graph should be looking as a bell curve here

Now to make it more perfect we have to increase the PTAT element.

To increase that we have to increase the value of R2.

Now give R_2=17k in Netlist.

>> Now Save the above file

In terminal Window

type>> clear >> ngspice Temp.cir

 Now we can see the graph of Vref having characteristics more like the PTAT but to get bell curve (perfect) lets try to make it more perfect by decrease R2.

When R2 is decreased, it will have more CTAT Characteristics

Now in our netlist lets give R_1=2k (as it is)

R_2 =16.5 K

>> Now again Save & Run the file.

Now we can see the v(vref) graph has shifted more towards the CTAT characteristics more.

now we will change the the values a little bit so we can get desired result

Now we will increase the value of R2,

let R_2 =16.7 k.

>> Save & Run the file.

So now we have got the bell curve in Vivref), this is what we required for comparison we can plot all the graphs together.

→ In line 51 of Spice netlist add

>>plot v (Vref), v (vret,t), v(t)

>>> Now Save and run the file

> Now we can see that in the graph the CTAT and PTAT Cancel out each other.

> and we are getting a constant voltage at output

> The bell curve is the v(vref) curve

we are getting fluctuations from 1.2095 to 12100

Now there is a next thing that we have to do…

Copy the whole Temp.cir file and paste it in the another file name it supply.cir

Now in Supply.cir file we are going to make Some changes

Now in Supply.cir file we will Change as

In 44th line write

>>.dc VDDA 2 4 0.1

Now open the terminal run

>>ngspice supply.cir

Here in the graph we are getting a very huge variation with the increase in voltage

So lets check the current through all branches in the circuit .

for that in line 50 type :

>> plot i(v2) i(v3) i(v)

>>Now save and run the file

Here we are getting the variation of around 0.10... this is some what acceptable.We have to keep in mind the temperature. variation curve that we have done before.It is very much dependent on the R1 and R2 ratio as we have seen that for the Variation from the 16k to 17k, it is fluctuating very much.Before we go any further in this supply We revisit the temperature plot again have to revisit the temperature plot again.

In Supply.cir we have changed the values of R1, R2,R3 and now we will do the same thing in Temp.cir.

In Temp.cir we will give the values

> R1 = 30K.

>R2 = 240K.

> R3 = 200K.

Now Save the above file and run

Now our bell curve has been disturbed and we are getting the Vref like this So we need to fix this.

Now clear the Window by typing clear in terminal.

Now in Temp.cir file we will put the R1 and R2 values same R1 = 30K , R2 = 30K.

>> Save the file and Run it.

The graphs which we have recieved now we will recieve the CTAT and PTAT for it

The slope of CTAT is found using , I mean by placing/clicking left button 40, by holding bring it to 60 and leave

For PTAT we use the same above procedure.

In terminal we have recieved the values as :

For CTAT

dy/dx = -0.00180873

dx/dy = -552.874

For PTAT

dy/dx = 0.000206081

dx/dy = -4852.46

In Calci actually Iam getting is 2863.3K,, this should be the value of R_2.

In Temp.cir file give the R_2 value as 263 K

>> Save and run the file
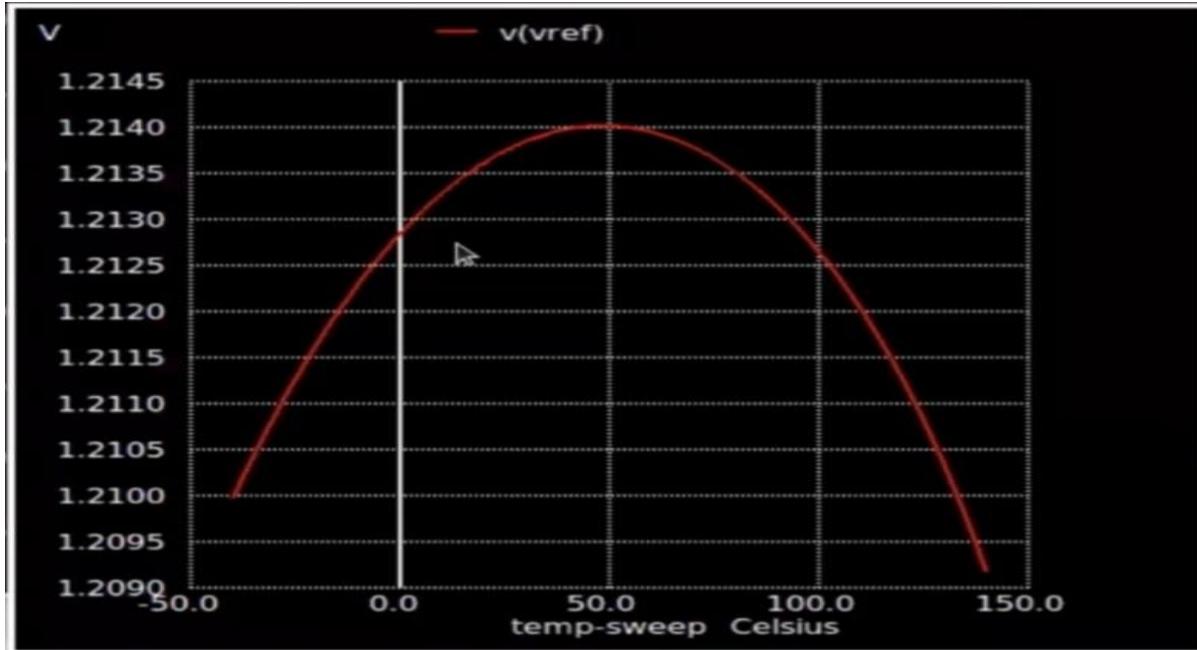
Fig.5.6

So finally now we are getting the bell curve

So now lets exit from Temp.cir and put the Same value in Supply.cir, so we graph by changing value of R2 get the correct

Open supply.cir file

give R2=273K

Save and run the file 000.0
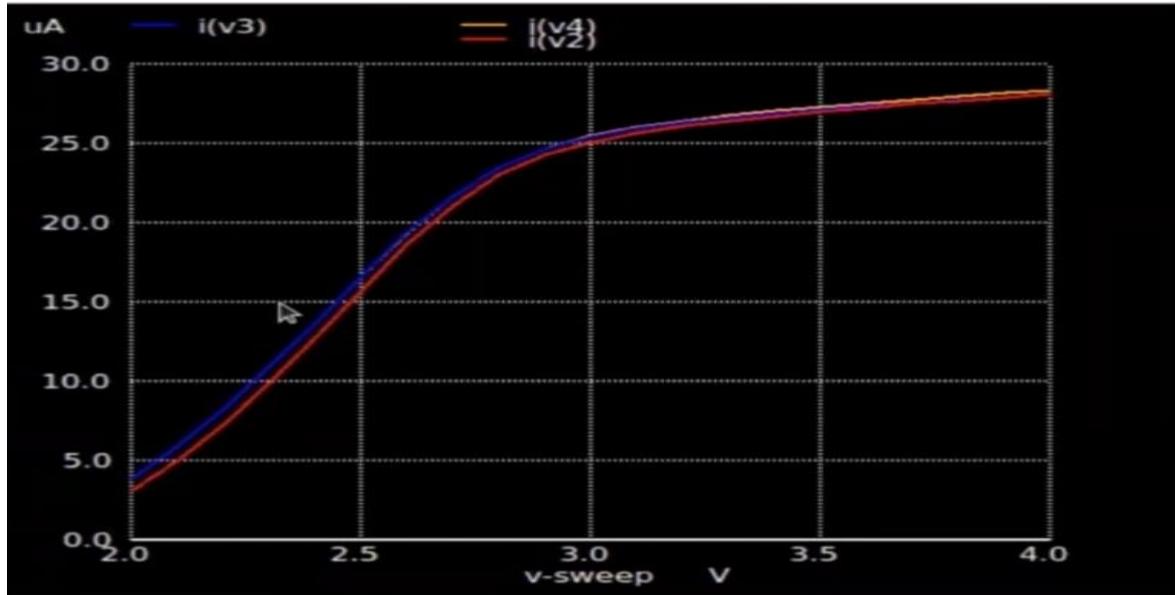
Fig.5.7

Now we are getting variation from 1.1 to 1.23 So around 0.11 variation This is acceptable

SO WE HAVE COMPLETED THE DESIGN AND PRE LAYOUT SIMULATION OF BGR
AND WE ARE GETTING ALMOST SATISFACTORY RESULTS

5.2. Layout Analysis

First we make a wire

First select the metal 1 than metal 2 than we well Put "'" metal 2 contact, than Connect the
wire..

we can make another wire

metal 1, metal 2 than put into metal 2 contact

The terminal XM9, XM10 are connected to ground.

We have to make a terminal for transistor. We have to follow the same procedure again then,we
will place contact, then connect it to the ground,then we have to connect XM9 to the XM14 using
metal 1.Now we have completed with the mosfet connections.Now we will do the, BJT XIN BIT
we can see that emitter Base, collector so we need to connect emitter and all the rest just will be
connected to the ground.we will connect collector and bare by using locali layer. will do this for
all of them.we need to make wire than connected to the ground, and we need to connect resistor.
the resistor.

30k is connected to XM12.

Now we need to make wine than conned using metal 1 and metal 2.

metal 1 wires cannot overlap each other. wherever overlapping we have to use the metal a wire.

Now we will connect the resistor and make the **contact for resistor.**

For making connection to the BJT we will use metal 1. then directly Connect it to the emitter.

R is connected to gate.

We have to connect XMl to the BJT.

We will use metal 1 for the connection...k

We also connect the XM13 to the Resistance again we will make wire.

We have to make the contact from Resistor to metals, local:

Now we will connect to the terminal.

Using metal 1 connected to the wire and connect the other terminal of the BJT.

We have completed the connection of BAR layout

After that we will do post layout simulation of the BGR circuit.After completing the post layout Simulation of the BGR circuit we will the get the graph,the values that we are getting for the Pre-layout are the same that we are getting in post layout of supply variation and temperature is slightly decreased.

After completing the post layout Simulation of the BGR circuit we will the get the graph.

Lastly these are the graphs which we have obtained throughout the Layout.
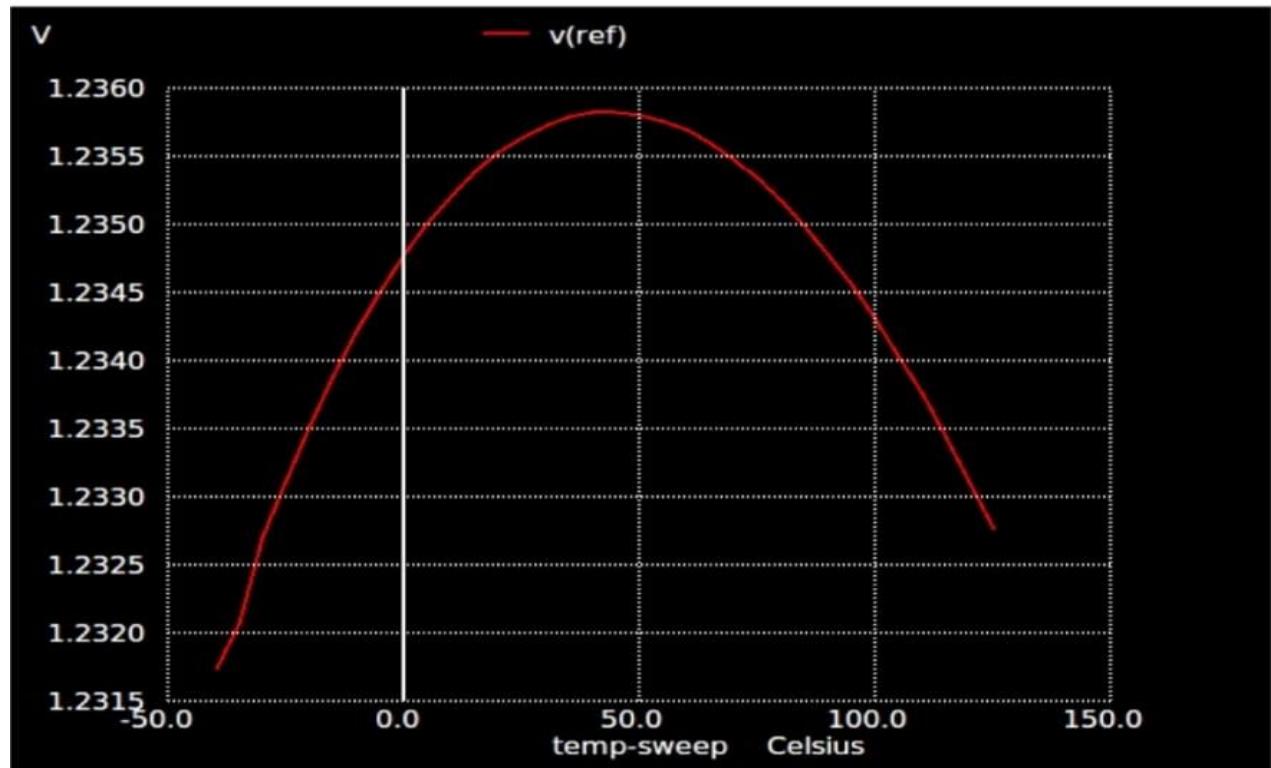
Fig. 5.8
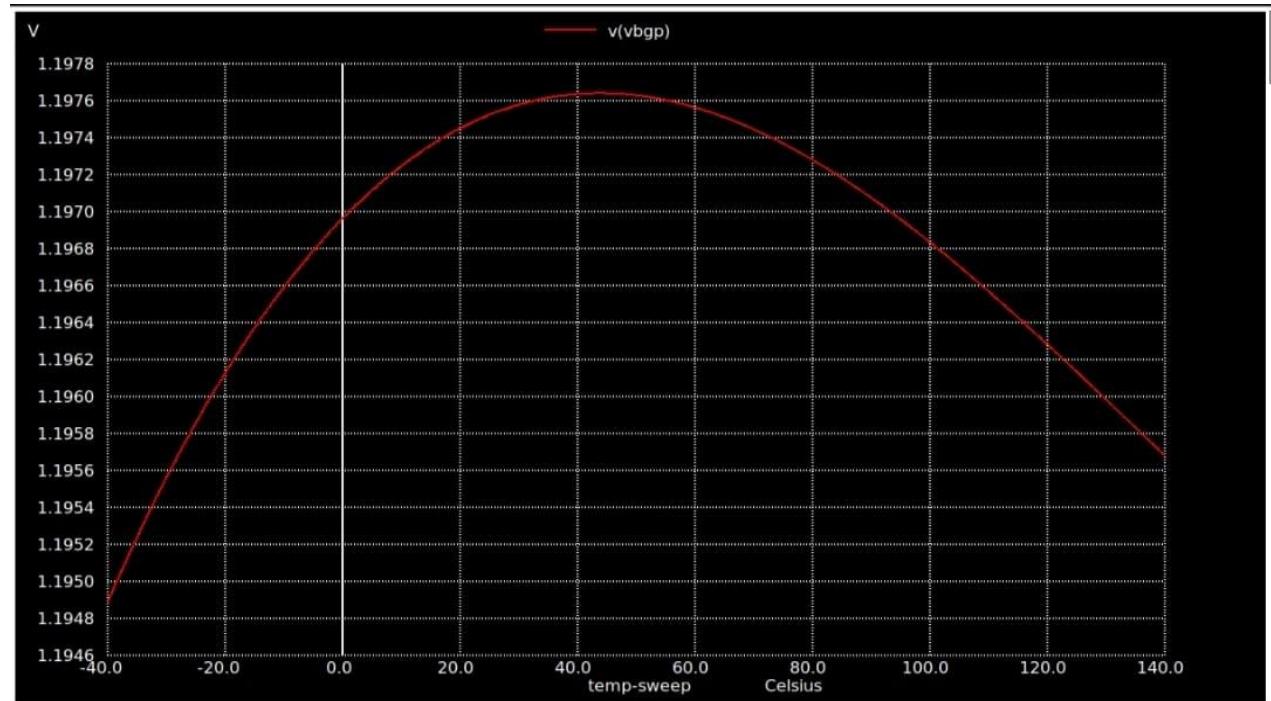
Fig. 5.9.
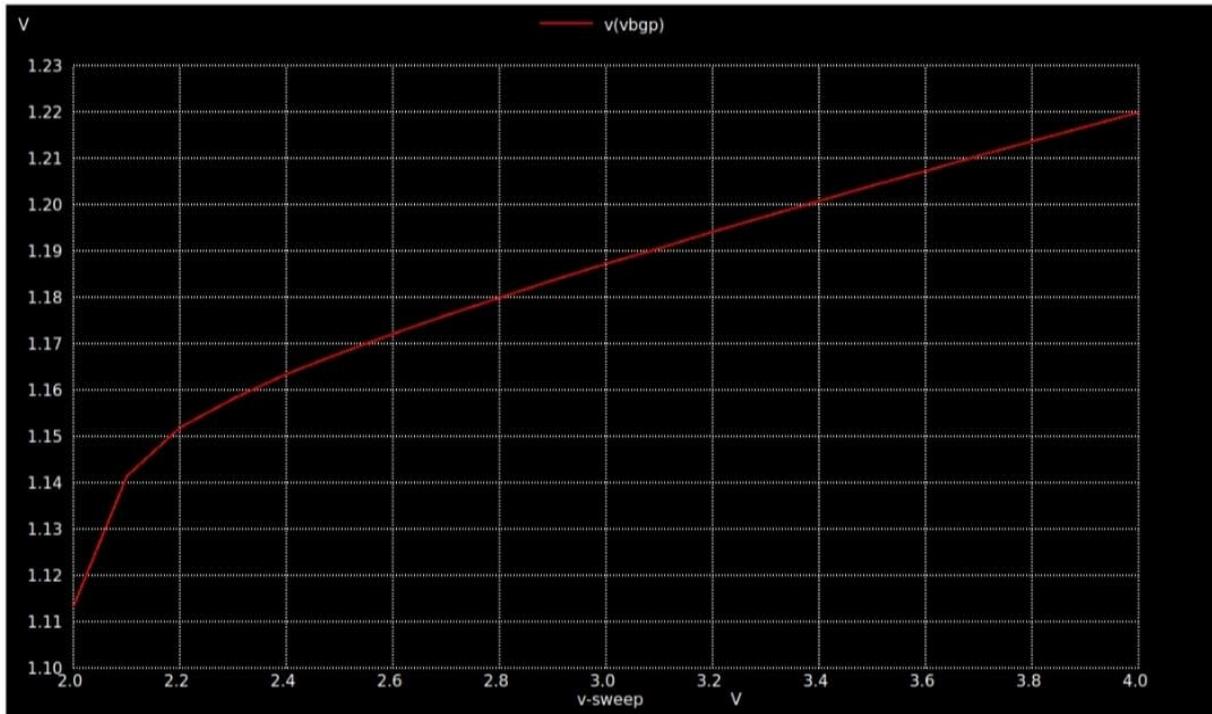
Fig.5.10
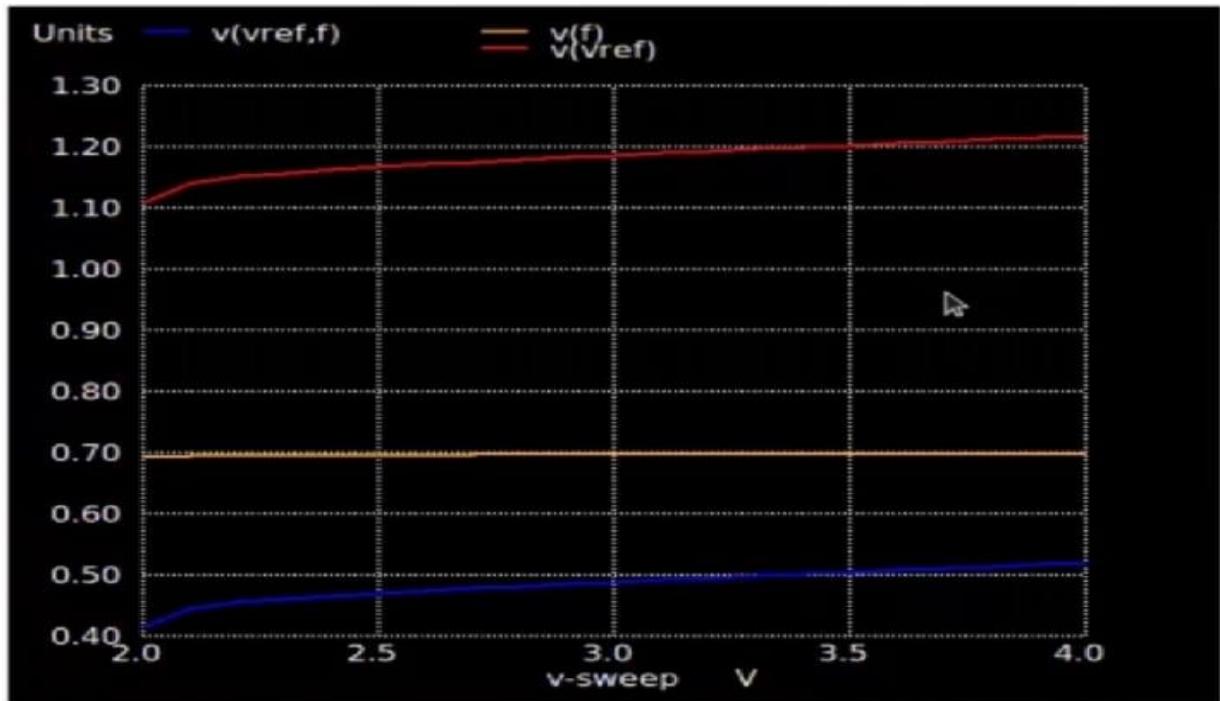
Fig.5.11

CHAPTER 6 :

CONCLUSION

The design of a bandgap reference circuit using the SKY130 PDK (Process Design Kit) successfully demonstrates the ability to generate a stable and process-independent reference voltage, typically around 1.2 V, which is crucial for analog and mixed-signal systems. By leveraging the BJT models available in the SKY130 platform and careful biasing techniques, the circuit achieves temperature compensation and maintains performance across voltage and process variations.

The design and implementation of the Analog Bandgap Reference (BGR) circuit using the SKY130 technology has been a valuable learning experience that deepened my understanding of analog integrated circuit design and CMOS process behavior. Through this project, I explored how temperature-independent reference voltages are generated by combining the characteristics of PTAT (Proportional To Absolute Temperature) and CTAT (Complementary To Absolute Temperature) voltages. By properly balancing these two temperature-dependent parameters, I was able to achieve a stable and predictable output voltage that remains nearly constant across variations in temperature and supply voltage.

Working with the SKY130 PDK helped me understand the practical aspects of using open-source tools and real CMOS process parameters. It gave me hands-on experience in schematic design, simulation, and analysis using tools like Ngspice. Observing how transistor-level behavior affects the final reference voltage made me realize the importance of layout symmetry, matching, and biasing conditions in analog circuits. Moreover, simulating the BGR over different temperature ranges showed me how crucial design optimization is for minimizing temperature drift and ensuring long-term stability.

Overall, this project helped me build a solid foundation in analog circuit design principles, particularly in precision reference generation. It also enhanced my ability to interpret simulation results and link them with theoretical expectations.

CHAPTER 7 :

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