

Lecture-9 (Memory Systems)

→ Memory is used to store instructions and data.

(0's and 1's)

→ Byte addressable :-

A memory is said to be byte addressable if every byte of data has a unique address.

1 byte = 8 bits has a unique address

→ Word addressable :-

Let 1 word = 4 bytes
= 32 bits

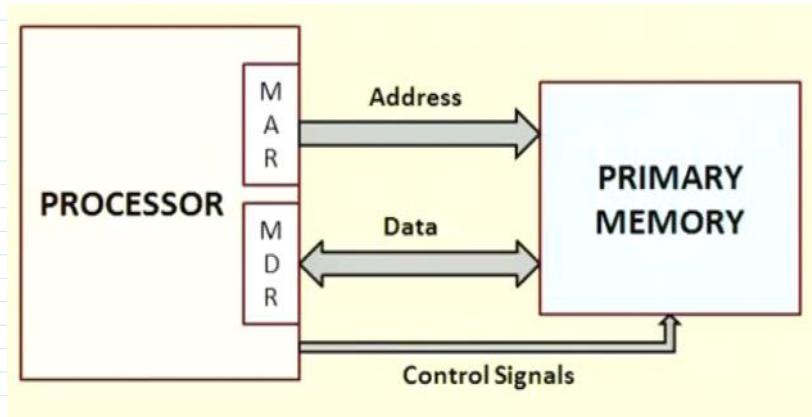
Then memory address will be incremented by 4.

0, 4, 8, and so on.

Let 1 word = 8 bytes
= 64 bits

0, 8, 16, and so on.

Processor and Memory :-



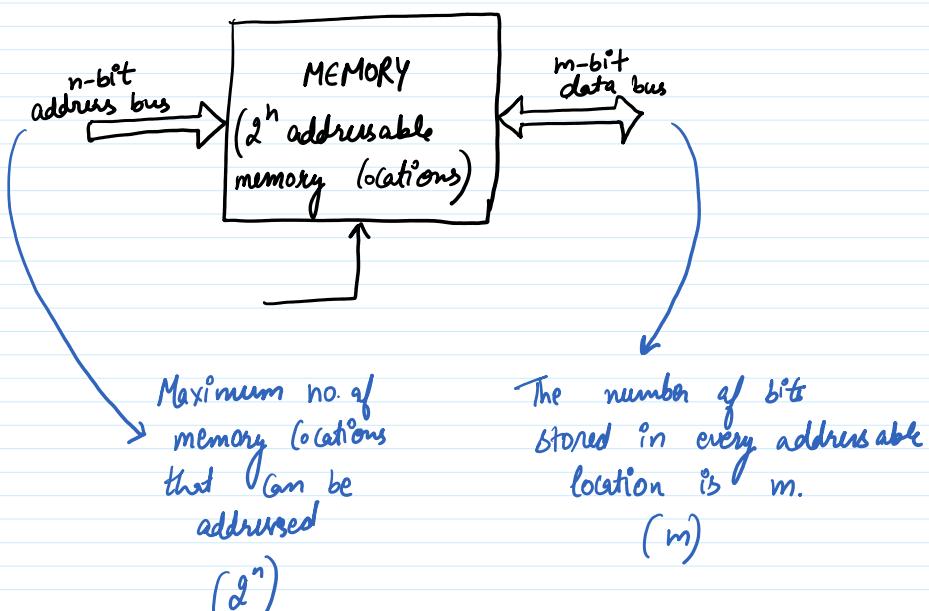
① Memory Address Register (MAR)

Address of data/instruction to be read or written.

② Memory Data Register (MDR)

Data to be read/written.
Bidirectional.

③ Control Signals , READ, WRITE etc.



$$\text{Total memory size} = 2^n \times m$$

② Volatile v/s Non-volatile

Volatile :- The stored data is lost when power is switched off.
CMOS Static & dynamic Memories.

Non-volatile :- Data is retained when power is switched off.

Read Only Memories :-
CD ROM, DVD, etc...

③ Random / Sequential / Direct Access Memory :-

Random Access :-

when read/write time is independent of memory location being accessed.
→ RAM and ROM

Sequential Access :-

when stored data can only be accessed in a particular order.
→ Magnetic tape

Direct Access :-

(Semi-random access)

when part of the access is random and part is sequential.
→ Magnetic Disk

④ Read-only v/s Random-access :-

Read-only Memory (ROM)

- data programmed during manufacturing or in the laboratory.
(permanent / semi-permanent)
- ROM, PROM, EEPROM, etc.

Random-access Memory (RAM)

- used in main memory and cache memory.
- Static RAM & Dynamic RAM

Terminologies :-

Memory Access Time :-

Time between initiation of a operation and completion of that operation.

Latency :-

Initial delay from the initiation of an operation to the time the first data available.

Bandwidth :-

Maximum speed of data transfer in bytes per second.

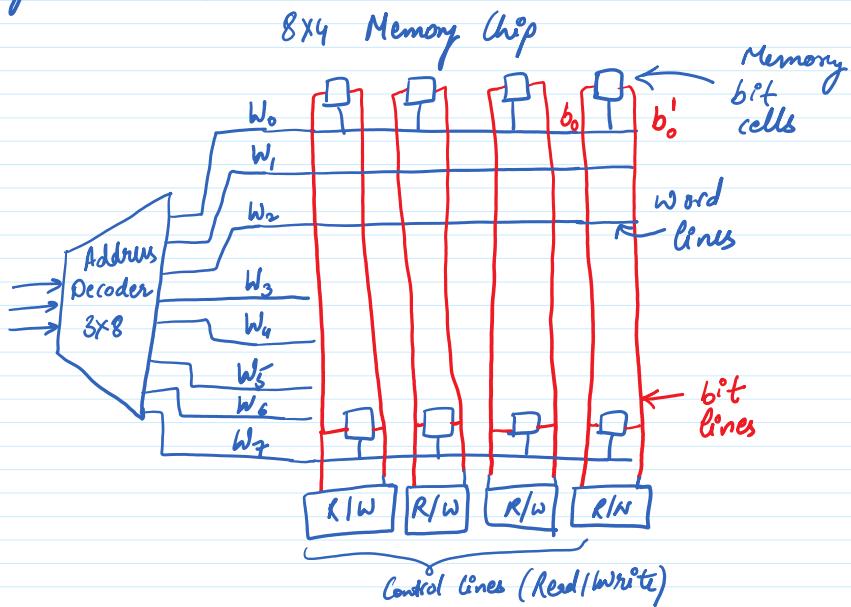
Memory Goals :-

- ① Make memory system work faster.
- ② Increase the data transfer rate between CPU and memory.
- ③ Increase the storage need.

Solutions :-

- ① Cache Memory :- ↑ effective speed.
- ② Virtual Memory :- ↑ effective size.

Memory Chip Organization :-

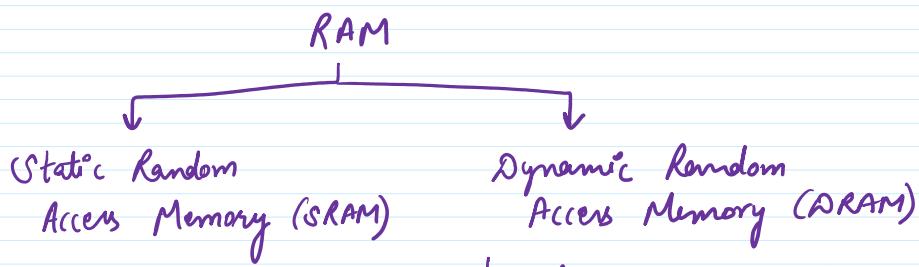


→ 32-bit Memory

→ 3x8 decoder is required to access any word out of 8 words.
(8 rows)

→ Two bit lines
Bit b and its complement b' for reading and writing

RAM Organization



- Asynchronous DRAM
- Synchronous DRAM

* Present day main memory systems are built using

Difference in terms of :-

Speed → how fast

Density → how many bits can be packed.

Volatility → if power supply is off.

Static RAM :-

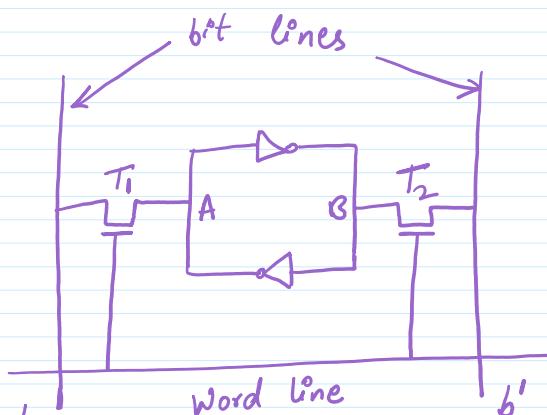
- Semiconductor memory uses flip-flops to store each bit.
- Can be arranged in rows and columns of memory cells.

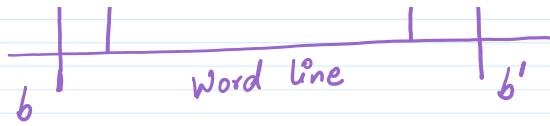
Word line and bit line

- These days -
6-transistors CMOS

- Widely used in small-scale systems like microcontrollers
- Cache Memories

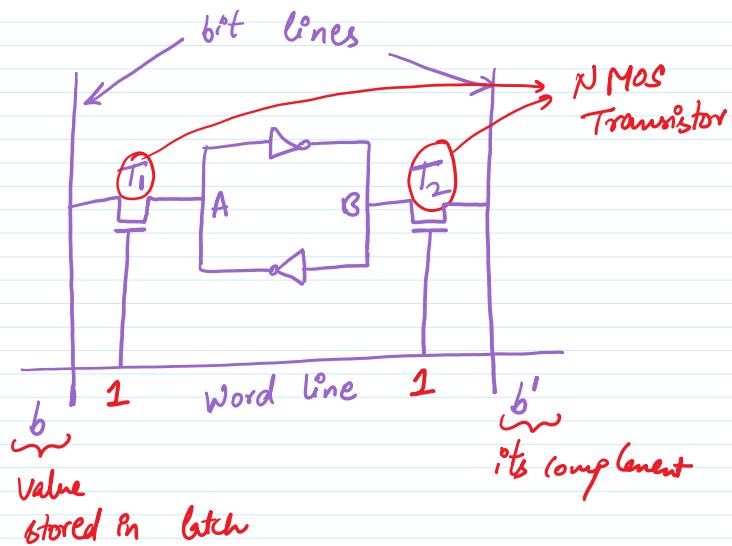
1-bit SRAM Cell





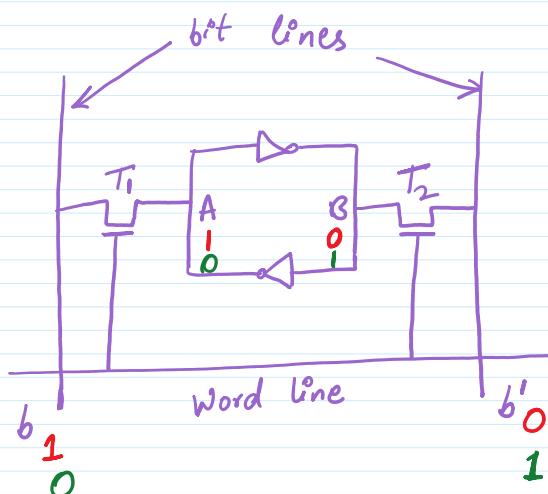
- Two inverters are cross connected to form a latch
- Connected to two bit lines with T_1 and T_2
- Transistors behave like switches that can be (OFF) and (ON) under the control of word line.

Read Operation :-



Write operation :-

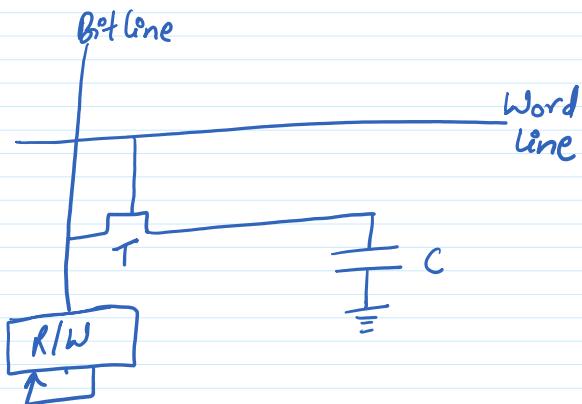
Write 1
Write 0



Dynamic RAM :-

- Do not retain its state even if power supply is ON.
- Data stored in the form of charge stored on a capacitor.

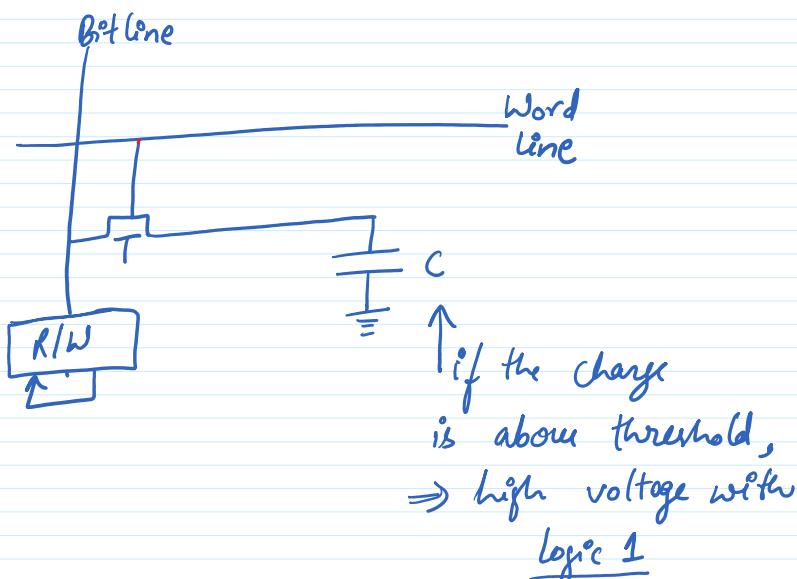
1-transistor DRAM Cell



→ Requires periodic refresh
(due to leakage in charge)

→ Less expensive.

READ Operation in DRAM

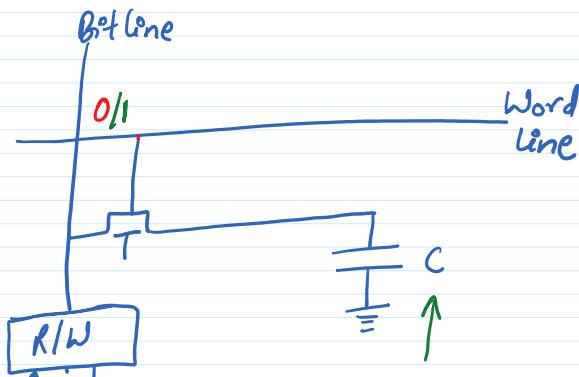


if below threshold, grounded
logic 0.

⇒ WRITE Operation in DRAM

To be written:-

0, 1



The capacitor gets charged to the required voltage state.

⇒ Refreshing of capacitor requires
READ-WRITE cycles.

Types of DRAM

ADRAM
(Asynchronous)

→ Timing of memory is handled asynchronously.

A special memory controller.

SDRAM
(synchronous)

→ Memory operations are synchronized by a clock.

Quiz :-

Register Indirect v/s Indirect Addressing.

(RI)

(IA)

RI : Less Address Space
More Memory Access

(a)

IA : Large Address Space
Less Memory Access

(b)

RI : More Address Space
Less Memory Access

IA : Large Address Space
More Memory Access

RI : Large Address Space
Less Memory Access

(c)

IA : Less Address Space
More Memory Access

(d)

RI : Large Address Space
Less Memory Access

IA : Less Address Space
Less Memory Access

OTP :- 6224-R-C