Malaviya National Institute of Technology Jaipur
Department of Computer Science Engineering
Computer Organization and Architecture
Assignment-1, Date: Feb 19, 2024

Deadline: Feb 23, 2024 (5:00 pm) Spring 2024, VI Semester Max marks: 30

All questions are compulsory.

1. The cache size is 256kB and a 4-way set associative mapping. The block size is 32B with a Physical Address of 32 bits. Each cache tag directory contains in addition to TAG address, 2 valid bits, 1 modified bit, and 1 replacement bit. Answer the following questions with explanations.
   (a) What is the total number of bits in the TAG field of an address? **(5)**
   (b) What is the size of the cache TAG directory? **(5)**

2. (a) A memory system is employed with 3 levels. The access time of L_1, L_2 & L_3 memories is 100ns/word, 150ns/word & 500ns/word. The L_2 & L_3 memories are divided into blocks of 5 words. When a page fault occurs in $L_1 or L_2$, the processor must read from L_3 memory only. The H_1 & H_2 are 80% & 90%. What is T_{avg}, explain in detail. **(5)**

3. For each of the following cases, state whether SRAMs or DRAMs would be appropriate building blocks for the memory system, and explain why. Assume that there is only one level in the memory hierarchy.
   (a) A memory system where performance was the most important goal. **(1.5)**
   (b) A memory system where cost was the most important goal. **(1.5)**
   (c) A design where data need to be stored for long periods without any action on the processor's part. **(2)**

4. (a) A processor accesses a 64-bit long word from memory with word assignment in a little-endian system, How will the long word be aligned? Explain in detail with the help of a figure. **(5)**
   (b) A processor can access a memory location having 20 bits address at an instance. How many are the total memory locations? What is the total memory size if all memory locations are available to the processor? **(5)**

*****Best wishes*****