Lecture - 5 (Addressing Modes)

Instruction Formats:-

O 1 address

LOAD X

opeode memory address

2 - address

ADD X,Y

optode memory memory address

3 Legister - memory

ADD RIX

opcode xegister memory address

6 Register - register

ADD RI, RZ, R3

oprode register register register

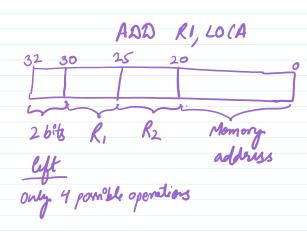
Example:
Instruction Set Architecture of a

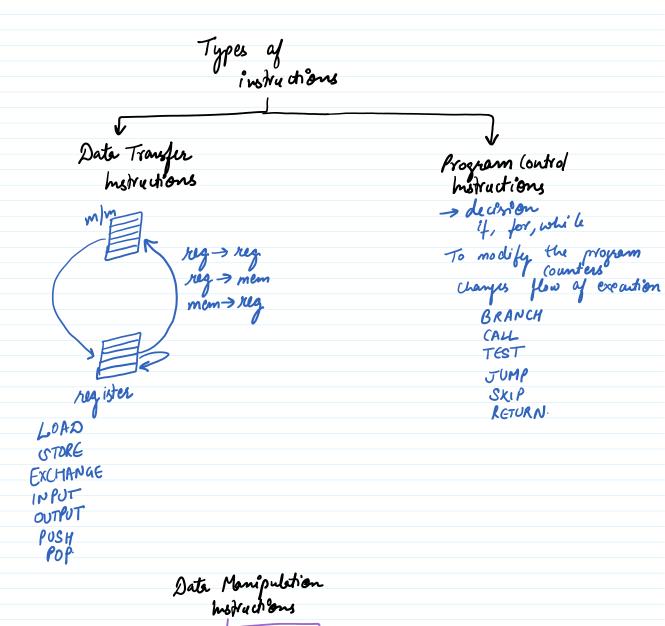
32-bit instruction

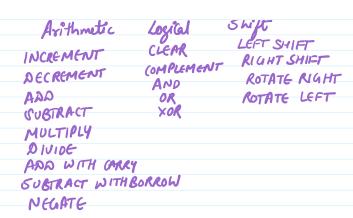
(Just an example not real)

Let us armine,

-> It is a fixed rize instruction -> 5 bits for 1 register. (32 registers)







## ADDRESSING MODES:

To specify the mechanism by which boation of OPERAND is specified in an instruction.

## Various Addressing Modes:-

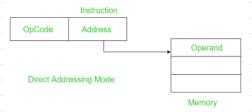


ADD #25

@ Direct Addressing

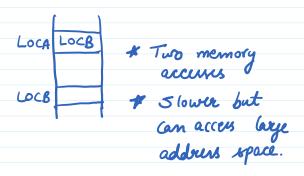


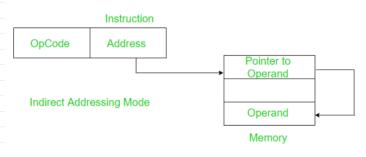
ADD RI, 20A6H



"Limited Address Space"

3 maired Addrewing ADD RI, LOCA





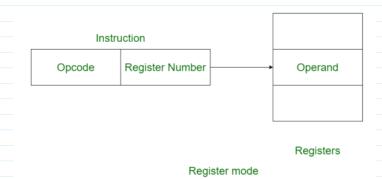
66 Large address space

9 Register Addrewing

ADD RI, R2, R3

\* Operands are stored in register bank.

No memory access, fast execution.

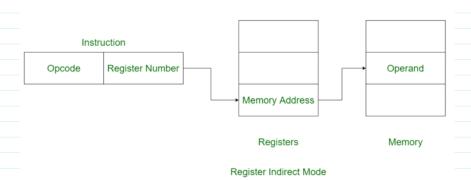


(Register hodirect Addrewing

ADD RI, Mem(RS)

From access (argue address space.

## to indirect addressing.



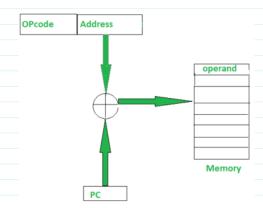
6 Relative Addrewing

(Program Counter Relative)

The instruction specifies an affect of displacement, which is added to the program counter to get the effective address of the operand.

opcode offsets

What is the range of relative addressing?

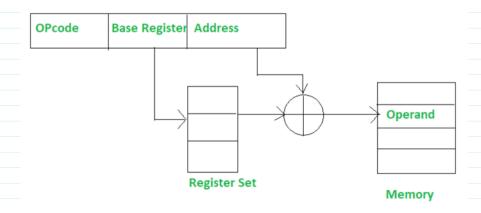


(7) Indexed Addrewing

\* Register is used as index.

LOAD RI, 1050(R3), Mem [1050+R3]

access the elements of an array.



1 Stack Addrewing

# Operand is on the top of the stack.

ADD PUSH X

10 Autoincrement and Auto decrement

The register holding the operand address is automatically incremented or decremented

a++