Input/Output
Interfacing :—

Interfacing I/O devices is more complex as compared to interfacing memory systems.

① Interfacing Memory Systems }
    Cache → Static RAM
    Main Memory → Dynamic RAM
          only these types

② Interfacing I/o devices }
    → Wide variety of peripherals
    → Widely varying speeds
    → Data Transfer rate can be irregular
    → Slower than processor and memory
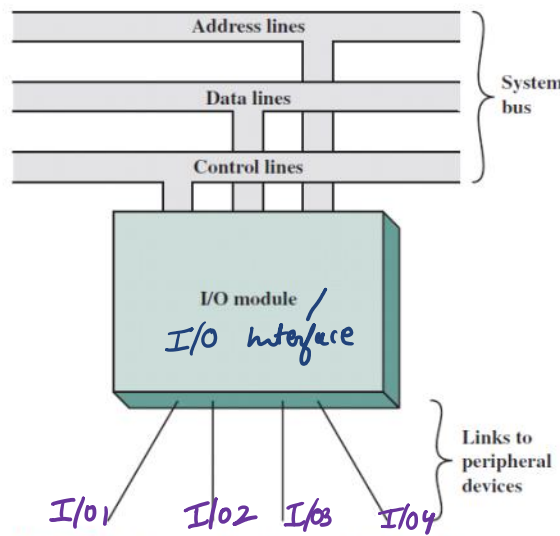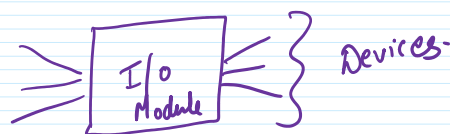
Input / Output Interface :—

Figure 7.1   Generic Model of an I/O Module

→ A programmable I/o interface is needed to handle widely different types of I/o devices.

Devices-

Peripheral / External Devices :—
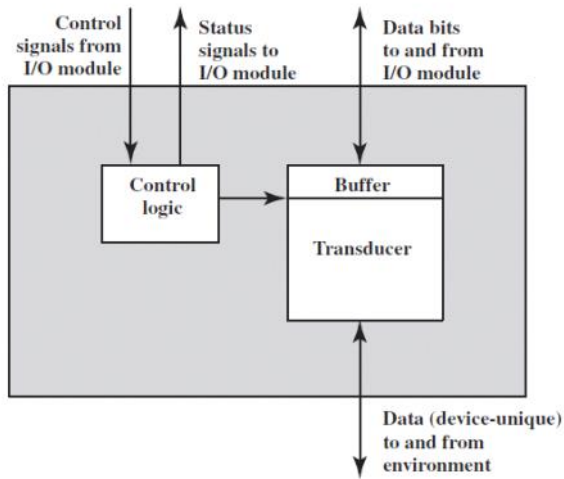
Peripheral / External Devices :—

Figure 7.2 Block Diagram of an External Device

Buffer :— Temporarily stores the data that is being transferred between I/O module and external environment.

Transducer :— Converts data from electrical to other forms during output and from other forms to electrical during input.

Typical I/O Module :—
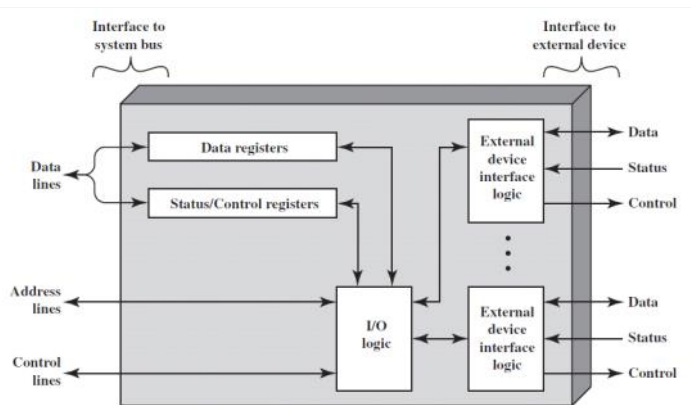

Figure 7.3 Block Diagram of an I/O Module

Steps :—

1. Processor requests the I/O Module for device status.

Interface to system bus   Interface to external device

Steps :—

1. Processor requests the I/O Module for device status.
2. I/O Module returns the status to the processor.
3. If device is ready, processor requests data transfer.
4. I/O module gets data from device.
5. I/O module transfers data to the processor.
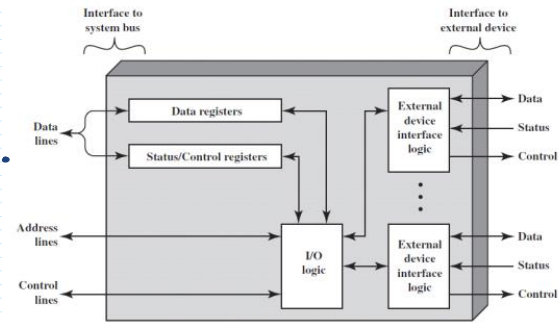6. Processor stores the data in memory.


Figure 7.3 Block Diagram of an I/O Module

Input/Output Ports :—

Output Port :—

① A PIPO register that is enabled when a particular output device address is given.

② Register inputs are connected to the data bus, and the register outputs are connected to the output device.

Input Port :—

① A parallel tristate bus driver that is enabled when a particular input device address is given.

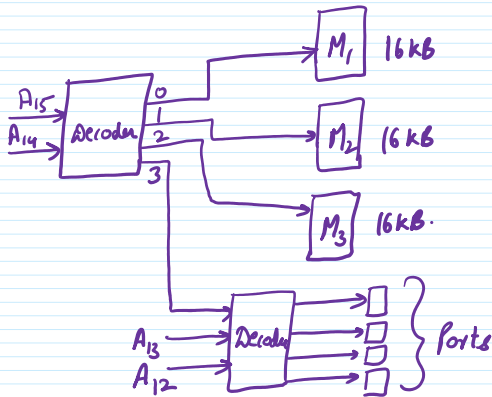② The driver outputs are connected to the data bus, while the inputs are connected to the input device.
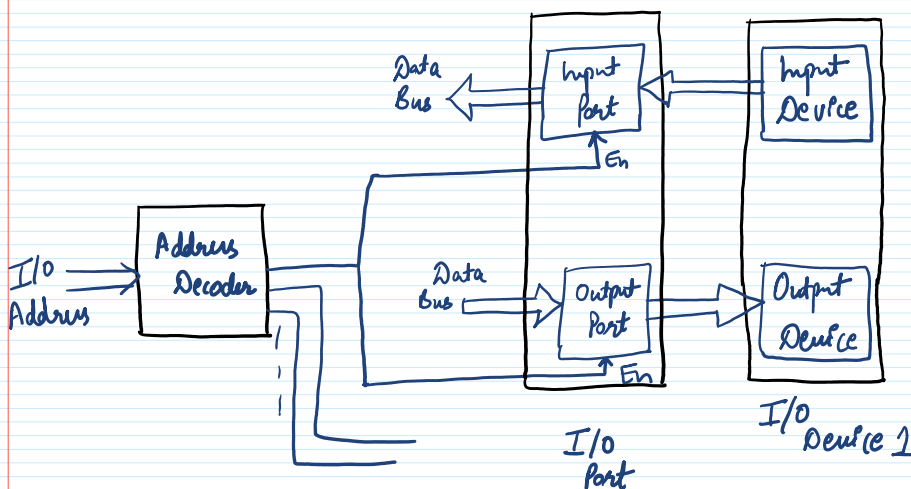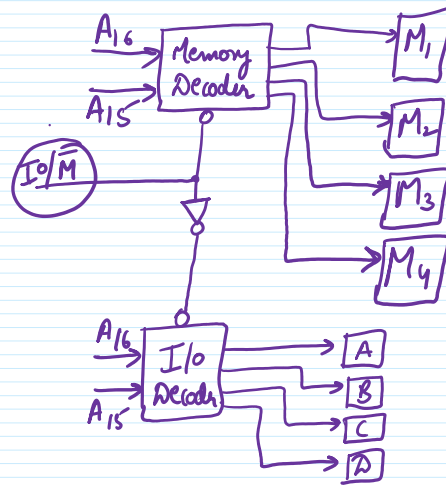

Types of Device Interfaces :—

Ways of connecting the I/O devices to the

address and data buses.

Memory – Mapped Device Interface

I/O Mapped Device Interface.

Memory – Mapped Device Interface	I/O Mapped Device Interface.
① Same address decoder selects memory and I/o ports.	① Separate instructions for I/o data transfer (IN/OUT).
② Some of the memory address space is occupied by I/o devices.	② A processor signal identifies whether a generated address refers to a memory location or an I/o device.
③ All data transfer instructions to/from memory can be used to transfer data to/from I/o devices.	③ Separate address decoders for selecting memory and I/O ports.
④ The processor need not have separate instructions for I/o, no <u>IO/M̄ address</u> signal.	④ The complete address space can be utilized.