### Lecture - 4 (Classification of Computer Architecture)

nstruction

Operand

To execute a program, two basic operations are required:

- a) LOAD: LOAD RI, 2000
- b) STORE: STORE 2020, R3

Example instruction :-

$$S = (A+B) - (C-D)$$

LOAD R1, A

LOAD R2, B

ADD R3, R1, R2 //R3 = A+B

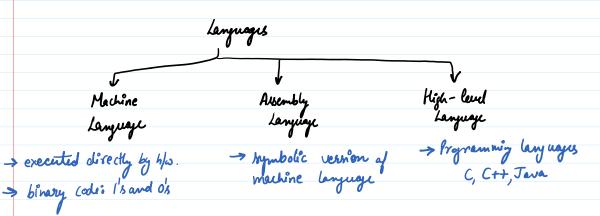
LOAD R1, C

LOAD R2,D

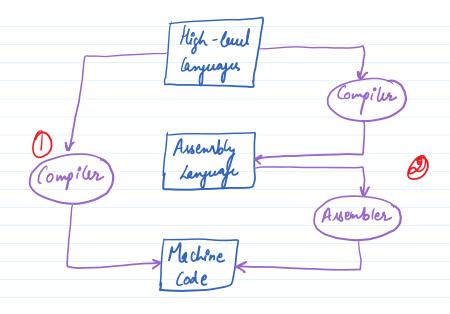
SUB R4, R1, R2 // R4 = C-D

SUB R3, R3, R4 // R3 = R3-R4

STORE S, R3



Compiler and Assembler



Program / Software: 
Set of instructions.

-> rimple programs

-> compiler

-> operating system

Application

System

Software

Ex:
To solve particular user-led

\*\* To solve particular user-led

\*\* Collection of programs, which helps users reen

other programs

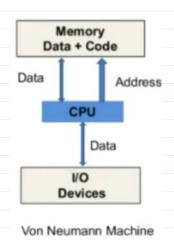
Types of programs

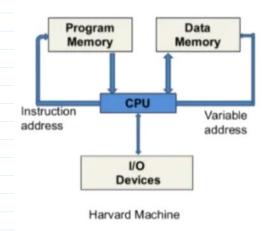
Committee v/k Calculator

## Computer v/s Calculator

# Clarification of Computer Architecture

Von-Neumann Architecture Horvard Architecture





#### Von-Neuman Architecture 3-

- O both instruction and date are stored in the same memory module.
- @ More flixible and carrier to implement.
- B Suitable for most of the general-purpose processors.

### Harvard Architecture :-

- 1) A saperate memory module for program and date.
- Date are stored in program memory.

B) Instruction and data access can be done in parallel.

Execution of instructions?

6 stayes of execution of instructions:

- 1 Instruction Fetch (IF)
- 10) histruction Derode (10)
- - 9 Memory Acces (MEM)
  - 3 Wrête back repult to register file (WB)

Baric 5-stage pipelining :-

Execution of their Sistructions in a pipeline.
(over apping)

Instr. No.	Pipeline Stage						
1	IF	D	EX	MEM	WB		
2		IF	D	EX	МЕМ	WB	
3			IF	ID	EX	МЕМ	WB
4				(F)	ID	EX	МЕМ
5					IF	ID	EX
	1	2	3	4	5	6	7

In clock cycle 4, instruction 4 is trying to fetch an instruction (IF), while instruction I is trying to access data (MEM)

/> Von-Neumann: - one of their two operations will have to wait - slow.

Architecture: the operations can go on without any speed penalty as the instruction and data memories are superate.