NOTE:

some of the instructions differ from some of the knowledge I find online, for example the sub instruction. SUB ra, rb, refers to rb = rb - ra, however the question says its rb = ra-rb. I have went with the assignment descriptions.

Question 2 - Instruction Set 2 – x295+

B. **Compiling and assembling a C program using our x295+ instruction set**

Table 1

C program (The C code below cannot be modified – it must stay as it is stated below)	x295+ assembly program	x295+ machine code program
z = (x + y) * (x - y);	LOAD Src1, r0	1010 000 XXX XXXXXX 0000 **<Src1 12 bits>**
	LOAD Src2, r1	1010 001 XXX XXXXXX 0000 **<Src2 12 bits>**
	ADD r0, r1, r2	
	SUB r0, r1, r3	0001 010 000 001 XXX
	MUL r2, r3, r4	0010 011 000 001 XXX
	STORE r4, Dest	0011 100 010 011 XXX
		1011 XXX 100 XXXXXX 0000 **<Dest 12 bits>**

C. Evaluating our x295+ instruction set using Memory Traffic criteria

Table 2

x295+ program (1 assembly instruction/ machine code instruction per row)	Fetch (number of memory accesses of word size) + Explain how you obtain your count	Decode/Execute (number of memory accesses of word size) + Explain how you obtain your count
Assembly instruction: LOAD Src1, r0 **Machine code instruction:** `1010 000 XXX XXXXXX 0000` **<Src1 12 bits>**	**Count: 2** **Explanation:** **The instruction 32 bit long, which is twice the size of the word.**	**Count: 1** **Explanation:** **Src1 is the only memory access**
Assembly instruction: LOAD Src2, r1 **Machine code instruction:** `1010 001 XXX XXXXXX 0000` **<Src2 12 bits>**	**Count: 2** **Explanation:** **The instruction 32 bit long, which is twice the size of the word.**	**Count: 1** **Explanation:** **Src2 is the only memory access**
Assembly instruction: ADD r0, r1, r2 **Machine code instruction:** `0001 010 000 001 XXX`	**Count: 1** **Explanation:** **The instruction is 16 bit long, which is 1 word size, thus only 1 memory access needed.**	**Count: 0** **Explanation:** **No memory access**

Assembly instruction:
 	
SUB r0, r1, r3
 	
Machine code instruction:
 	
`0010 011 000 001 XXX`
	Count: 1
	
	Explanation:
	
	The instruction is 16 bit long, which is 1 word size, thus only 1 memory access needed.
		Count: 0
		
		Explanation:
		
		No memory access

Assembly instruction:
 	
MUL r2, r3, r4
 	
Machine code instruction:
 	
`0011 100 010 011 XXX`
	Count: 1
	
	Explanation:
	
	The instruction is 16 bit long, which is 1 word size, thus only 1 memory access needed.
		Count: 0
		
		Explanation:
		
		No memory access

Assembly instruction: STORE r4, Dest **Machine code instruction:** `1011 XXX 100 XXXXXX` `0000 `**`<Dest 12 bits>`**	**Count: 2** **Explanation:** **The instruction is 16 bit long, which is 1 word size, thus only 1 memory access needed.**	**Count: 1** **Explanation:** **Dest is the only memory access**
Grand Total: 12	**Total: 9**	**Total: 3**

Once completed, submit it on Crowdmark as your answer to Question 2.