

CSE 3203 CT 4 Assignment
Roll No: 1803051

Assignment Problem:

Build CPU based on following requirements:

1. Word Size of CPU = 5
2. ALU Operations = ADD ,ROR,OR
3. Register Number = 3
4. Size of RAM = 10
5. Word size of ISA and RAM = 15
6. CPU Instructions = JMP,JNE

Solution:

Simulator Design:

1. ALU Circuit (Top to Bottom all circuits):

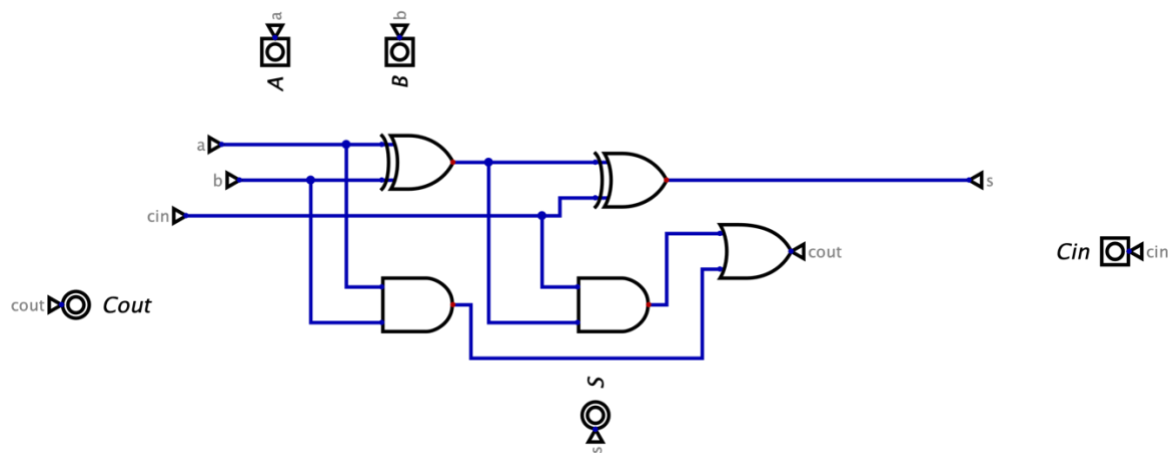


Fig: FA

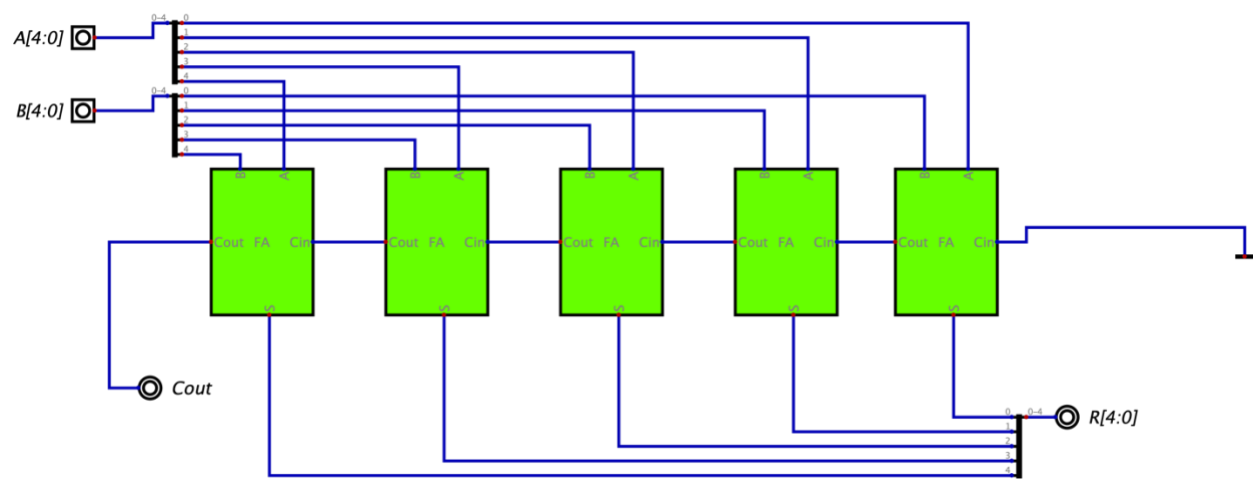
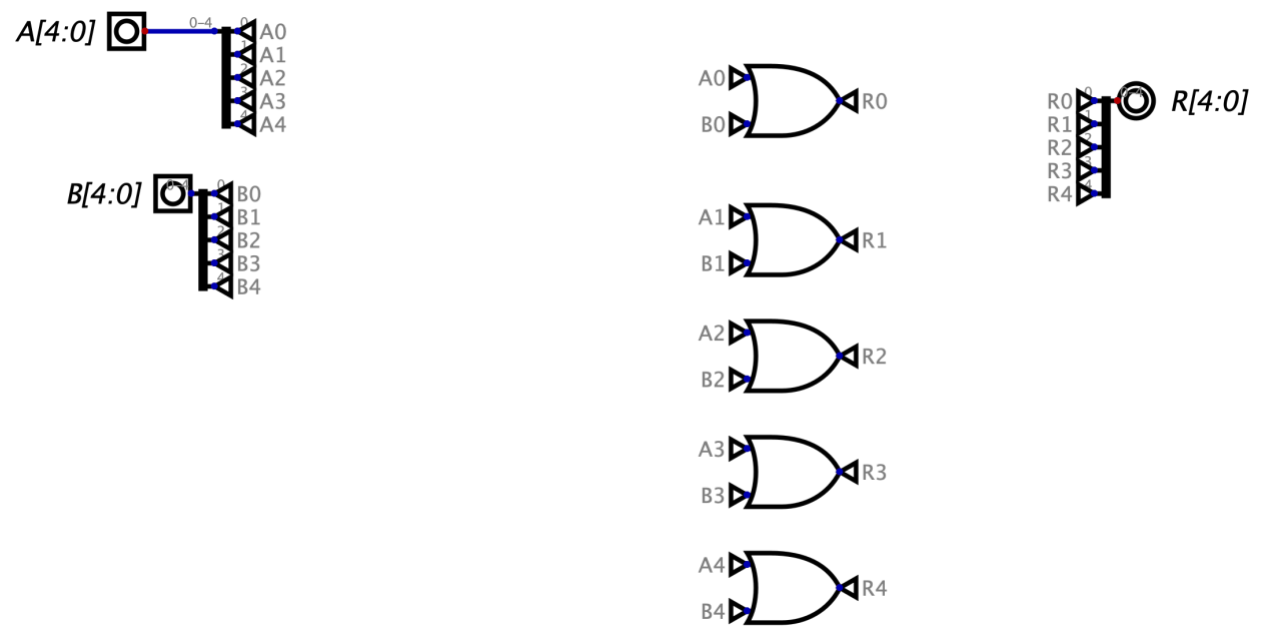
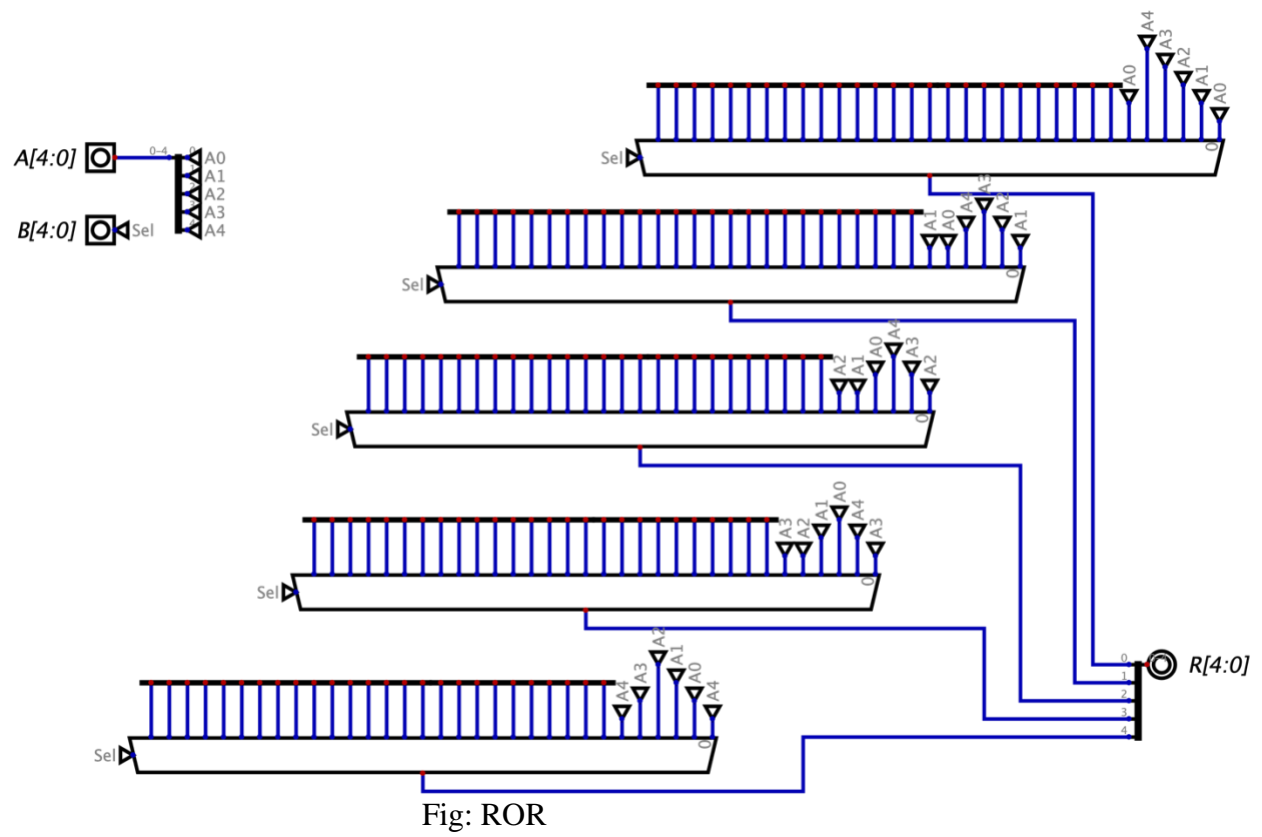


Fig: 5-bit FA



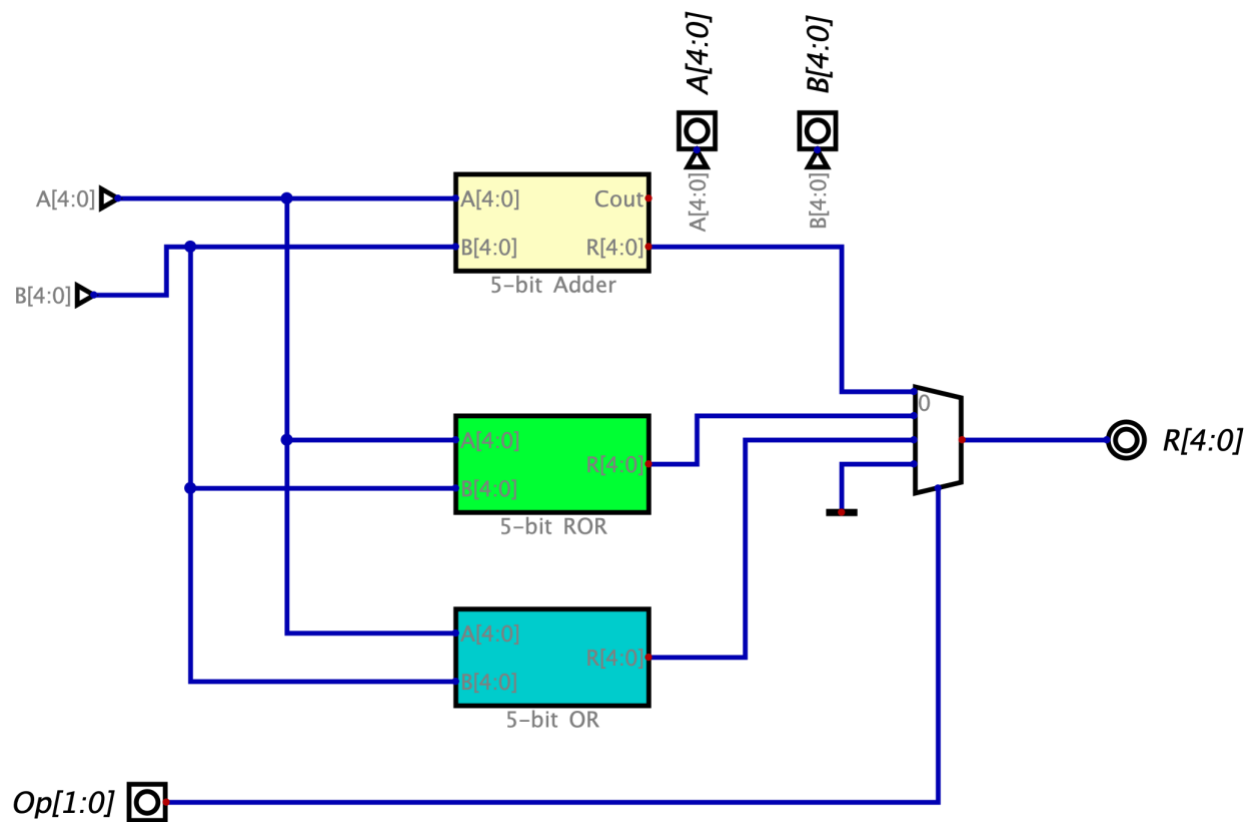


Fig: ALU

2. Register Set Circuit (Top to Bottom all circuits):

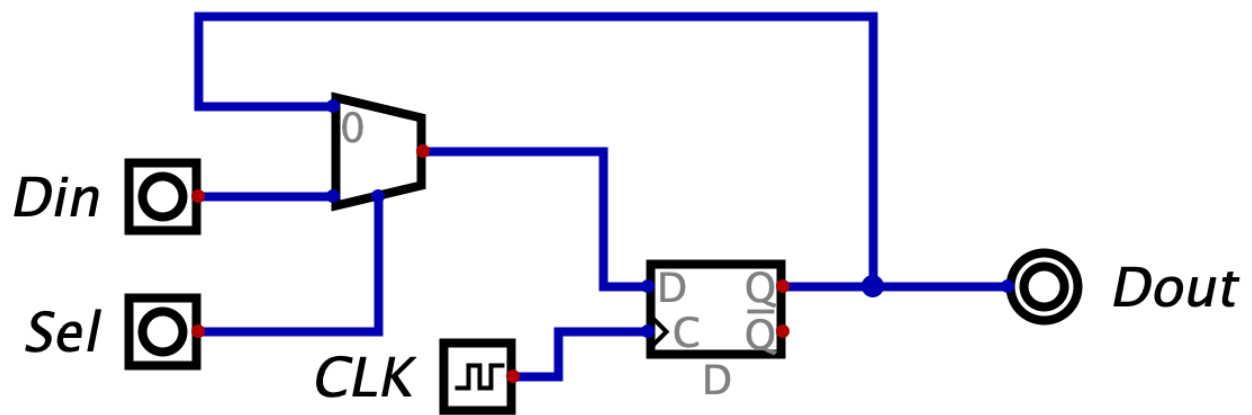


Fig: 1bit register

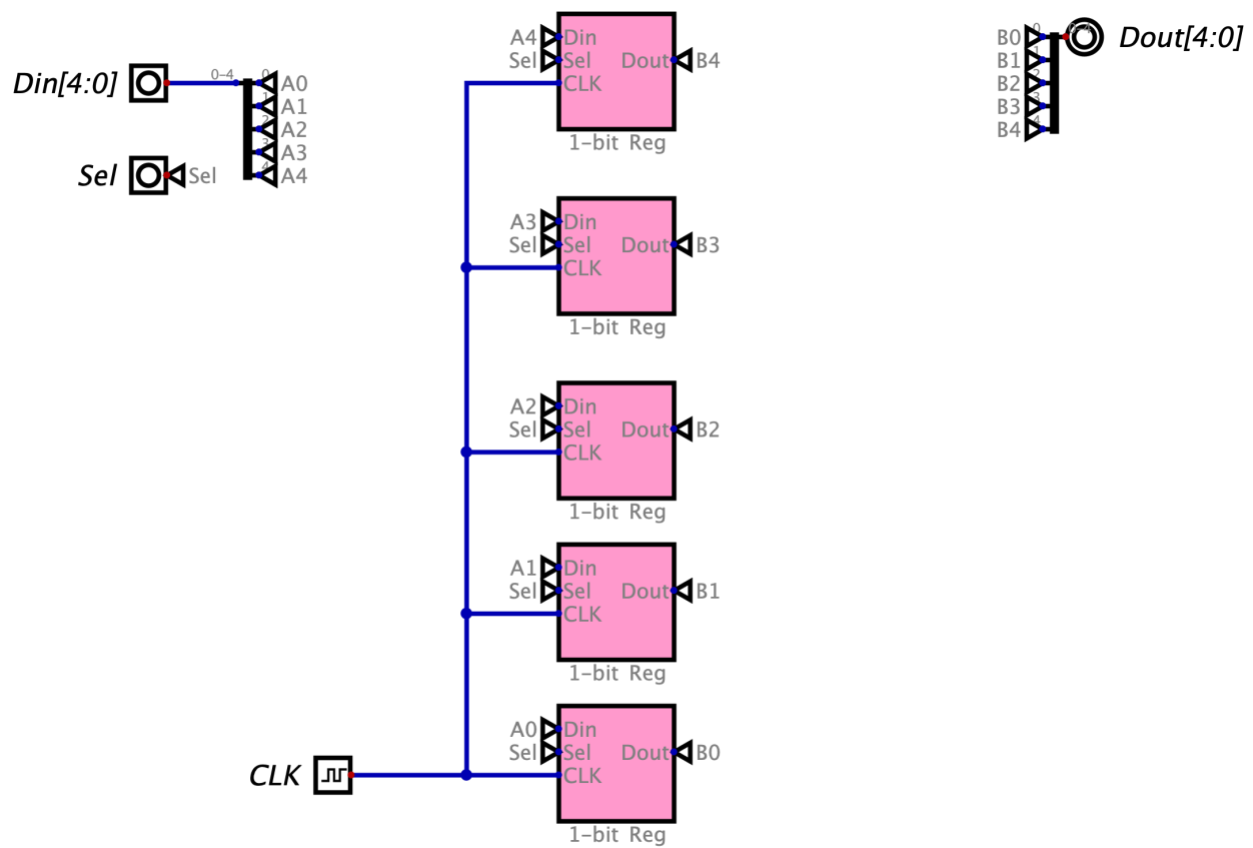


Fig: 5bit register

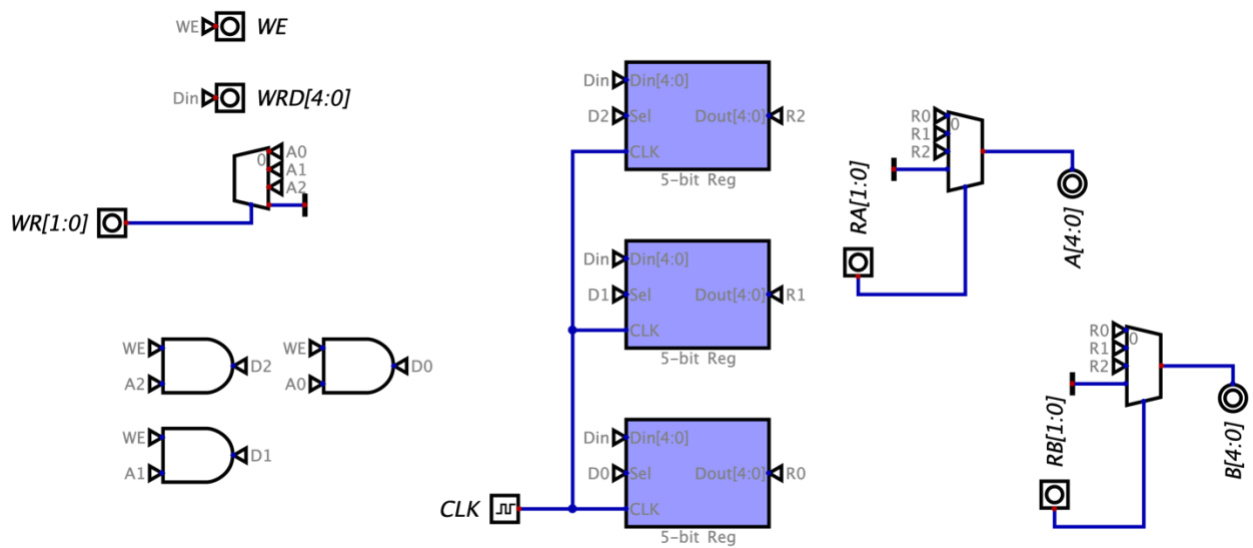


Fig: Register set

3. RAM Circuit (Top to Bottom all circuits):

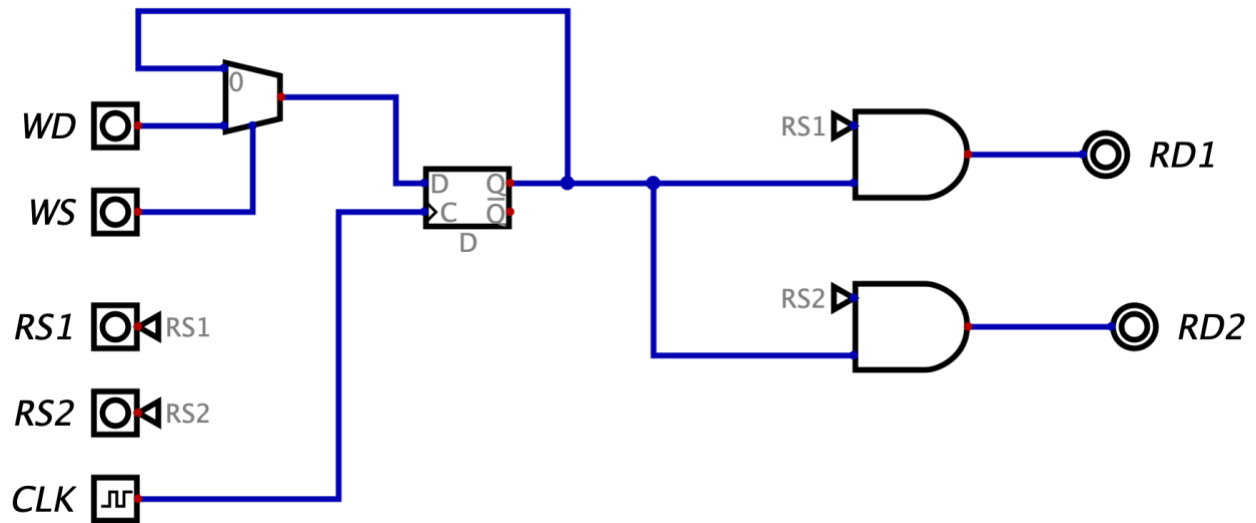


Fig: 1x1 SRAM

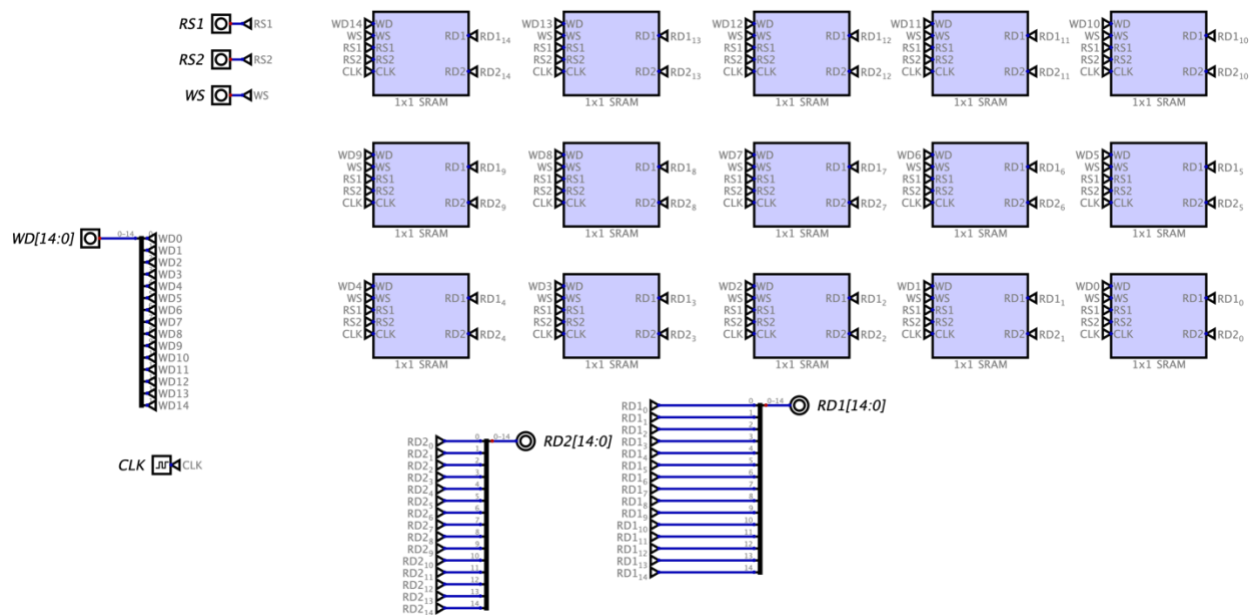


Fig:1x15 SRAM

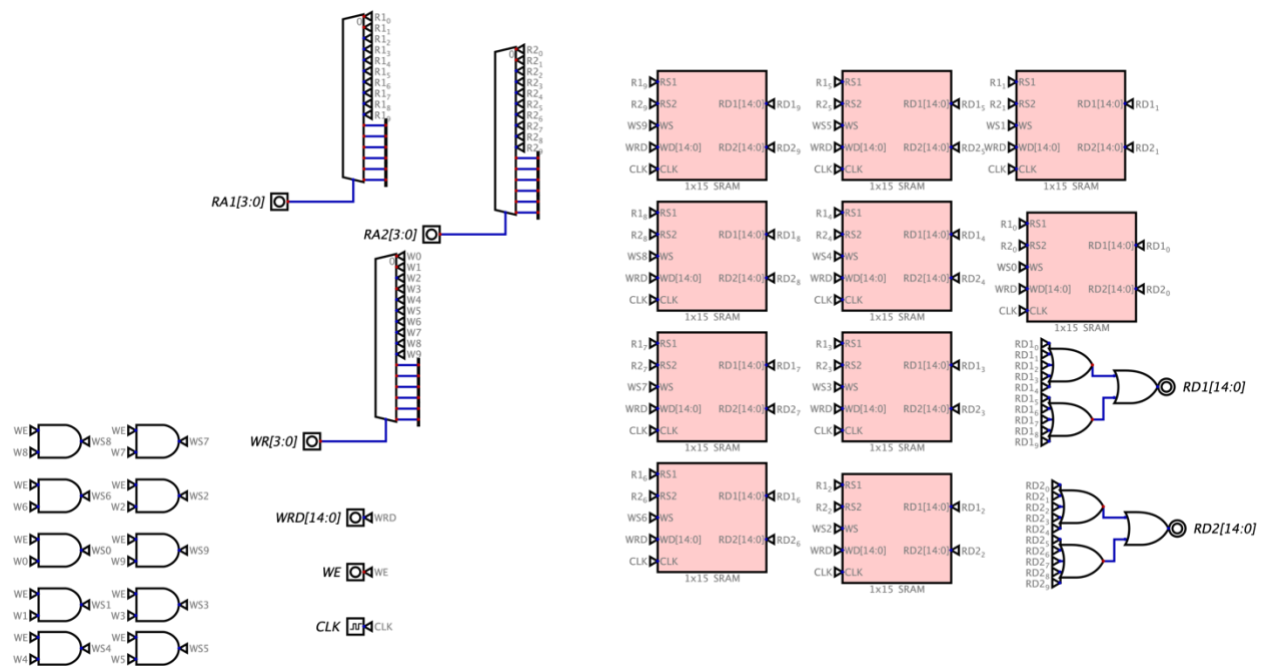


Fig:10x15 SRAM

4. ISA

ISA of Arithmetic & Logic Instruction (Register Mode)

Type of Op ->00

ADD (Op -> 00)

ROR (Op-> 01)

OR (Op->10)

Opcode (4 bit)		Register 1	Register 2	Unused
2 bit	2 bit	2bit	2bit	7bit
Types of Instruction	Operations (ALU selection lines)	00-10 Ra	00-10 Rb	xxxxxxx

Example: Add R1,R1 ->000001010000000

ISA of Arithmetic & Logic Instruction (Immediate Mode) :

Type of Op ->01

Opcode (4 bit)		Register 1	Constant	Unused
2 bit	2 bit	2 bit	5 bit	4 bit
Types of Instruction	Operations (ALU selection lines)	00-10 Ra	Value(00000-11111)	xxxx

Example: Add R1,2 ->010001000100000

ISA of Branching :

Type of Op ->10

JMP (Op -> 00)

JNE (Op -> 01)

Opcode (4 bit)		Address		Unused
2 bit	2 bit	4 bit		7 bit
Types of Instruction	Operations	0000-1001		xxxxxxx

Example: JNE 2(label) (1001001000000000)

5. CPU (Top to Bottom all circuits):

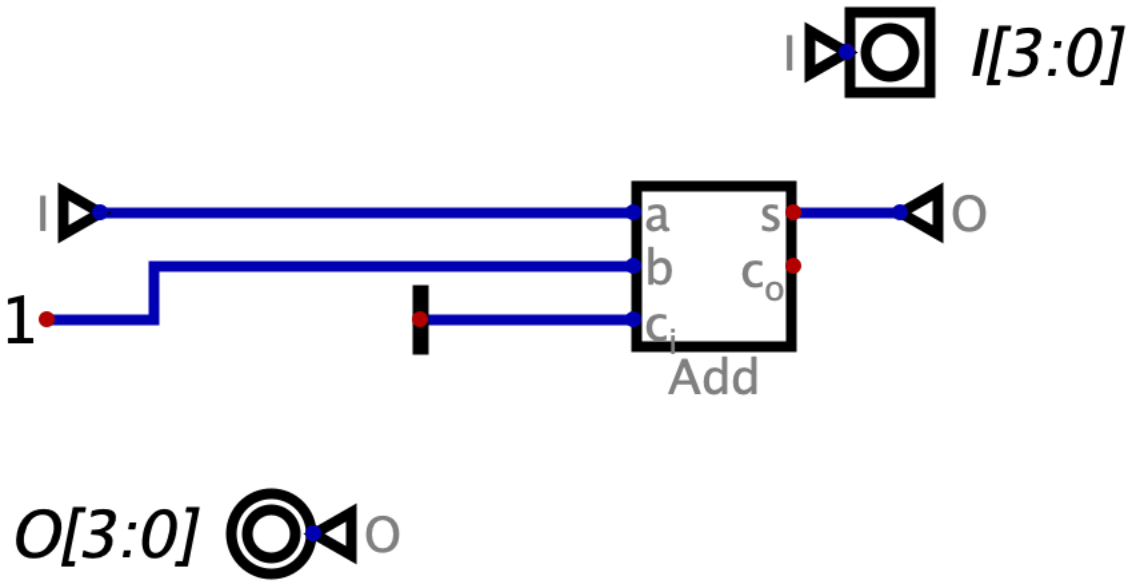


Fig: 4-bit PC Adder

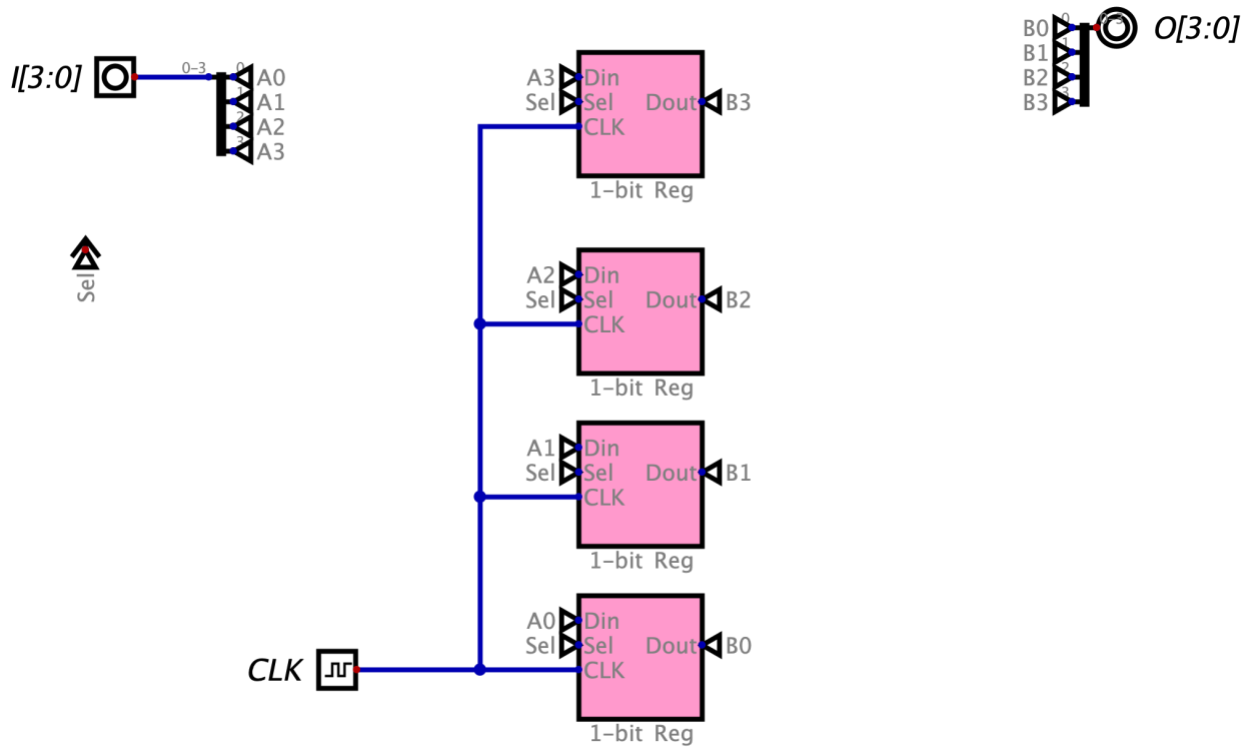


Fig: 4-bit PC register

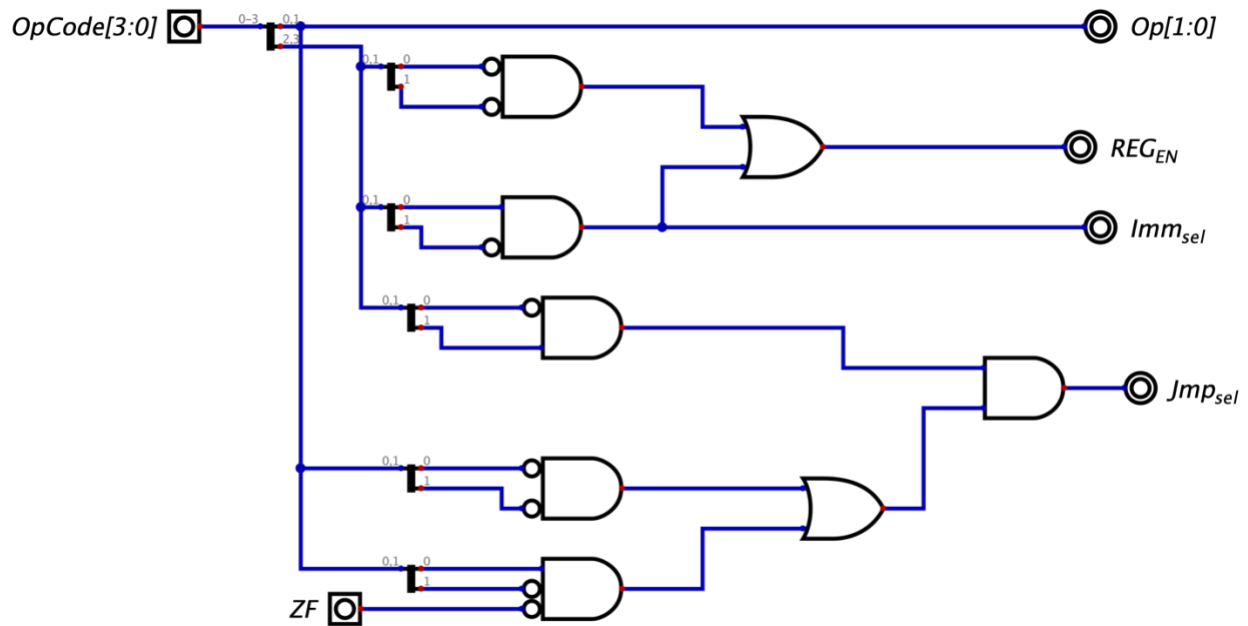


Fig: Control unit

Register Mode(type Of Op==00)2bit(Type of op)+2bit(op)+2bit(Reg1)+ 2bit(Reg2)+7 bit don't care
 Imm Mode(type Of Op==01)2bit(Type of op)+2bit(op)+2bit(Reg 1)+ 5bit(Imm value)+4bit don't care
 Jump Mode(type Of Op==10)2bit(Type of op)+2bit(op)+4bit(Addr)+ 7bit don't care
 Add(op=00),ROR(op=01),OR(op=10)
 JMP(Op=00),JNE(Op=01)
 JNE START -> 1001000100000000
 START: OR R1, R1 -> 0010010100000000
 JMPTO:ADD R1,5 -> 0100010001010000
 JMP JMPTO -> 1000000100000000

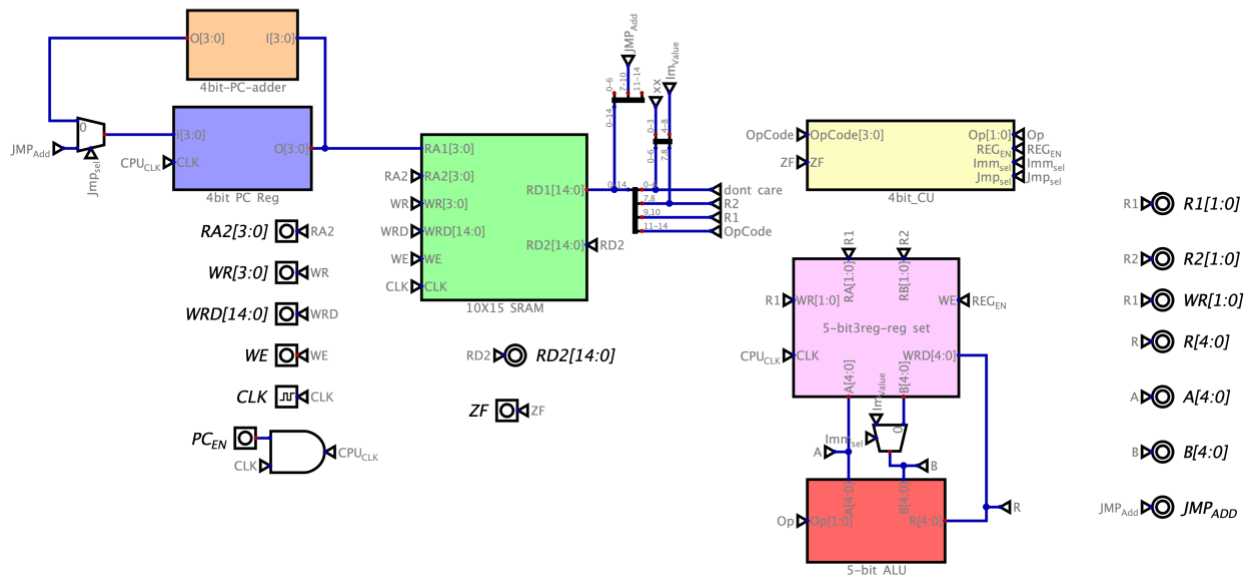


Fig: 5 bit CPU