East West University
Department of Computer Science and Engineering

Course: CSE251 Electronic Circuits
Expt No.: 7
Title: Biasing of a Common-Source Voltage Amplifier

Objectives:
1. Identify an appropriate DC operation point for a NMOS transistor.

Theory: The common-source amplifier with a NMOS transistor is shown here.
1. The biasing is done by fixing the gate voltage with a voltage divider and also by using a source resistor R_S. The source resistor gives negative feedback and stabilizes the bias current as a function of temperature variations and transistor characteristics. This is a popular biasing scheme for discrete transistor circuits.
2. Select source resistor such that voltage Vs at source terminal is about 1/3rd to 1/5th of V_{DD}. The resistance R_D is chosen such that drain voltage V_D is about in the middle of V_{DD} and V_S. This is done so that the signal at the drain has a relatively large and symmetrical output swing.

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \qquad V_{GS} = V_t + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}}. \quad V_G = V_S + V_{GS} = V_S + V_t + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}}$$

3. We choose the resistors such that the parallel resistor is relatively large to ensure a large input resistance of the amplifier and prevent loading of the signal source $R_{in} = R_{G1} || R_{G2}$.
4. An important characteristics of a transistor is its *transconductance* g_m. It is a measure of the rate of change of output current with respect to input voltage v_{gs}. The g_m can be written as follows,

$$g_m = \frac{\partial i_D}{\partial v_{GS}}|_Q = k_n' \frac{W}{L}(V_{GS} - V_t) = \sqrt{2I_D k_n' \frac{W}{L}}, \quad g_m = \frac{2I_D}{V_{GS} - V_t}$$

Circuit Diagram:

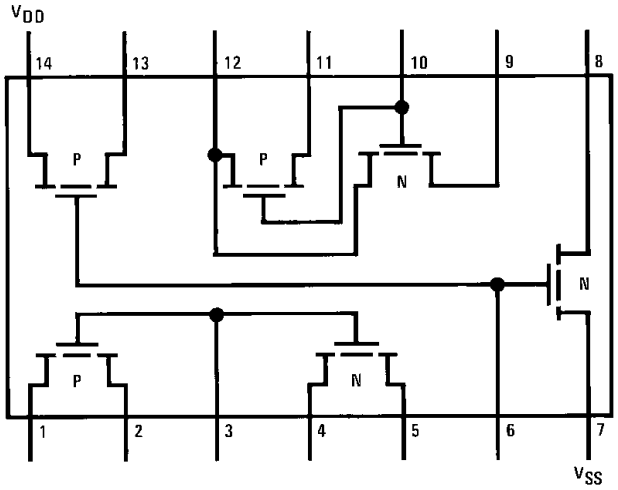


Figure 1. Pin diagram of CD4007C IC.

Equipments and Components Needed:

1. Digital trainer board
2. DC power supply
3. Digital multimeter
4. DC Voltmeter
5. CD4007C IC (1 pc)
6. Resistor (1KΩ 1 pc)
7. Breadboard
8. Connecting wires

Lab Procedure:

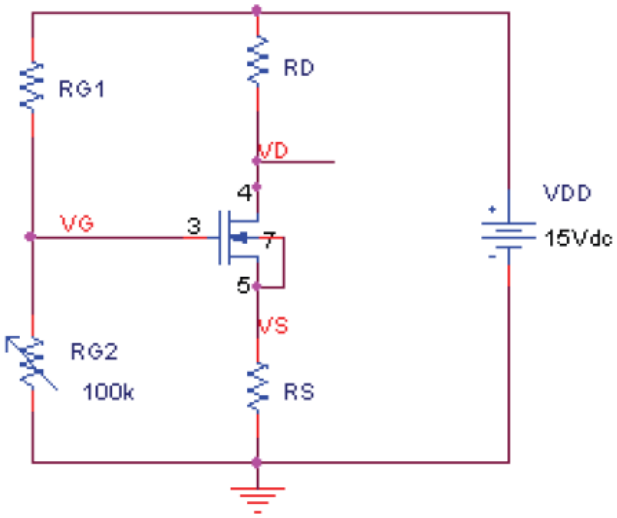
Pre-Lab:

a. Read: Section 4.5.2 (example 4.9) Sedra-Smith, 5th ed.
b. You have to bias the transistor with a bias current $I_D = 0.6mA$. Let the source voltage V_S be 4V.
c. Choose drain voltage V_D such that it is in the middle of V_{Sn} and V_{DD}.
d. The input resistance R_G should be larger than 15 kOhm.
e. The NMOS transistor (CD4007CN array) characteristics are: $V_t = 1.2V$, $k_n'W/L = 0.7mA/V^2$,

a. Following example 4.9 procedure and information above determine the value of V_D, R_S, and R_D, R_{G1} and R_{G2}
b. What is the total DC power dissipation in the amplifier? (hint: power dissipation is $V_{DD}I_{total}$).

PROCEDURE:

In this part you will bias the transistor (Figure to the right) using pre-lab data.



a. Build the circuit to the right. Use the transistor between the pins 3, 4 and 5. Connect the pin 7 source (pin 5) of the NMOS transistor; drain-to-source short is done to eliminate the back-gate (body) effect on the threshold voltage. (If this transistor does not work try any of the other two NMOSes). For the biasing resistor R_{G2}, use a 100 kOhm pot. For R_{G1}, R_D and R_S use the values from pre-lab.
b. Set the pot R_{G2} such that the drain voltage V_D (pin 4 of MOSFET) is between 9 and 10 V. Note the drain voltage V_D=___V. Now measure the gate and source voltages. V_G=___V. V_S=___V. Calculate the drain current I_D = ___A?