Assignment-1

Marks: 20 (10+5+5)

1. Transfer of bus control from processor to device takes **200 ns**. Transfer of bus control from device to processor takes **300 ns**.
   I. If one of the input/output devices employs **DMA** in **Burst** Mode and takes **20,000,500 ns** to transfer **2048 bytes** of data. Find the data transfer rate of the device in **KB/s**.
   II. Suppose, you are transferring **2048 bytes** of data in both Burst Mode and Cycle Stealing Mode. For the **first half** of the bytes, you use Burst Mode and for the **rest half**, you use Cycle Stealing Mode. Assume that in Cycle Stealing Mode, data is transferred 4 bytes at a time. How long will it take to transfer a total block of 2048 bytes? (Use the data transfer rate found from (a))

2. Suppose, execution of a signed addition instruction **(7A34H + 4DC2H)** occurred. What would be the values of the sign flag (SF), parity flag (PF), carry flag (CF), and overflow flag (OF)?

3. CS = E47BH, DS = 4C18H, BX = 0100H, BP = 0F20H

   To access the physical address in the **Data Segment**, what should be the value of

   I) the **segment register** if the offset register holds the value of B290H.
   II) Find the last physical address of the given **Code Segment**.