

Bashundhara
Exercise Book
Write Your Future

Sadman [REDACTED]
← → MICRO(A)
011221592

C.W
8.6.29

CT \rightarrow 25/6/24

slide \rightarrow 1, 2

Micro

Standard I/O or I/O port vbn

$$M/I \overline{I}O = \text{high}/\text{low}$$

\rightarrow memory operation.

$$M/I \overline{I}O = \text{slow } I/O$$

\rightarrow I/O operation

LDA \rightarrow load address

STA \rightarrow store address.

AL \rightarrow Accumulator register.

MOV \rightarrow Input/Output/Load/Store

6.24
11

Micro

Interrupts on AMD

- * $\text{Ctrl} + \text{C} \rightarrow \text{copy}$ temp reg $\leftarrow 0$
- * Windows keyboard GSR
- * Windows keyboard Interrupt
- * Windows keyboard Stack service routine
- * Windows keyboard timer and $\leftarrow \text{WDT}$

External interrupts

- * maskable $1011 > \text{multiply}$
- * maskable 0001
- * non-maskable 0001 ~~maskable~~
- * ~~forcefully making zero.~~
- * ~~power failure~~
- * ~~infinite loop~~

Internal interrupts

- * ~~over flow~~
 - * ~~division by zero~~
 - * ~~infinite loop~~
- ~~software based,~~

* DMA → Direct Memory Access

DQ → Request

BK → Bus Request

HLDA → Hold Acknowledge

BG → Bus Grant

~~segmented memory~~

~~Math~~ 1000
1000
1000

~~500 × 10~~ segments work
0.0005
75 kB/sec → 75 × 2 bytes/sec

~~75 × 2~~ bytes/sec → ~~500 × 10~~ bytes/sec

~~start~~ 31

256

=

1 byte \rightarrow 8 bit

1 kB \rightarrow ~~1024 B~~ \rightarrow ~~1024 × 8 B~~

1 MB \rightarrow ~~1024 kB~~ \rightarrow ~~1024 × 1024 B~~

1 GB \rightarrow ~~1024 MB~~ \rightarrow ~~1024 × 1024 × 1024 B~~

$$\begin{aligned} B &\rightarrow 2 \\ kB &\rightarrow 1024 \\ MB &\rightarrow 1024 \times 1024 \\ GB &\rightarrow (1024)^3 \end{aligned}$$

2 kB

$\rightarrow 2 \times 1024$ MB

$\rightarrow 2 \times 1024 \times 1024$ kB

$\rightarrow (2 \times 1024) \times 1024$ Byte

$75 \times 1024 \rightarrow 2^3$

1 byte $\rightarrow \frac{1}{75 \times 1024}$

256 byte $\rightarrow \frac{256}{75 \times 1024}$

$$\Rightarrow 3.33 \times 10^{-3} \text{ sec}$$

$$\text{total time} = (3.33 \times 10^{-3} + 500 \text{ ns})$$

Q1

Find 8 \leftarrow std. dev.

$$75 \times 1024 \text{ B} \xrightarrow{\text{1 fs}} 8 \text{ M}$$

$$1 \text{ Byte} \xrightarrow{\text{8 M}} \frac{1}{75 \times 1024 \text{ M}}$$

$$= 1.3 \times 10^{-5} \text{ sec}$$

$$= 1.3 \times 10^{-5} \times 10^3 \text{ ms}$$

~~$= 13000 \text{ ms}$~~

$$\text{std. dev.} \xrightarrow{\text{1 fs}} \text{total} = (13000 + 500) \approx 13500 \text{ ms}$$

$$256 \text{ byte} \xrightarrow{\text{1 fs}} (256 \times 13500) \text{ ms}$$

$$= 3456000 \text{ ms}$$

$$\frac{3456000}{1000 \times 10^3} \text{ sec}$$

~~$= 3.456 \text{ sec}$~~

$$(3.456 + 0.01 \times 66.6) = \text{with lot of}$$

~~(c)~~ suppose 50% os the data is transferred in burst mode at first, then the remaining data transferred two byte at a time using cycling mode

total time

$$75 \times 10^{24} \rightarrow 1$$

$$2 \rightarrow \frac{1}{75 \times 10^{24}}$$

(bytes) goes to $\frac{128}{75 \times 10^{24}}$
 $128 \rightarrow \frac{1}{75 \times 10^{24}}$
 $\Rightarrow 1.67 \times 10^{-3}$ sec

first 1670000 ms

($1670000 + 500$) \times ~~(n + 500)~~

$\Rightarrow 1670500 \text{ ms}$

~~75 × 10² m²~~ → 2
 to show forward
 peripheries ~~2~~
 to shed out $3 \times 2.6 \times 10^3$ m²
 36 m² per 8000 sec
~~128~~ bytes $\times 26000$ ms
~~128~~ bytes $\times 26000$ ms lot of
 $\rightarrow (26000 + 500)$ ms
 $\rightarrow 26500$ ms

~~124 Mbytes~~ \rightarrow 64 cycle (2 bytes)
 $\rightarrow 12501 \times 2^2$ $\leftarrow 851$
 $\rightarrow 12501 + (64 \times 26500)$ ms

$\rightarrow 1696000$ ms
 total = $\rightarrow 1696000 + 1670500$ ms
 $\rightarrow 33661500$ ms

~~Q2~~

~~Show how~~

$$\text{Total overhead time} = (100 + 150) \text{ ms}$$

~~100~~ ~~150~~ ~~250~~

$$= 250 \text{ ms}$$

~~Actual data transfer time~~

$$= (10000 - 250) \text{ ms}$$

$$= 9750 \text{ ms} = \frac{1 \times 10^7}{1 \times 10^9} = 0.015$$

$$512 \text{ bytes of data} = \frac{512}{1024} \text{ KB}$$

~~1024~~ ~~512~~ ~~0.5~~

$$= 0.5 \text{ KB}$$

~~i.e. Data transfer rate~~ $= \frac{0.5 \text{ KB}}{0.015 \text{ s}}$

$$= 50 \text{ KB/sec}$$

$$512 \text{ bytes} = \frac{512}{0.015 \text{ sec}}$$

$$= 51200 \text{ bytes/sec}$$

$$0.1 \times 51200 = 5120 \text{ bytes/sec}$$

~~$$0.1 \times 51200 = 5120 \text{ bytes/sec}$$~~

~~$$0.1 \times 51200 = 5120 \text{ bytes/sec}$$~~

~~Ex - mode~~

Burst mode

~~51200 bytes~~ \rightarrow 1 sec
burst mode

$$256 \text{ bytes} = \frac{256}{51200} \text{ sec}$$

$$\approx 10.0 \text{ ms} = \frac{0.01 \times 10^{-3}}{0.01 \times 10^6} = 5 \times 10^{-9} \text{ sec}$$

~~total time = $(5 \times 10^6 + 250)$ ms.~~

~~cycle mode: $= 5.00025 \times 10^6$ ms~~

~~512000 bytes \rightarrow 1 sec~~

~~4096 bytes \rightarrow $\frac{1}{512000}$ sec~~

$$= (39062.5 + 250) \text{ ms}$$

~~256 bytes \rightarrow 128 cycle~~

~~time = (128×39312.5) ms~~

$$= 5 \times 10^6 \text{ ms} \rightarrow 5.032 \times 10^6 \text{ ms}$$

~~total time = $(5 \times 10^6 + 250)$ ms~~

$$\text{total time} = 5.032 \times 10^6 \text{ ms} \quad \underline{\text{Ans}}$$

Fall-22

No.

8 address and bus width 320 bits

(c) cycle \rightarrow 1000 bytes of memory work

burst \rightarrow 2000 bytes of data

$$195.03125 \times 10^2 = 2 \times 10^5 \text{ bytes/sec}$$

AMQ $2 \times 10^5 \rightarrow 1 \text{ sec}$ [not mentioned]

for 1000 bytes $\rightarrow \frac{1}{2 \times 10^5} \text{ sec}$ how many bytes movement in cycle

$$\text{start end } (5000 \text{ not } 3 \text{ room}) = 8000 \text{ m}$$

$$\text{time} \rightarrow (1000 \times 8000) \text{ ms} = 8 \times 10^6 \text{ ms}$$

~~total time~~ = ~~10000000 ms~~

with what time is it?

burst $2 \times 10^5 \rightarrow 1 \text{ sec}$ 1 sec

$$2000 \rightarrow \left(\frac{2000}{2 \times 10^5} \times 10^3 \right) \text{ ms} = 1 \times 10^7 \text{ ms}$$

$$\text{time} = (1 \times 10^7 + 300) \text{ ms} \\ = 1.0003 \times 10^7 \text{ ms}$$

$$\text{total time} = 1.8003 \times 10^7 \text{ ms}$$

6.1
22.6.24

CS.1117

(c)

* suppose transfer of bus control from processor to device 2000 ns. device to processor takes 2000 ns.

one of the I/O devices has a data transfer rate of $10.5 \times 10^6 BPS$.

and employs DMA.

If the processor does not use DMA, then it takes 3.003 milisec.

to transfer data in one minute, then determine time it will take to transfer

the 3000 bytes data in transparent mode.

$$w (one + F_{01X1}) = 3000$$

$$w F_{01X8000.1} =$$

if $F_{01X8000.1} = 1000$

Point-to-point link

$$3000 \text{ ms} = 3000 \times 10^{-3} \text{ s}$$

$$= 3 \times 10^3 \times 10^{-3} \times 10^6 \text{ ms}$$

$$= 3 \times 10^3 \text{ ms}$$

$$= 0.003 \text{ ms}$$

Transmission time

$$2 \text{ ms} \rightarrow (15.3125 \times 10^4) \text{ bits}$$

$$2 \text{ ms} \rightarrow \frac{15.3125 \times 10^4}{1000}$$

$$3.003 \text{ ms} \rightarrow 600.6 \text{ bytes}$$

$$\text{Total time} \rightarrow \frac{3000}{600.6}$$

$$= 4.995 \text{ ms}$$

(transparent mode)

Micro Lecture-1

Processor Memory

→ It refers to the microprocessor registers which are used to hold temporary results when computation is in progress.

Primary Memory

This is the storage area in which all programs are executed.

→ ROM RAM

Secondary Memory

It stores program & data in excess of main memory.

→ Floppy disk, Hard disk, lot of

Bus

The bus is an electrical path that connects the CPU, memory and other hardware devices on the motherboard.

Address bus

The address bus is a set of wires. It consists of 16, 20, 24, 32, 36 parallel unidirectional signal lines. The number of locations that the CPU can address is determined by number of address lines.

Data bus

A set of wires, consists of 8, 16, 32 parallel bidirectional signal lines.

Many devices in the system will have their output connected to data bus, but only one device at a time will have its output enabled.

P.T.O

Control Bus

and address bus.

set of wires consists of 4 to 10 parallel signal lines. The CPU sends out signals on the control bus to enable the outputs of addressed memory devices or I/O devices.
→ memory read.
→ memory write.

Lecture-2

and output bus

* Peripherals are the I/O devices that connected to a microcomputer and provide an efficient means of communication between the micro-computer & the outside world.

Programmed I/O

In programmed I/O the data transfer is accomplished through an I/O port and controlled by software.

I/O Port (1)

- 2 types:
- for one type, each bit in the port can be configured individually as either input or output.
- For the other type, all bits in the port can be setup as all parallel input or output bits.

I/O Port (2)

- I/O port is made up of group of 8 pins.
- ~~either~~ either input or output.

I/O Port(3)

- 2 special function
- control register called data-direction register (DDR A & DDR B) controls whether pin is determined as inputs or outputs.

→ Data register (Port A & Port B)

holds data travelling in or out through the port.

I/O Port(4)

- bit of DDR is 2 (Output) ↓
- n n n n o (input) ↑

(DDR A)

0	1	1	0	1
---	---	---	---	---

↓ controls

↓ I/O status

(Port A)

--	--	--	--	--

↑ ↓ ↓ ↑ ↓

Fig: Bit config I/O port with (DDR)

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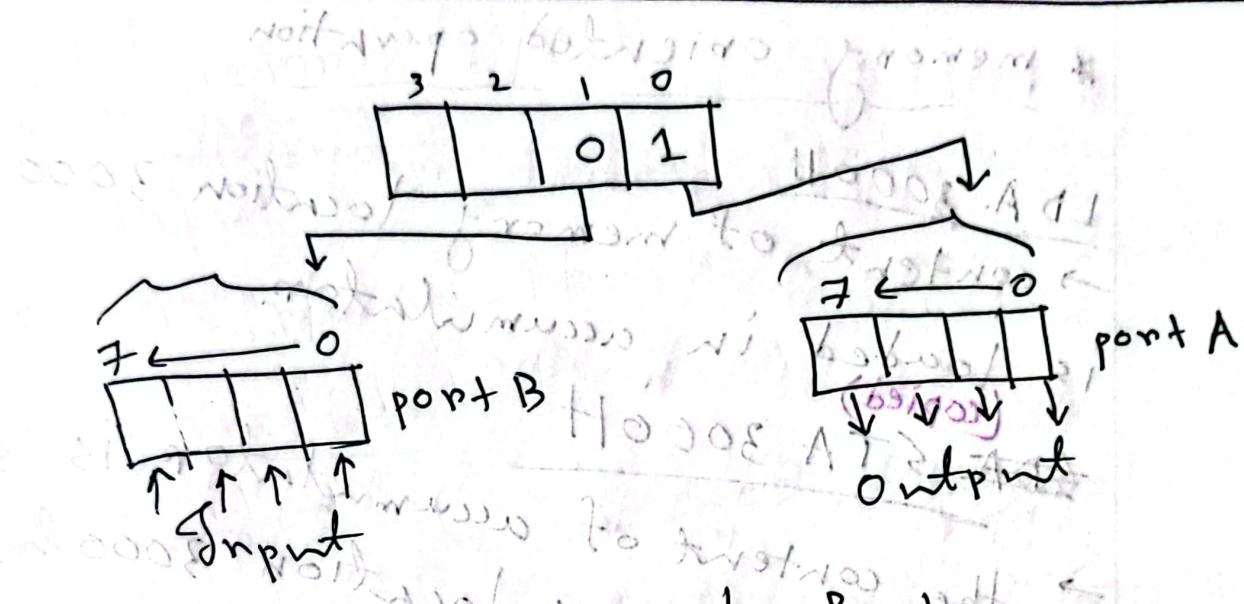


Fig: Parallel I/O Ports.

- # Programmed I/O
- addressed using two techniques.
 - (I) Standard I/O
 - (II) Memory-mapped I/O

Standard I/O

- two separate address space
- memory location (mem read & write)
- I/O devices. (I/O read & write)

- * M/I^O = High (memory operation) } output
M/I^O = low (I/O operation) } control
int pin.

* memory oriented operation

LDA 3000H

→ content of memory location 3000h
is loaded in accumulator.

(copied)

STA 3000H

→ the content of accumulator is stored
into the memory location 3000h.

Memory-mapped I/O

→ single address space is used by CPU.
→ some addresses are assigned to
memory locations & others to I/O
devices.

→ the (most) of the address can be
used.

MSB = 1 ; (I/O port selected)

MSB = 0 ; (memory location is selected)

This reduced the microprocessor
memory by 50% with 16 bits

#

Input/Output Instructions

MOV mem, reg

- Input the contents of a register into a port mapped as a memory location.

MOV reg, mem

- Output the contents of a port mapped as a memory location into a register.

Interrupt I/O

- The I/O devices will interrupt the processor, and initiate data transfer.
- An external device can force the microprocessor to stop executing the current program temporarily so that it can execute another program.

→ External Interrupt

Internal

I.T.O

External Interrupt

→ maskable, non-maskable

maskable:

→ It can be enabled & disabled by instructions.

→ mouse click, keystroke on keyboard.

non-maskable

→ can not be enabled or disabled by instruction.

→ power failure interrupt.

Internal Interrupt

→ activated internally by exceptional conditions

→ overflow, division by zero, execution of an illegal op-code

P.T.O

Direct Memory Access (DMA)

→ Data transfer between memory and I/O can be performed by

bypassing the micro-processor

(with out micro-processor involvement).

→ DMA controller chip 8237

* DMA operation

→ The controller chip activates the

microprocessor HOLD pin, requesting

to release the bus to RAM.

→ The microp. sends HLDA (hold

acknowledge) back to the DMA

controller, indicating that the bus

is disabled. The DMA controller places

the memory address on the address

bus and sends a DMA acknowledge

to the peripheral device.

DMA Registers

* DMA address register:

→ contains the memory address to be used in data transfer.

* DMA count register:

→ contains the number of bytes of data to be transferred.

* Control register

→ accept commands from the CPU.

modes of data transfer in DMA

* Burst mode:

→ DMA controller uses BR (Bus request)

& BR_g (Bus grant) signals to control system timer.

operations AND P.T.O timer with bus and burst length set of

- Transfer an entire block of data continuously once access is granted.
- CPU is inactive during this transfer.
- Efficient for loading large data, but temporarily halts CPU's operation.
- Cycle stealing mode is used.
- Suitable for systems where the CPU can't be disabled for long periods.
- BR & B/R
- Transferring large blocks of data at a time, then release the bus for the CPU to process an instruction.

P.T.O

→ DMA & CPU take turns using
the system bus, so the CPU
isn't idle for long, but
data transfer is slower than

Burst mode.

* Component mode

→ DMA transfers data only when
CPU is not using the system

bus.

→ Slowest mode but maximizes
overall system performance

→ The complexity lies in detecting
when the CPU is not using
the bus.

Micro

$$\begin{array}{r}
 0111 & 1111 & 7F11 \\
 0000 & 0001 & + 211 \\
 \hline
 1000 & 0000 &
 \end{array}$$

Carry flag \rightarrow 0 111 111 111

~~Parity~~ flag \rightarrow 0 ((odd number of 1))

1 → when even number of '1' s

$AF \rightarrow$ 3 to 4 bit carry $\rightarrow 1$

Zero flag \rightarrow 0 (result non-zero)

Sign flag \rightarrow 1 (mde value 1 (negative))

(6) max value $\rightarrow 1 \rightarrow (1)$
 \nwarrow \nwarrow $\rightarrow 0 \rightarrow (0)$

$$\begin{aligned} m_s b + m_b b &> m_s b \\ 0 + 0 &= 1 \\ 1 + 1 &= 0 \end{aligned}$$

$$OF = 1 \quad (\text{positive} + \text{positive} = \text{negative})$$

\downarrow overflow $(\text{neg} + \text{neg} = \text{pos})$

overflow

(neg + neg = pos)

cang mba in ≠ mba out

FF/FF
FFFF

1111
1000
1110

1110

DDDD 0DD1

1111 1111 1111 1111

1111 1111 1111 1111 ← soft form

① 1111 1111 1111 1110 → odd number of 1's
Last 8 bit → odd number of 1's

Carry → 1
Forms first number of 2 in last 8 bit
PF → 0 (odd number of 1's) (3-4) bits

AF → 2 (carry over) ← soft overflow

ZF → 0 (odd number of 1's) ← soft overflow

SF → 1 (odd number of 1's) ← soft overflow

OF → 0 (neg + neg = neg) ← soft overflow

($f = 70$)

two last + next two → work

TM

~~20,000H → CS (Physical location)~~

~~2000H → CS (Internal Address)~~

~~0000H → IP (Offset)~~

$$\begin{array}{r} & \text{A} \\ & \text{01111} \\ \text{20,000 H} & \text{---} \\ \text{0000 H} & \text{---} \\ \hline & \text{20,001 H} \end{array}$$

Actual, 20,000 H → Actual 20,001 H

→ CS: IP

~~2222H: 0016H address~~

~~2222H × 10H (Physical location)~~

$$\begin{array}{r} & \text{A} \\ & \text{00111} \\ \text{22220 H} & \text{---} \\ \text{0016 H} & \text{---} \\ \hline & \text{22236} \end{array}$$

(Ans)

~~45~~ (without divisor) 25 \rightarrow 4000.05

(without divisor) 25 \rightarrow 4000.05

2222H^o 1232 H \rightarrow 4000.05
~~1111~~ ~~10~~

4000.05
11110 H

4000.05
1232 H 000.05

H 4000.05
12342 H 4000.05 (x)

~~55~~ (without divisor) 25 \rightarrow 4000.05

55 : SP

2526 H 1100 H \rightarrow 2526 X 10

(without divisor) 25260 H \rightarrow 2526 X 10

25260 H

1100 H

26360 H

26360 H

~~DS~~ ~~DT~~

~~DS~~ ~~DT~~

~~3333 H : 0020 H~~ ~~3333 H~~ ~~0020 H~~ ~~3333 H~~ ~~0020 H~~

33330 H

0020 H

33350 H

Micro

26 bit Address lines } total memory
10 bit Data lines } of ram?

\rightarrow ~~32~~ $(2^{16} \times 10)$ bits.

$$\textcircled{2} \rightarrow 2^{32} \times 16 = 6.872 \times 10^{10} \text{ bits}$$

~~$$2^{32} \times 2^{4.32} \rightarrow 38 \text{ bits}$$~~

$$2^{10} = 1K \quad | \quad H = \frac{2^{36}}{2^3} \text{ byte}$$

~~$$2^{20} = 1M \quad | \quad H = \frac{2^{36}}{2^3} \text{ byte}$$~~

~~$$2^{30} = 1G \quad | \quad H = \frac{2^{36}}{2^3} \times 2^3$$~~

Convert into { units with 16 bits }
 P or to { units with 18 GB } ✓

~~$$\textcircled{2} \rightarrow 2^{16} \times 2^5 = 2^{21} \text{ bits}$$~~

$$= 2^{21} / 2^3 \text{ byte}$$

$$= 2^{18} \text{ byte}$$

$$= 2^{10} \times 2^8 \text{ byte}$$

$$= 1K \times 256 \text{ byte}$$

~~$$= 1.5K \text{ KB}$$~~

8086 Part-1

8086 architecture

AD₀ - AD₁₅ (Bidirectional)

Address bus/ Data bus

When AD lines are used to transmit memory address the symbol A is used instead of AD. (A₀ - A₁₅)

When data are transmitted, used D.

- D₀ - D₇
- D₈ - D₁₅
- D₀ - D₁₅

A₁₆/S₃ - A₁₇/S₆

High order address bus with status signal.

6 fingers ground
tie 05 address ←
tie 8 strobe ←
tie 21 and strobe ←

BHE/S₇

outputs 2808

Bus high enable/status
 $S_7 \rightarrow D_7$

It used to enable data onto the
most significant half of data
bus ($D_8 - D_{15}$) with words from

MN/MX ($S_7 \rightarrow A$) A to bus
minimum/maximum

This pin signal indicates what mode
the processor is to operate in.

RD (Read active low)

It is an output signal. $S_7 \rightarrow A$

memory capacity

- address 20 bit

- data 8 bit

- data bus 16 bit

8086 capacity

$2^{10}(K)$

memory = 2²⁰

$2^{20}(M)$

data = 8 bit

$2^8(8)$

Total memory size:

$$\begin{aligned} & 2^{20} \times 8 \text{ bit} \\ & = 1M \times 1 \text{ byte} \\ & = 1MB \end{aligned}$$

* CS: IP \rightarrow 2222H : 0016H

22220H \rightarrow 2222H

0016H (A)

22236H

* CS: IP

* SS: SP / BP (H)

* DS: BX / DI / SI

* ES: BX / DI / SI

3.1

6f100000 2808

→ Physical address → 1256AH

(i) Segment → 1256H

offset → ?

$$PA = (\text{segment} \times 10) + \text{offset}$$

$$\text{offset} = PA - (\text{segment} \times 10)$$

for segment 1256H

$$\begin{aligned} \text{offset} &= 1256A - (1256 \times 10) \\ &= 000A(H) \end{aligned}$$

for segment 1240H

$$\begin{aligned} \text{offset} &= 1256A - (1240 \times 10) \\ &= 016A(H) \end{aligned}$$

100011000101

I2 BX DI : 23 *

I2 DI BX : 22 *

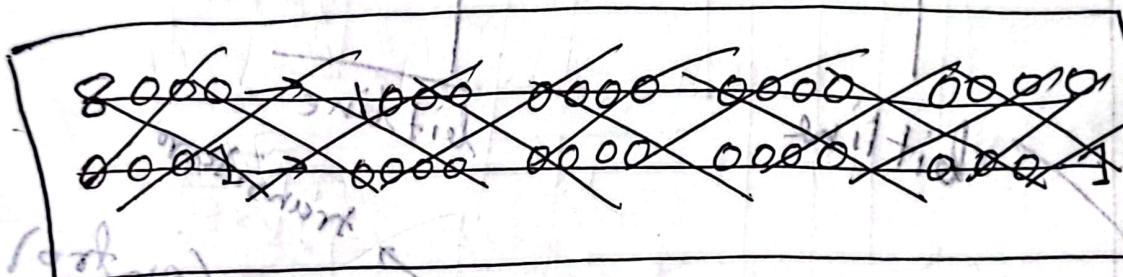
I2 FA BX : 23 *

* PA \rightarrow 805D2 (H) *read bits*

Offset \rightarrow BFD2 (H)

segment = $\frac{PA - \text{Offset}}{10}$ *size of*

\rightarrow 7460 (H)



8000 (H)

(\rightarrow) 0001 (H)

7FFF (H)

0111 1111 1111 1111

CF \rightarrow 0 [*no carry*]

PF \rightarrow 1 [*Even num of 1's in Last 8 bit*]

SF \rightarrow 0 [*msb = 0*]

OF \rightarrow 1 [*adding two num*] [*neg-pos = pos*]

AF \rightarrow 1 [*3-4 bit carry move*]

ZF \rightarrow 0 [*non zero result*]

C.W
2.72V

Micro

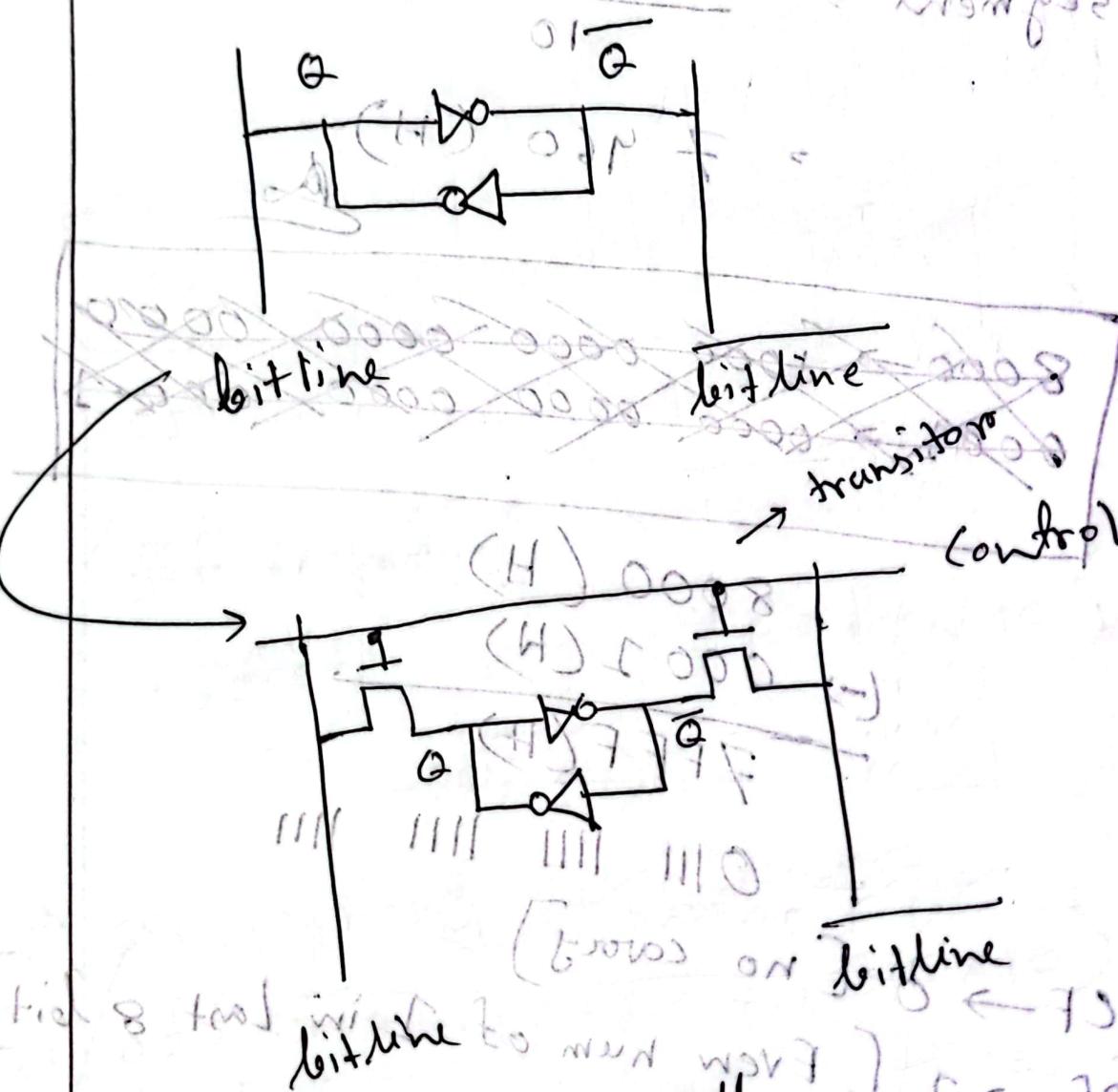
static Ram

(H) → 5V → 8 →

4T
6T

who need any controller
to store the data.

flip-flop

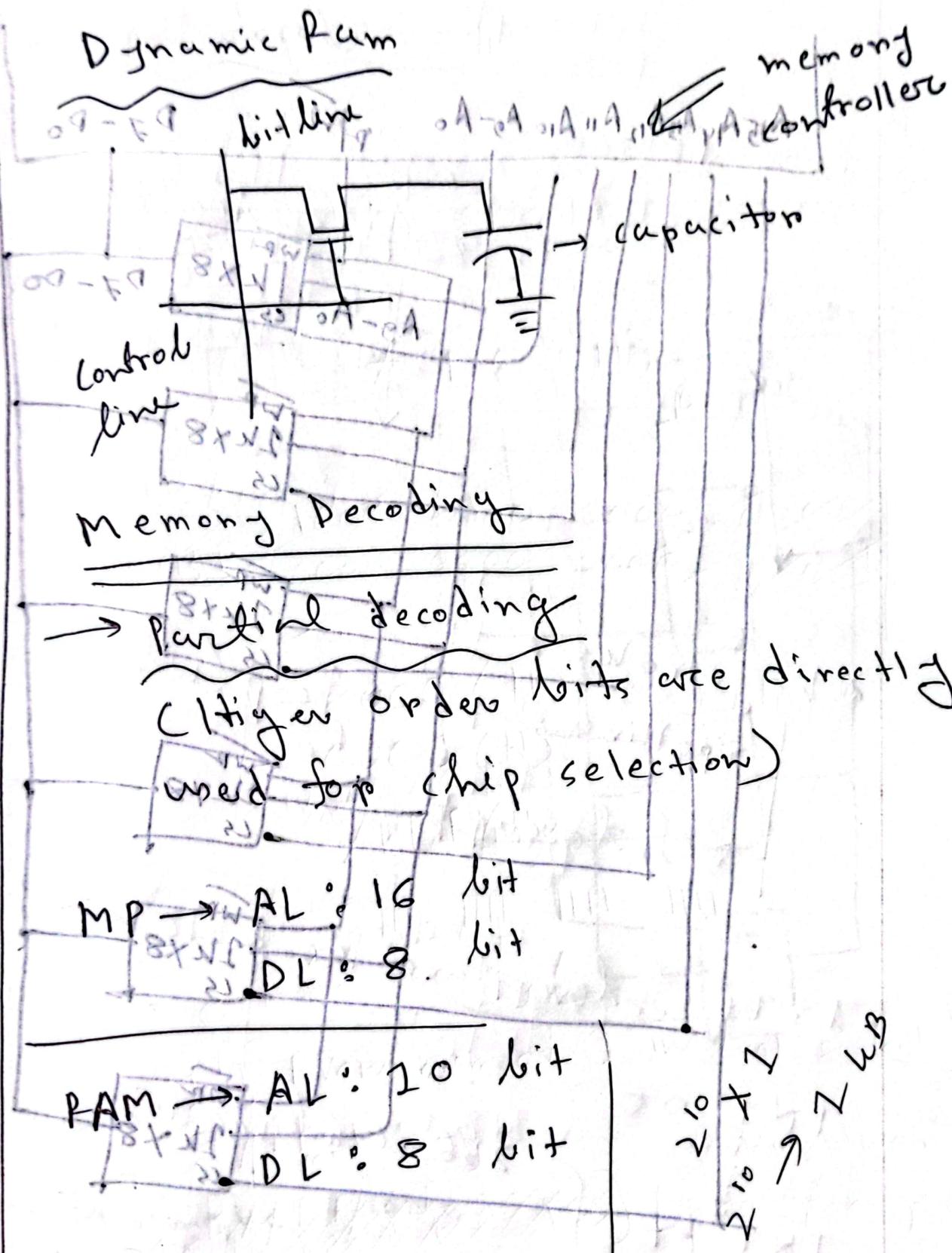


[field 8 tied with bitline to next word] ← 73
[6 most pribbs] ← 79
[209 = 209 - P34] ← 72

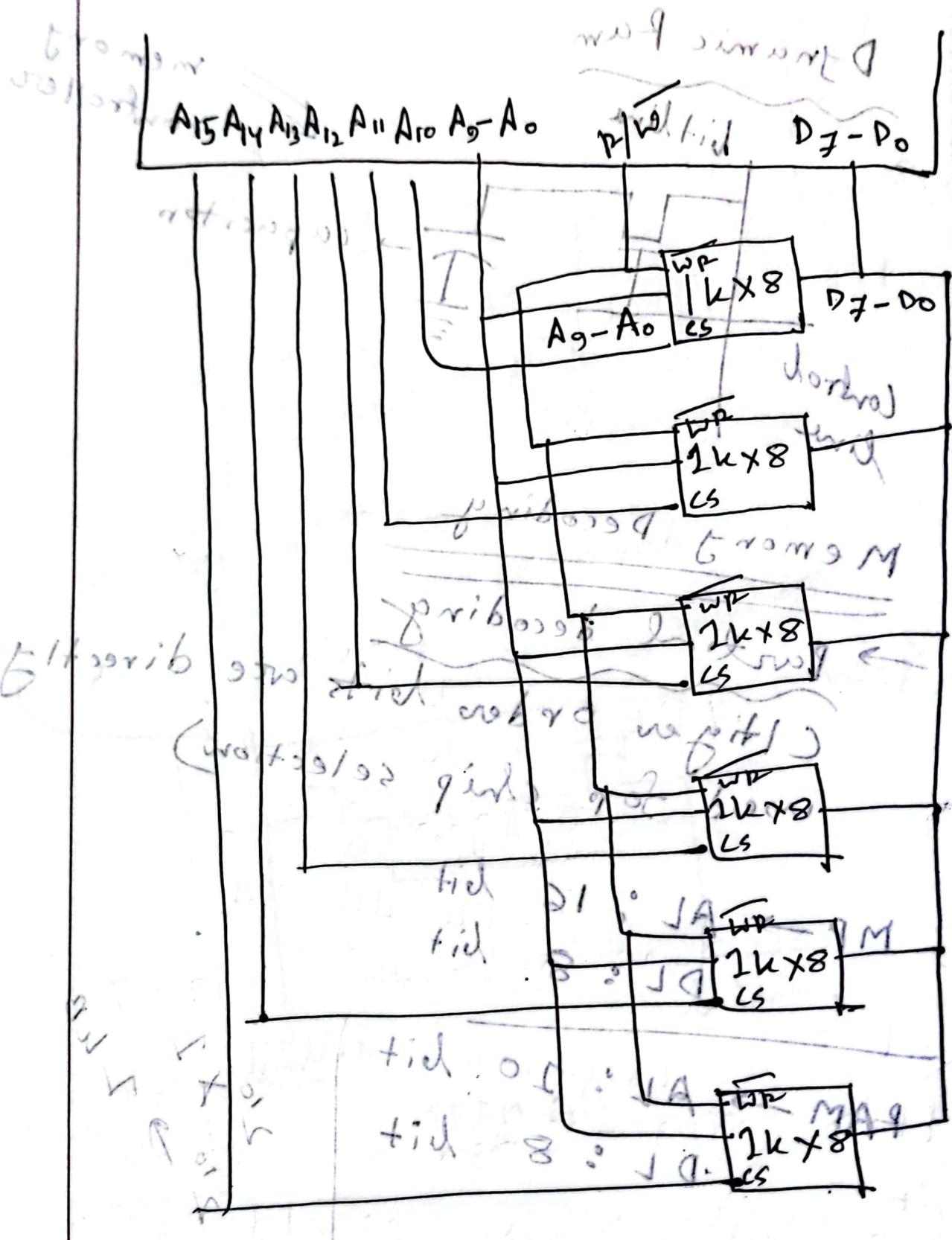
SRAM cell

[2nd row [rows field 1-8]] ← 71
[lower ones ... 7]

and store under faster guidelines



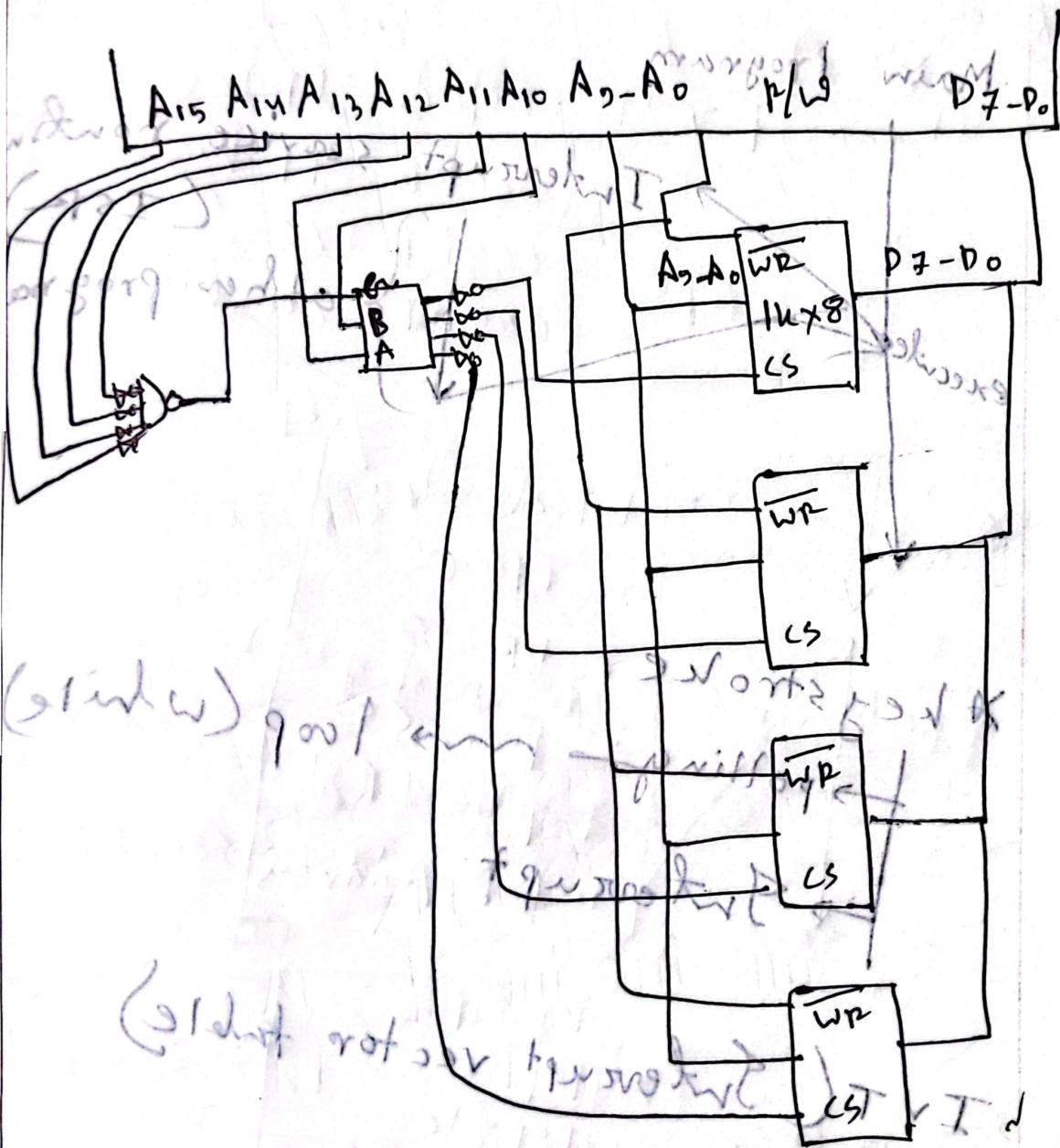
$CS \rightarrow$ Chip Select, $\overline{WP} \rightarrow$ Write Ban



→ full decoding

it's not T

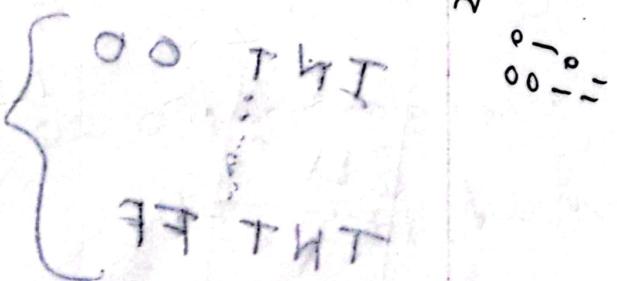
wand \rightarrow F. 1



Unique Address

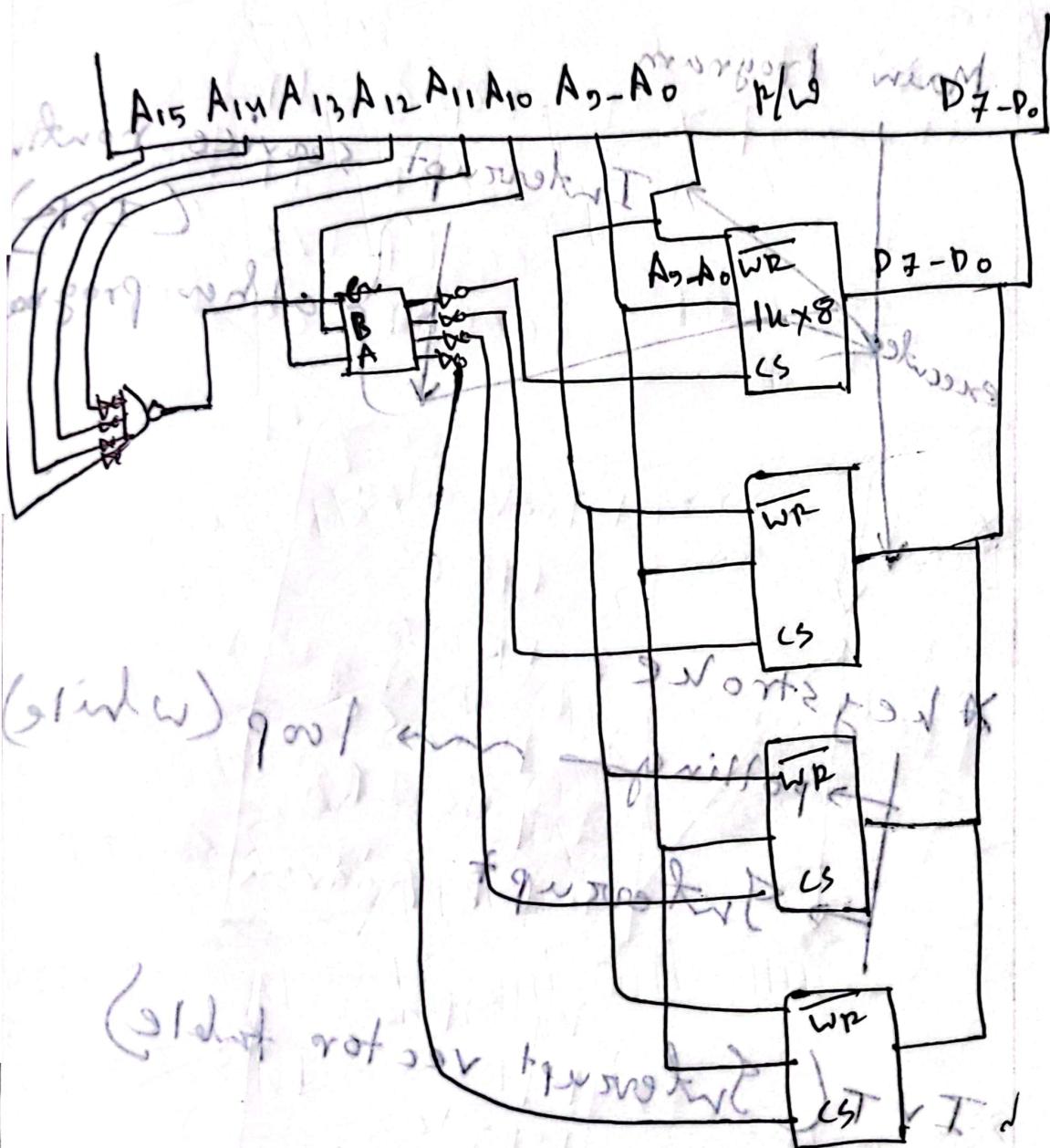
$2^4 = 16$ count

$n \rightarrow 2^n$ (Decoder)



wand

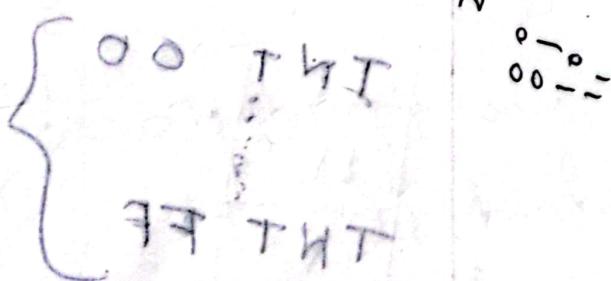
→ full decoding



Unique Address

$2^4 = 16$ count

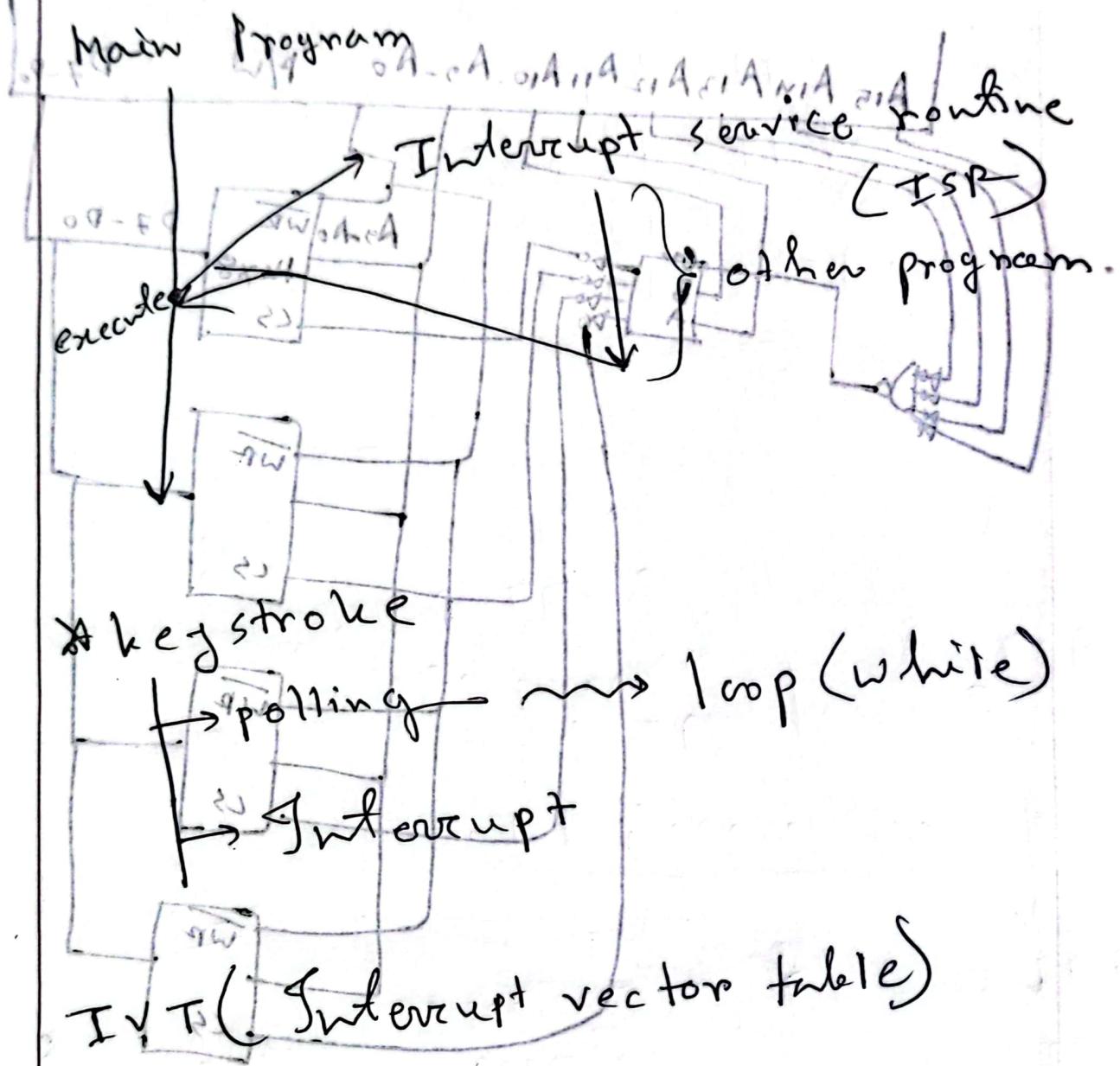
$n \rightarrow 2^n$ (Decoder)



6.2
16.7 2.4

Interrupts

probabilistic logic



INT 00 }
;:
INT FF }

256 combination.

memory A surprise N

trials P ~ S

(reduced) ~ S ~ N

Int vector
(IA address) \rightarrow CS : IP

2 byte

\rightarrow 2 bytes

INT 9T 000000

INT 25 000000

INT 23 7A0000

CS high
CS low
IP high
IP low

Address

256 x 4 byte

$2^8 \times 2^2 = 2^10 B = 1KB$

part word 1

0 - 7T . . .

0 - 7T . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

0000 0 . . .

INT 00

INT 01

INT 02

INT 03

* Calculate memory address of

CH X 4H = 000030 IP low
31 9T IP high
32 23 CS low
33 4807 CS high

Count

~~Int 2F H~~

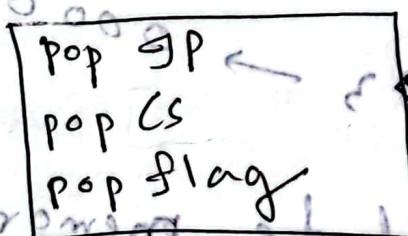
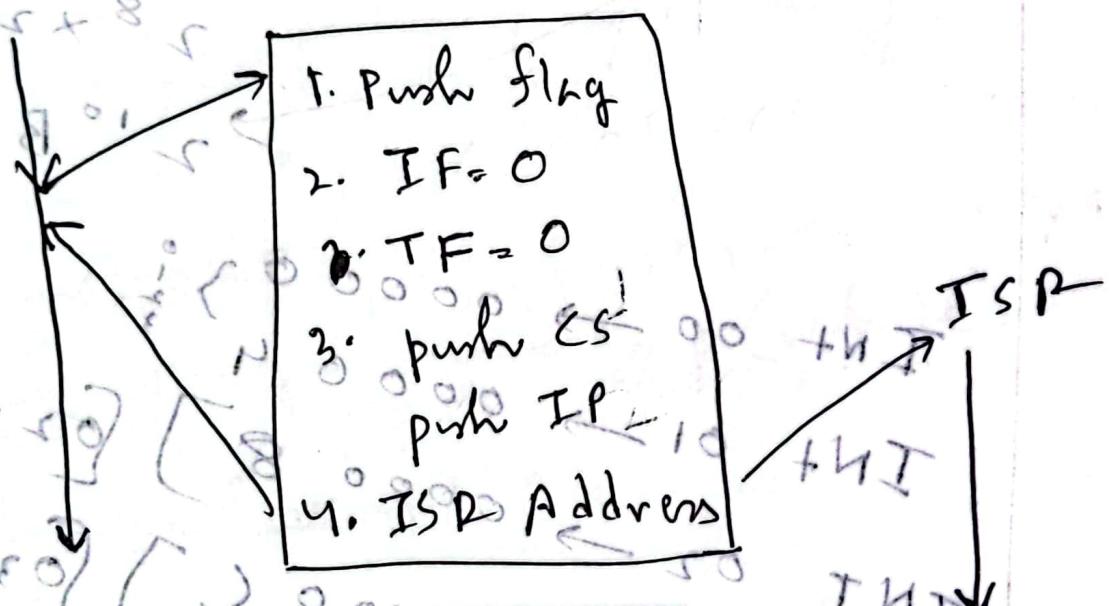
med 122F x 4 = 000B6 (IP-low)

000BD IP high

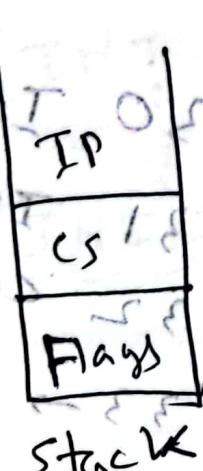
000BF CS long

OOOBEE is high

00013F CS ~~MIS~~



IPRET
(return)



$H^N \times H^S$

(Interrupt
Return)

Transfer : Processor \rightarrow Device : ~~100~~ m
for Bus $D \xrightarrow{\text{Through}} P_A$: ~~150~~ m

burst mode \rightarrow 10,000 2^{50} ns

~~Data transfer time = 10,000 ms~~

$$\text{Rate} = \frac{512 \text{ byte}}{10^7 \text{ ns with interrupt}}$$

$$8 \times 150 \frac{k_B / \text{sec}}{\text{Hz}} = \cancel{1200} \text{ a.u.}$$

2025-26

~~(10) 1983~~

~~b~~ time to receive & report : $T_{receive}$

~~b~~ $256B \rightarrow$ Burst

$$\frac{256 \text{ Byte}}{50 \text{ kbps}} = \frac{2^8}{50 \times 2} \text{ sec} \quad \text{show round trip}$$

~~with network overhead~~

$$= \frac{1}{50 \times 14} \text{ sec}$$

$$= 0.0001000 \text{ sec}$$

$$= 0.005 \text{ sec}$$

~~total~~

$$\text{Total time} = 10^{-5} \text{ sec} + 2^{10} \text{ m} + 0.005 \times 10^9 \text{ m}$$

~~out + For~~

$$= 5000 \text{ m}$$
~~10^-5~~
~~10^-5~~

cycle

~~A~~

$$\text{chuncks} = \frac{256 \text{ B}}{2 \text{ B}} = 128$$

$$\text{rate} = 50 \text{ kbps}$$

~~Time to receive & report~~

$$\text{time required for 1 chunk} = \frac{2B}{50 \times 2^{10}}$$

$$1110 \quad 1100 \quad 1111 \quad 0010 \leftarrow F87F \\ 0100 \quad 1000 \quad 0000 \quad 1100 \leftarrow 3.90625 \times 10^{-5} \text{ sec}$$

total time for 1 chunk, CN 7F

$$= 100 \text{ ns} + 150 \text{ ns} + 3.9 \times 10^{-5} \text{ ms} \leftarrow 7F$$

$$= 392.59 \text{ ns} \leftarrow 72$$

$$t_{idle} = 3.9259 \text{ ns} \times 660 \leftarrow 70$$

$$\text{total time} \leftarrow 128 \times 3.9259 \leftarrow 502.900 \text{ ms}$$

total time

$$(H) 185A \times 25 \leftarrow 4.14 \text{ ms}$$

$$(H) (Burst + cycle)$$

$$= H(01 \times 185A) \rightarrow A9A685$$

$$= (H) 7777 + (01 \times 185A) = 70858$$

$$(H) 70858$$

~~4F37~~ → 0100 1111 0011 0111

~~300124~~ → 0011 0000 0001 0010

~~(+)~~ 7F 49 → 0111 1111 0100 1001

not enit lot of
ZF → 0

SF → 0

PF → 0 { odd number of 1's }

OF → 0 { positive + positive = positive }

CF → 0

W.N.D CS = A231(H) enit lot of

1st PA = $(A231 \times 10)_H \approx A2310(H)$

last n = $(A231 \times 10) + FFFF(H) =$
= B230F(H)

Flag Register

6 - status flags ~~get set~~ 71

Overflow, Sign, Zero, Auxiliary, Parity,

Carry.

3 - control flags ~~get set~~ 77

Direction, interrupt-enable, Trap.

DF

IF

TF

Status flag

reflect the result of an instruction
executed by the processor.

Control flag ~~enable or disable~~

The control flag enable or disable
certain operations of the processor.

DF: It indicates left or right for
moving or comparing string data.

IF: Indicates whether external interrupts are being processed or ignored.

TF: Permits operation of the processor in single step mode. Set (1) for step by step debugging.

8086 Interfacing

CS / WE to the ~~part software~~ ~~part hardware~~ (chip select) / (chip enable) used to select or enable the memory devices usually controlled by the microprocessors through the higher address lines via an address decoding circuit.

RD: Read control signal to memory

Micro

Online

Lecture-1

, Lecture-2 → (standard I/O)

M / \overline{IO}

→ 0 = I/O operation

→ 1 = memory operation

IN, OUT, LDA, STA

Instructions

(memory mapped I/O)

mb = 1 = I/O

mb = 0 = memory

M / \overline{IO} ga
3 mbs

Lecture-3

DMA math

8086 Pins

$(AD_0 - AD_{15}) \rightarrow$ Addr + Data Pins
multiplexed

$\overline{RD} \rightarrow 0$ (read mode)

ALE \rightarrow Address latch enable

(memory / (I/O) address)

$M/\overline{IO} \rightarrow 1$ (memory)

$0 (\text{I/O})$

RESET $\rightarrow 1$ (initial state)

$(A19 - AD_0) \rightarrow 20$ bit Addr

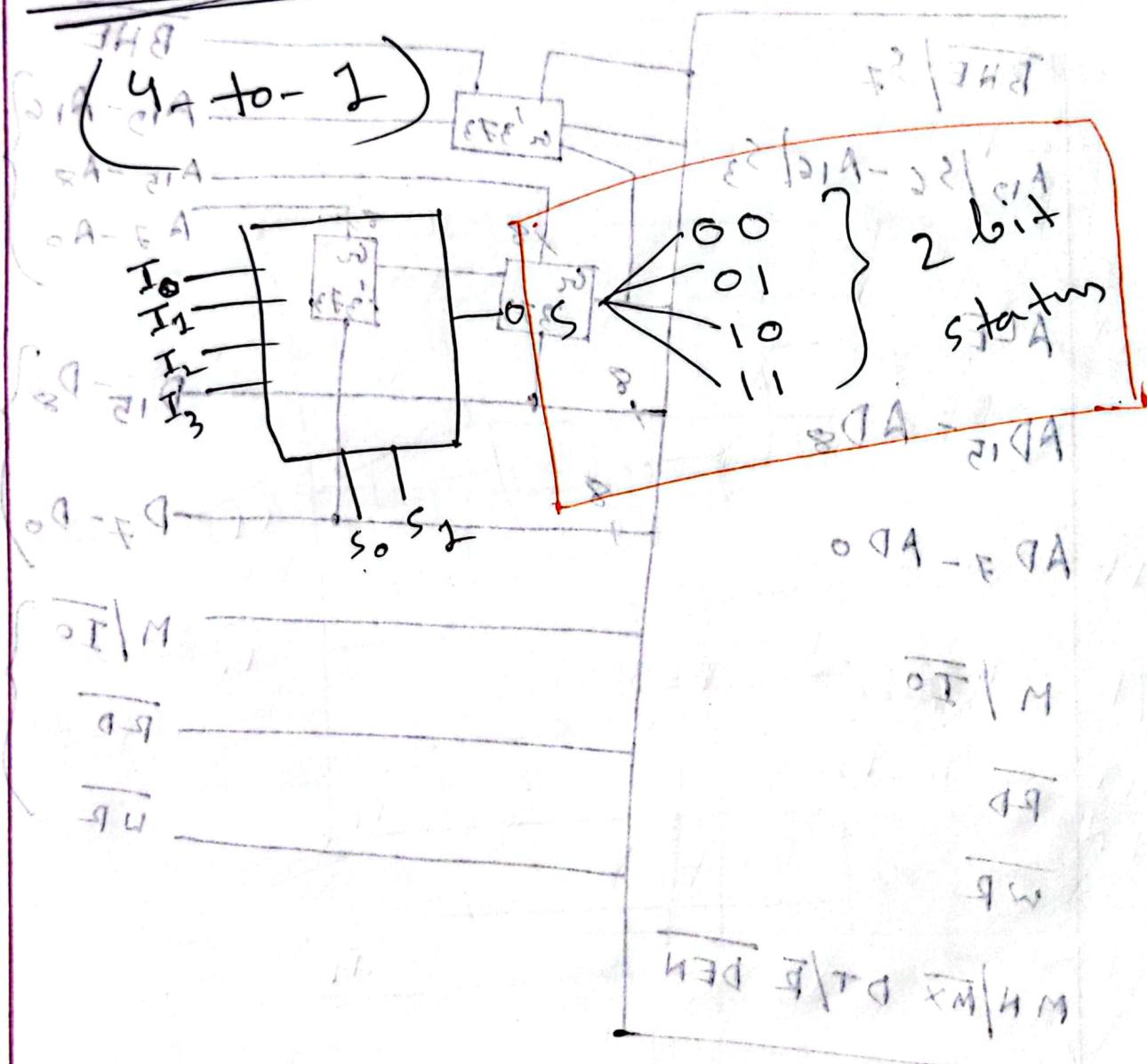
$S_3/S_4 \rightarrow$ segment

~~$S_6 \rightarrow$~~ fix

$S_5 \rightarrow$ IF contents

$AD \rightarrow (\text{Multi} / \text{DeMulti})$

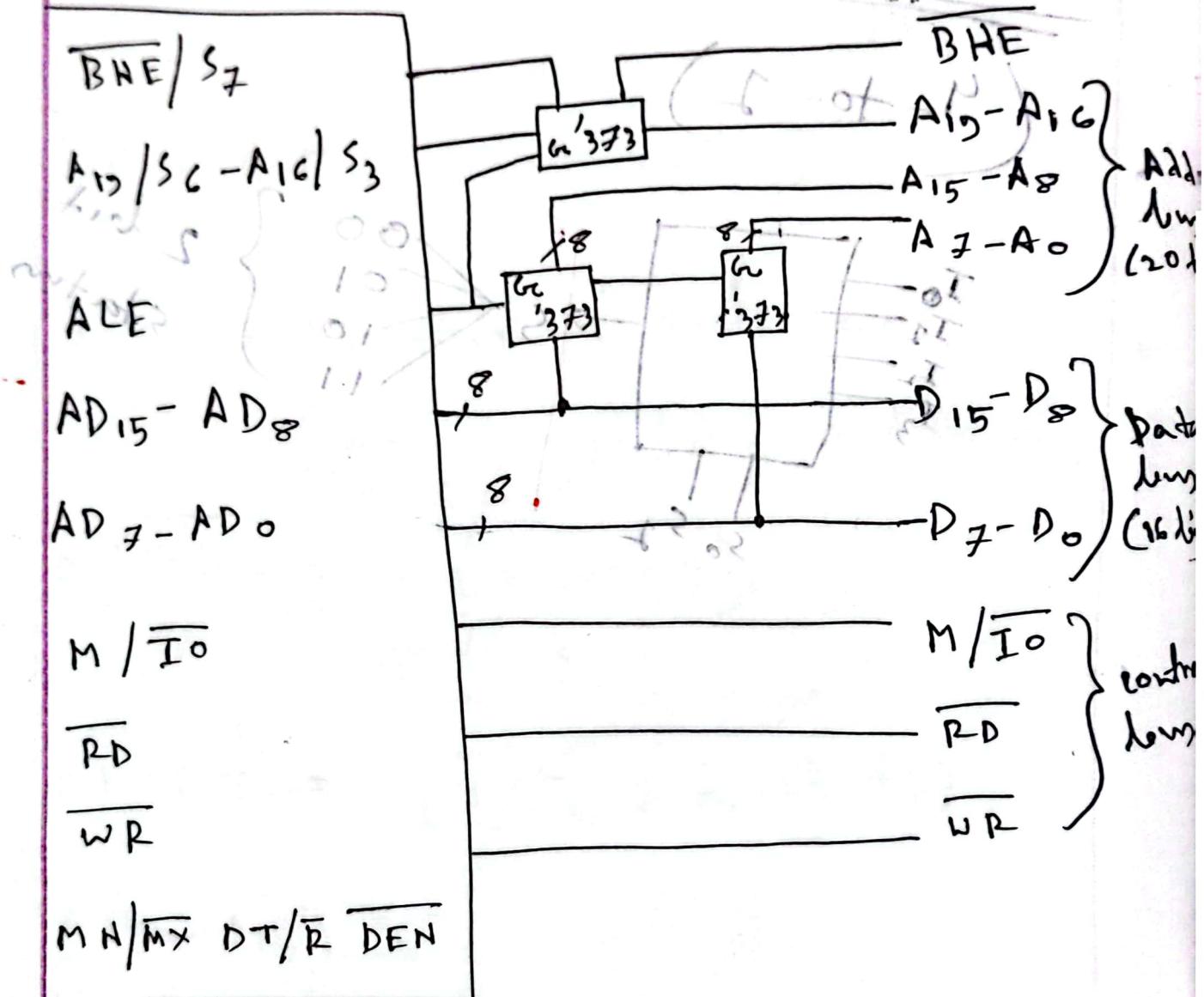
Multiplexers



Micro

Demultiplexing 18086 | Address M) ~ QA

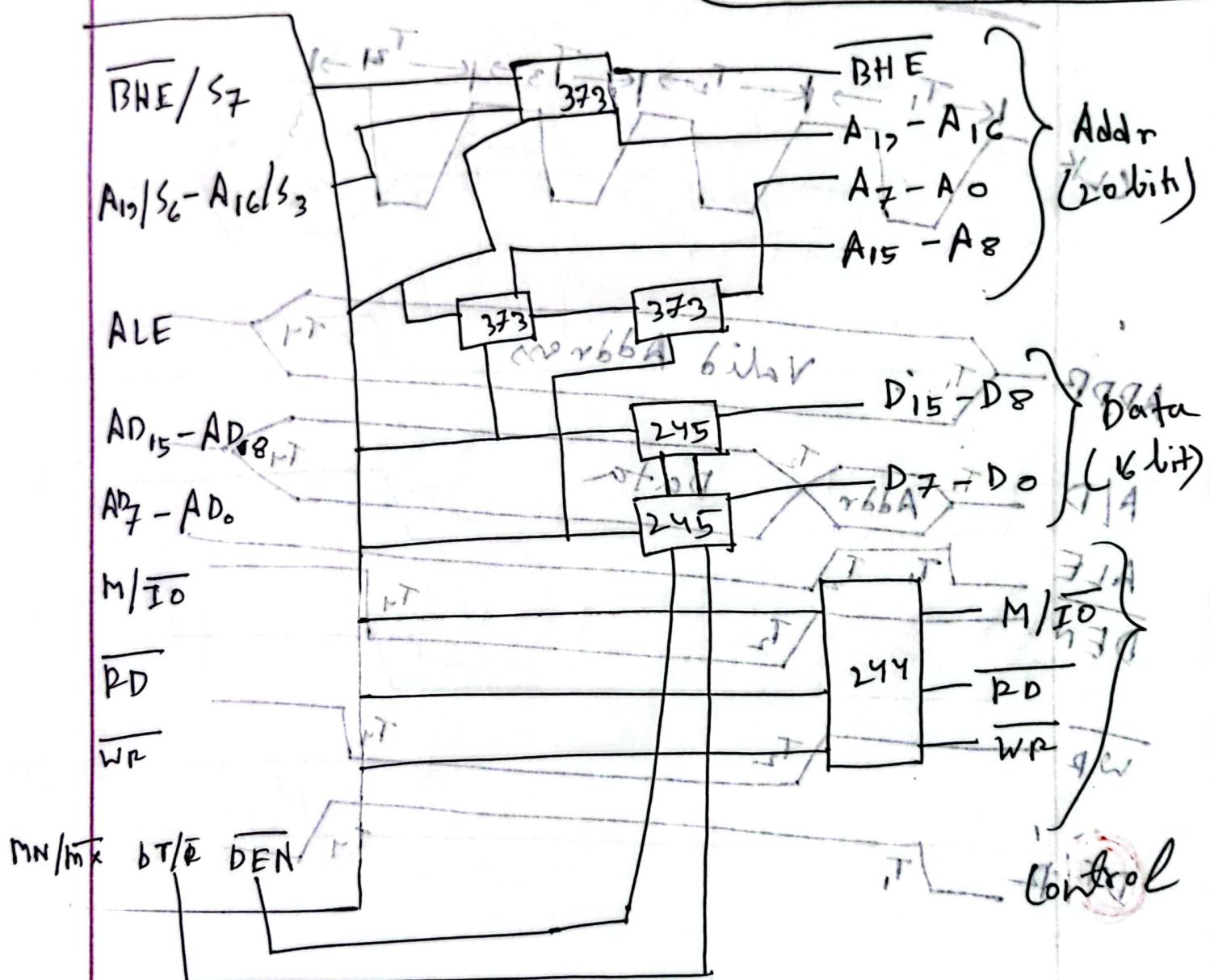
74373 - Octal D - I/O
Transparent Int.



Buffering 8086

742244 - Octal buffer

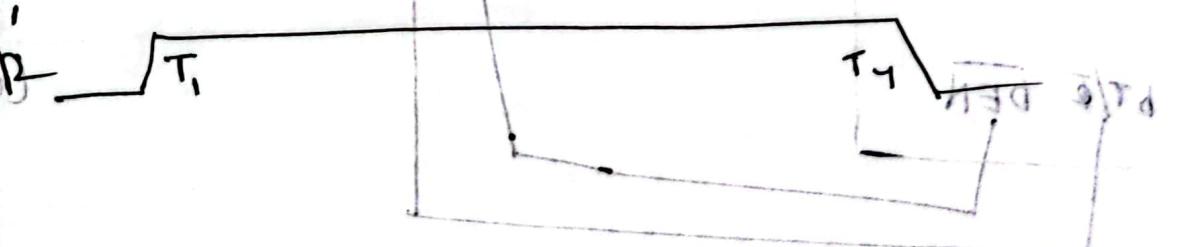
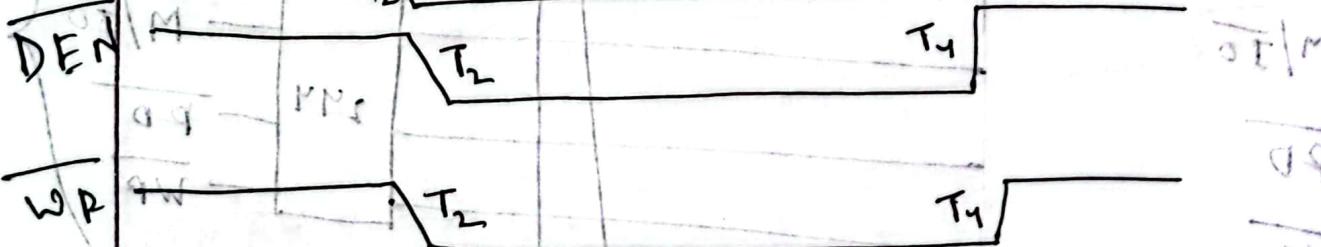
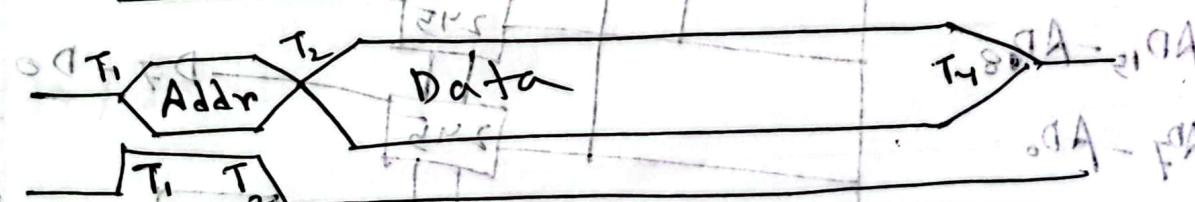
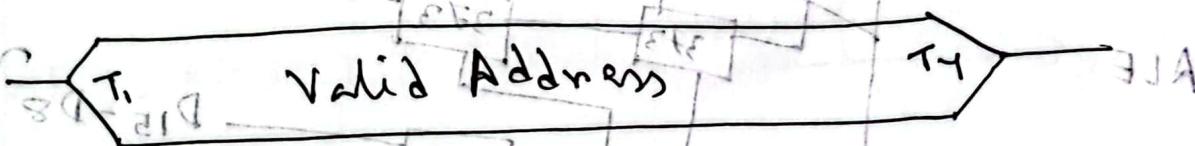
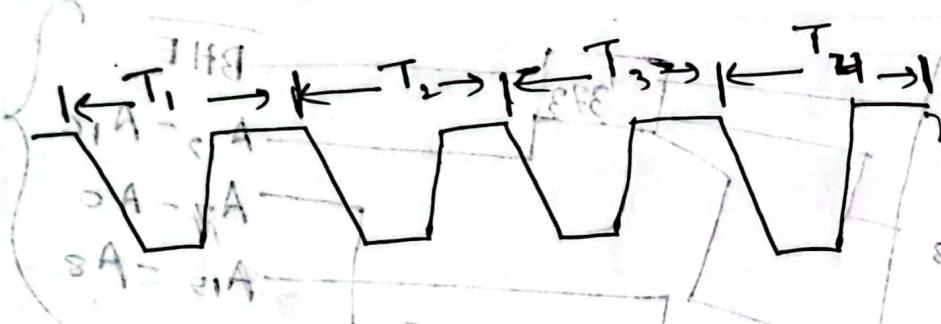
74245 - Octal bidirectional buffer



Bus timing & wait state

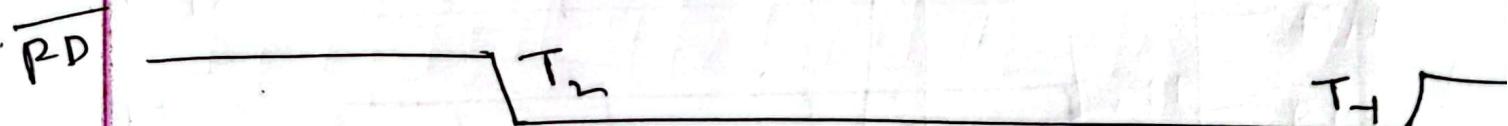
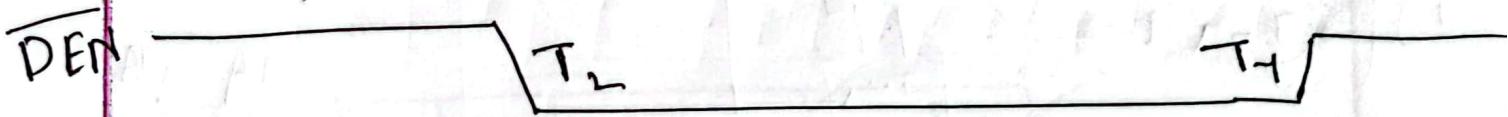
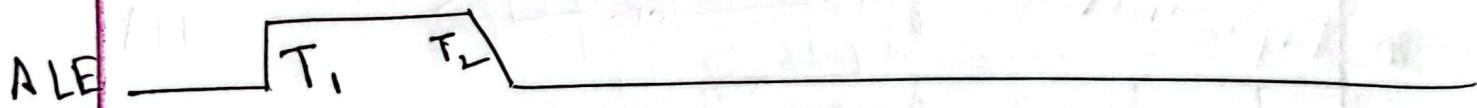
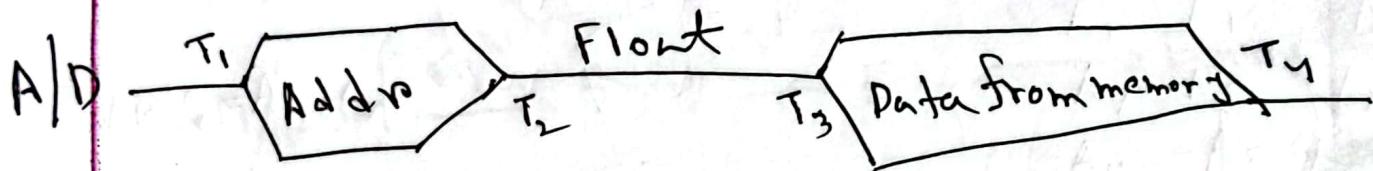
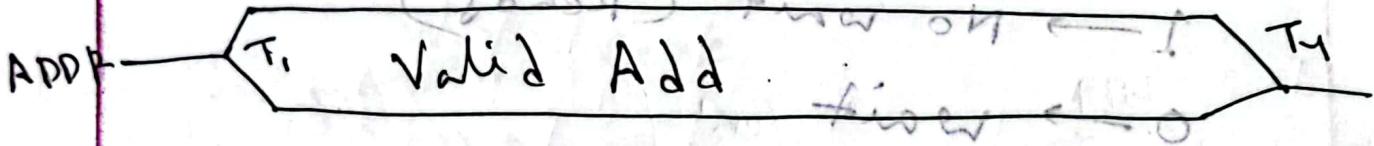
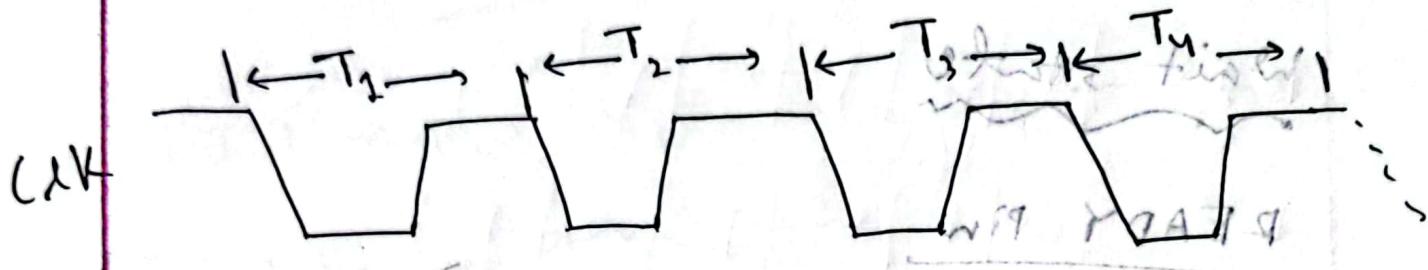
During

WP



RD

MAP and function of memory

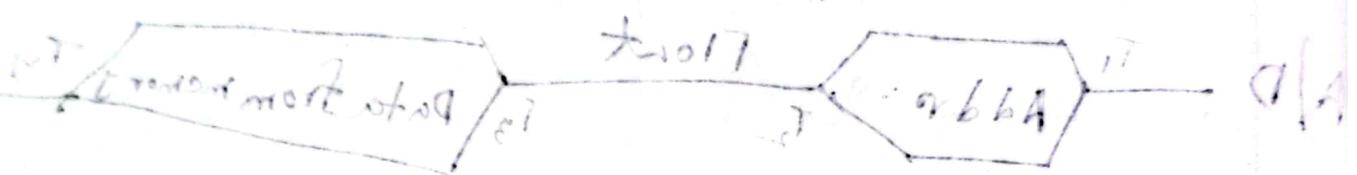


* Processor is faster than RAM.



1 → No wait (ready)

0 → wait



CW

Micro

~~Pipelining privilege trapping~~

BIU → Bus Interface unit (AB, DB)

EU → Execution Unit

Instruction queue

RAM/ROM → BIU → EU → Execute

decode

External
peripheral



BIU

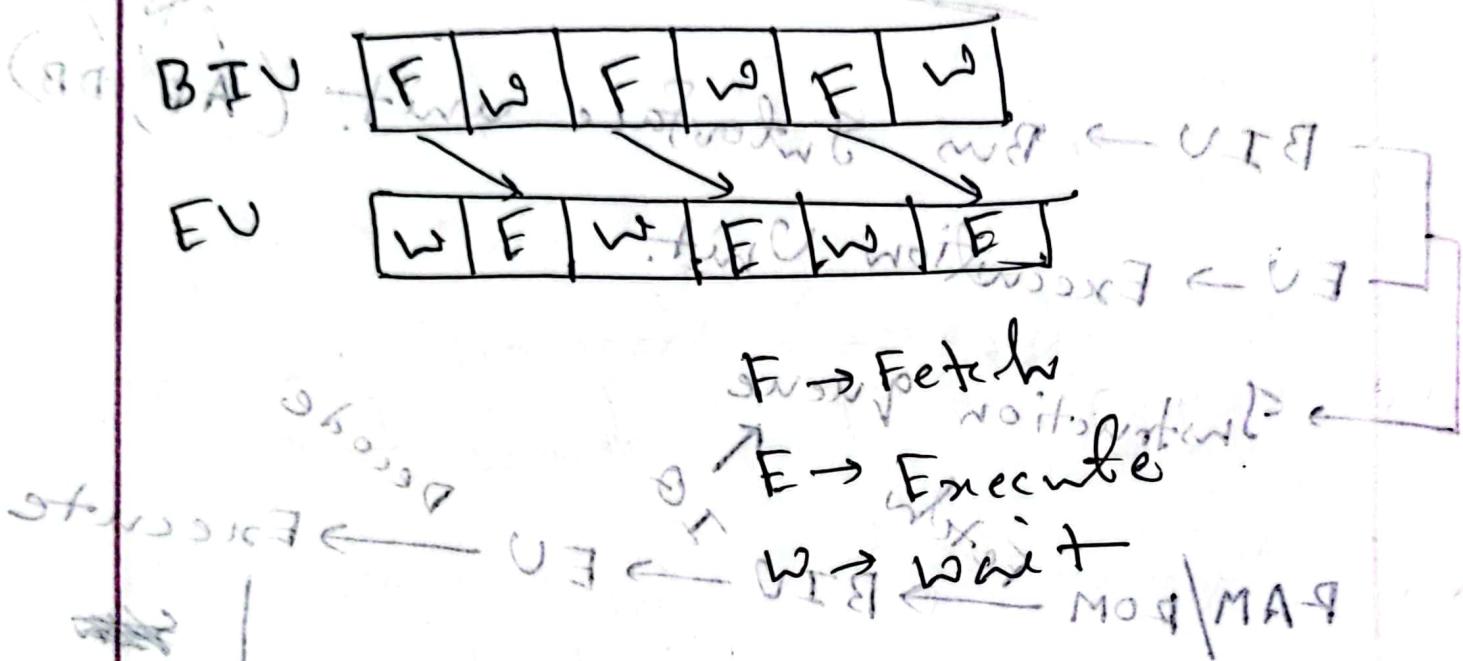


EU

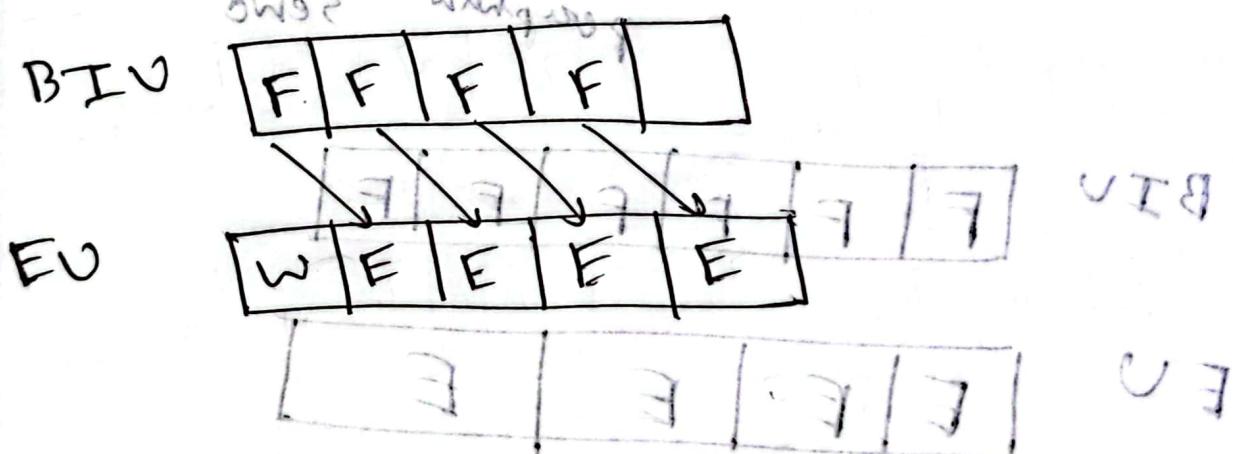


P.T.O

* without pipelining



* Pipelining

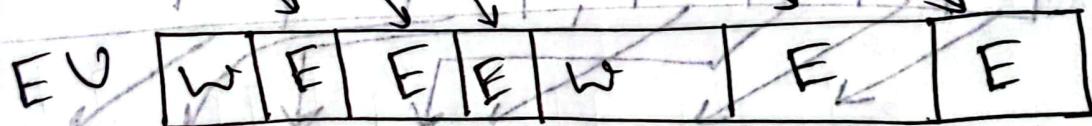


O.I.P.

* Memory Access



* Jump to Address



(b)

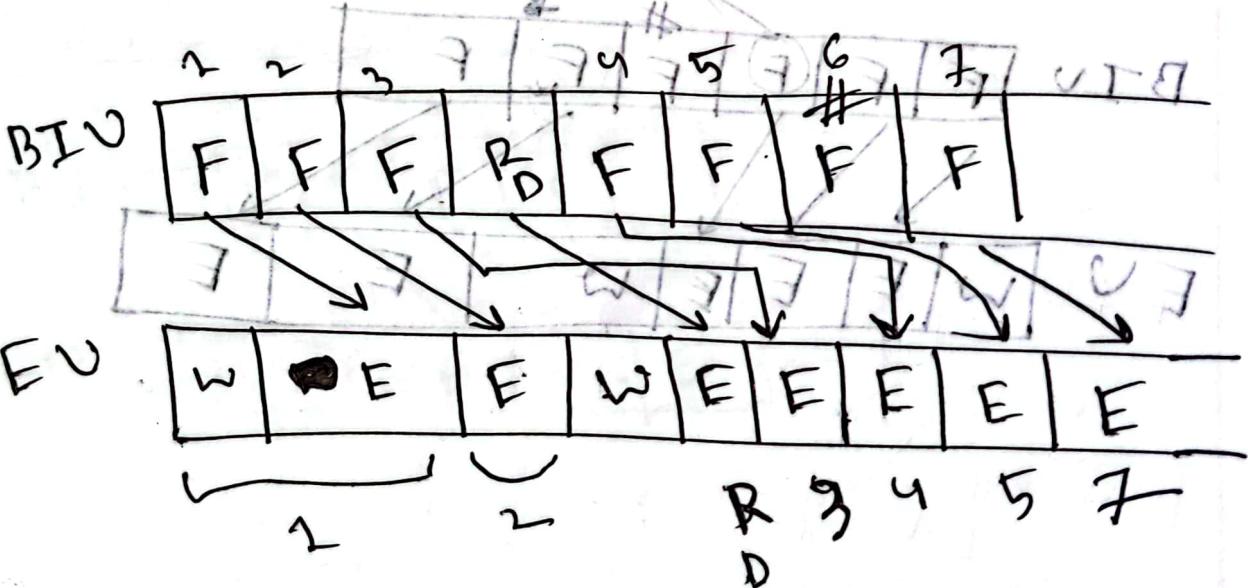
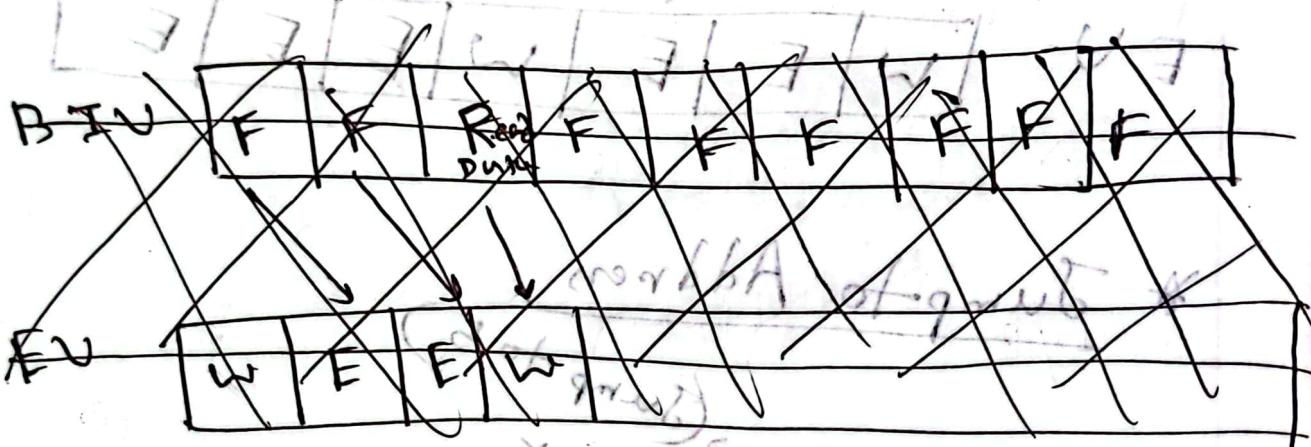
2nd Instruction

MOV [Address] → mem A from M

5th is Jump

7th address

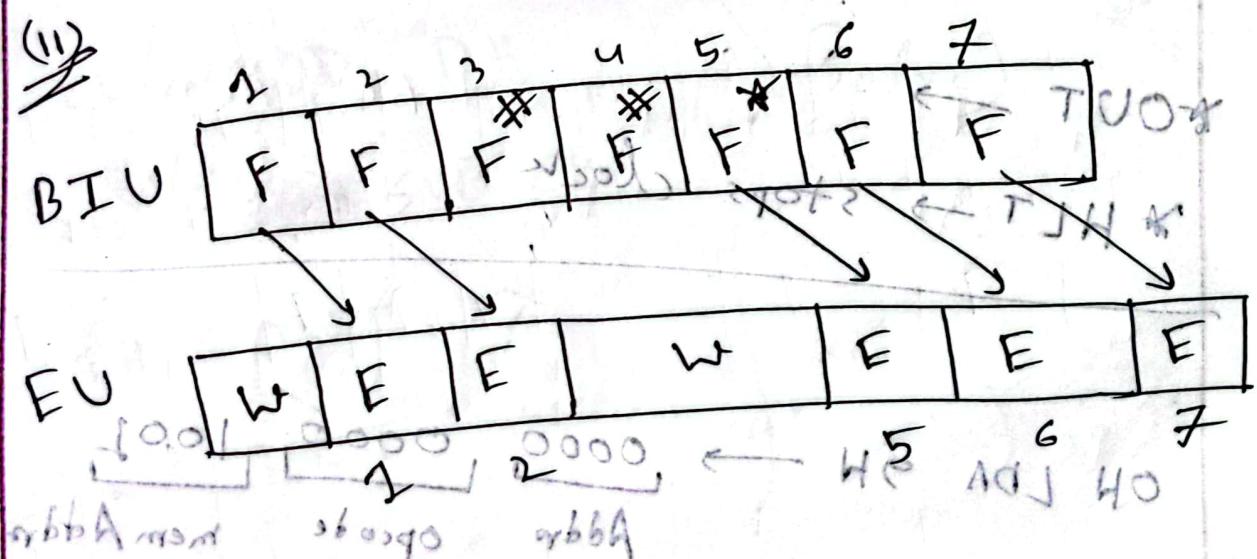
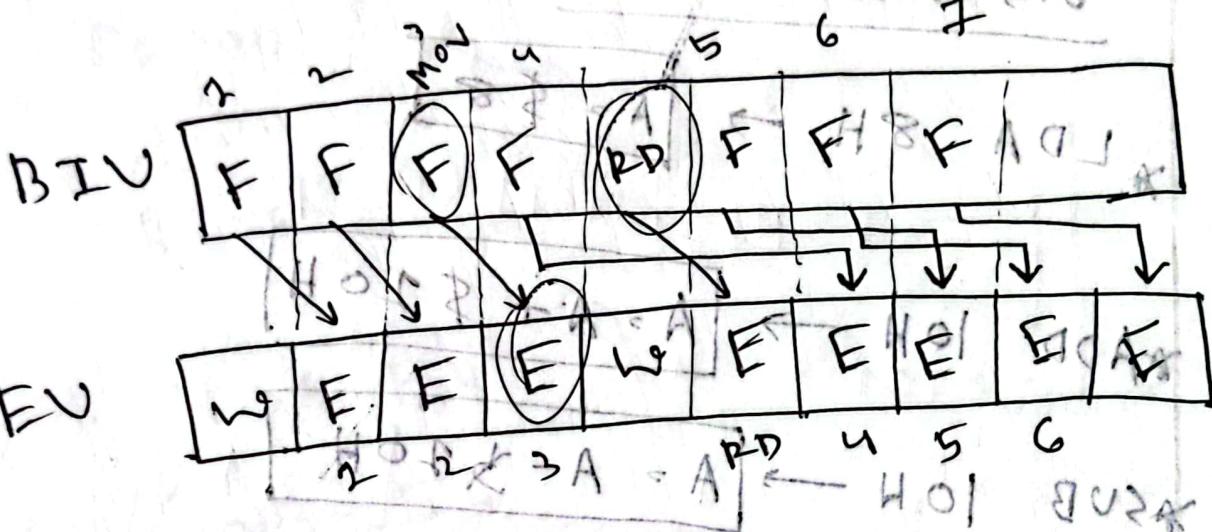
8



(5.9 AR)

~~Co~~ (writing) school of A sign is

(i) 3rd Sys (mov)



1101, 0100, 1000, ← BH 802, H5

XXXX, 0111, 0100, ← TVO H5

CW
11.9.24

(SAP-2)

Micro

Simple As Possible Computers

Instruction set

- * LDA 78H → $A = \$8$
- * ADD 10H → $A = A + \$10H$
- * SUB 10H → $A = A - \$10H$

- * OUT →
- * HLT → stops clock

OH LDA 9H → 0000 0000 1001,
 Addr opcode mem Addr

1H SUB BH → 0001 0010 1011

2H OUT → 0010 1110 XXXX

$$25 - 9 + 10 - 18 = 2$$

CH 18 D

DR 10 D

EH 9 D

FH 25 D

OH LDA FH
1H SUB EH

2H ADD DH

3H SUB CH

4H OUT XX

5H HLT XX

{Solve}

(G7)

HT

HT

8

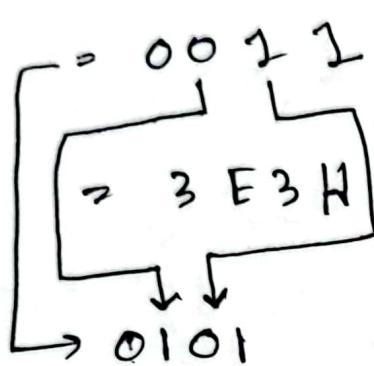
(G)

0 CCC

HT

Timing Stale $S = 81 - 01 \rightarrow 81 - 25$

$CON = C_P E_P \overline{L_M} \overline{CE} \quad \overline{L_I} \overline{E} \overline{I} \overline{A} F_A \quad S_U E_U \overline{L_B} \overline{L_O}$



1110 0011

[NOP] (No operation)

1110 0011

3 $\Rightarrow [T_2]$ 402 40

5 E

T_1 (PC & Input & M_{AP} Active High)
(E_P) ($\overline{L_M}$ high) 48

T_2 (PC (C_P) pin active high) 4N
4Q

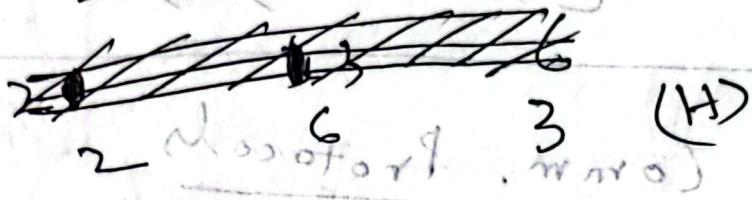
1011 1110 0011

B E C H

T₃

$(\overline{CE} \& \overline{L_I})$ active high
 permit and forward logic

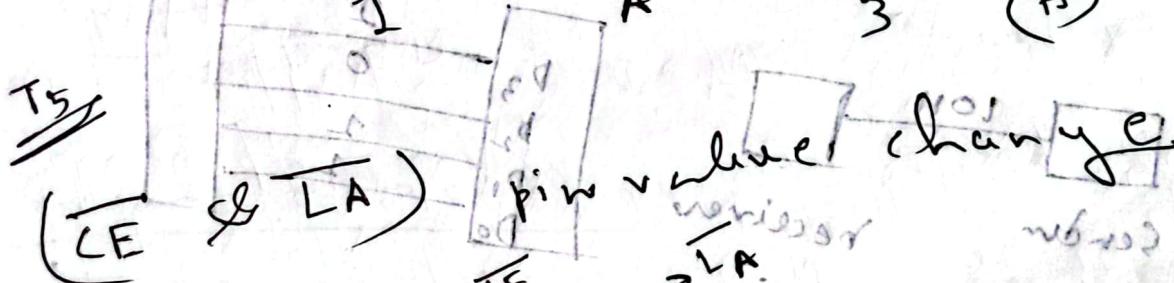
CON = 0010 (0110 0011
 shift)



T₄

Pin value change
 $(\overline{L_I} \& E_I)$ pin value driver

CON = 0001 (0110 0011
 shift)



T₅

$(\overline{CE} \& \overline{L_A})$

pin value change
 selector word

CON = 0010 (\overline{CE} 1100 0011
 shift)

2

3 (H)

T₆

$\{ T_6 = \text{NOP} \text{ [initial state]} \}$

C.W
17.9.24

Micro

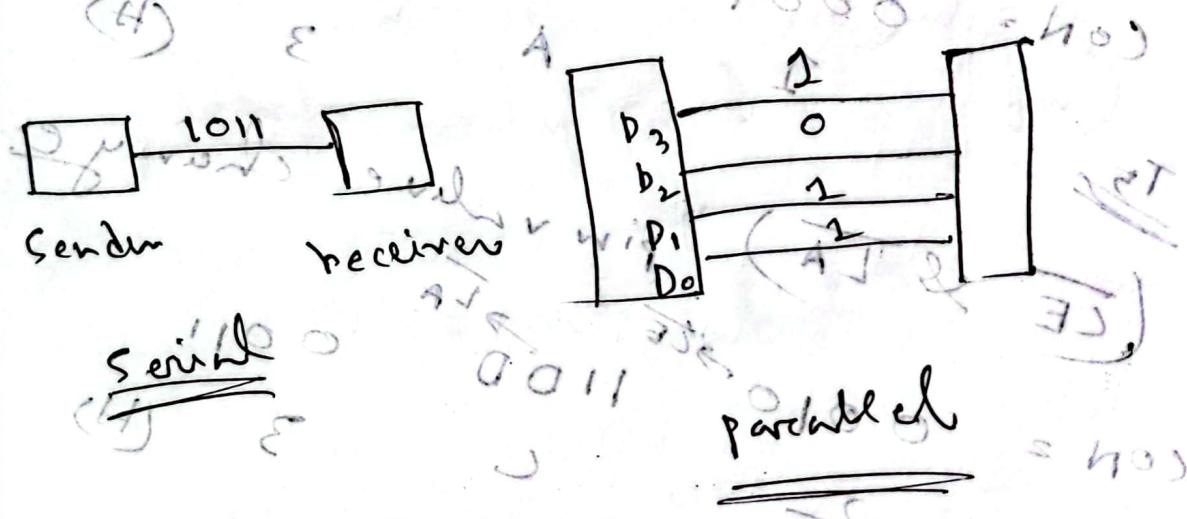
[24 sept - 24 C.T-3]

Pipelining + bus timing

(slide 2, 3), 1000 ns

Comm. Protocols

1. Serial (one bit at a time)
2. Parallel (multiple bits at the same time)



{ [shorter duration] 90ns] }

Parallel

→ speed (clock skew phenomenon)

→ length (Cross talk)

VART

USART

D₁₅
D₀



Parallel → Serial

TX

network & org

Serial Protocols

SPI (Serial Peripheral interface)

I₂C (Inter Integrated circuit)

Ethernet

O.T.I

SPI → 3 wires

I₂C → 2 wires (data, clock)

allowing
multiple
bus usage

* SPI

→ MISO (Master Receiver)

→ MOSI (Master Transmitter)

→ SCK (synchronizing)

data + x (transmission)

* 2 master allowed

* Master → micro controller

* Slave → Peripheral

(data, control, address, control lines)

P.T.O

terminal

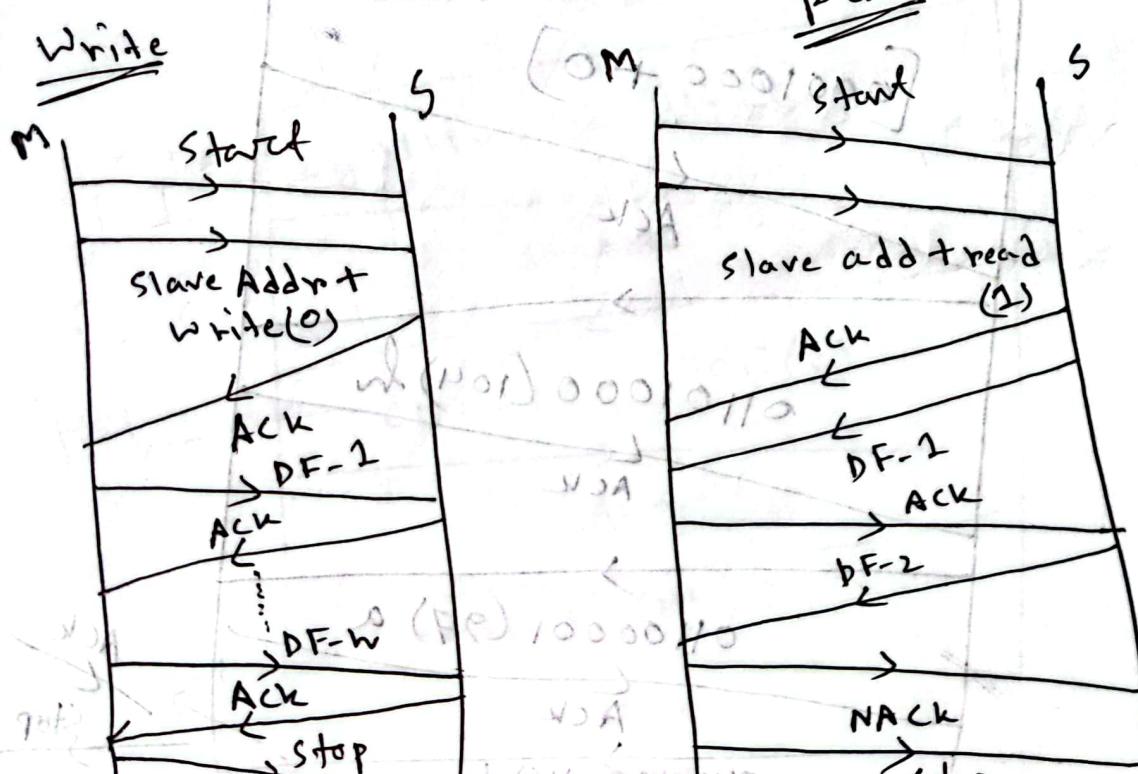
I₂C [exam important]

→ (7-10 bit) address

- * SDA (Serial Data) ↔ (bidirectional)
- * SCL (Serial Clock) → waveform

Start	7/10 bit Addr	Read	ACK	8 bit	ACK	8 bit	ACK	STOP
-------	---------------	------	-----	-------	-----	-------	-----	------

Address frame Data frame 1 Data frame 2



(Byte sequence) SCI

master send data → write

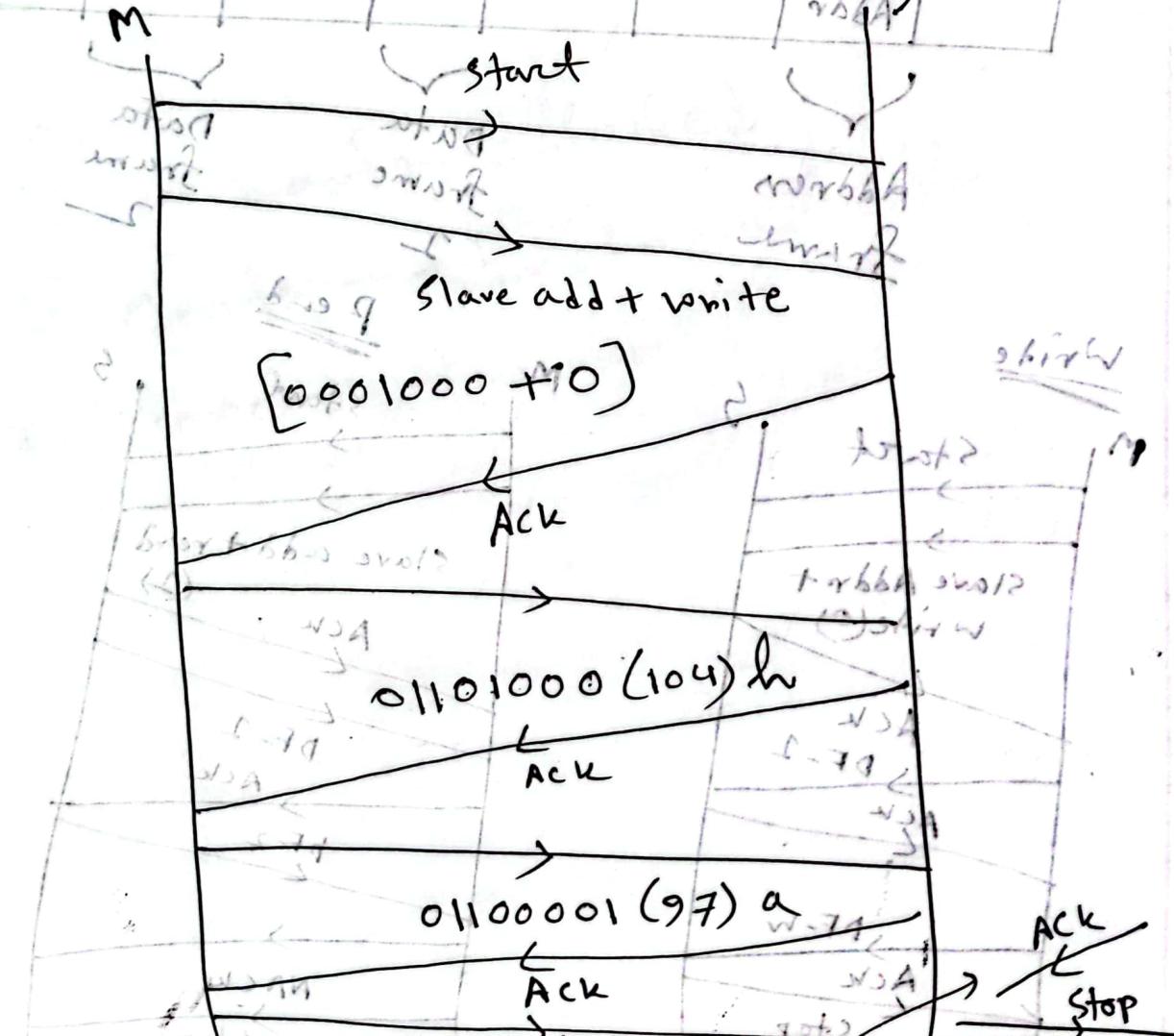
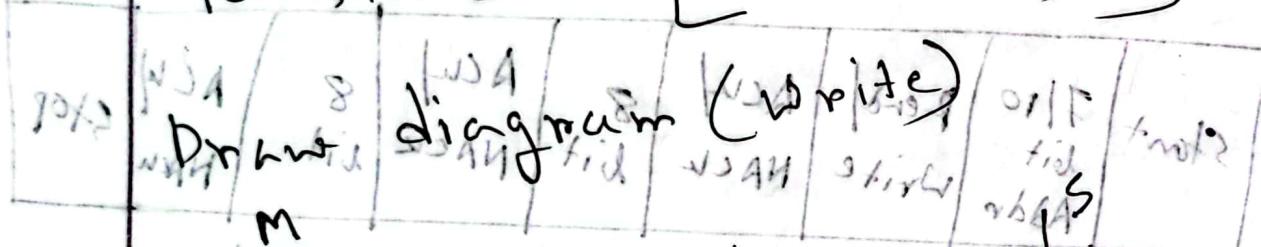
work (addr 01F) ←

receive → read

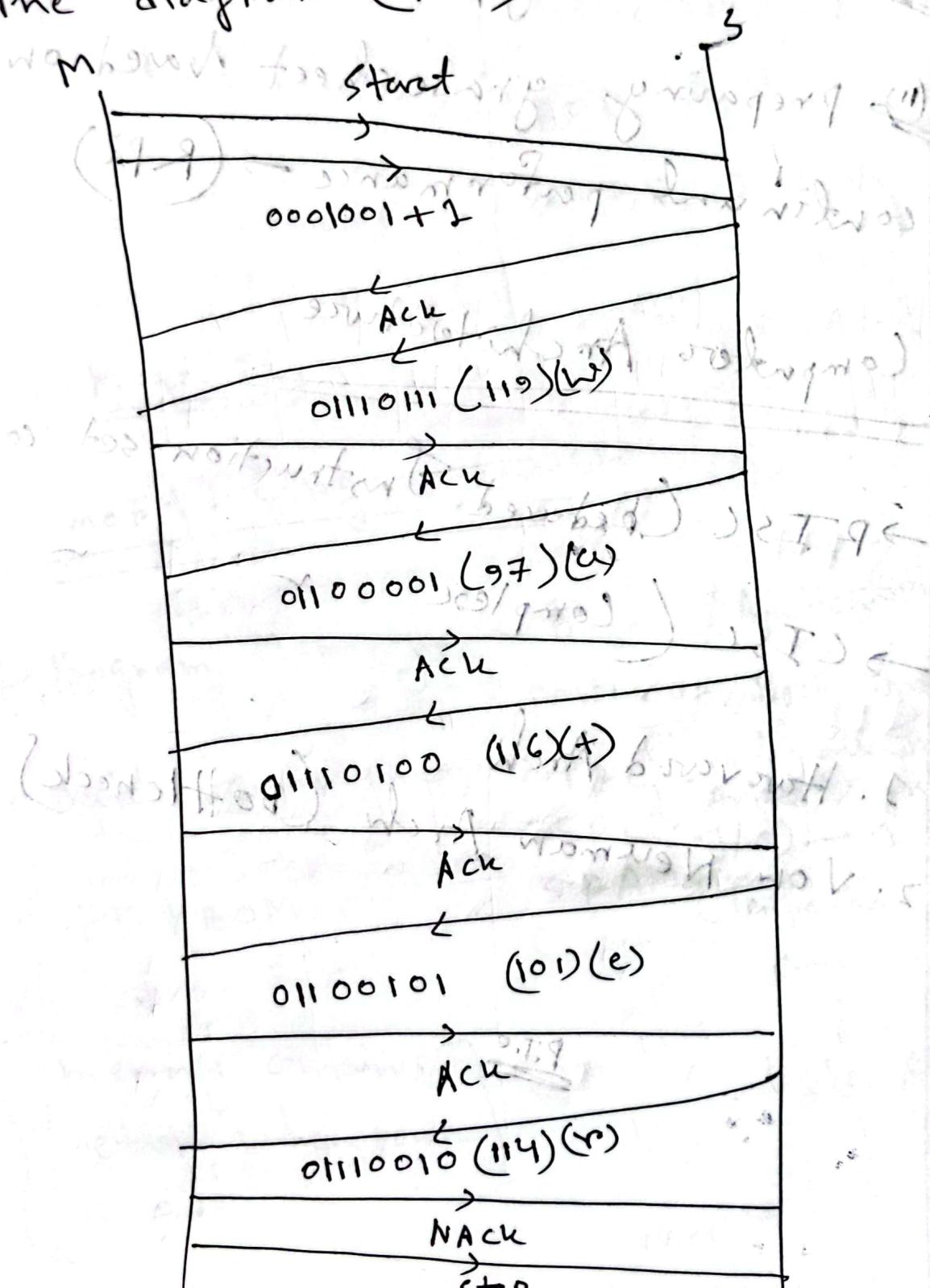
(start bit) ← (start bit) Add 8

master send data (char)

to slave at index (81H)



* Master receives 5 byte data ("water") from the slave (index: 0H). Draw the diagram (Read)



GW
21.9.24

Micro

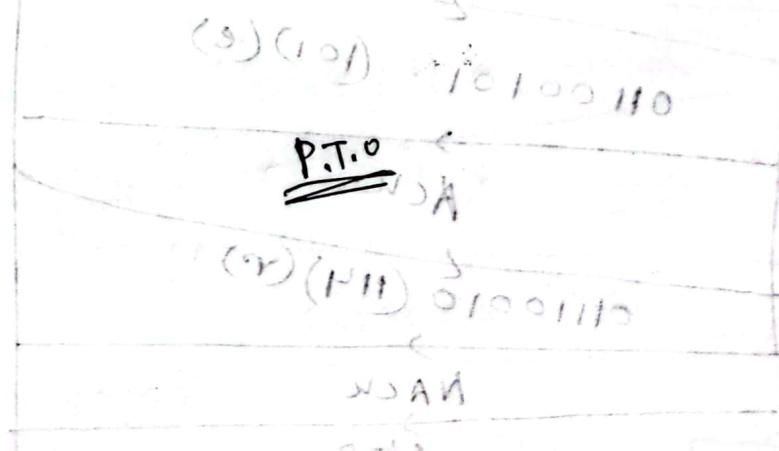
- (i) Microcontroller vision system *
- (ii) (and Scanning / Punch → (Arduino))
- (iii) Preparing gradesheet based on continual performance → (RPI)

Computer Architecture

→ RISC (Reduced Instruction set computing)

→ CISC (Complex Instruction Set Computing)

1. Harvard Arch
2. Von Neuman Arch (Bottleneck)



(Instruction word (I-bit))
CISC (Complex Instruction Set Computer)

MULT $2^3 \cdot 3, 5^2 \cdot 2$
(Complex operations)

(Result 80 bits/16V)

RISCA

LOAD A, g_0, g_2, g_3, A same length

LOAD B, g_0, g_2, g_3, B

PROD A, B

STORE $2^3, A$, g_0, g_1, g_2, g_3, A

ATMega 32

Memory - Organization

1. Program Memory → Program / Application codes
↓
power on / Boot Instruction
2. Data Memory →
 - Registers (Used by all Ins)
 - SFRs (Arith / logic)
SFRs \rightarrow (g1/g0) \rightarrow 1 byte
 - SRAM (Temporary storage)
3. EEPROM

memory contains
retain when power
is off

Byte Addressable

Q.W
28.7.21

Micro

- ADC → (light, sound, distance)
→ Analog sensor (continuous data)
→ Digital sensor (discrete data)
A/D → (Voltage level)

Analog sensor

- Thermistor, LDR

Digital sensor

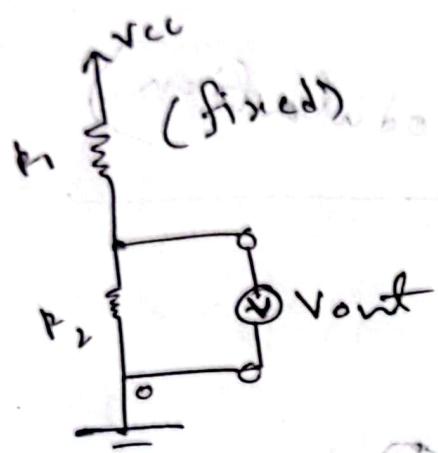
- PIR, Ultrasonic

LDR sensor

resistance \downarrow depends on light intensity \uparrow
depends on light intensity \uparrow

P.I.O

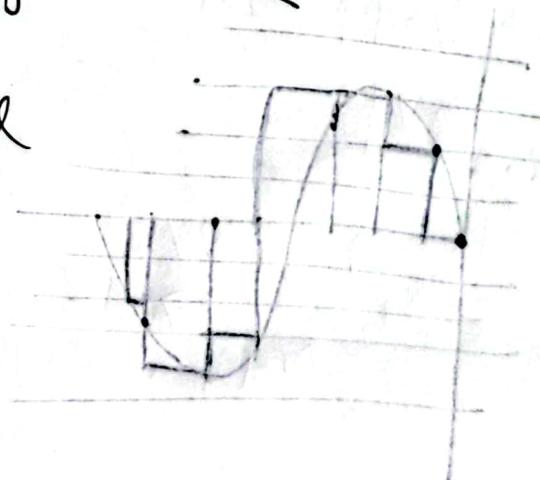
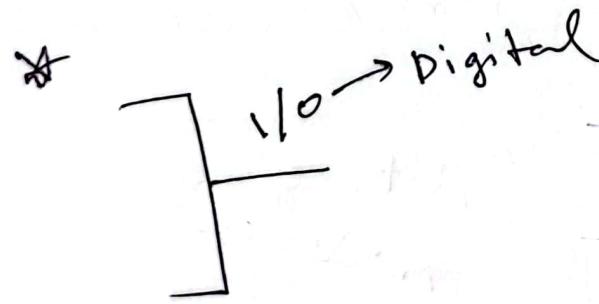
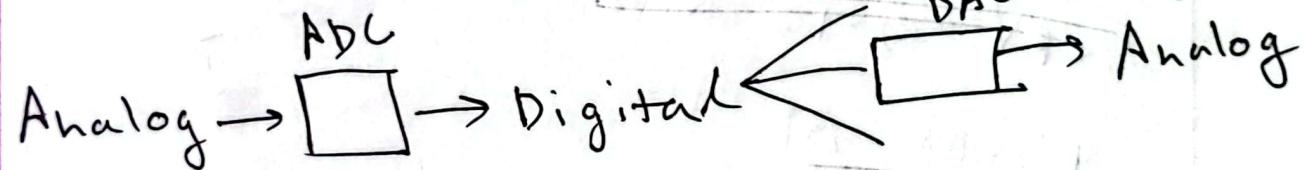
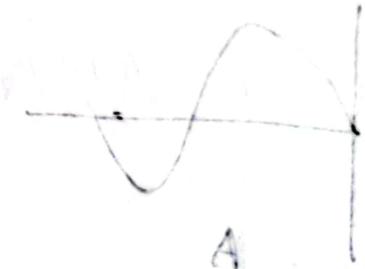
{ resistance from
new value resistor }
{ new value resistor }
R₁ = 10KΩ



$$V_1 = \frac{R_1}{R_1 + R_2} V_{cc} - A$$

$$V_2 = \frac{R_2}{R_1 + R_2} V_{cc} - B$$

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{cc}$$

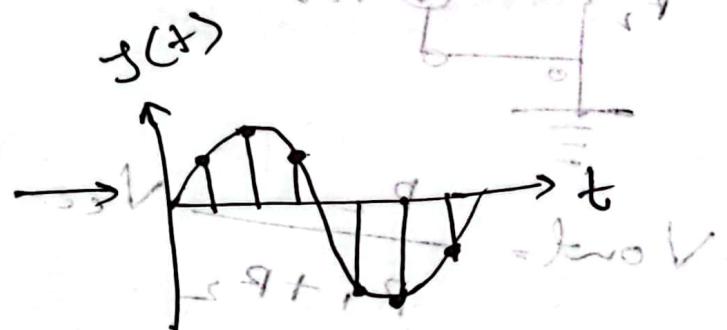
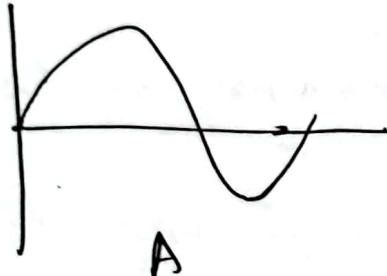


P.T.O

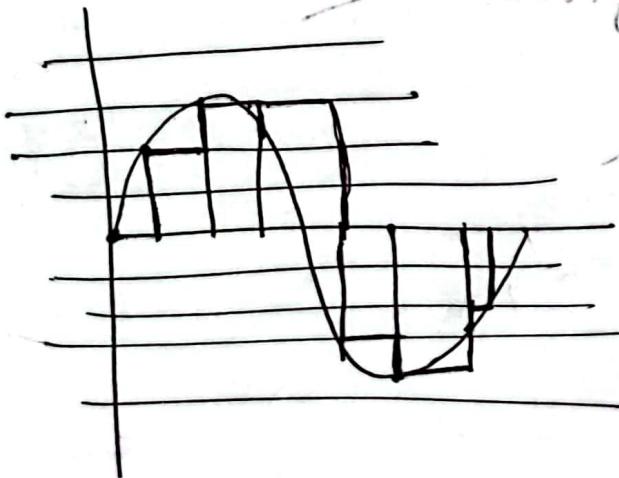
A → D

PCM (Pulse Coded modulation)

→ Sampling



→ Quantization

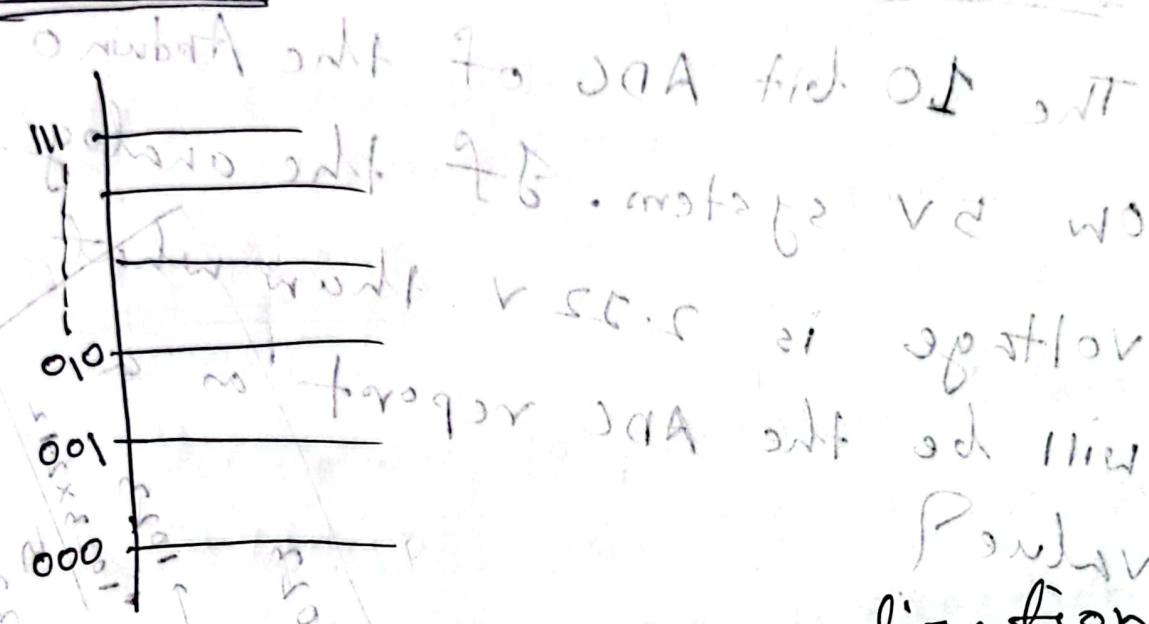


Quantization



2.7.9

Encoding



3 bit resolution of quantization.

$$3 \text{ bit ADC} \rightarrow 2^3 = 8 \text{ D/A block}$$

$$10 \text{ bits} \rightarrow 2^{10} = 1024 \text{ D/A block}$$

$$16 \text{ bits} \rightarrow 2^{16} = 65536 \text{ D/A block}$$

V.A D/A to waveform

$$\frac{\text{P.T.O}}{\text{Digital}} \text{ D/A} = \frac{\text{ESOT}}{2}$$

$$\text{P.E.P} = [52F.88P] = \text{D/A} = 8$$

→ Question

The 10 bit ADC of the Arduino
on 5V system. If the analog
voltage is 2.12V then what
will be the ADC report as a 10bit
value?

→ ~~V_{CC} = 5V~~

A.V = 2.12V

10 bit ADC

ADC =

$$\frac{\text{Resolution of ADC}}{V_{CC}} = \frac{A.P}{A.V}$$

$$\Rightarrow \frac{1023}{5} = \frac{ADC}{2.12}$$

$$\Rightarrow ADC = \lceil 433.752 \rceil = 434$$

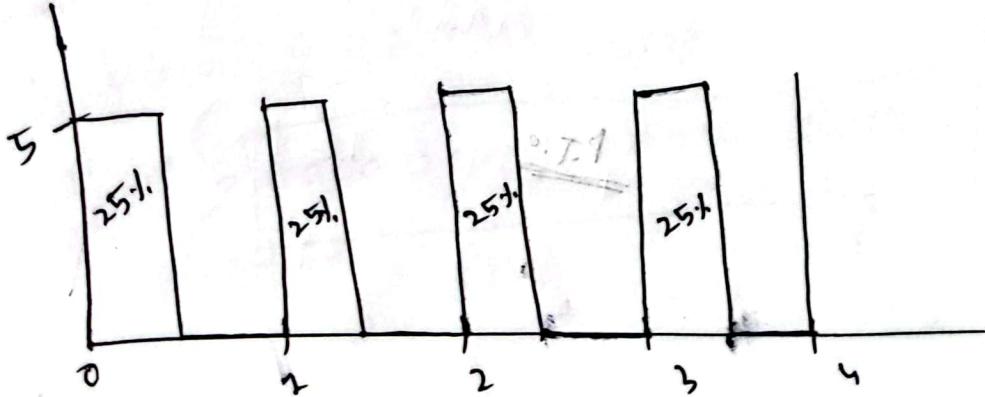
D → A

PWM (Pulse Width Modulation)

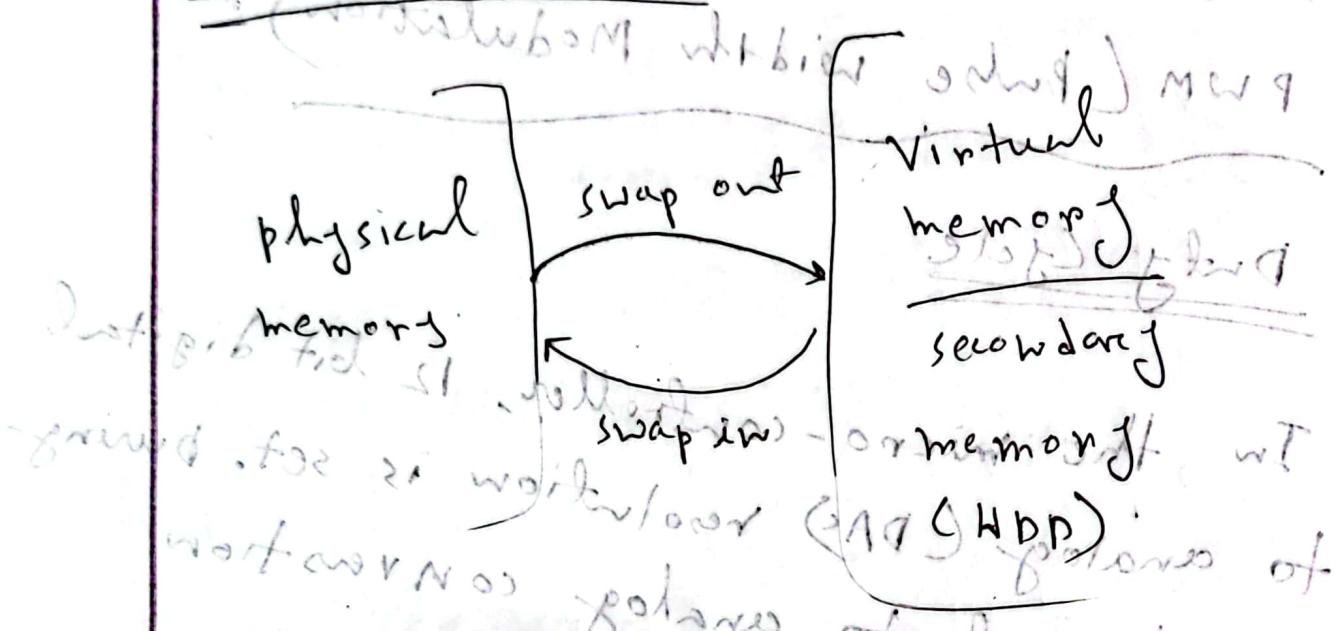
Duty Cycle

In the micro-controller, 12 bit digital to analog (D/A) resolution is set. During the digital to analog conversion programming, you have called "analogWrite(1024)" instruction. Calculate the duty cycle. Draw the duty cycle diagram. Consider 5V.

$$\rightarrow \frac{1024}{2^{12}} = 25\%$$

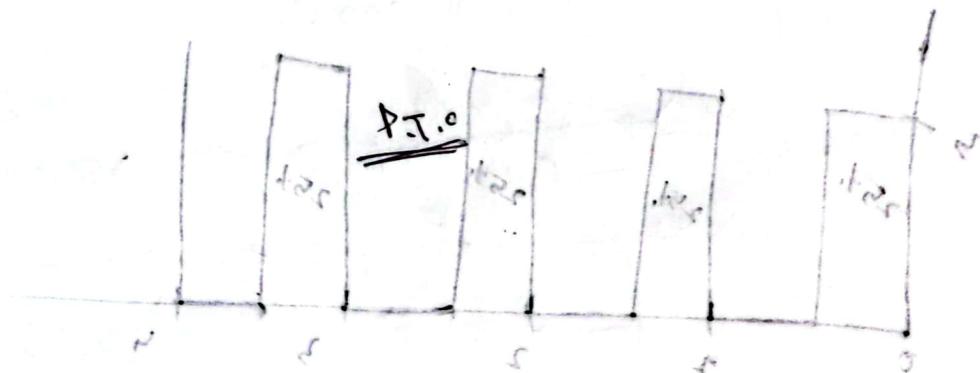


Protected mode



Advantages of Virtual memory with protection

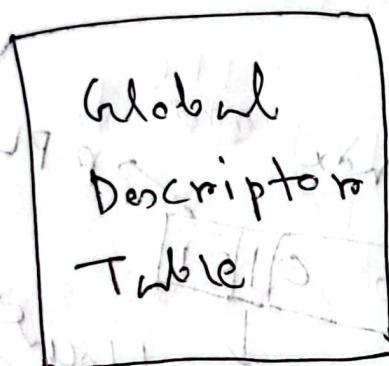
- Solve limited physical memory size.
- Solve discontinuous memory address problem.
- Provide program protection.



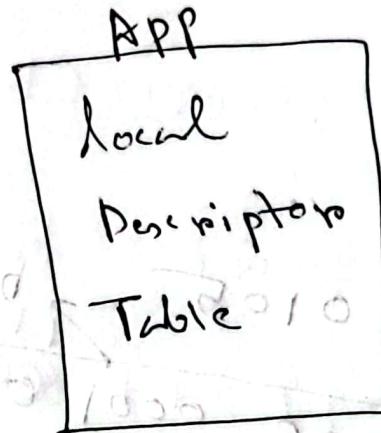
* Protected mode (80286)

→ Segment Register
→ Descriptor

Desc. Index	TI RPL
13 bit	16 26



TI = 0



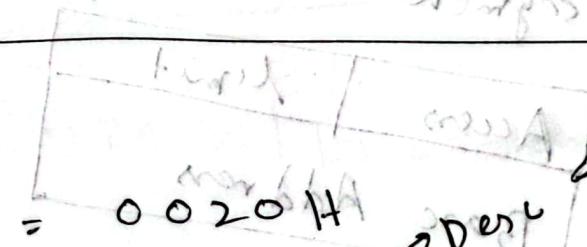
TI = 1

00 High (Kernel)

11 Low (APP)

Math

$$20. DS = 0020H$$



0000 0000	0010 0000	0000	RPL
-----------	-----------	------	-----

0000 0000	0010 0000	0000	RPL
-----------	-----------	------	-----

0000 0000	0010 0000	0000	RPL
-----------	-----------	------	-----

$$20. DS = 0020H$$

58 ← 28 & 08

3^o

DS = 0103

→ 0000 0001 0000 0011

RPL

3¹

DS = 0105

base index

RPL

→ 0000 0001 0000 0101

20(H)

TI (lock)

32(D)

Descriptor Table

segment descriptor

Access	limit
Base Address	

80286 → 24 bit (16M)

80386 → 32 bit (4G)

bit (Granularity bit) \rightarrow 1

$$2^9 \rightarrow 2^9 (1M) \rightarrow \boxed{1 \times 4K} \rightarrow 1M$$

$$\text{Base} = \text{start} = 10000000H$$

$$\text{Limit} = 001FF H$$

$$Gr = 0^9 = 512 \text{ bytes}$$

$$\text{End} = \text{Base} + \text{Limit}$$

$$= 100001FF H$$

$$\text{Segment Size} = |\text{End} - \text{Base}|$$

$$= |\text{limit}| = 9 > 2^9$$

$$= 512 \text{ bit}$$

$$6 = 2 \quad \text{End of first paragraph} \rightarrow 2^2 + 2^1 = 2^3 = 8$$

$$\text{End} = \text{Base} + \text{Limit} \times 4 \text{H}$$

$$= 1000 \text{H} + (0000 \text{H} + 02 \text{FF} \times 1)$$

$$= 10000000 \text{H} + 1 \text{FF} \cancel{\text{H}}$$

$$= 101 \text{FF} \cancel{0000} \text{H} = \text{first 8 bytes}$$

Segment size = 21 = 20 = 16 bit

first + next = 64B

10000000

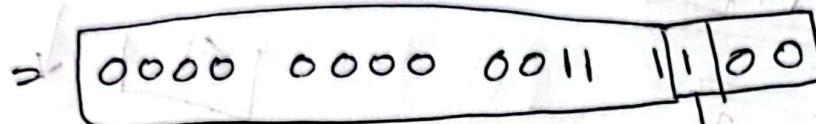
length - 64B = 512 bytes

size of first =

first + next = 64B

~~F. + M~~

$$DS = 3C H$$



7H

found

$$\text{Base} = \text{start} = B5 0000 H$$

$$\text{offset} = 10 H$$

$$\text{End} = \text{Base} + \text{limit}$$

$$\Rightarrow B5 0000 + 0FFF$$

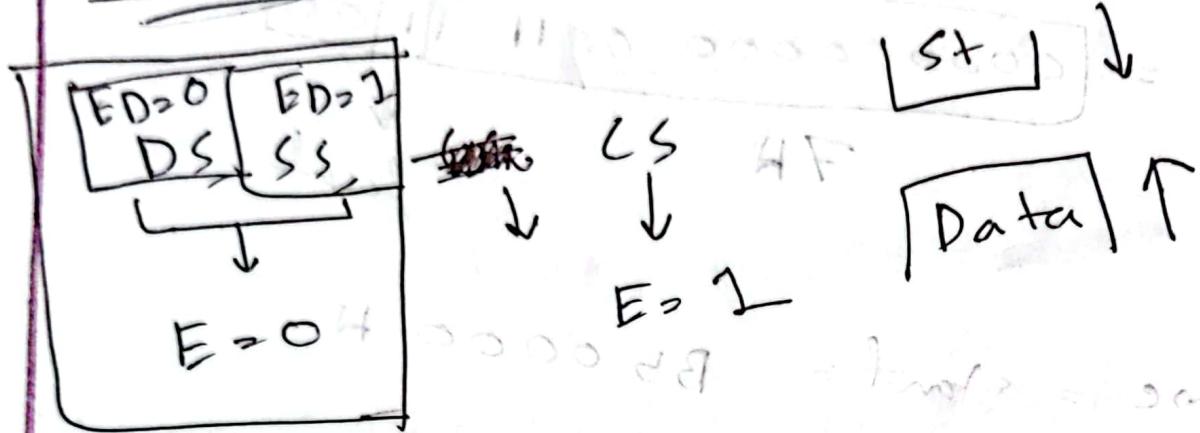
$$\Rightarrow B5 \text{ OFFF } 1100$$

$$\text{Physical memory} \rightarrow \text{start} + \text{offset}$$

$$\Rightarrow B5 0000 + 10 H$$

$$= B5 0010 H$$

Access rights



Exm

$$L_{15} - L_0 = 0$$

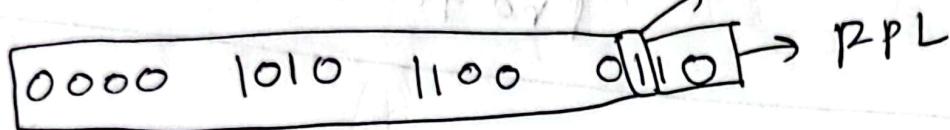
$$L_{15} - L_0 = 00FF \text{ H}$$

$$\text{Base} = 1000000000 \text{ H}$$

Access right byte = 92 H

Ques 1

~~12 ALC~~



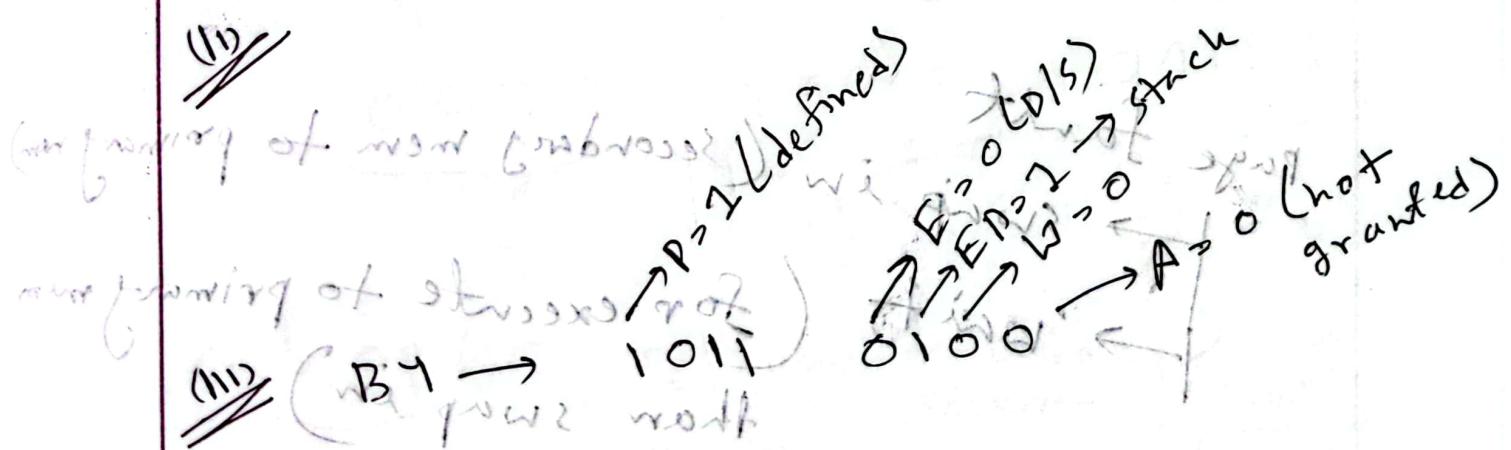
158 H

Base = $2A00E + 2A00E$

$$\begin{aligned} \text{End} &= (002A00E + 2A043H) \times 2 \\ &\rightarrow (002A00E(H)) + 2A043H \end{aligned}$$

~~1000D
FFFN~~

2 ~~for 1st 16 bits~~



symbol → ADC

protected

CPU
5.10.25

Paging

HR 21

Micro

Physical Address → Actual memory location

linear addr → Address generated by a program

Fixed size pages

OS → Page table

Page fault

→ swap in (secondary mem to primary)
→ wait (for execute to primary mem than swap in)

SAP-1 (control-pin)

Add operation

$$T_4 = C_p E_p \overline{L}_M \overline{CE} \overline{L}_I \overline{E}_I \overline{L}_A E_A S_u E_u \overline{L}_B \overline{L}_o$$

$$= \underbrace{0001}_{1} \quad \underbrace{1010}_{A} \quad \underbrace{0011}_{3(H)}$$

$$T_5 = C_p E_p \overline{L}_M \overline{CE} \overline{L}_I \overline{E}_I \overline{L}_A E_A S_u E_u \overline{L}_B \overline{L}_o$$

$$= \underbrace{0010}_{2} \quad \underbrace{1110}_{E} \quad \underbrace{0001}_{1(H)}$$

$$T_6 = C_p E_p \overline{L}_M \overline{CE} \overline{L}_I \overline{E}_I \overline{L}_A E_A S_u E_u \overline{L}_B \overline{L}_o$$

$$= \underbrace{0011}_{3} \quad \underbrace{1100}_{C} \quad \underbrace{0111}_{7(H)}$$

Sub op (T_4, T_5 same as add op)

$$T_6 = C_p E_p \overline{L}_M \overline{CE} \overline{L}_I \overline{E}_I \overline{L}_A E_A S_u E_u \overline{L}_B \overline{L}_o$$

$$= \underbrace{0011}_{3} \quad \underbrace{1100}_{C} \quad \underbrace{1111}_{F(H)}$$