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WC640 Datasheet

MCU Embedded Wi-Fi 802.11 a/b/g/n + Bluetooth 5.0 + 802.15.4 (ZigBee) Module with Integrated Antenna

Revision 1.0
March 21, 2020

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Revision History:

Revision	Revision Date	Originator	Changes
1.0	Mar 21, 2020	SF	Initial version Datasheet

1. Overview of WC640

WC640 series is Wi2Wi's first MCU Embedded, Multi-Protocol (Tri-mode), highly integrated plug and play module with Dual Antenna on-board. With embedded microcontroller(s), WC640 module series is a complete wireless sub-system with multiple wireless technologies: Dual Band (2.4/5GHz) Wi-Fi, Bluetooth 5.0 (BLE), 802.15.4 (Zigbee) making it a perfect candidate for a vast variety of applications, including Internet-of-Things (IoT), Industrial IoT (IIoT), M2M, etc. This is low power host-less Internet of Things (IoT) wireless module offering multiple radios, wireless standards, protocols and connectivity framework support. WC640 multi radio embedded wireless module supports advanced seamless coexistence across multiple wireless technologies. Multi-core processing for optimized performance with a dedicated ARM Cortex-M4F processor for customer applications reducing development cost & efforts, which accelerates their time-to-market and low power ARM Cortex-M0 CPU dedicatedly used for BLE/802.15.4 protocol and Xtensa-based Wi-Fi CPU to offload Wi-Fi stack. WC640 host-less module is a subsystem that includes two antennas, baseband, LNA, PA, crystals, filter, RF front-end and flash for storing Firmware/s, calibration data, MAC addresses. WC640 self-contained wireless sub-system supports interfaces SPI, UART, I2C, PWM, I2S, ADC and GPIOs for external peripherals.

1.1 Features

- Dimensions: 30.5 mm x 20.5 mm x 1.86 mm
- WC640 tri-mode integrates Bluetooth 5.0 (BLE), Dual-Band Wi-Fi and 802.15.4 technologies
- Supports advanced seamless coexistence across multiple wireless protocols (Wi-Fi / Bluetooth / 802.15.4)
- IEEE 802.11 a/b/g/n Wi-Fi (20/40MHz bandwidth)
- Supports Station, Access Point, Con-current (simultaneous AP + Station) and Wi-Fi Direct Modes.
- Supports Open, WPA/WPA2-PSK, WPS & WEP
- Supports 10 Stations/Clients in AP Mode
- Supports 16 TCP/UDP sockets
- Maximum Wi-Fi transmit power up to 18 dBm
- Wi-Fi Receive Sensitivity -97 dBm
- Supports single mode Bluetooth version 5 (BLE)
- Supports MESH protocol
- Bluetooth Modes: Central, Peripheral
- 802.15.4 Zigbee/Thread
- Onboard 2 Trace Antennas
- Single power supply operation, 3.3V DC
- Operating temperature Industrial grade (-40℃ to +85℃)

The WC640 module contains three processors. The first is an ARM Cortex-M4F, used as the application, or host processor. It runs the networking stack as well as OEM application code. The second processor is an ARM Cortex-M0, which is used as the connectivity control processor for the

BLE and 802.15.4 subsystems. The third processor is XTENSA7 running at 130MHz, which is a dedicated processor to run the Wi-Fi dual band function.

There are multiple advantages to the multiple processor configuration:
- Wi-Fi, BLE and 15.4 code has a known execution environment without generating competition for processor resources from customer code.
- The execution environment of code is easier to separate from customer code from a security perspective.

1.1.1 Wireless interfaces

The WC640 implements three wireless subsystems on-chip, and supports a master and slave configuration:
- 1x1 dual band 802.11abgn Wi-Fi function
- Bluetooth Low Energy (BLE) compliant to the SIG v5.0 specification.
- IEEE 802.15.4 compliant to the v2006 specification and also featuring Coordinated Sample Listing (CSL) from the 802.15-2015 specification.

1.1.2 Wi-Fi Link

Wi-Fi link is a full-featured, dual-band, single stream 802.11n solution. The Wi-Fi link is highly integrated, and includes an energy efficient on-board power amplifier and LNA.
- Green Tx power saving mode
- Low power listen mode
- Data rates up to 150 Mbps
- Full security support: WPS, WPA, WPA2, WEP.

1.1.3 System cost optimization

The WC640 is optimized for low system cost, and minimizes the number and cost of any components required to achieve a
- Reliable
- Highly Integrated Wi-Fi solution
- RF link does not need any external matching components
- Integrated IPv4/IPv6 TCP/IP stack
- Integrated Network services such as HTTP, DNS, FTP
- Small Form Factor 30.5 mm x 20.5 mm x 1.86 mm
- Firmware is stored and automatically loaded from on-board serial flash memory

1.1.4 Manufacturing

- USB 2.0 device interface, providing a simplified, high-speed, and scalable manufacturing test and configuration interface for WC640-based systems, using an integrated controller and PHY

1.2 Standard Interfaces

The following additional I/O interfaces are provided by WC640.

- 1 SPI Master and 1 SPI Slave interface
- 1 UART and 1 high-speed UART interface
- 1 I2C interface
- Up to 6 of PWM for LED lighting application
- Keypad interface
- JTAG debug port

NOTE: Some of the above interfaces have dedicated pins while most are configurable using the programmable GPIOs. This allows various configurations covering a wide range of applications while maintaining a small footprint.

1.2.1 GPIO

WC640 GPIO pins are fully configurable. They are shared with other interfaces such as I2C, SPI, and serial flash. Pin Description provides the set of pin configurations options. Each of the GPIO pins supports multiple configurations via Internal pull-up/down options.

1.2.2 UART interface

WC640 includes one Universal Asynchronous Receiver/Transmitter (UART) and one High-Speed UART interfaces, which might be configured to serve as either a host interface link or a debug message console and other one for any kind of sensor data.

- **UART**: UART_0 supporting baud-rates are 300, 4800, 9600, 115200 by default it is set to 115200 bps.
- **HS-UART**: UART_1 is a High Speed UART and its supporting baud-rates are 4800, 9600, 115200, 500000, 1000000, 2000000, 4000000 bps.

By default, both the UARTS are set in 115200 bps baud.

Other Setting:
Data bits   : 8
Stop bits   : 1
Parity   : None

1.2.3 SPI Interface

WC640 supports 2 SPI interfaces, one as SPI Slave and the other as SPI Master.

- When SPI is in slave mode, the WC640 is ready to be driven by an external Host processor and it support Max clock frequency up to 50MHZ.
- When SPI is in Master mode, any SPI slave peripheral can be connected to WC640 and the maximum clock frequency supported by WC640 is 24 MHz.

1.2.4 I2C Interface

WC640 supports one I2C interface and I2C core supporting Clock is 20 MHz

1.2.5 Keypad

WC640 supports 4X4 keypad using the GPIO pins. User can configure and dedicate pins for an external Keypad connection.

1.2.6 PWM

PWM interface available with handles to configure duty cycle and frequency. This configurable PWM can be used for multiple applications.

1.2.7 JTAG

The WC640 has dedicated pins for connecting a JTAG. JTAG is used for establishing a connection between the Host PC and the WC640 module, for software development and debugging purpose.

1.2.8 RESET Power up/down sequencing

The RESET# is the reset pin, and all supplies should be stable for a minimum of 10 µs before RESET# is de-asserted. If VIO = 3.3V, then VDDA, VIO_BE and VIO_WL can share same 3.3V power rail.
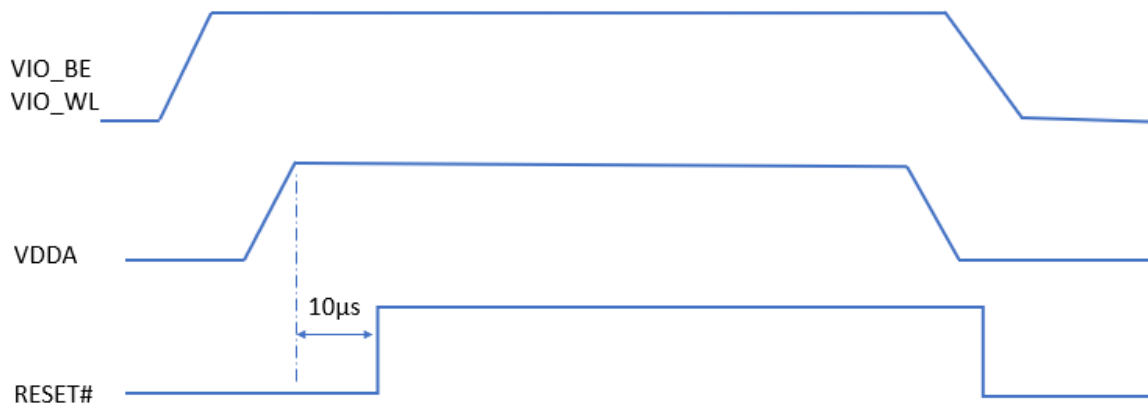
Figure 1 RESET Timing

1.3 Power transition

The WC640 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed.
- Shutting down unneeded high-speed clock sources
- Reducing voltage levels to specific blocks in some states

1.4 System clocking

1.4.1 Low-speed clocking

The WC640 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states.

2. Block Diagram

WC640 core block includes a high-performance IEEE 802.11 a/b/g/n + BT5 / 802.15.4 SOC with integrated antennas. This module has built-in MCU which enables the user to write their applications on to it directly without an external HOST. This highly integrated module has multiple GPIOs, UART, I2C, I2S, PWM, SPI and Keypad ready interfaces for any external peripheral loads. A master Reset pin can be used to completely reset the module. It requires a single power source of 3.3V. This module has dual trace antenna for multiple protocols. An external RF pad is also available on the module exclusively for user convenience. Dedicated USB and JTAG interfaces for debugging and flashing purpose with new firmware/s. This module also can be driven by an external Host through UART/SPI interfaces.

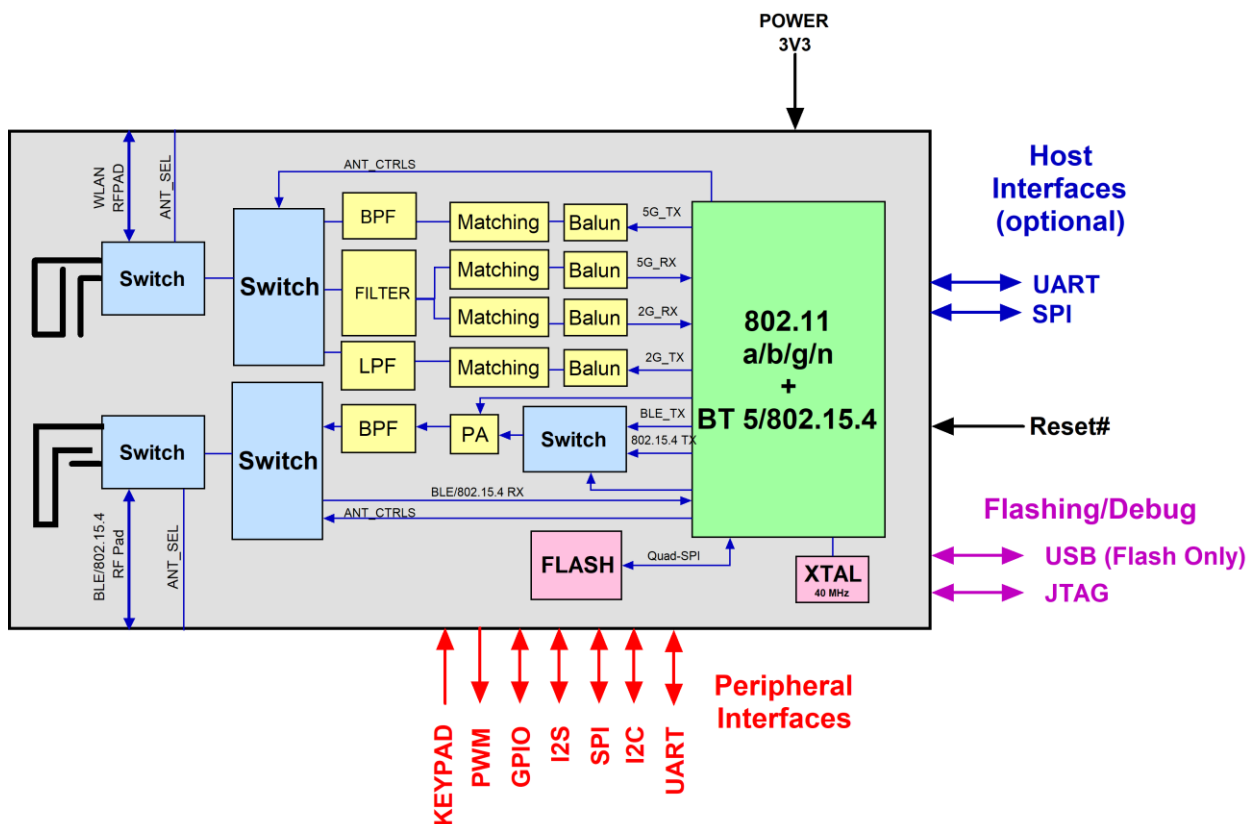Figure 2 figure shows a block diagram of WC640 module.

Figure 2 : Block Diagram

3. Pin Diagram of Module

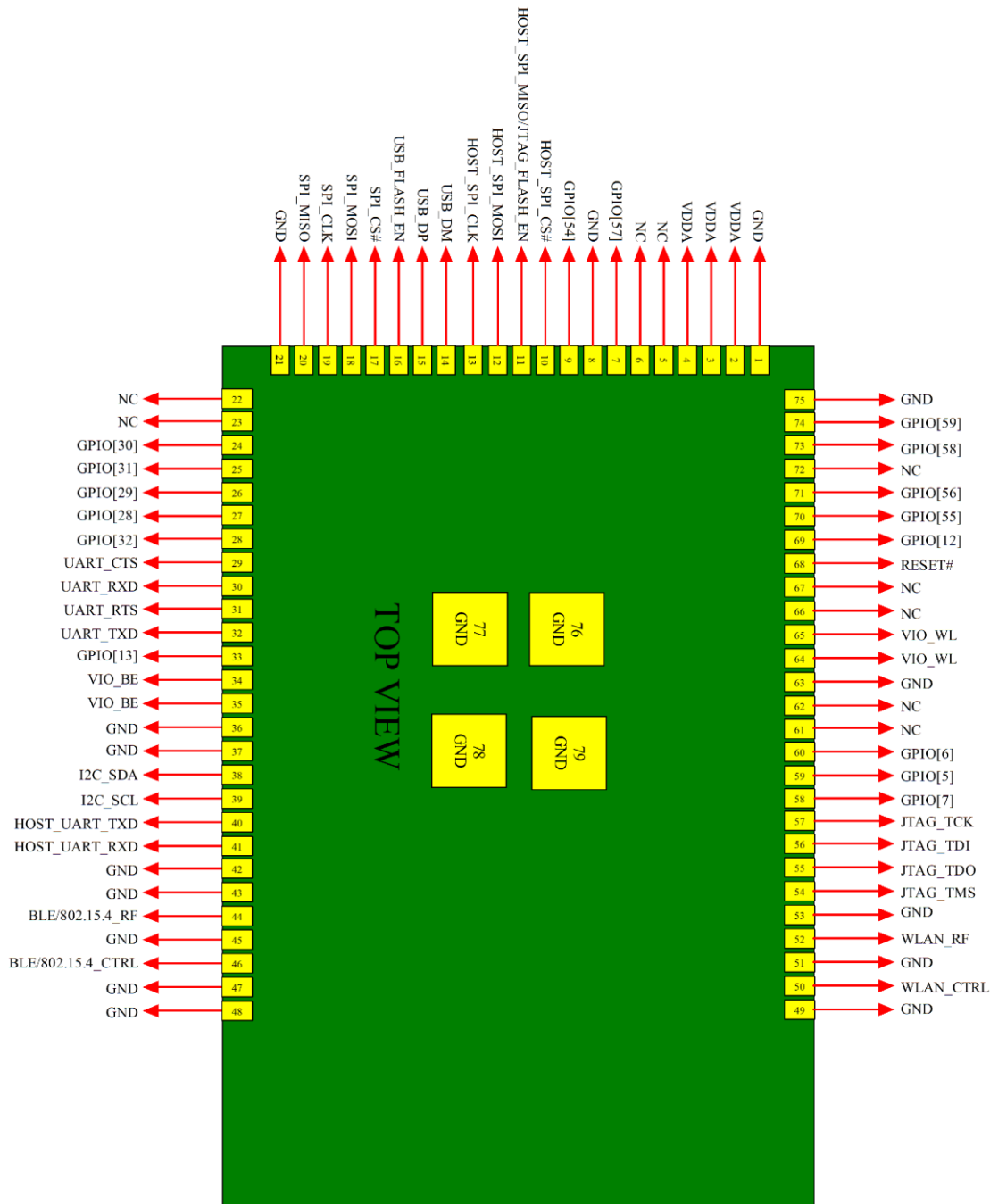Figure 2 shows the pin assignments for the 79-pin QFN package.

Figure 3 : Pin Diagram

4. Pin Description

Pin No	Pin Name	Type	Supply	Description
Flashing/Debug				
Flashing Interface USB				
14	USB_DM	I/O	VDDA	USB Differential Data-Minus
15	USB_DP	I/O	VDDA	USB Differential Data-Plus
16	USB_FLASH_EN	I	VDDA	Pull HIGH to VDDA for Enabling Flash Only Mode. Default: Pull LOW internally (Disable)
Debug/Flash Interface JTAG				
54	JTAG_TMS	I	VDDA	JTAG Test Mode Select
55	JTAG_TDO	O	VDDA	JTAG Test Data Out
56	JTAG_TDI	I	VDDA	JTAG Test Data In
57	JTAG_TCK	I	VDDA	JTAG Test Clock
11	JTAG_FLASH_EN	I	VDDA	Pull HIGH to VDDA for JTAG Flash mode Default: Pull LOW internally
	HOST_SPI_MISO	O		SPI Slave Data-Out
Peripheral Interfaces				
UART				
29	UART_CTS	I	VDDA	UART handshake signals CTS
30	UART_RXD	I	VDDA	UART Receive
31	UART_RTS	O	VDDA	UART handshake signals RTS
32	UART_TXD	O	VDDA	UART Transmit
I2C				
38	I2C_SDA	I/O	VDDA	I2C Serial Data
39	I2C_SCL	O	VDDA	I2C Serial Clock
SPI				
17	SPI_CS#	O	VDDA	SPI Master Chip Select Output
18	SPI_MOSI	O	VDDA	SPI Master Data-Out
19	SPI_CLK	O	VDDA	SPI Master Clock Output
20	SPI_MISO	I	VDDA	SPI Master Data-In
I2S*				
24	I2S_TXD	O	VDDA	I2S Transmit data
	GPIO[30]	I/O		General Purpose I/O
25	I2S_FSYNC	O	VDDA	I2S Frame Sync
	GPIO[31]	I/O		General Purpose I/O

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26	I2S_RXD	I	VDDA	I2S Receive data
	GPIO[29]	I/O		General Purpose I/O
27	I2S_BCLK	O	VDDA	I2S Bit Clock
	GPIO[28]	I/O		General Purpose I/O
28	I2S_MCLK	O	VDDA	I2S Master Clock
	GPIO[32]	I/O		General Purpose I/O
GPIOs				
33	GPIO[13]	I/O	VDDA	General Purpose I/O
	PWM_OUT7	O		PWM Output
58	GPIO[7]	I/O	VDDA	General Purpose I/O
59	GPIO[5]	I/O	VDDA	General Purpose I/O
60	GPIO[6]	I/O	VDDA	General Purpose I/O
69	GPIO[12]	I/O	VDDA	General Purpose I/O
	PWM_OUT0	O		PWM Output
7	GPIO[57]	I/O	VDDA	General Purpose I/O
9	GPIO[54]	I/O	VDDA	General Purpose I/O
70	GPIO[55]	I/O	VDDA	General Purpose I/O
71	GPIO[56]	I/O	VDDA	General Purpose I/O
73	GPIO[58]	I/O	VDDA	General Purpose I/O
74	GPIO[59]	I/O	VDDA	General Purpose I/O
RESET				
68	RESET#	I	VDDA	Reset the Module
RF Pad and Controls				
52	WLAN_RF	I/O	VDDA	WLAN RF Pad OUT for External Antenna
44	BLE/802.15.4_RF	I/O	VDDA	BLE/802.15.4 RF Pad OUT for External Antenna
50	WLAN_CTRL	I	VDDA	Pull HIGH to VDDA for WLAN RF OUT Default: Pull LOW internally
46	BLE/802.15.4_CTRL	I	VDDA	Pull HIGH to VDDA for BLE/15.4 RF OUT Default: Pull LOW internally
Host Interfaces				
Host UART				
40	HOST_UART_TXD	O	VDDA	UART Transmit data (Host Mode)
41	HOST_UART_RXD	I	VDDA	UART Receive data (Host Mode)

Host SPI				
10	HOST_SPI_CS#	I	VDDA	SPI Slave Chip Select – Input (Host Mode)
11	HOST_SPI _MISO	O	VDDA	SPI Slave Data-Out (Host Mode)
	JTAG_FLASH_EN	I		Pull HIGH to VDDA for JTAG Flash mode Default: Pull LOW internally
12	HOST_SPI _MOSI	I	VDDA	SPI Slave Data-In (Host Mode)
13	HOST_SPI _CLK	I	VDDA	SPI Slave Clock input (Host Mode)
POWER				
2, 3, 4	VDDA	Power	3.3V	Power to the Digital section
34, 35	VIO_BE	Power	3.3V	VIO for Application controller
64, 65	VIO_WL	Power	3.3V	VIO for WLAN controller
GROUND				
1, 8, 21, 36, 37, 42, 43, 45, 47, 48, 49, 51, 53, 63, 75	GND	Ground	GROUND	Connect to Ground
76, 77, 78, 79	EPAD	Ground	GROUND	Exposed Pad, connect to Ground
RESERVED				
5	NC	I	VDDA	Reserved for Future use; Leave floating
6	NC	I/O	VDDA	Reserved for Future use; Leave floating
22	NC	I	VDDA	Reserved for Future use; Leave floating
23	NC	O	VDDA	Reserved for Future use; Leave floating
61	NC	I	VDDA	Reserved for Future use; Leave floating
62	NC	O	VDDA	Reserved for Future use; Leave floating
66	NC	I	VDDA	Reserved for Future use; Leave floating
67	NC	I	VDDA	Reserved for Future use; Leave floating
72	NC	I	VDDA	Reserved for Future use; Leave floating

Table 1: Pin Description
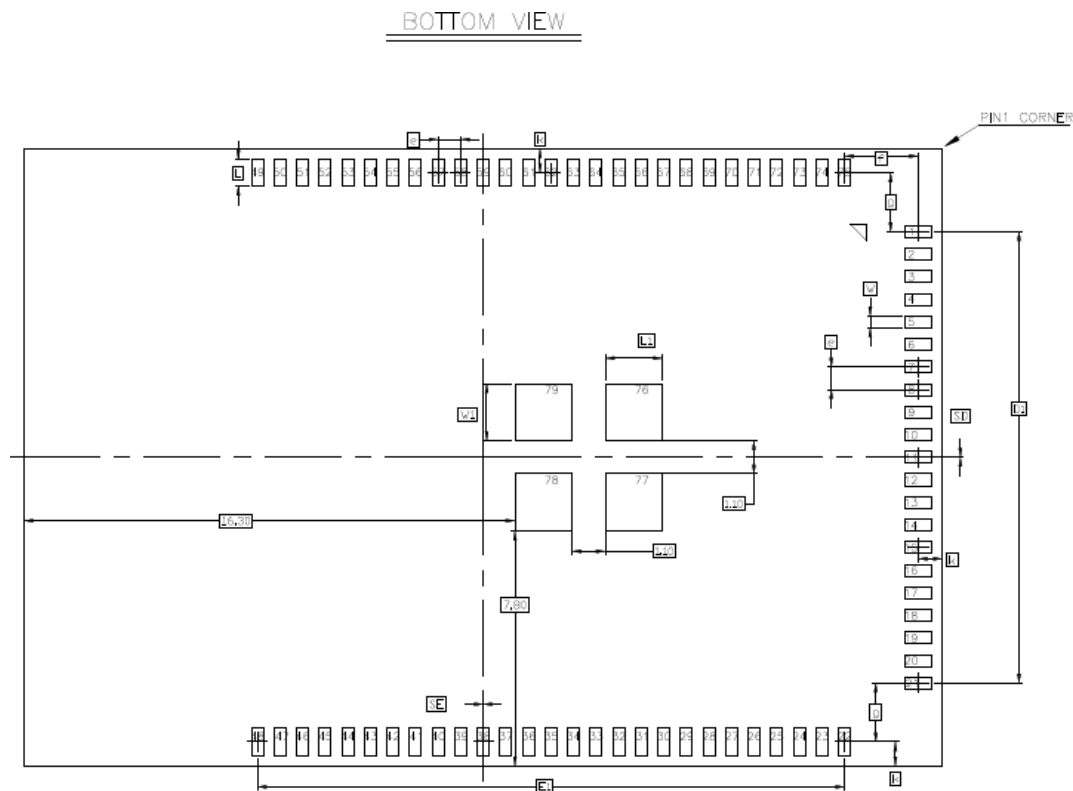
5. Physical Dimensions and Pad Locations

Figure 4 : Module Bottom view

- 79-pins with pads on 3 sides of the module and 4 ground pads in the middle of the module on the bottom side.
- Module Physical Size: 30.5 x 20.5 x 1.86 mm (including shield)
- Solder Pad Size: 0.40 x 0.90 mm
- Pad Pitch: 0.750 mm
- Pad Center to Module Edge: 0.8 mm
- Pad Finish: ENIG (Electro-less Nickel Immersion Gold)
- Pads: [(Three sides (21 + 27 + 27) + 4 Ground Pads in the middle)]

☞ For Hardware Application notes and module dimensions and symbol library files please contact Wi2Wi sales or send an email to sales@wi2wi.com

6. Electrical Characteristics

Parameter	Test Condition	MIN	TYP	MAX	UNITS
Absolute Maximum Ratings					
Storage Temperature		-45	-	125	°C
VDDA, VIO_WL, VIO_BE		2.7	3.3	4.0	V
Recommended Operating Conditions					
Operating Temperature	Industrial	-40	-	+85	°C
VDDA		3.14	3.3	3.46	V
VIO_WL		3.14	3.3	3.46	V
VIO_BE		3.14	3.3	3.46	V
V_{IH} (3.3V I/O) High Level Input Voltage		2.4	-	3.6	V
V_{IL} (3.3V I/O) Low Level Input Voltage		-0.3	-	0.3	V
V_{OH} (3.3V I/O) High Level Output Voltage		3.0	-	3.6	V
V_{OL} (3.3V I/O) Low Level Input Voltage		-0.3	-	0.4	V
Current Consumption UART Mode					
Transmit Mode current Consumption	WLAN 2.4GHz Tx with 11Mbps data rate and Tx power 18dBm	-	265	-	mA
Receive Mode current consumption	WLAN 2.4GHz Rx with 11Mbps data rate	-	69	-	mA
Current consumption in IEEE 802.11 Power Save Mode	Deep Sleep Mode	-	485	-	µA
802.11 RF System Specifications					
Transmit Power Output		-	-	18	dBm
Receive Sensitivity	1 Mbps	-	-	-97	dBm

Table 2 : Electrical Characteristics

7. Software Specifications

Wi2Wi provides all the handles required to operate WC640 and make use of all its features. It provides instructions in the form of commands to configure and control the module. These commands are proprietary to Wi2Wi and can be easily executed. These commands are shown as Internal APIs in the below figure. The user application space is provided to write own programs and make the module itself a final system by itself.

There is an optional method as shown in the below figure, when an external host is available and if the user desires to drive WC640 module through their own external Host, then a serial interface (UART/SPI) to be used between the Host and WC640 module. Wi2Wi provide a set of APIs to run on the external Host to drive the WC640.
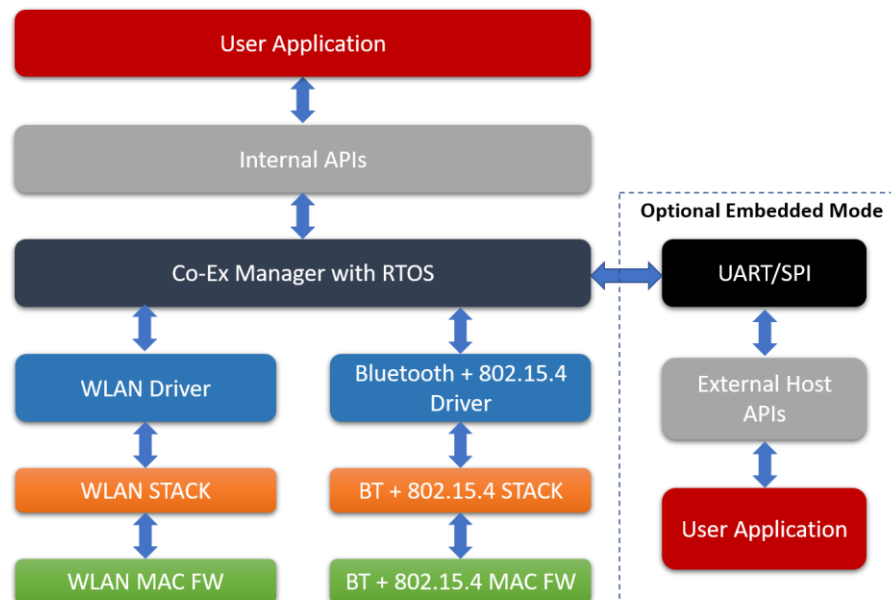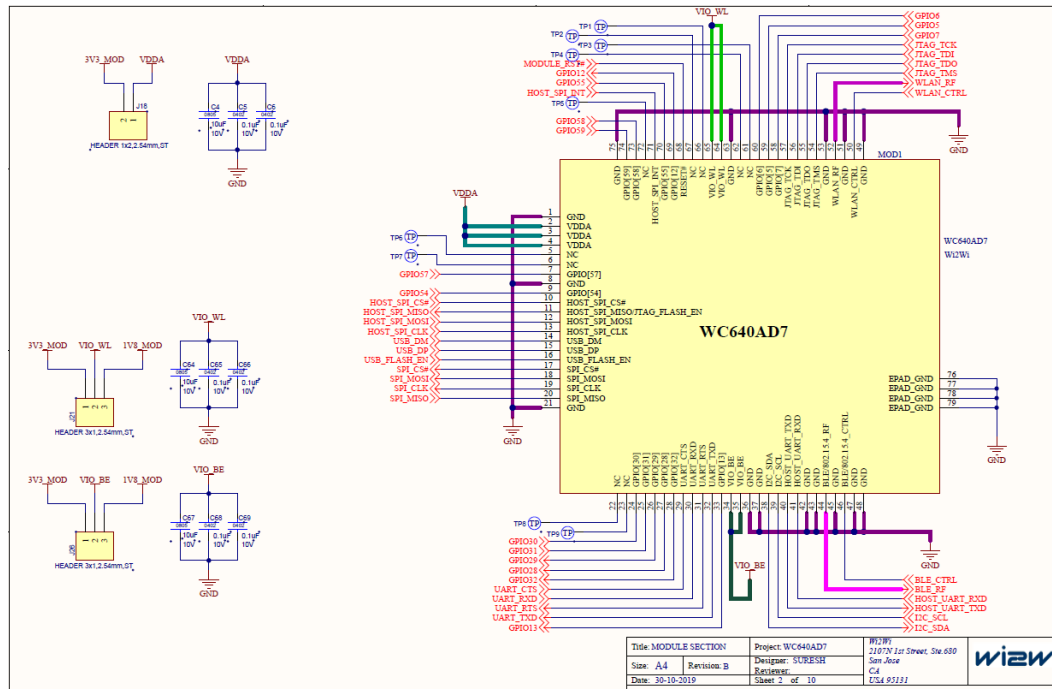

Figure 5 : Software Architecture

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8. Reference Schematics

Figure 6 : Reference Schematics Page 1

Figure 7 : Reference Schematics Page 2

Figure 8 : Reference Schematics Page 3

Figure 9 : Reference Schematics Page 4

Figure 10 : Reference Schematics Page 5
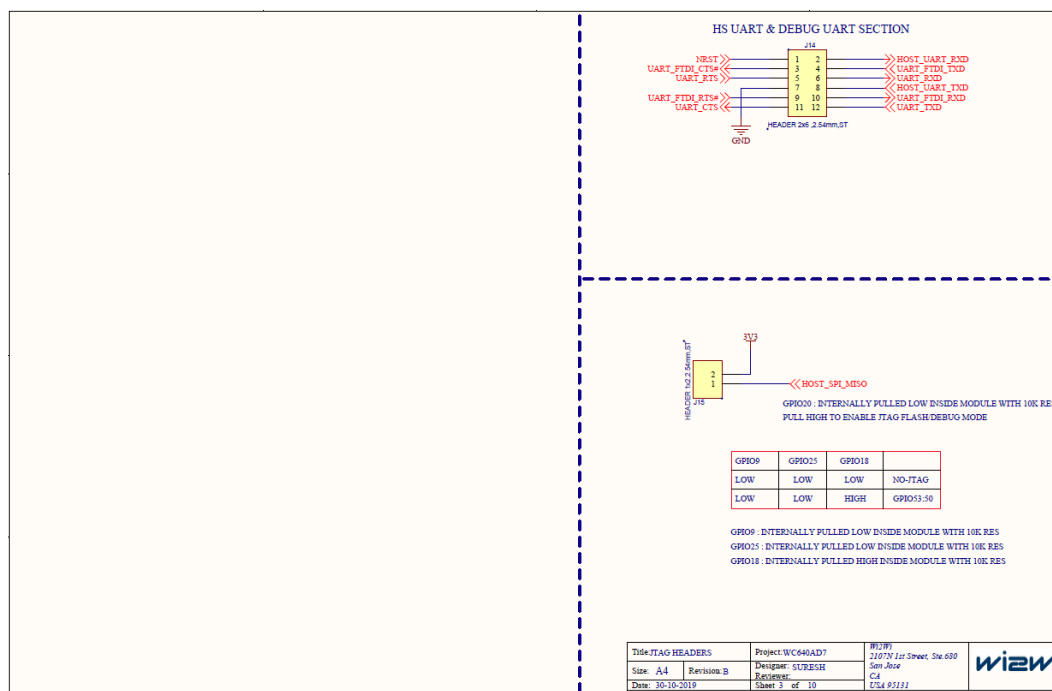

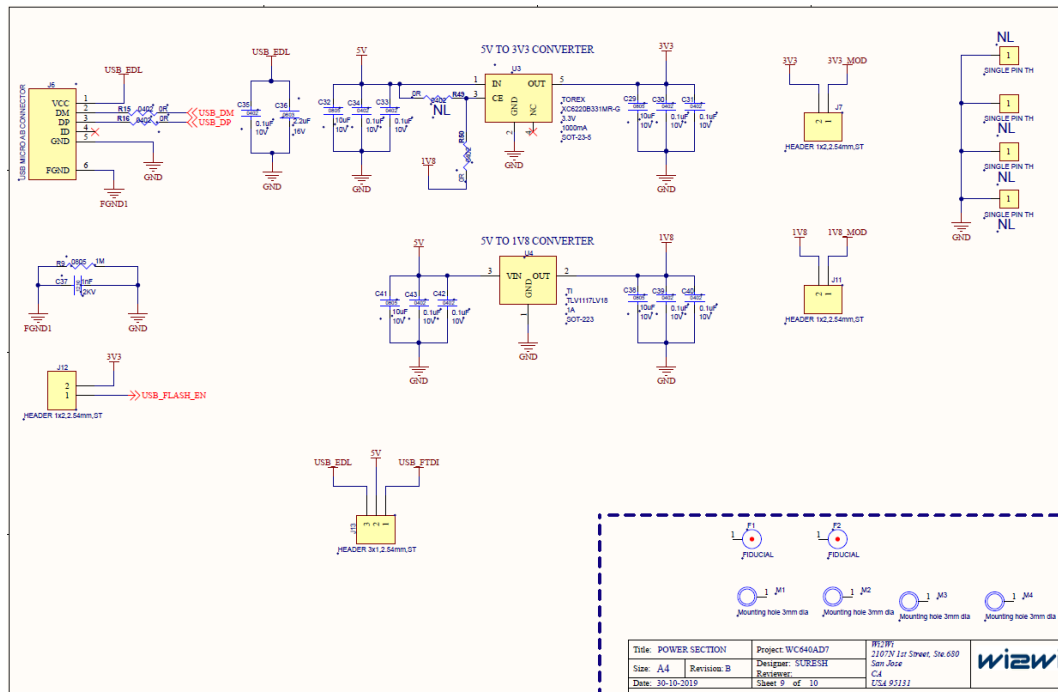**Figure 11 : Reference Schematics Page 6**

Figure 12 : Reference Schematics Page 7

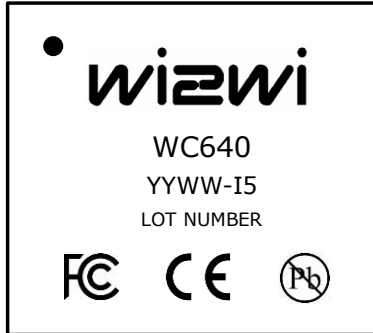# 9. Manufacturing Notes

9.1 Shield Marking

Figure 13 : Shield Marking (Top View)

YY indicates Year
WW indicates Work Week
- -I indicates Industrial operating temperature range (-40°C to +85°C)
- 5 indicates Trace Antenna and RF Pad

9.2 Storage and Baking Instructions

WC640 is an MSL3 qualified package.
- After opening the bag, the parts should be stored as per J-STD-033 standard, and mounted within 168 hours of factory conditions (≤ 30°C, 60% RH)
- If the parts have been exposed in transit, they need to be baked at 125°C for 16 hours

9.3 Recommended Reflow Profile

Assembly Guidelines:
1. Follow solder paste manufacturers recommended profile
   a. All RoHS solder pastes contain the same basic chemistry; however, each manufacturer may have a recommended reflow profile that performs best for their product
2. The profile illustrated below is for reference only
   a. There is no one profile that fits all scenarios
3. Profiles must be dialed in to the specific assembly type
4. ENIG finishes are more susceptible to voids and air entrapment
   a. Selecting a RoHS solder paste that is "ENIG" compatible is recommended
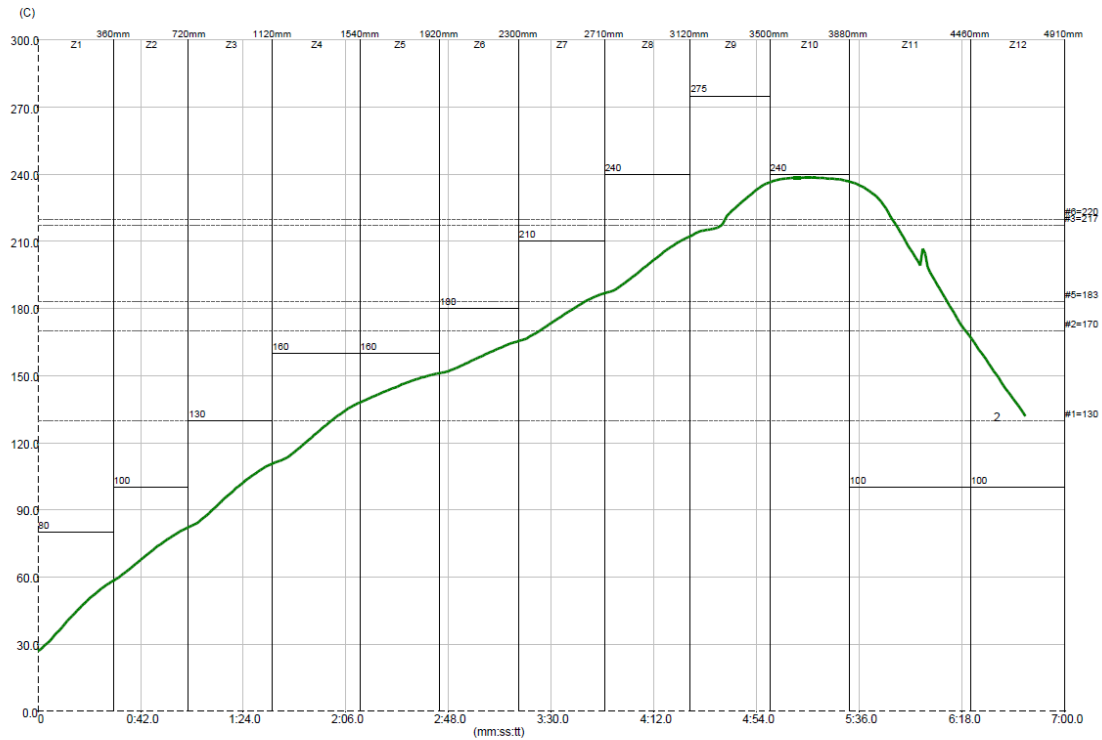
Figure 14 : Recommended Reflow Profile

10.Ordering Information

Part Order Number	Operating Temperature Range	Packaging Method
WC640A00-I5QT	MCU + Wi-Fi 802.11 a/b/g/n	Tray
WC640AD7-I5QT	MCU + Wi-Fi 802.11 a/b/g/n + Bluetooth 5.0 + 802.15.4	Tray

Table 3 : Ordering Information for Modules

Part Order Number	Contents of the Evaluation Kit	Packaging Method
WC640-DVK5	WC640AD7 Module on Evaluation Board and an USB cable	Box

Table 4 : Ordering Information for Evaluation Kits

11.Data Sheet Status

Wi2Wi, Inc. reserves the right to change the specification without prior notice in order to improve the design and supply the best possible product. Updated information, firmware and release notes will be made available on www.wi2wi.com. Please check with Wi2Wi Inc. for the most recent data before initiating or completing a design.

12.References Details

12.1 Specifications

IEEE 802.11 a/b/g/n Wireless LAN Specification
BLE 5
802.15.4
Trademarks, Patents and Licenses

12.2 Disclosures

WC640-DVK5: Development Kit
The specification maximum and minimum limits presented herein are those guaranteed when the unit is integrated into the Wi2Wi's Development System. These limits are to serve as representative performance characteristics of the WC640 when properly designed into a customer's product. Wi2Wi makes no warranty, implied or otherwise specified, with respect to design and performance characteristics presented in this specification when used in customer designs.