ASIC/FPGA Chip Design

802.11a WLAN PHY Implementation

Project

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In this project, you are supposed to implement the physical layer (PHY) of the well-known WLAN standard on both MATLAB and HDL platform. The implemented design in each section should be synthesized and verified on a Virtex-6 FPGA. This project is based on the 802.11a and the goal is to implement the transmitter and receiver side of this standard.

The project timeline is as follows:

Phase	Task	Description	Due Date
0	Read the Standard completely (the main focus from page 1 till 25)		۰۰/۰۱/۲۹
1	Frame structure, scrambling, and de-scrambling	Matlab & HDL both TX and RX side	۰۰/۰۳/۲۱
2	Encoding and decoding	Matlab & HDL both TX and RX side	۰۰/۰۳/۲۸
3	Interleaving and de-interleaving	Matlab & HDL both TX and RX side	۰۰/۰۴/۰۱
4	Integration and matching	Matlab & HDL both TX and RX side	۰۰/۰۴/۱۱

A) Project Definition and Structure:

Please note that all the following steps are required to be done in this project:

1) Software implementation for generation of test vectors (with Matlab or C++)
2) HDL implementation
3) Report of your propose hardware-level VLSI architecture
4) Complete test-bench with all required test vectors (For this you need to have at least four files i) the Verilog code ii) its test-bench iii) The input test vector iv) the expected output golden vector. The test-bench has to create and write the final output in a file.)
5) Complete ASIC flow (synthesis, placement and routing) for the final step.

6) Final formal report (See part B below)

B) Final Report Structure:

1) **Specifications**:
   The specifications document should include a high-level overview of the IP block you are implementing; a description based on a block diagram or set of diagrams is the best way to do this. It should also include a summary of the logical interface the block presents to its environment (input/outputs and control signals). In addition, the document should include the area, power, and performance numbers you achieved after final ASIC implementation.

2) **Design:**
   The design document should include a description of how you will implement the specification, the basic VLSI architecture and algorithms. All RTL codes and modules should be explained in detail. (Make sure that you have enough comments on the HDL code itself.) You should also make notes on the optimization techniques you used and their implications to your design, and the trade-offs they will entail. The design document should also include an overview of the tool suite you used. Think of the design document as something you would give to an engineer just joining the project to help him/her come up to speed. (Design documents also spell out a regular system of "code reviews," where designers have to explain what they have done to their colleagues, at a very detailed level, e.g., a walk-through of RTL code.)

3) **User document:**
   The user document describes how end-users are to integrate the IP block into their designs—think of it as being like the datasheet you get with a chip. In particular, the user document should include detailed information on interfacing to the block, i.e., the timing on the different signals.

4) **Testing:**
   In this part, you are to describe the set of tests you applied to your design to check for logical errors, and your coverage metrics. Classify the bugs you encountered, and how you corrected for them. In addition, discuss the traces you applied to determine the critical path, and compute the delays. It is required to write a high-level model in Matlab or C++ and do performance simulations.