# Nested Processors, Virtual Memory, Hardware Platforms

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# Approach

**Hardware platform and virtual hardware platform**

**Processor, memory, bus without subcomponents**

# Processor and Virtual Processor

**Separate Hardware and Software concerns**

- Processor: specification of hardware aspects (chip, core, multi-threads)
- Virtual Processor: (OS, partitions, schedulers)
- Processor binding points: for cycles and storage

V3 proposal: Virtual Processor no longer contained in a processor

**Virtual Processor**

Logical resource with capacity/budget

Containment region

**“Nested” Processor and hardware platform**

- processor as system (platform) subcomponent

Properties to describe hardware constraints (endianness)

# Bus & Virtual Bus

- Separation of physical and logical concerns
  - Binding of logical to physical
- Bus
  - Physical entity for transferring data
  - Use for physical resource transfer? Fluids, electricity
  - Similar to question of ports with data/event communication
- Virtual bus
  - Logical channel resource with resource capacity/budget
  - Containment region for security/safety
  - Protocol with wrapper overhead
- Bus as system (platform) subcomponents
  - Subcomponents as binding points
  - Network architecture with AADL bus to bus connectivity

# Memory & Virtual Memory

- Separation of physical and logical concerns
  - Binding of logical to physical
- Memory
  - Storage with binding points
  - Need for representing different section of memory addresses: binding points have properties to indicate base address and range (size)
  - Memory binding point on devices can model device registers without requiring memory subcomponents.
- Virtual memory roles
  - Represent logical addresses that are mapped to addresses in different components in the platform
  - Logical resource with capacity/budget
  - Logical containment regions
  - Represent segments of address space
- Memory as system (platform) subcomponents
  - Subcomponents as binding points
  - Memory system architecture with connectivity via bus
  - Platform with memory and processor

# Platform & Virtual platform

- System implementation
  - Physical system model
  - Memory, bus, processor as leaves
  - Visibility for configuration
  - Visibility of binding points
- Virtual platform
  - Connectivity between virtual buses, virtual processors, virtual memory
- Processor, memory, bus, device implementations
  - Implementation of configured component with explicit choice points
  - Visibility boundary for choice points and binding points
  - Implementation of protocols, etc.

# Platforms and Physical Systems

- Hardware platforms & physical systems
  - Restrictions on subcomponents
  - Properties for physical characteristics
- Physical features
  - Separate from generic (abstract) features
- Separate category vs. property/model constraint
  - Platform, virtual platform, physical

# Summary/Actions

- No nested processors, memory, buses: composition via system
- No virtual x as subcomponent of x: handled by bindings
- Virtual platform with connectivity between virtual bus, virtual processor, virtual memory
- Composition through system component: no new platform category
- Virtual memory and binding points: work examples to validate need for both
- Features: non-directional, directional, bi-directional
- Observable feature: for reasoning and for actual observation
- Physical features: draft proposal of description and properties. Don't reinvent but align with SysML and Modelica
- Need for physical component? Nested physical component?
- Binding -> allocation

- Alignment of spec sheet for variants with component type?