AADLv3: Nested Processor & Virtual Memory

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Processor and Virtual Processor

Separate Hardware and Software concerns

- Processor: specification of hardware aspects (chip, core, multi-threads)
- Virtual Processor: (OS, partitions, schedulers)

Virtual Processor Binding to Processor

- V3 proposal: Virtual Processor no longer contained in a processor

Nested Processor

- Description of core, hyper threading, etc.
- Processor instances in processor implementation
  - Also contains memory, bus? Why not use system?
  - Concepts of hardware system, virtual platform system, app system
- Properties to describe hardware constraints (endianness)

Memory & Virtual Memory

Memory

- Memory as subcomponent: currently yes.
  - Enclosing system/memory may have binding point for whole memory
  - Need for representing different section of memory addresses: binding points have properties to indicate base address and range (size)
  - Memory binding point on devices can model device registers without requiring memory subcomponents.
  - May be able to eliminate memory as subcomponent. Use system.
- Virtual memory roles
  - Represent logical addresses that are mapped to addresses in different components at the next level.
  - Represent segments of address space
  - Enforcement: property of requirement and specification of whether it is supported. Who is supporting it (processor, memory, VP?
- Virtual memory binding and subcomponents
  - Nested, in memory, virtual processor, processor?