AADLv3: Nested Processor & Virtual Memory

Software Engineering Institute
Carnegie Mellon University
Pittsburgh, PA 15213

Processor and Virtual Processor

Separate Hardware and Software concerns

- Processor: specification of hardware aspects (chip, core, multi-threads)
- Virtual Processor: (OS, partitions, schedulers)

Processor containment

- Description of core, hyper threading, etc.
- Processor have bus access
- Properties to describe hardware constraints (endianness)

Virtual Processor Binding to Processor

- Virtual Processor no longer contained in a processor
- Should we have an implicit virtual processor per processor?

Processor & Virtual Processor

Processors

- Processor as subcomponent: no. put processors inside system
- Virtual processor inside processor: currently yes.
  - Also relates to binding point
  - Virtual processor inside processor provided for binding vs. processor is target of virtual processor binding
  - Is there a need to indicate that a virtual processor subcomponent is available as binding target?
  - Binding only approach: how to represent pre-bound partitions? How to distinguish internal and external binding points. Enclosing system with both VP and P. system binding point mapped to VP.
  - White box binding see binding points down hierarchy without requiring them mapped to the enclosing component. Offer way to restrict visibility down the hierarchy.
- Virtual processor inside virtual processor
  - Currently allowed.

Processor & Virtual Processor

Processors

- Virtual processor inside virtual processor
  - Currently allowed.
- Can processor represent OS in addition to HW
  - Yes. Properties regarding context switch etc. are on both.
- Scheduling_Protocol property: enumeration literal vs. ref to VP classifier

Bus & Virtual Bus

Bus & virtual bus

- Virtual bus acts as channel and as protocol
- Virtual bus can be connected
- Bus as subcomponent: no. Connected to bus.
- Virtual bus inside bus/processor: currently yes.
  - Provided_Virtual_Bus_Class property: superceeded by binding point on provides side specifying the classifier of the resource that is available for binding. If no classifier then it is the component itself that is available as resource.
  - Virtual bus as protocol: how do we specify that we only support one end of directional protocol? Do we need to indicate whether the protocol is directional or bi-directional.
  - On processor bindingpoint (incoming and/or outgoing end of protocol.
- Virtual bus inside virtual bus: currently supported
- Action: white paper (same as for processor about preconfigured binding by nesting vs. new configuration/binding concept.

Memory & Virtual Memory

Memory

- Memory as subcomponent: currently yes.
  - Enclosing system/memory may have binding point for whole memory
  - Need for representing different section of memory addresses: binding points have properties to indicate base address and range (size)
  - Memory binding point on devices can model device registers without requiring memory subcomponents.
  - May be able to eliminate memory as subcomponent. Use system.
- Virtual memory roles
  - Represent logical addresses that are mapped to addresses in different components at the next level.
  - Represent segments of address space
  - Enforcement: property of requirement and specification of whether it is supported. Who is supporting it (processor, memory, VP?
- Virtual memory inside memory:
- Virtual memory inside virtual memory:

- When defining binding: capacity and linearity of addresses.

Virtual bus connections

Allow connectivity in virtual platform

First step: virtual bus connections

- Virtual bus to Virtual processor
- Virtual bus to virtual bus
- Component itself or only via provides clause (follow what is in V2.1 in early prototype)

- Proposal:
  - Allow virtual bus access on virtual processor, virtual bus.
  - Allows access connections.
  - Consistency rules about binding between layers and the topology at each layer
  - It is not required. It also can be derived.

Virtual Memory

Example of use

- Configuration of physical memory layout
- Virtual memory capture memory segments and bound to RAM

Containment

- Memory can contain memory
  - Still needed?
- Virtual Memory containment?

Binding

- SW components to virtual memory
- Virtual memory to virtual memory
- Virtual Memory to memory