Modeling the Interactions between Core Allocation and Overload Control in μs-Scale Network Stacks

Jehad Hussien **Pratyush Sahu** Eric Stuhr Ahmed Saeed

Current Trends in Datacenter Workloads

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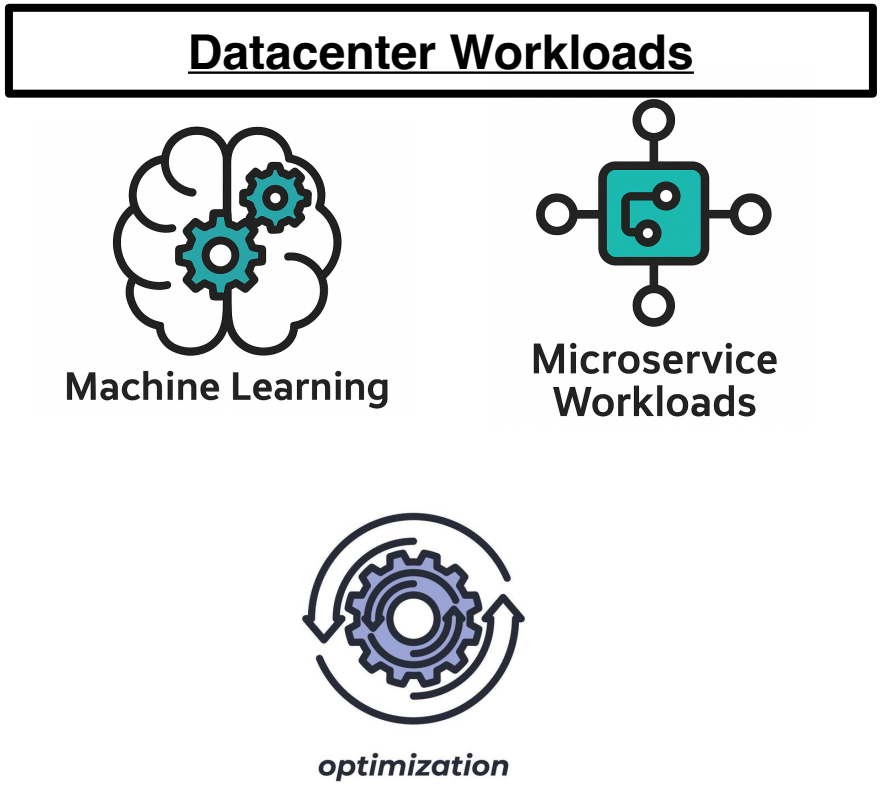

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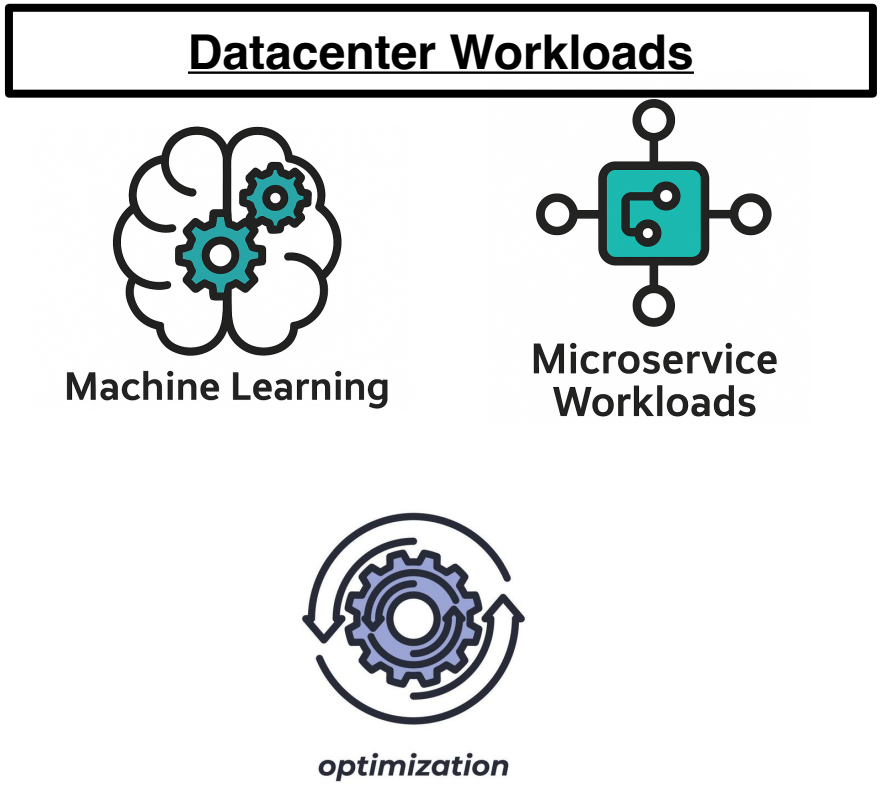

Service Level Objectives (SLO)

1. 99% “GET” RPCs completed in less than 10 µs (latency SLO)
2. Maintain an average of 1 million requests per second (throughput SLO)

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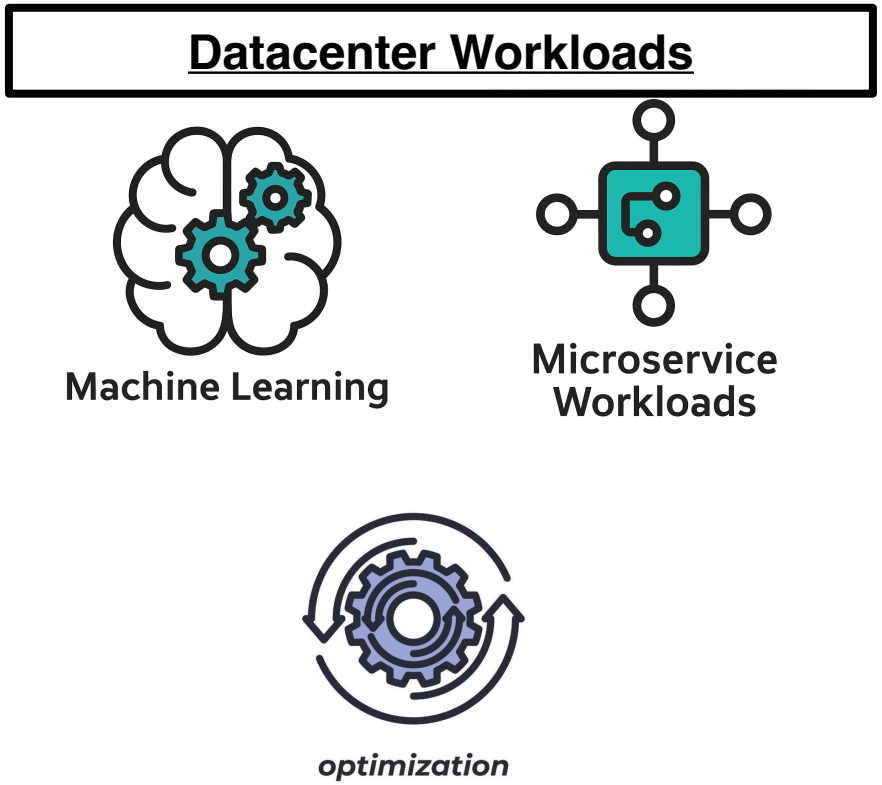

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High Utilization

10-20% CPUs utilized in current datacenter servers leading to wastage of CPU cycles and energy

Multiple Controllers in a Single Server

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Core Allocation

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*Ensure no wastage of CPU cores by dynamically **allocating/parking cores** based on **incoming load**.*

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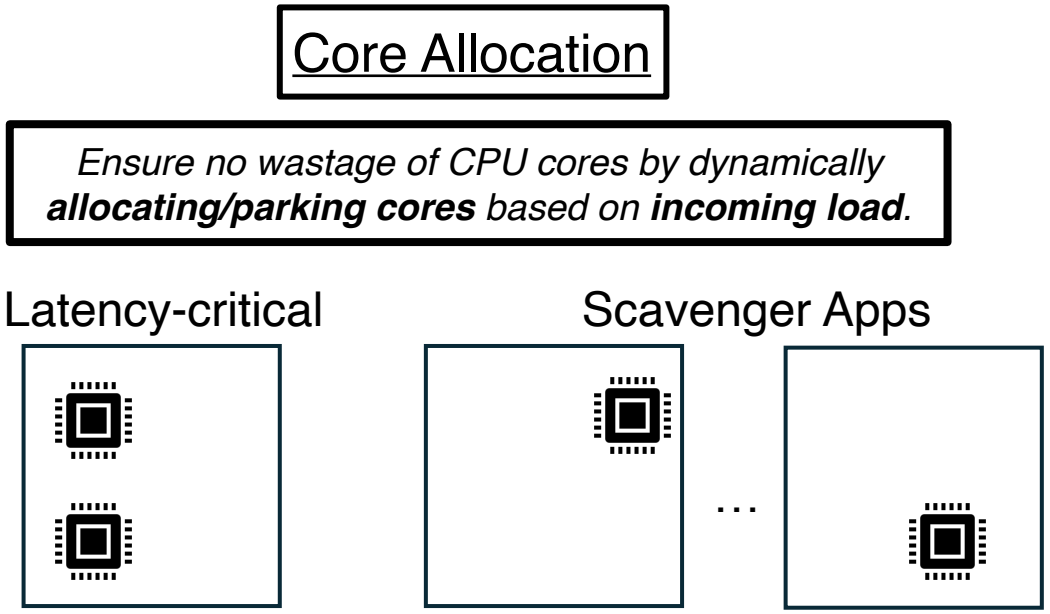

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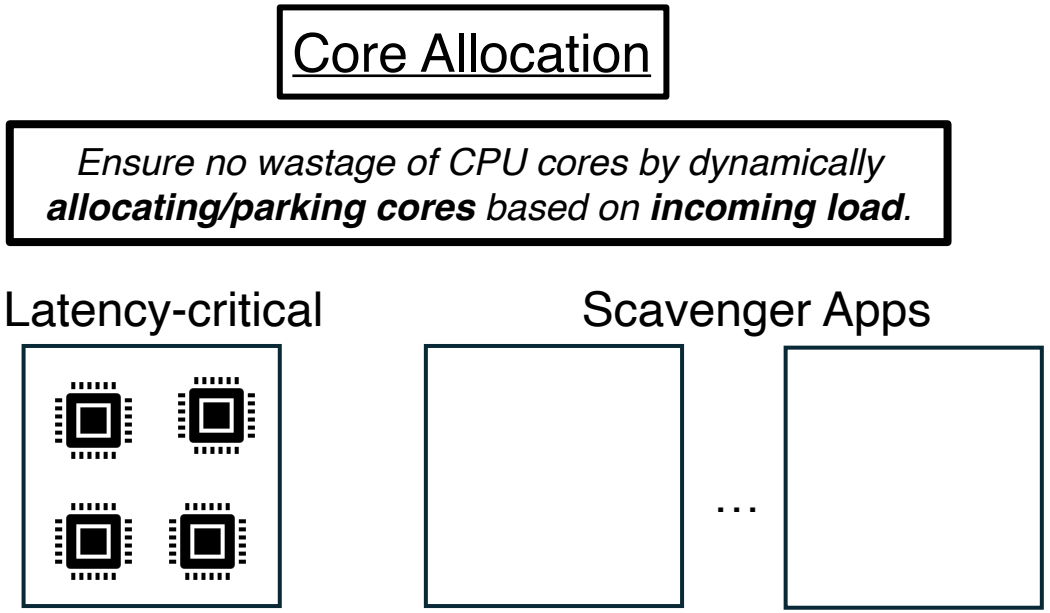

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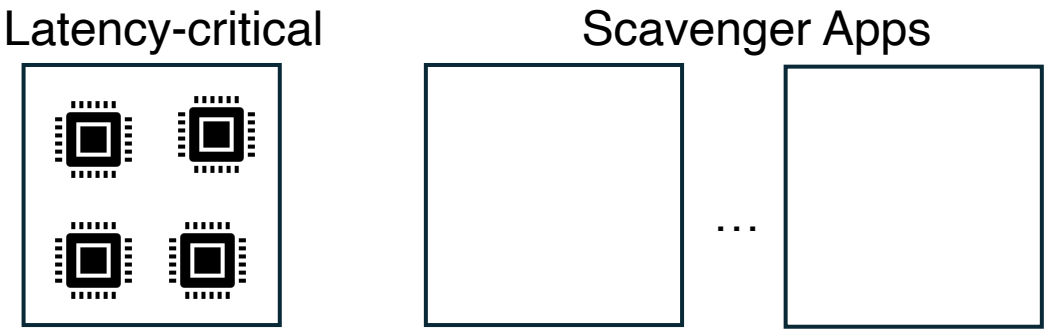

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Credit-based Overload Controller

*Avoid Congestion Collapse and ensure high performance by **controlling admission of requests***

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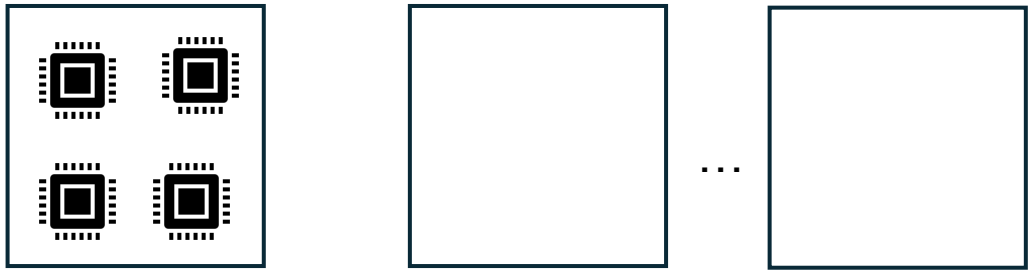

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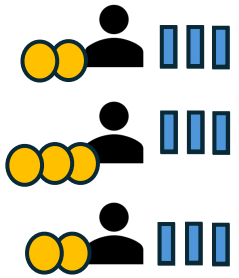
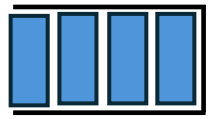


Server

Incoming Queue



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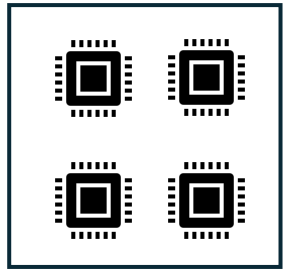

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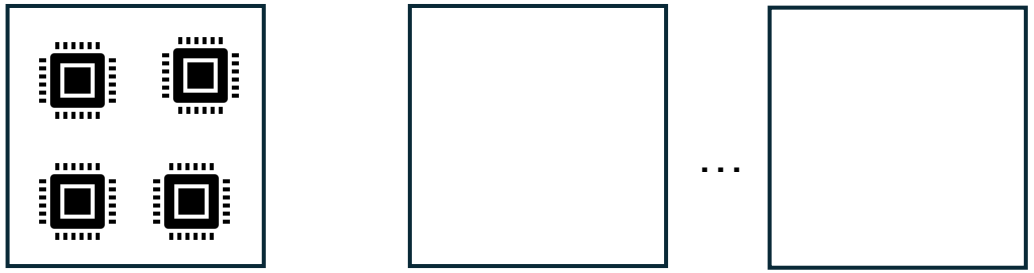

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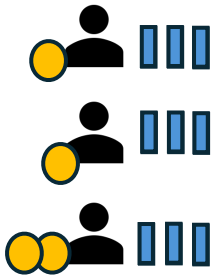

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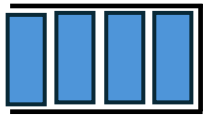

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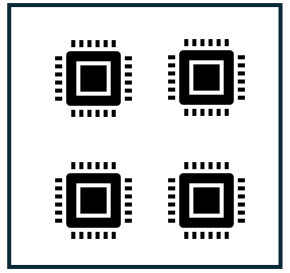

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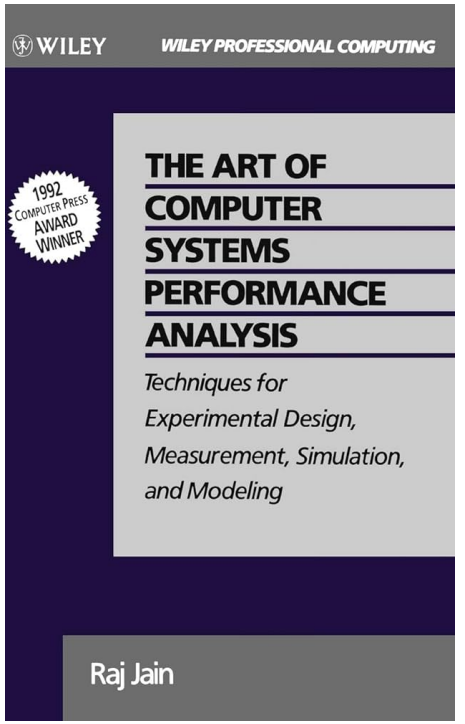
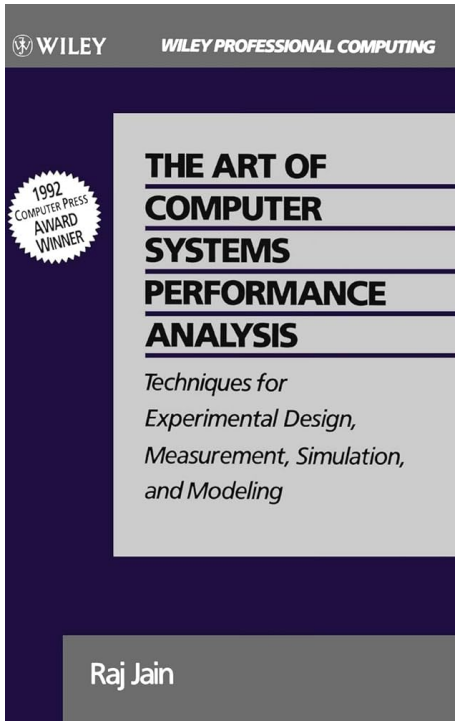


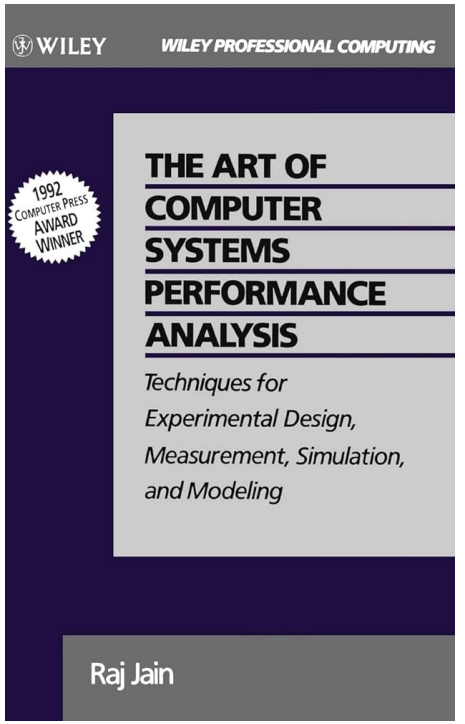
How do we model these controllers?

	Implementation	Simulation	Analytical



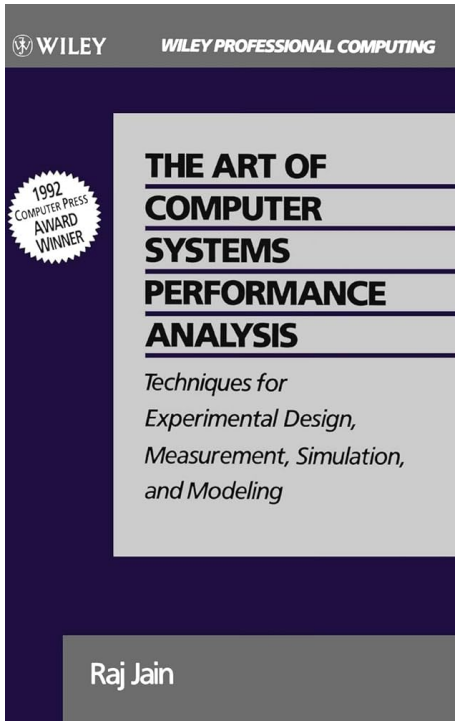
How do we model these controllers?

	Implementation	Simulation	Analytical
Proof of Performance			



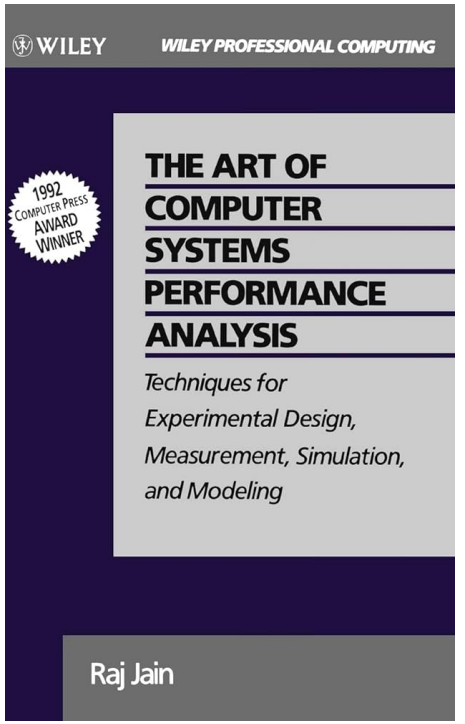
How do we model these controllers?

	Implementation	Simulation	Analytical
Proof of Performance	Only empirical		



How do we model these controllers?

	Implementation	Simulation	Analytical
Proof of Performance	Only empirical	Statistical	



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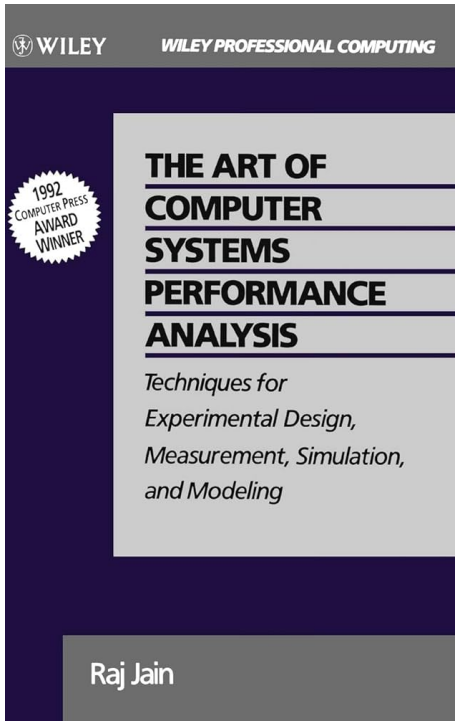
Proof of Performance	Only empirical	Statistical	Guaranteed



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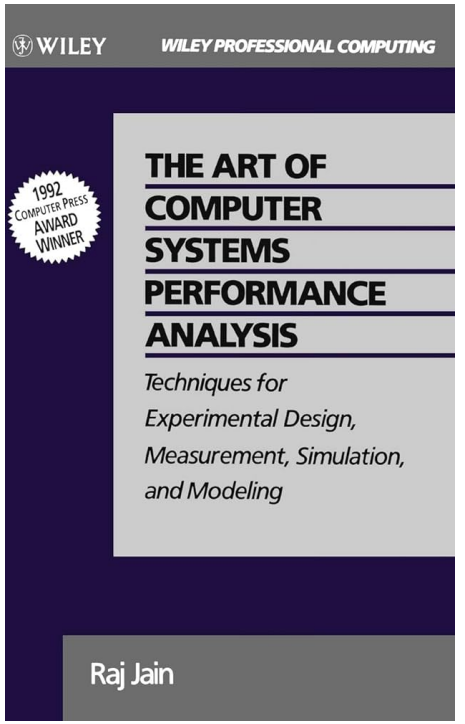
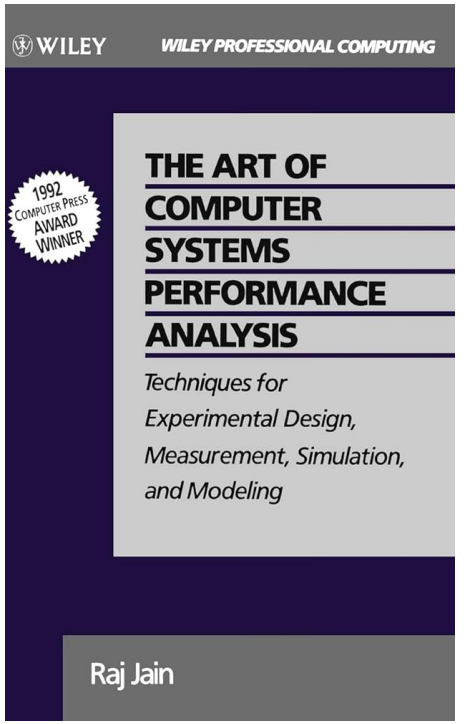
Proof of Performance	Only empirical	Statistical	Guaranteed
Complexity and Extensibility			



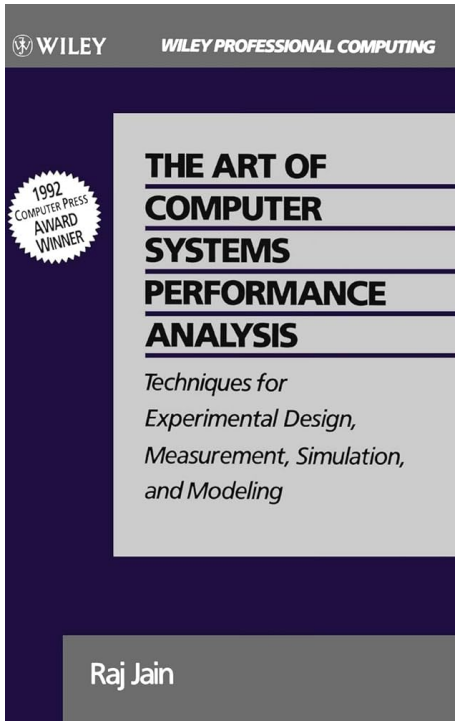
How do we model these controllers?

	Implementation	Simulation	Analytical
Proof of Performance	Only empirical	Statistical	Guaranteed
Complexity and Extensibility	Hard		



How do we model these controllers?

	Implementation	Simulation	Analytical
Proof of Performance	Only empirical	Statistical	Guaranteed
Complexity and Extensibility	Hard	Easy	



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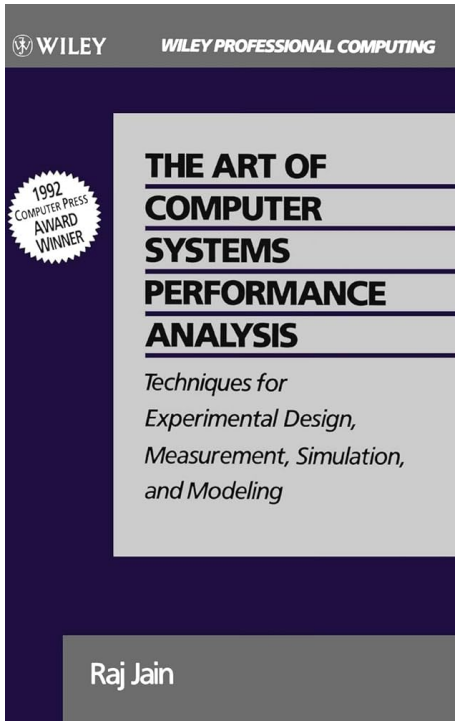
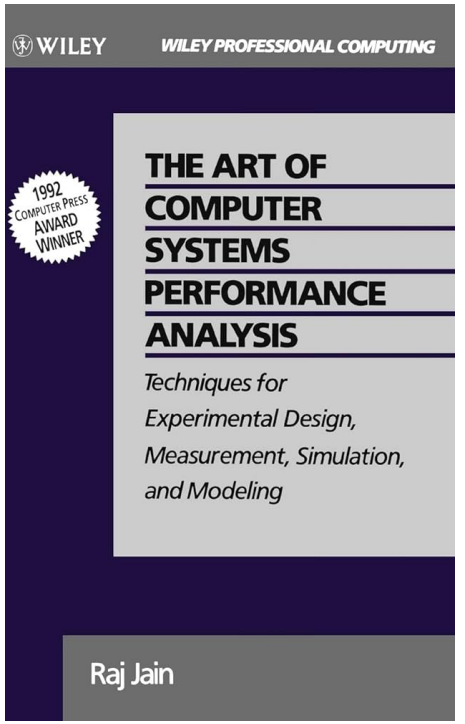
Proof of Performance	Only empirical	Statistical	Guaranteed
Complexity and Extensibility	Hard	Easy	Hard



How do we model these controllers?

	Implementation	Simulation	Analytical
Proof of Performance	Only empirical	Statistical	Guaranteed
Complexity and Extensibility	Hard	Easy	Hard
Realistic			



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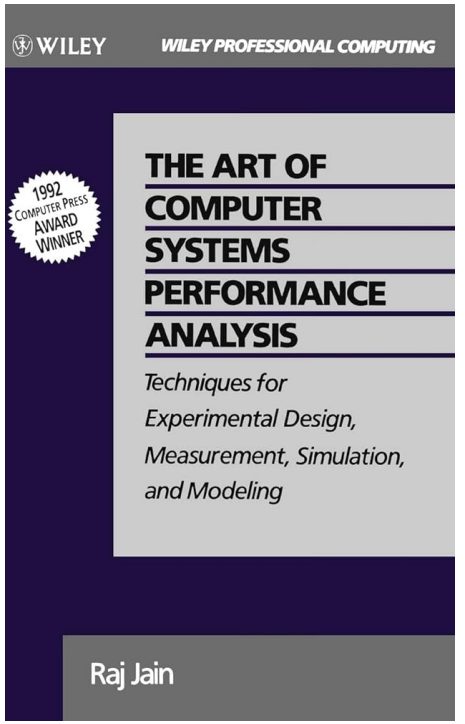
Complexity and Extensibility	Hard	Easy	Hard
Realistic	Yes		



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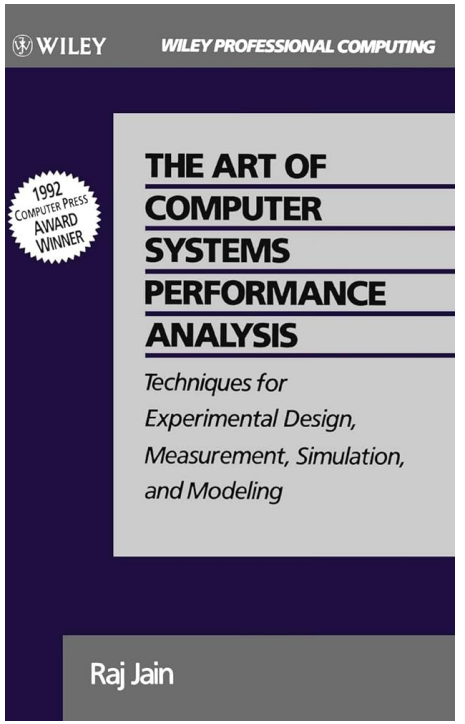
Proof of Performance	Only empirical	Statistical	Guaranteed
Complexity and Extensibility	Hard	Easy	Hard
Realistic	Yes	Simplified	



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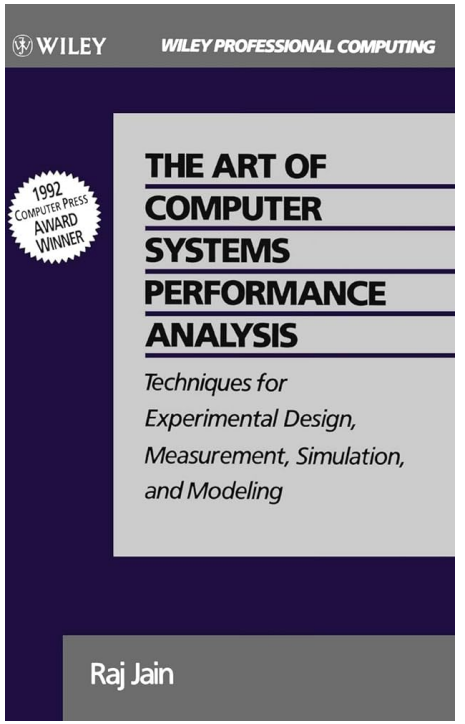
Complexity and Extensibility	Hard	Easy	Hard
Realistic	Yes	Simplified	Oversimplified



Performance Verification

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Definition: Using finite model checking to verify performance properties of a system that is modeled as logical predicates

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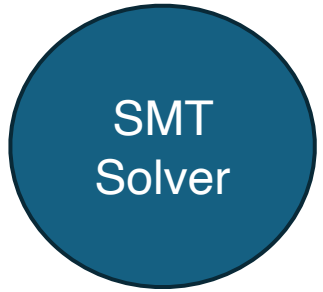
Use **Satisfiability Modulo Theories Solvers (SMT Solvers)** to find a possible scenario where a particular performance is met



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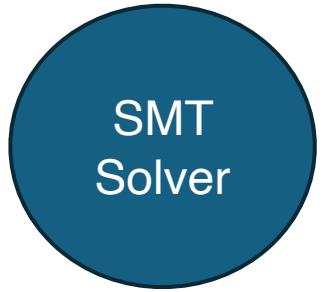

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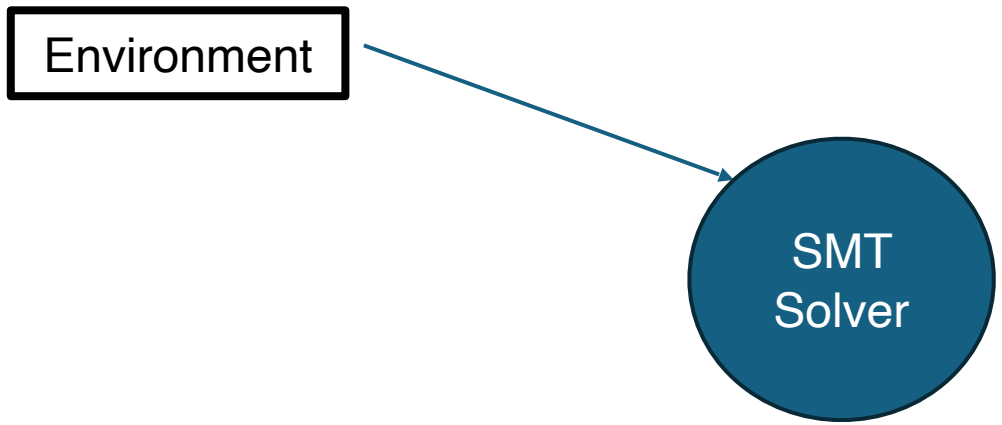

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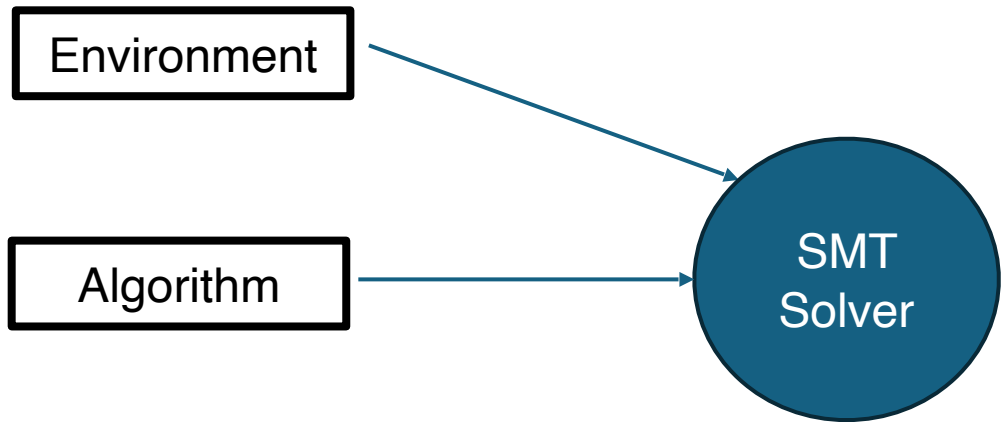

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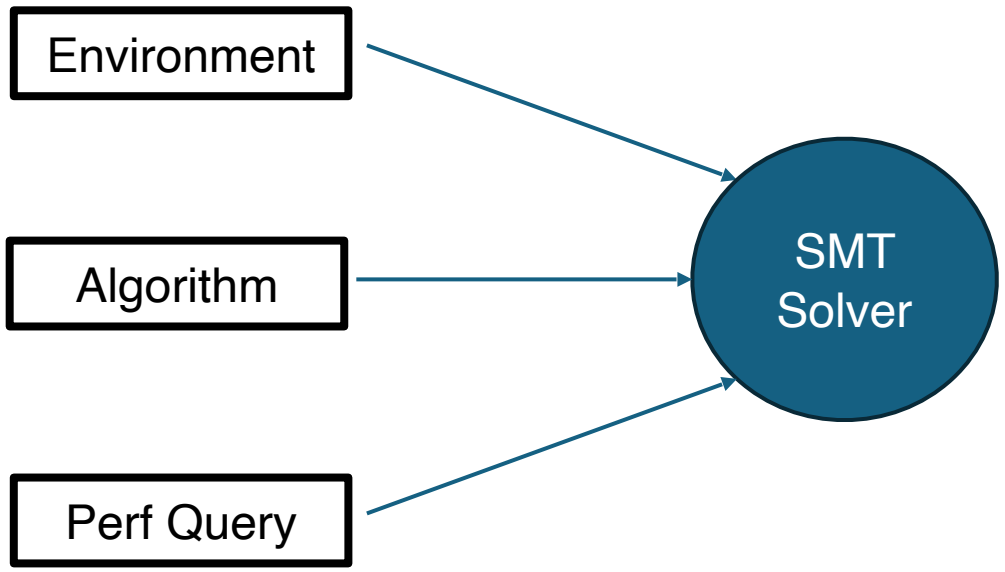

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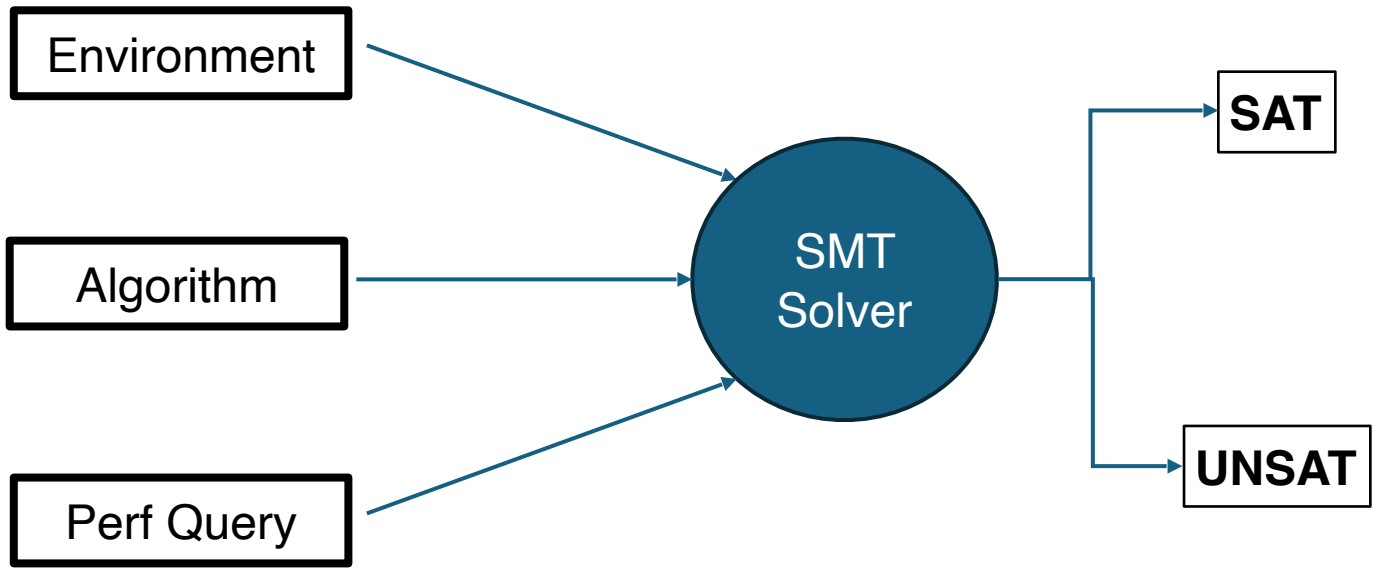

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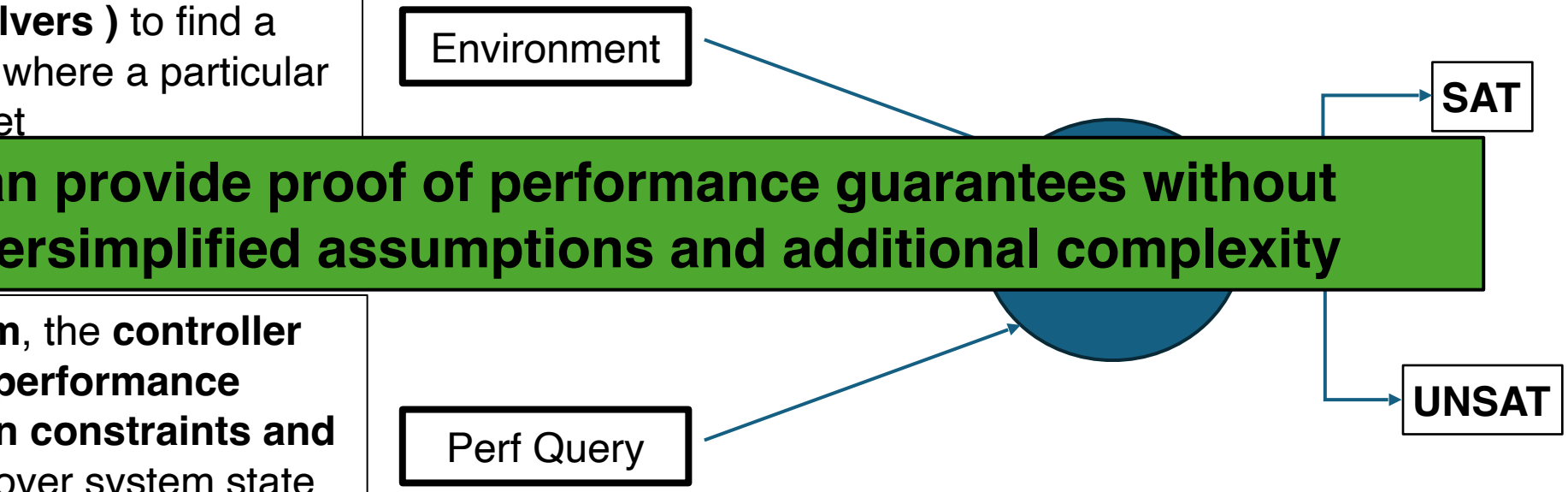

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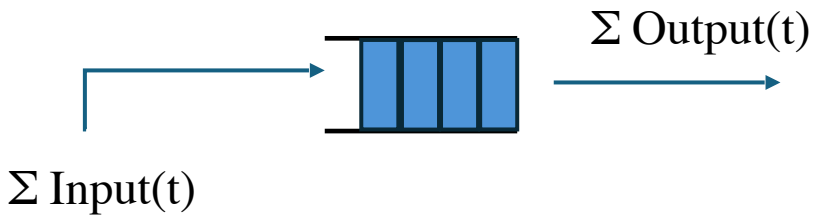

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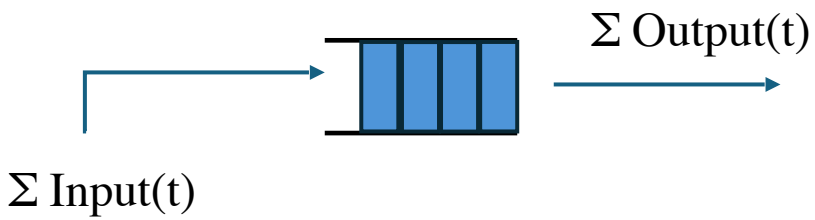
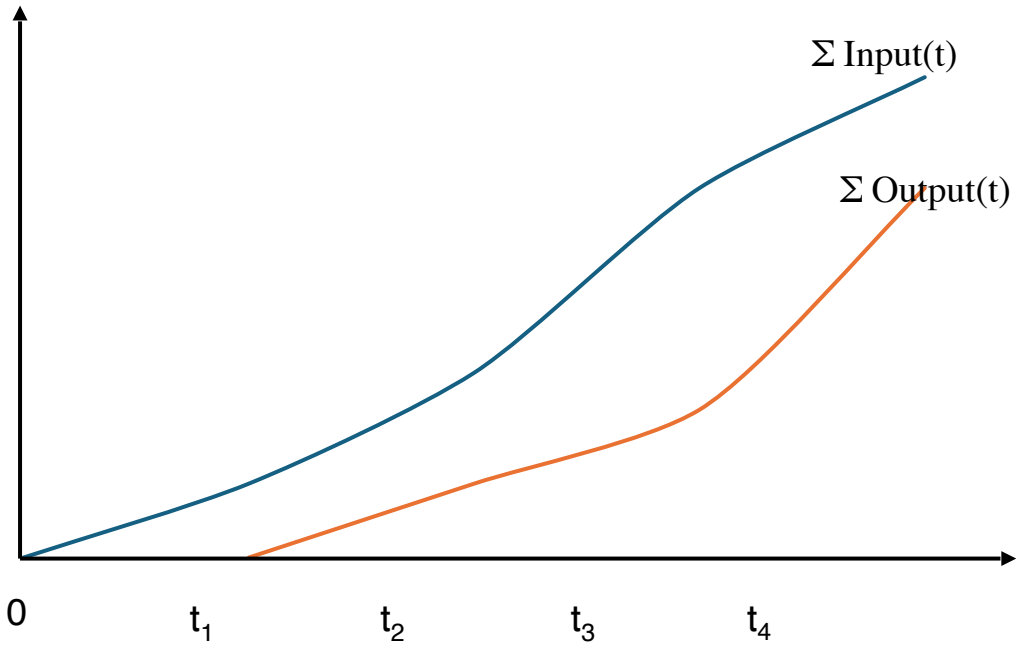
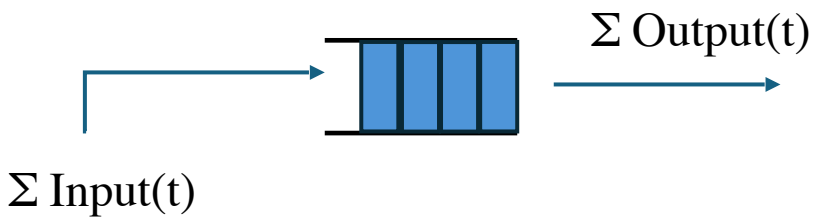
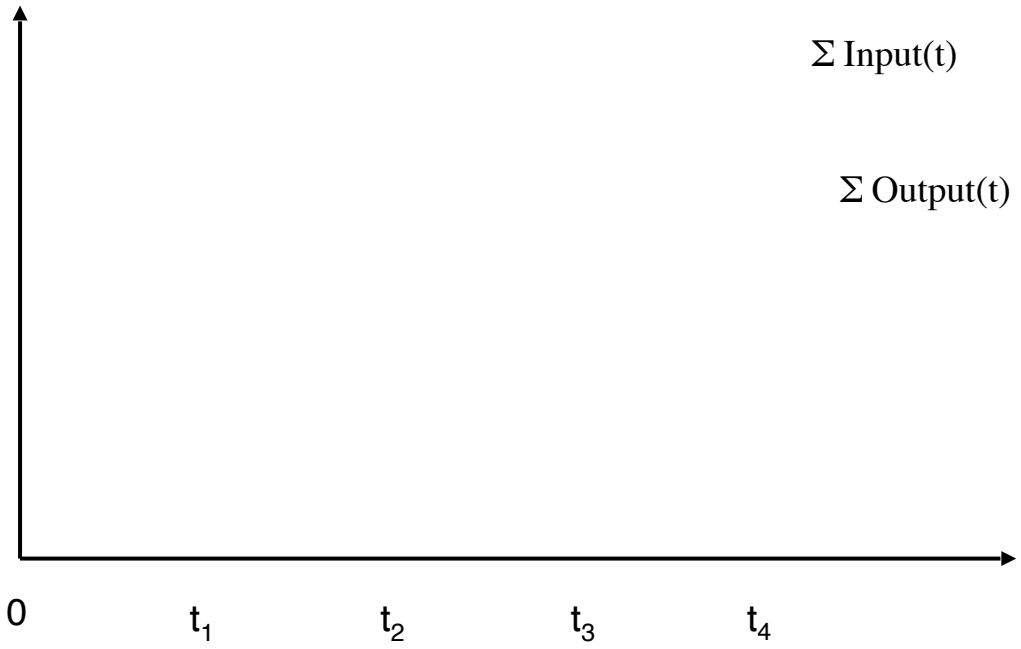




Model Abstraction and Discretization





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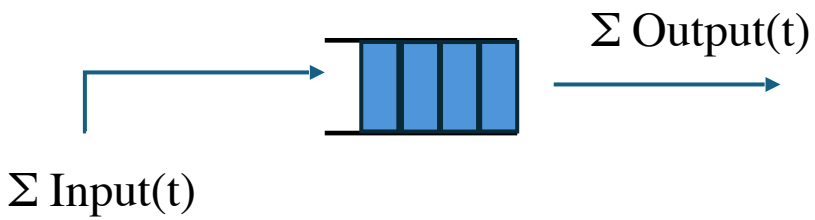

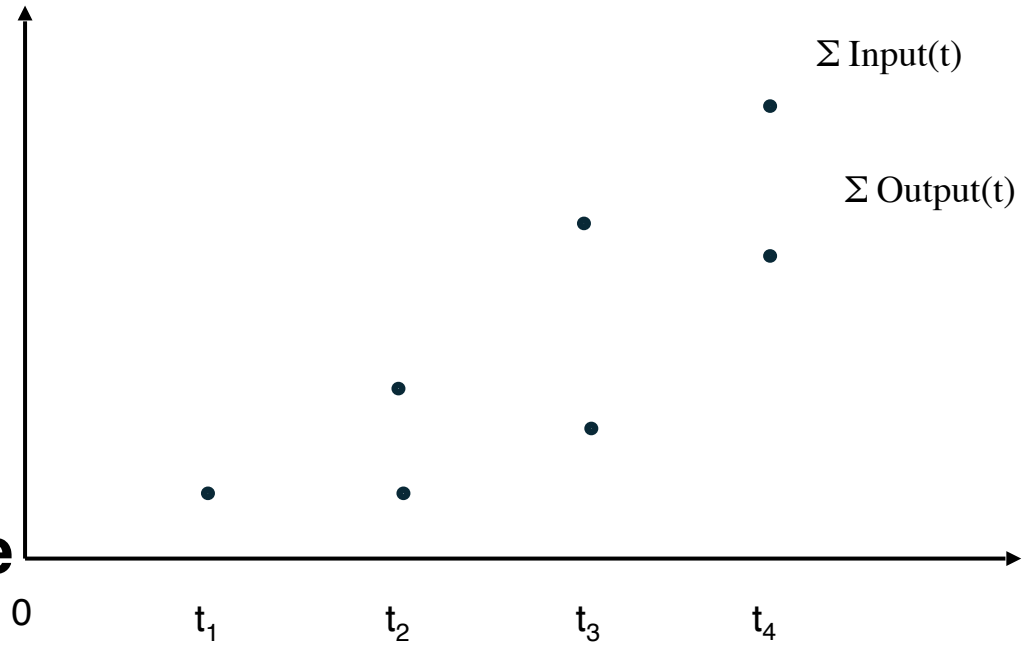

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- Define Boolean constraints for **cumulative variables**
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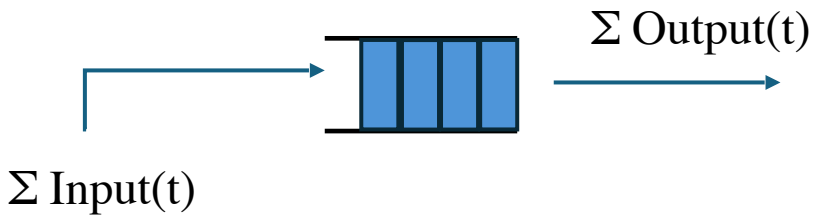

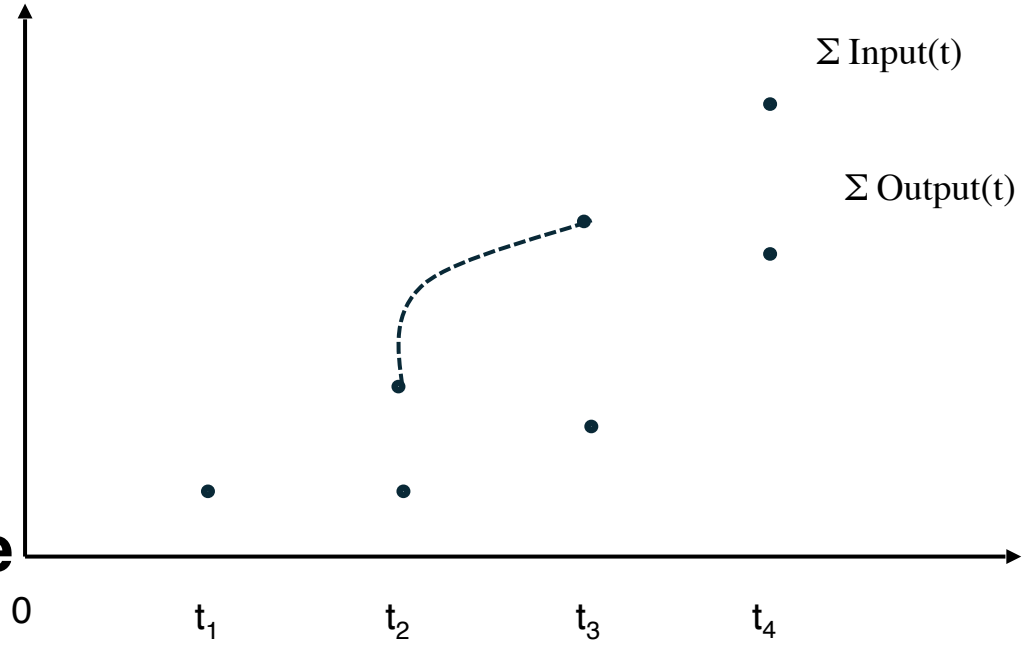

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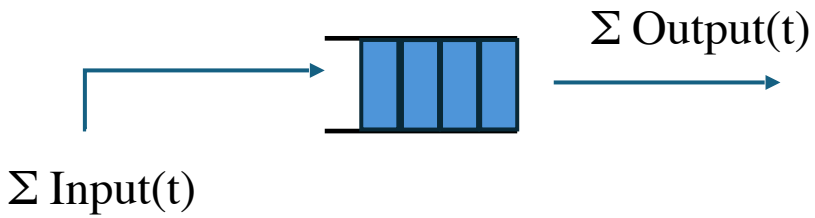

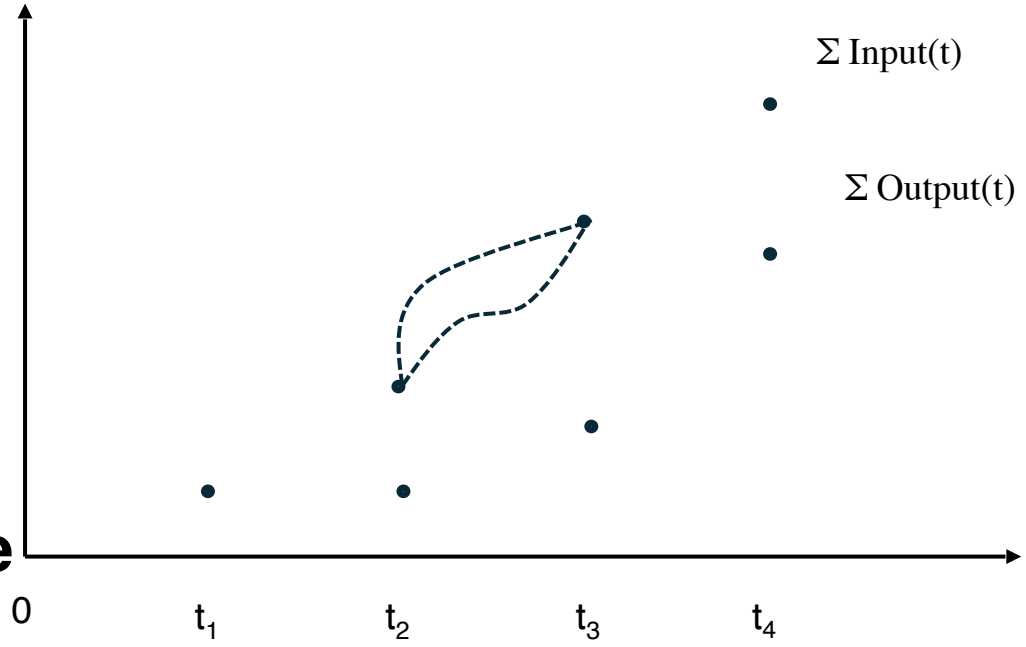

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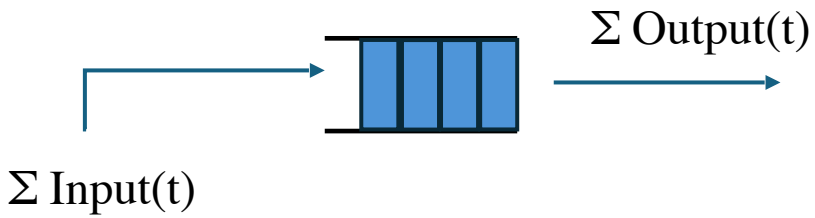

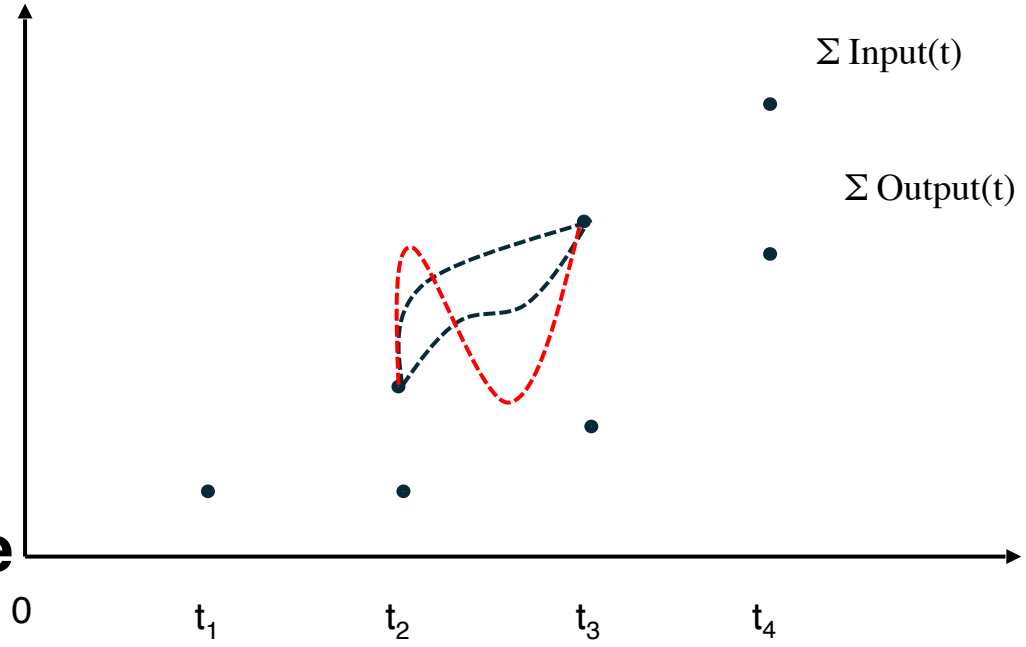

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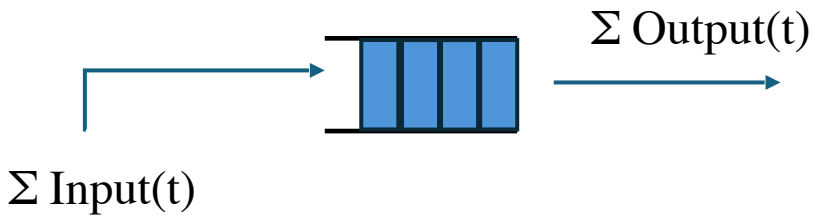

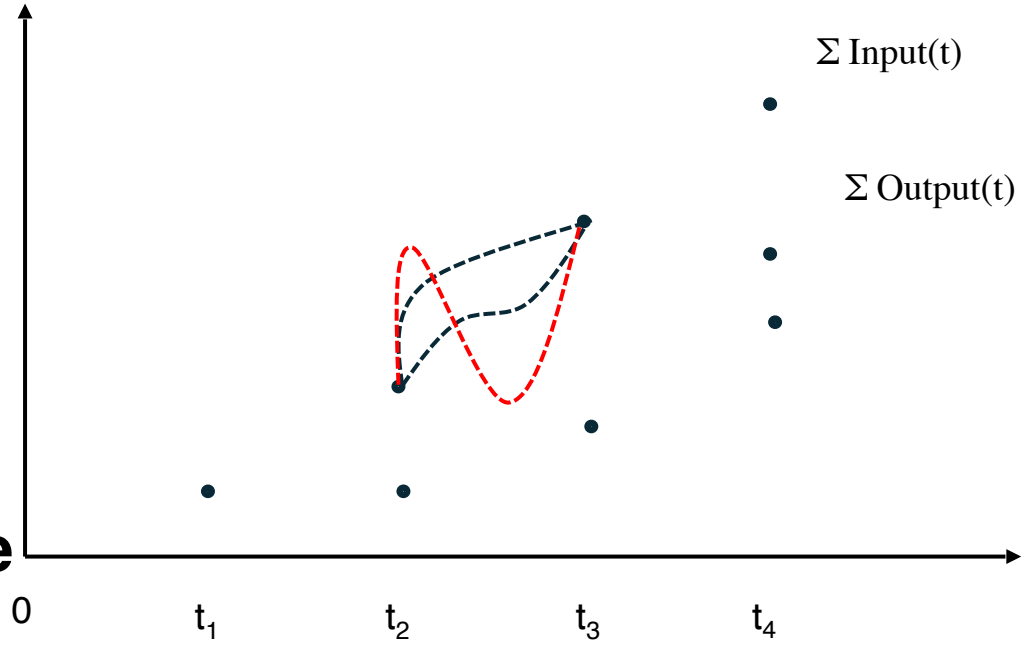

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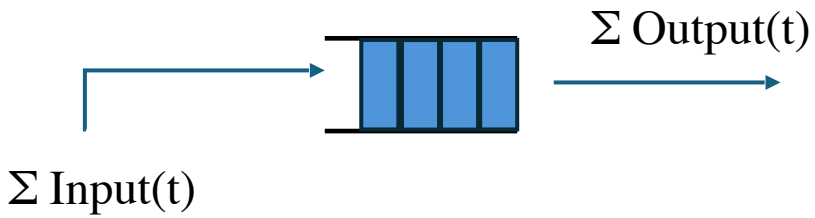

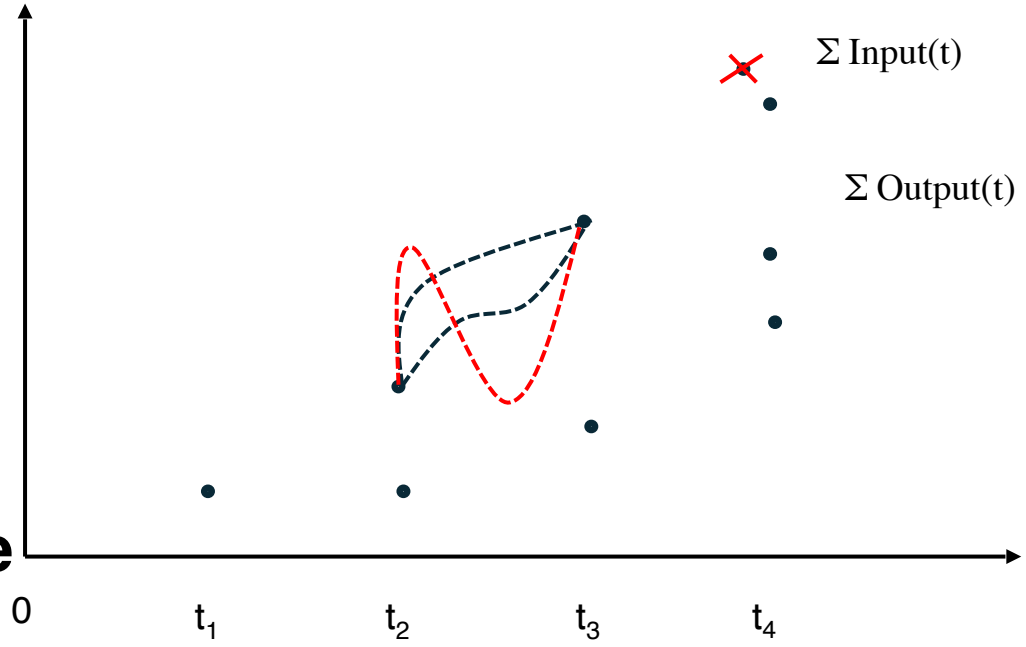

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$$\text{Input}(t_x) \geq \text{Output}(t_x)$$

System of Network Queues

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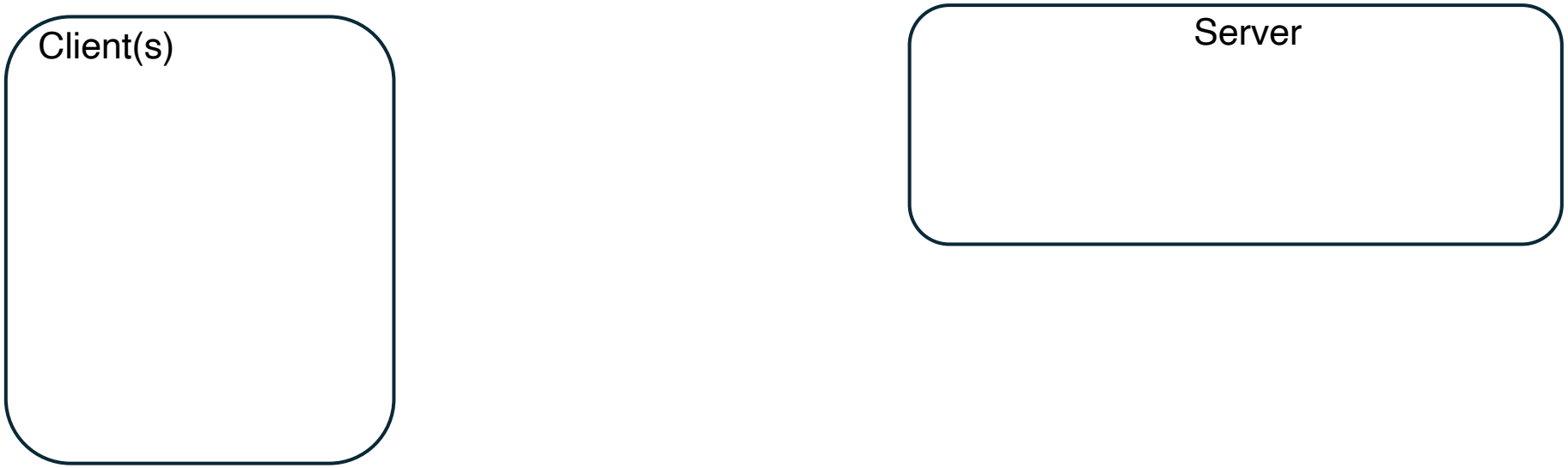

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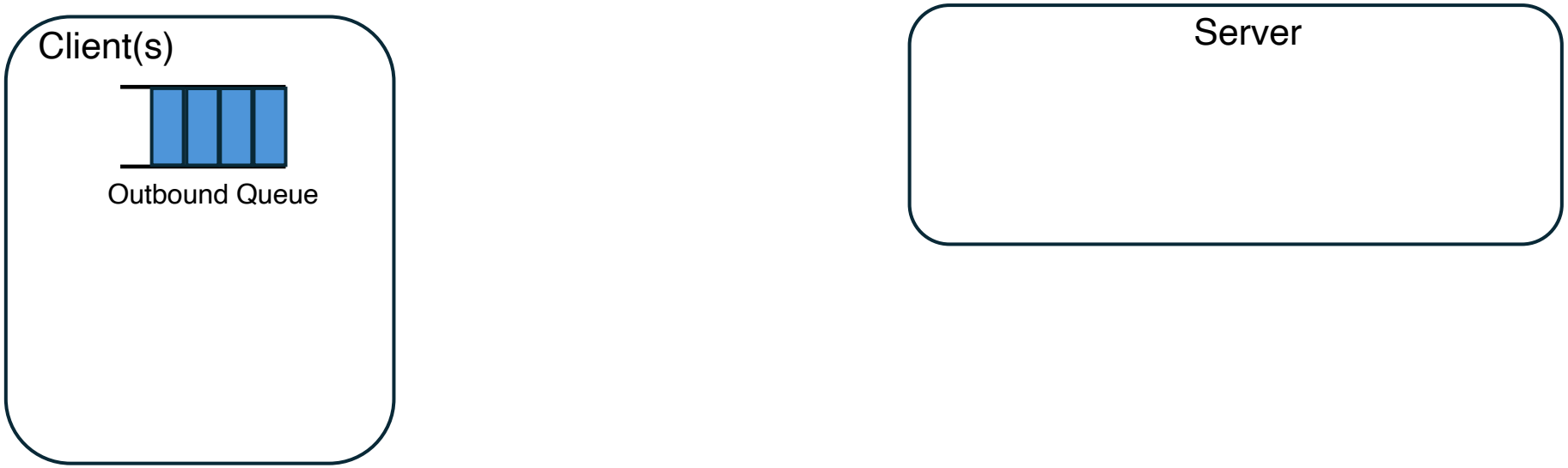

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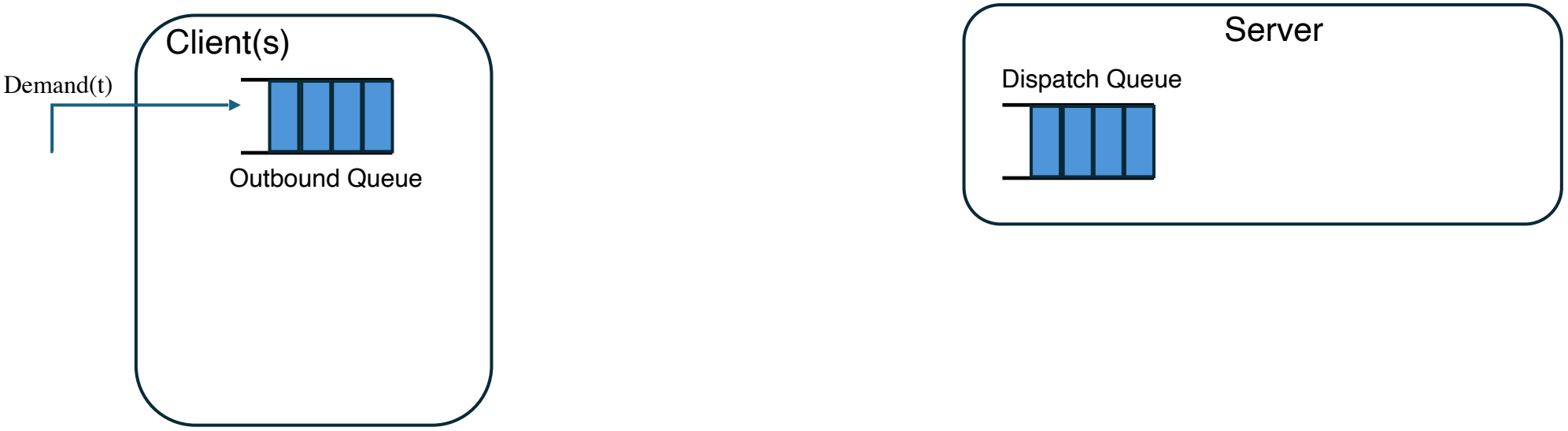

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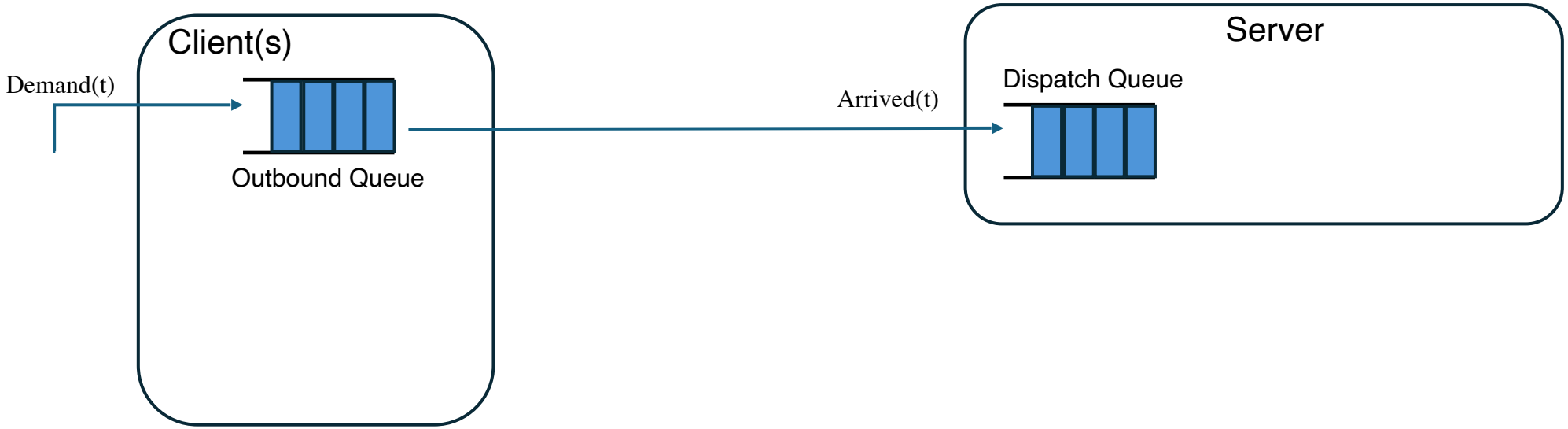

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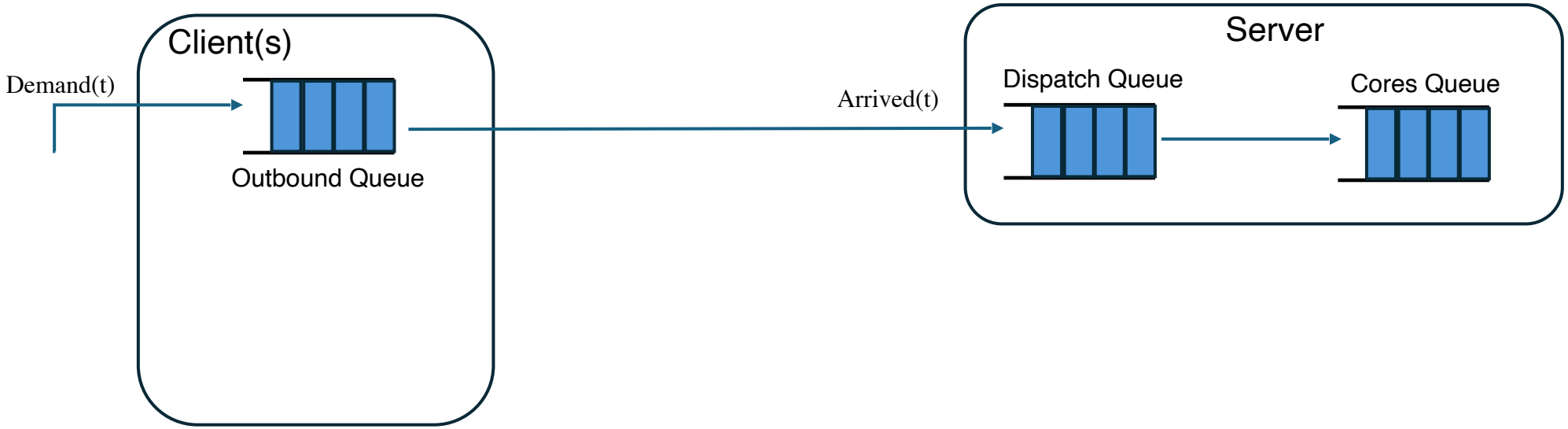

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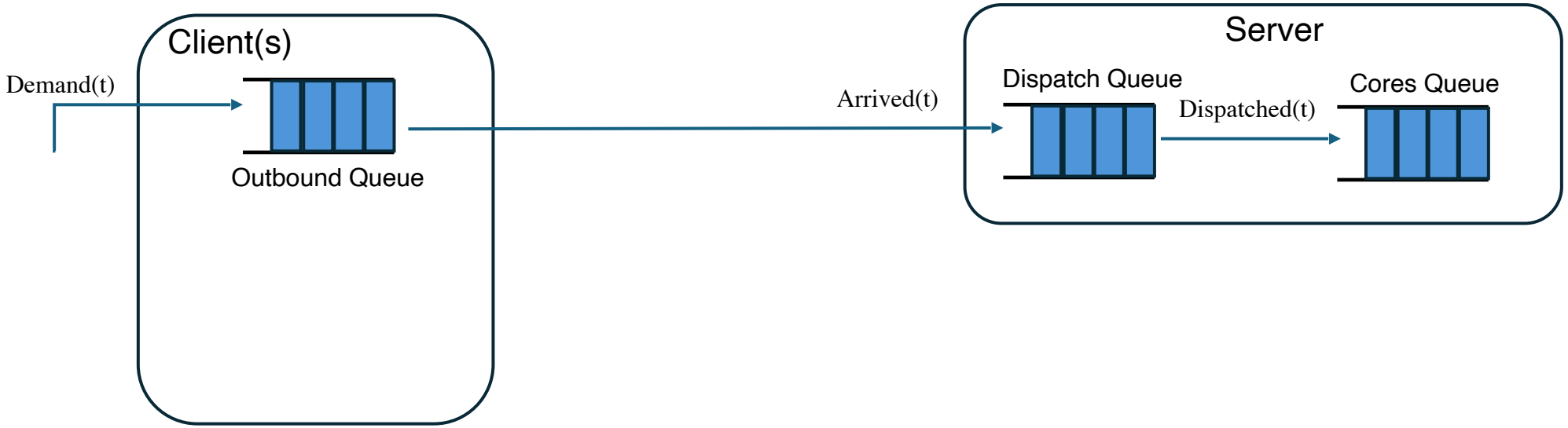

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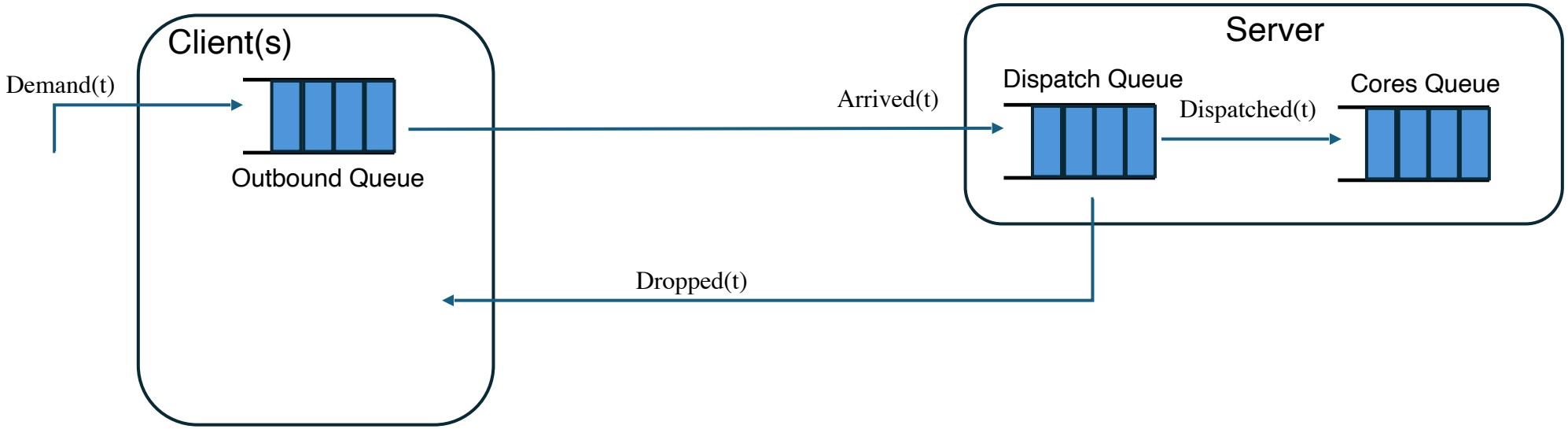

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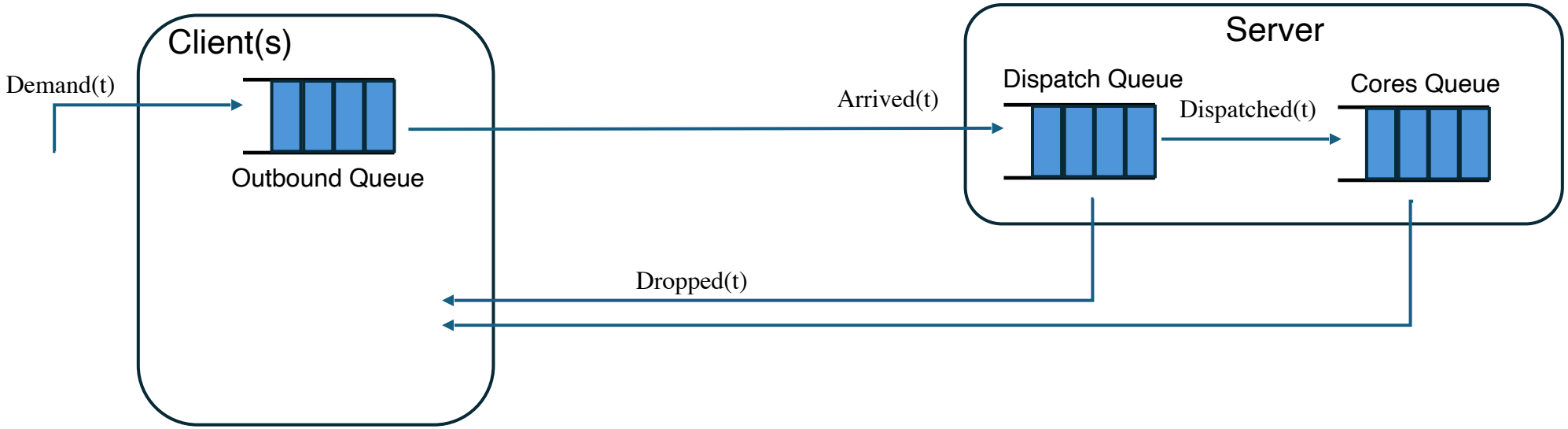

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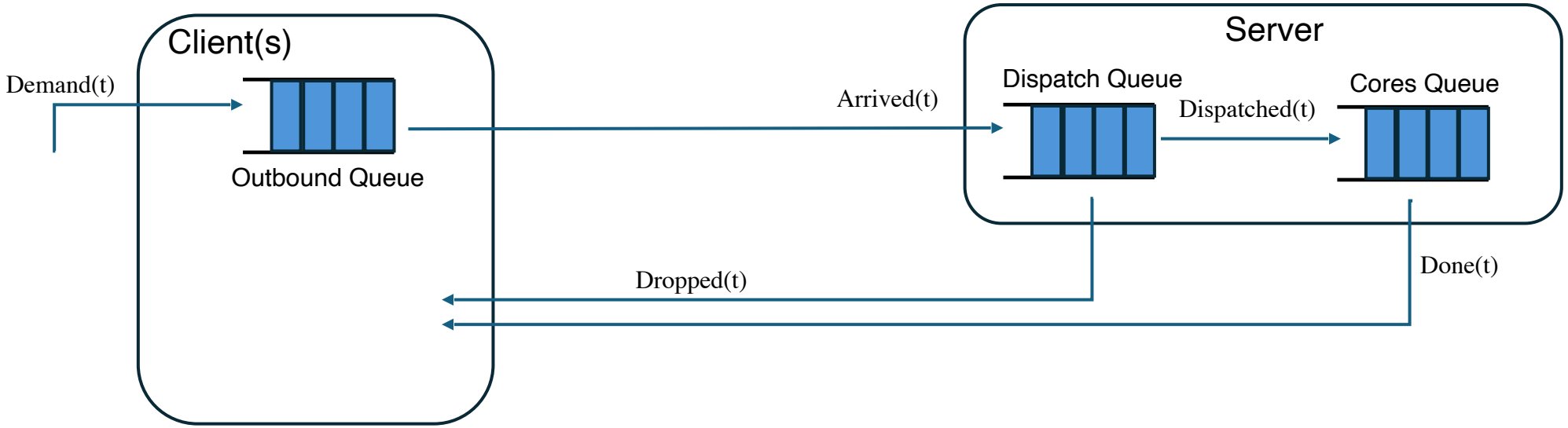

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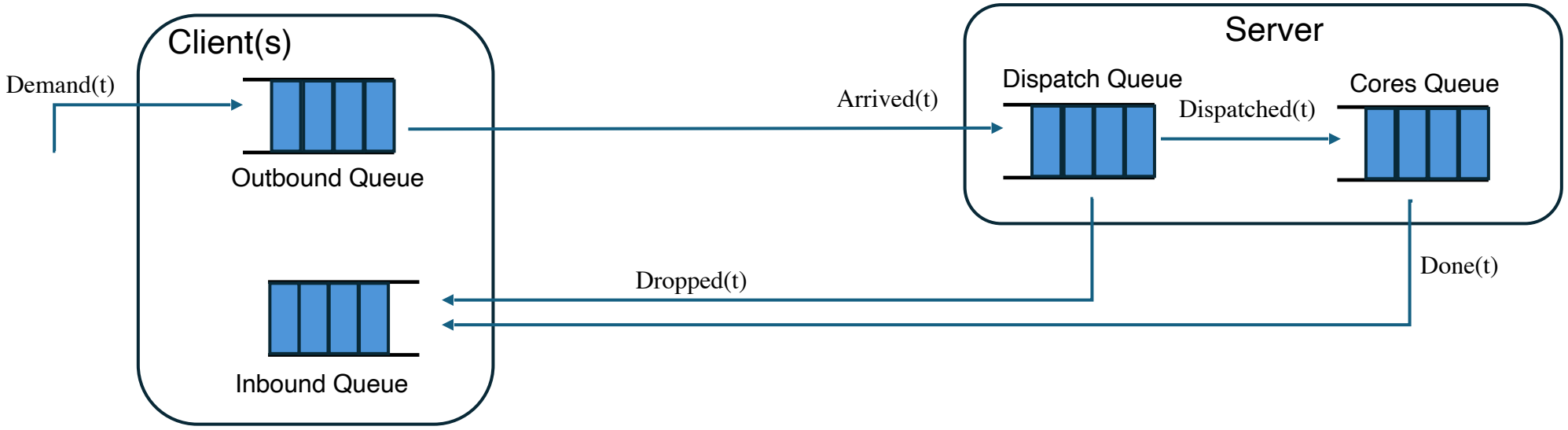

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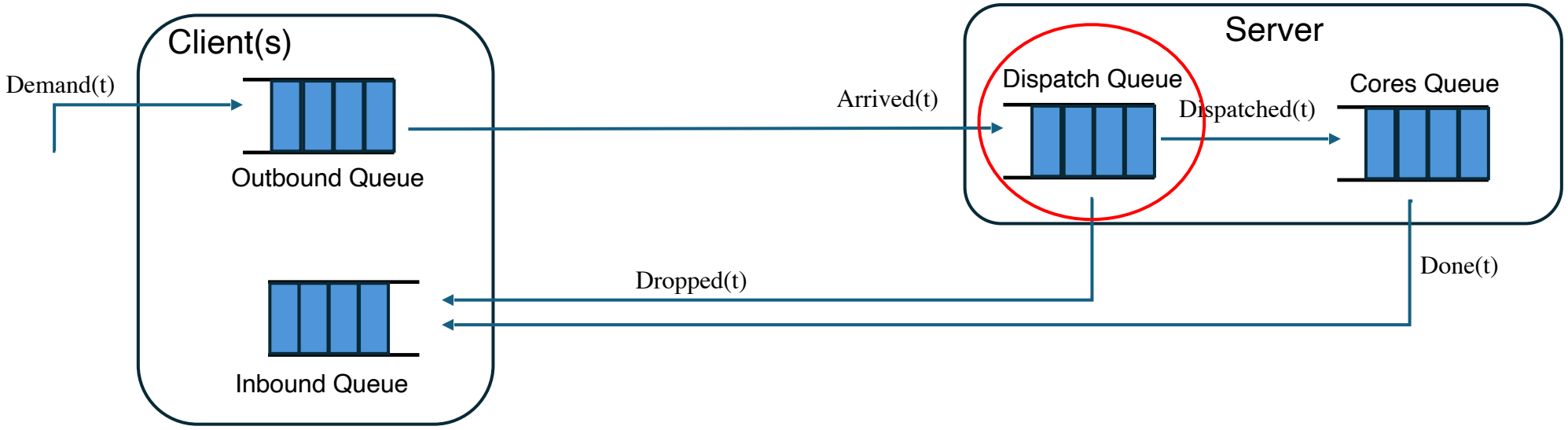

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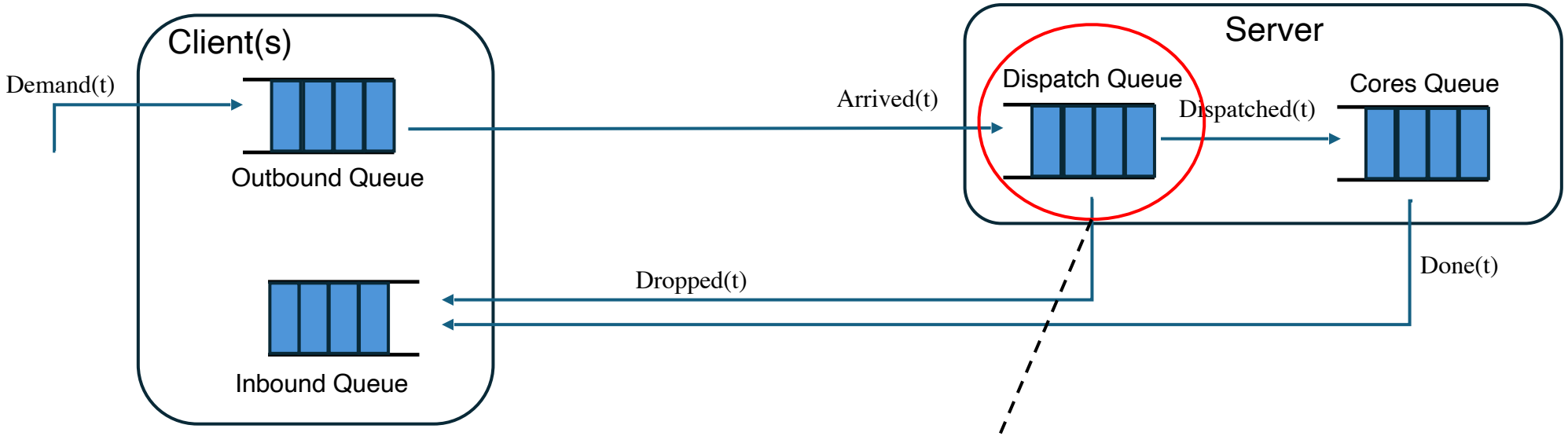

CoDel-like AQM Constraint on Dispatch Queue

$$\frac{d}{dt}(\text{arrived(t)}) > 0 \bigwedge \frac{d}{dt}(\text{dropped(t)}) > 0 \Rightarrow \text{delay[t]} > \boldsymbol{Threshold}$$

Overload Control: **Breakwater**

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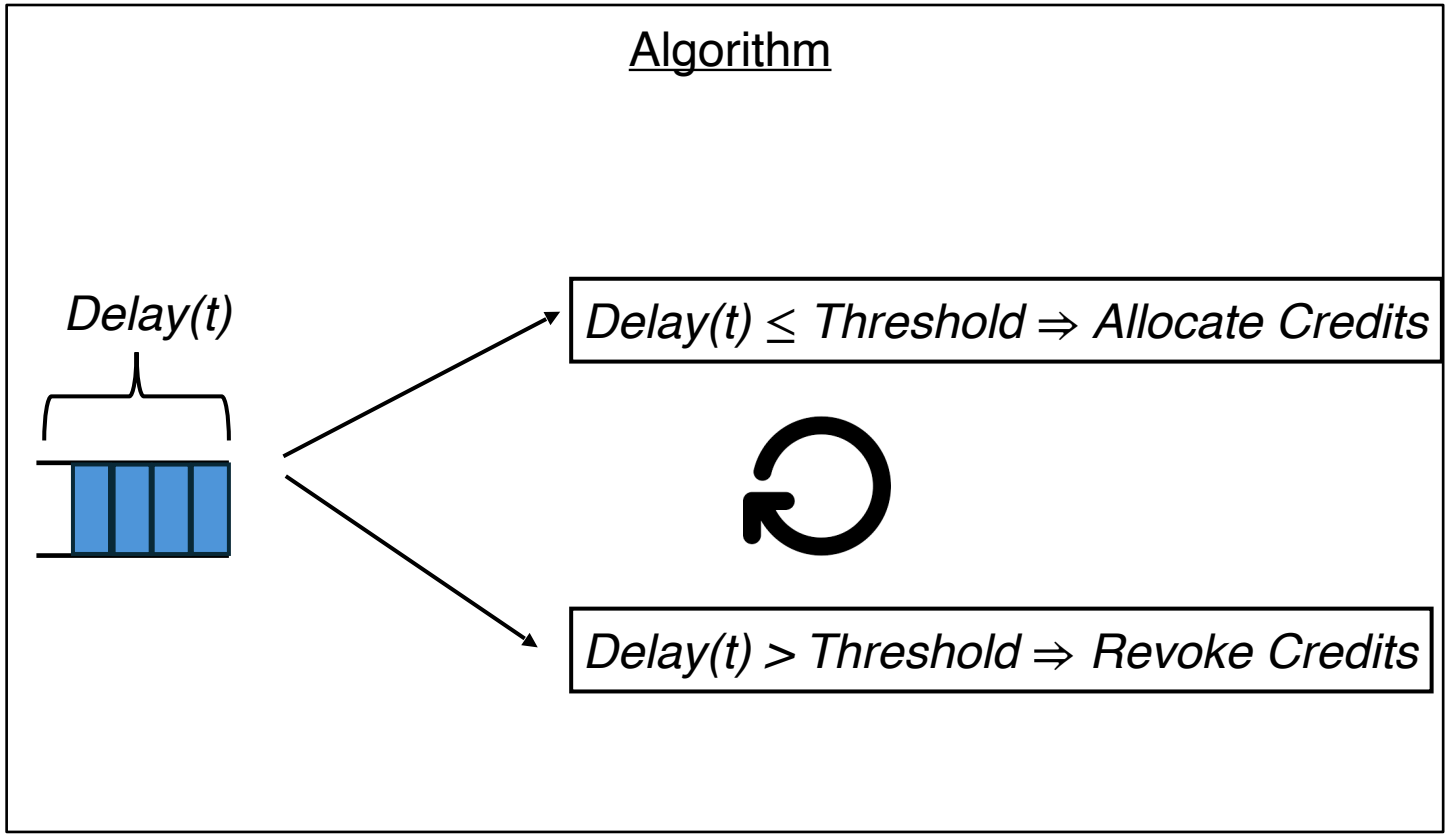

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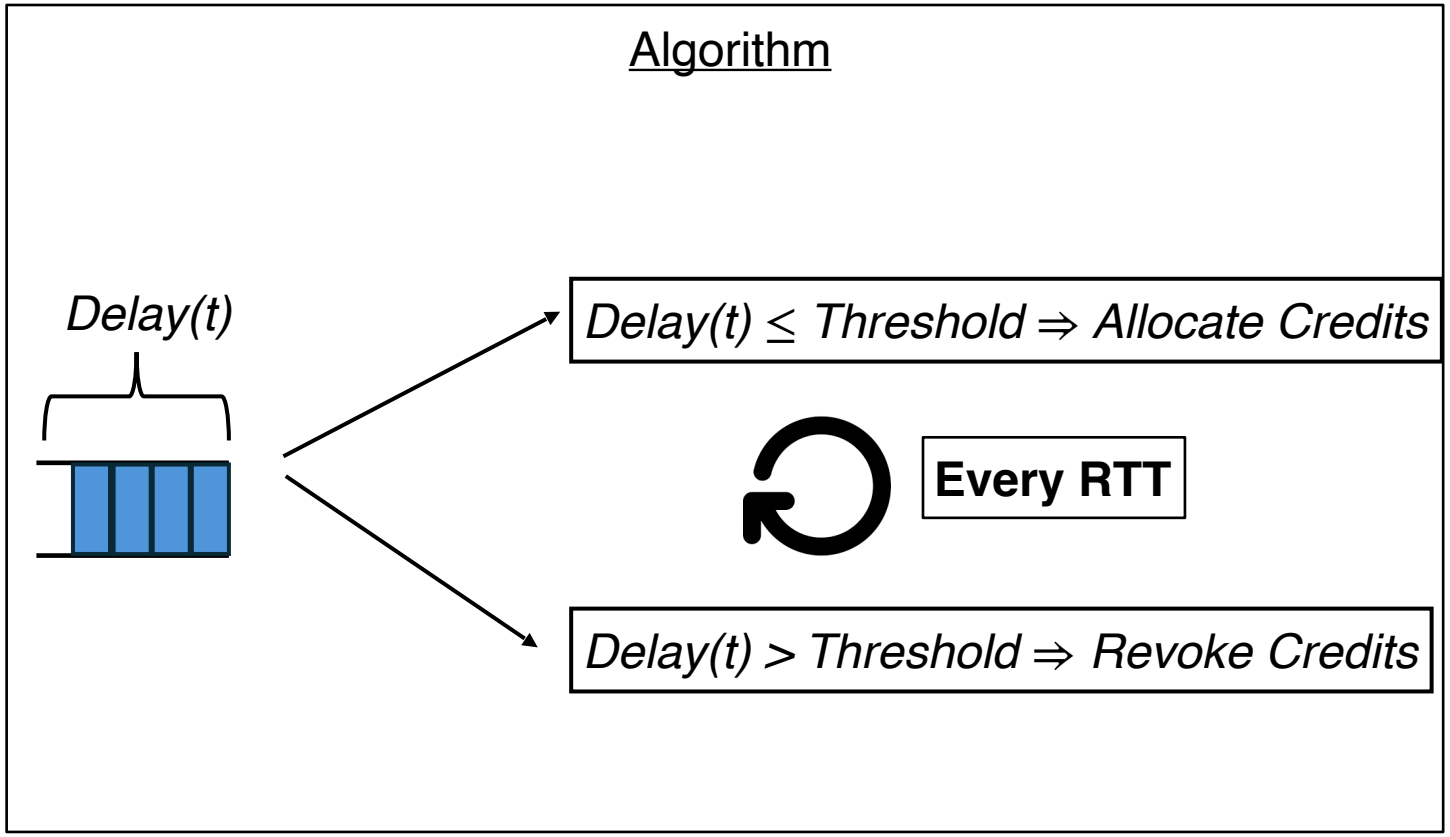
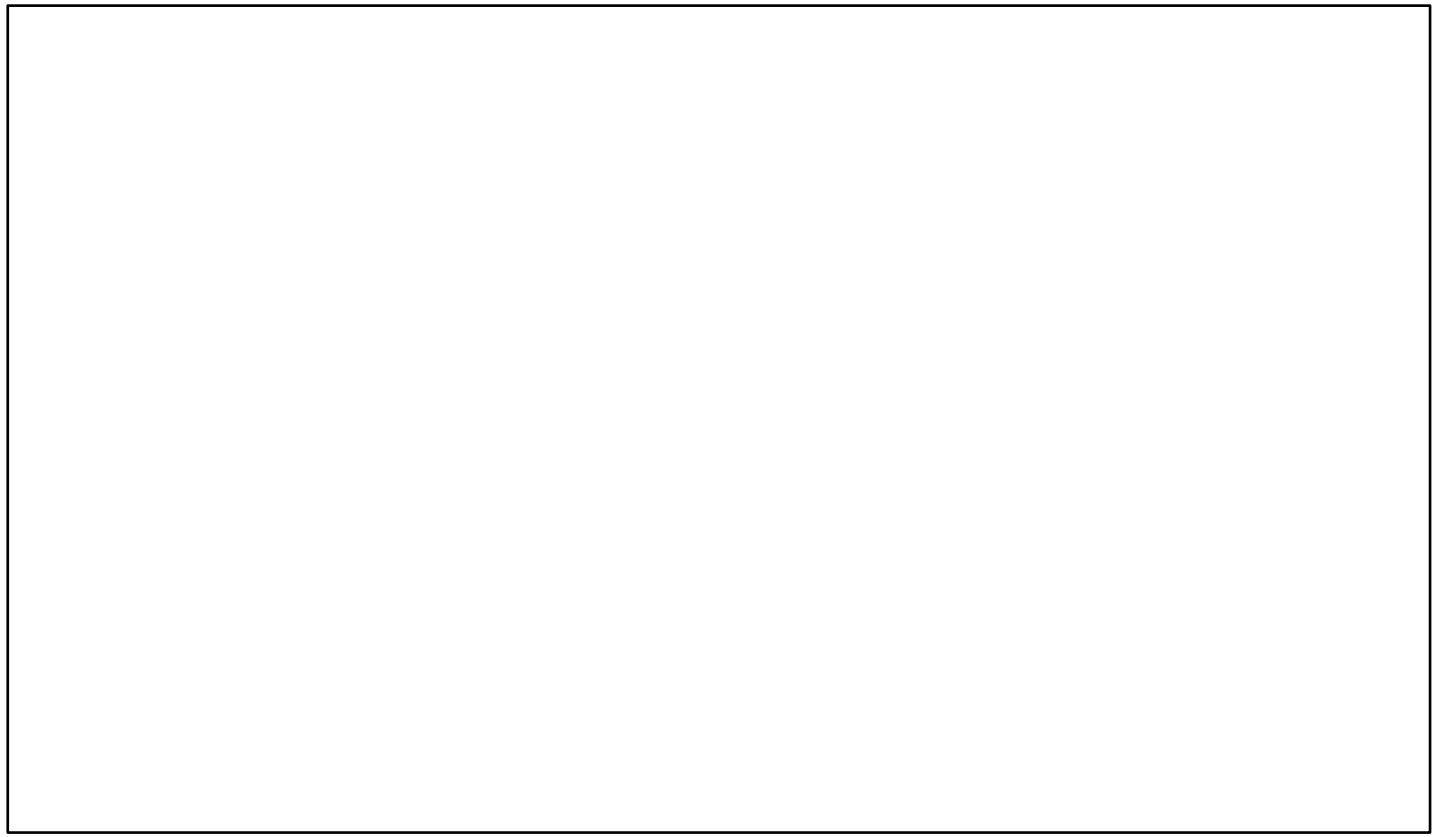


Core Allocation: **Shenango**



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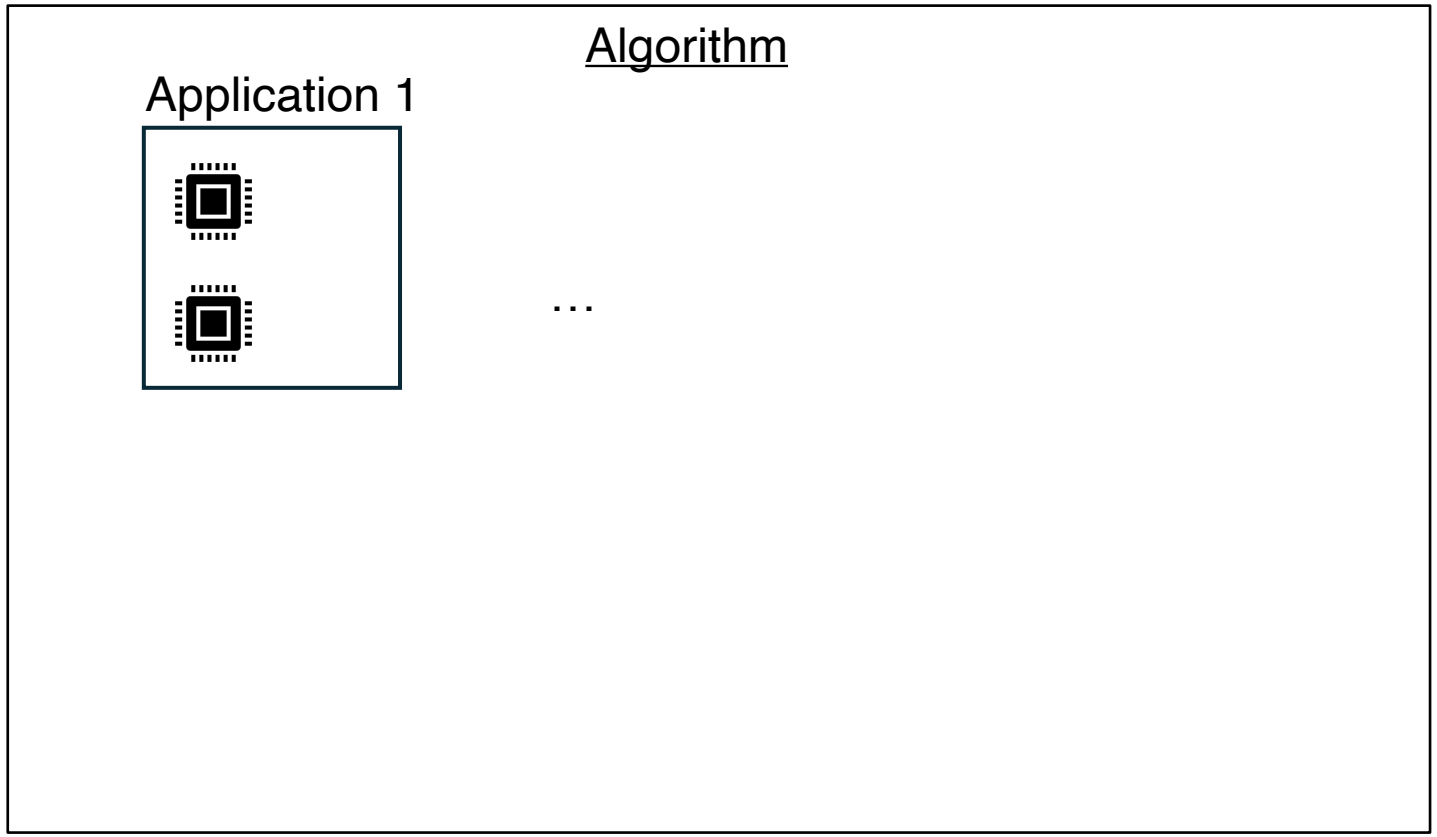

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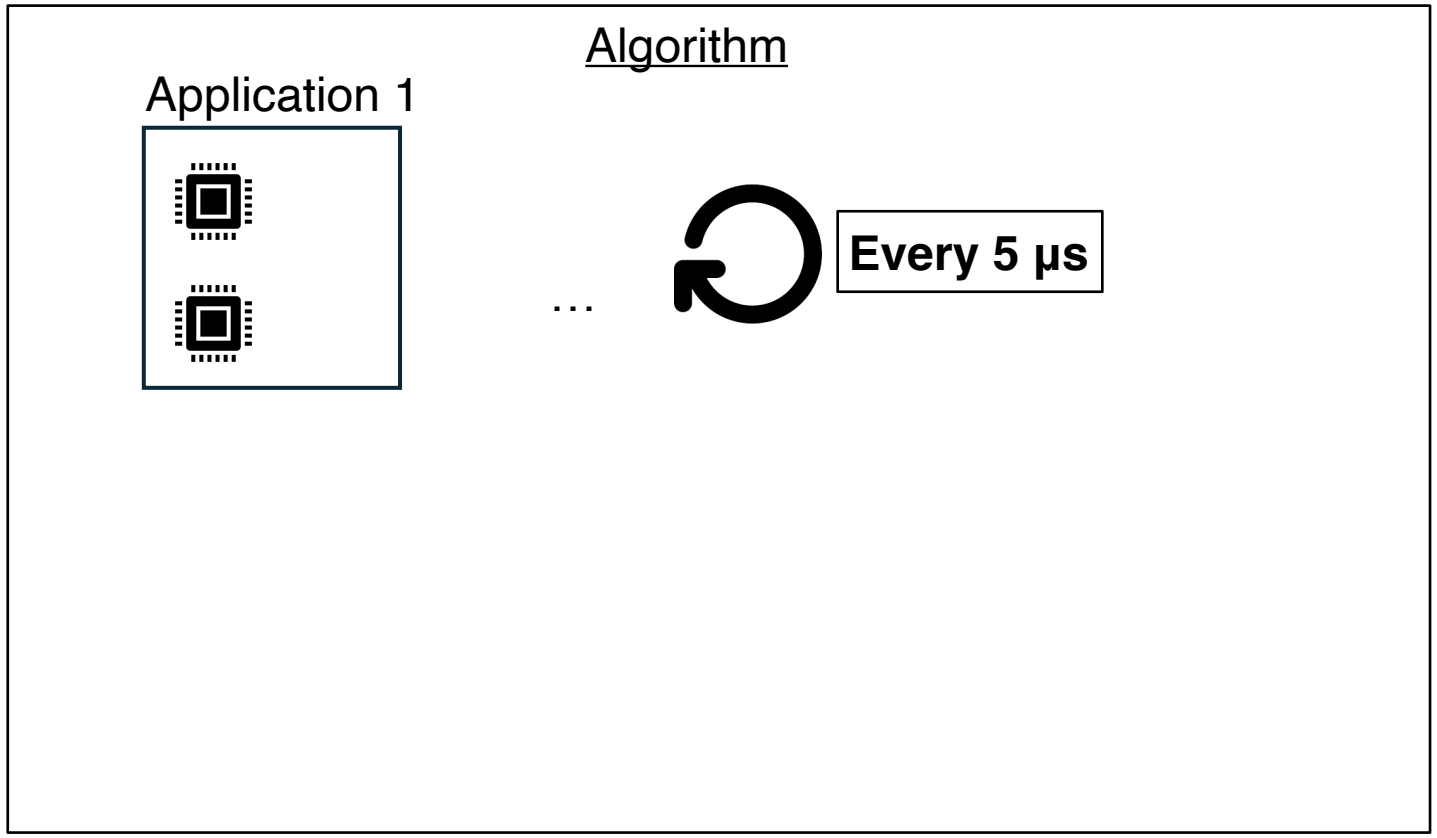

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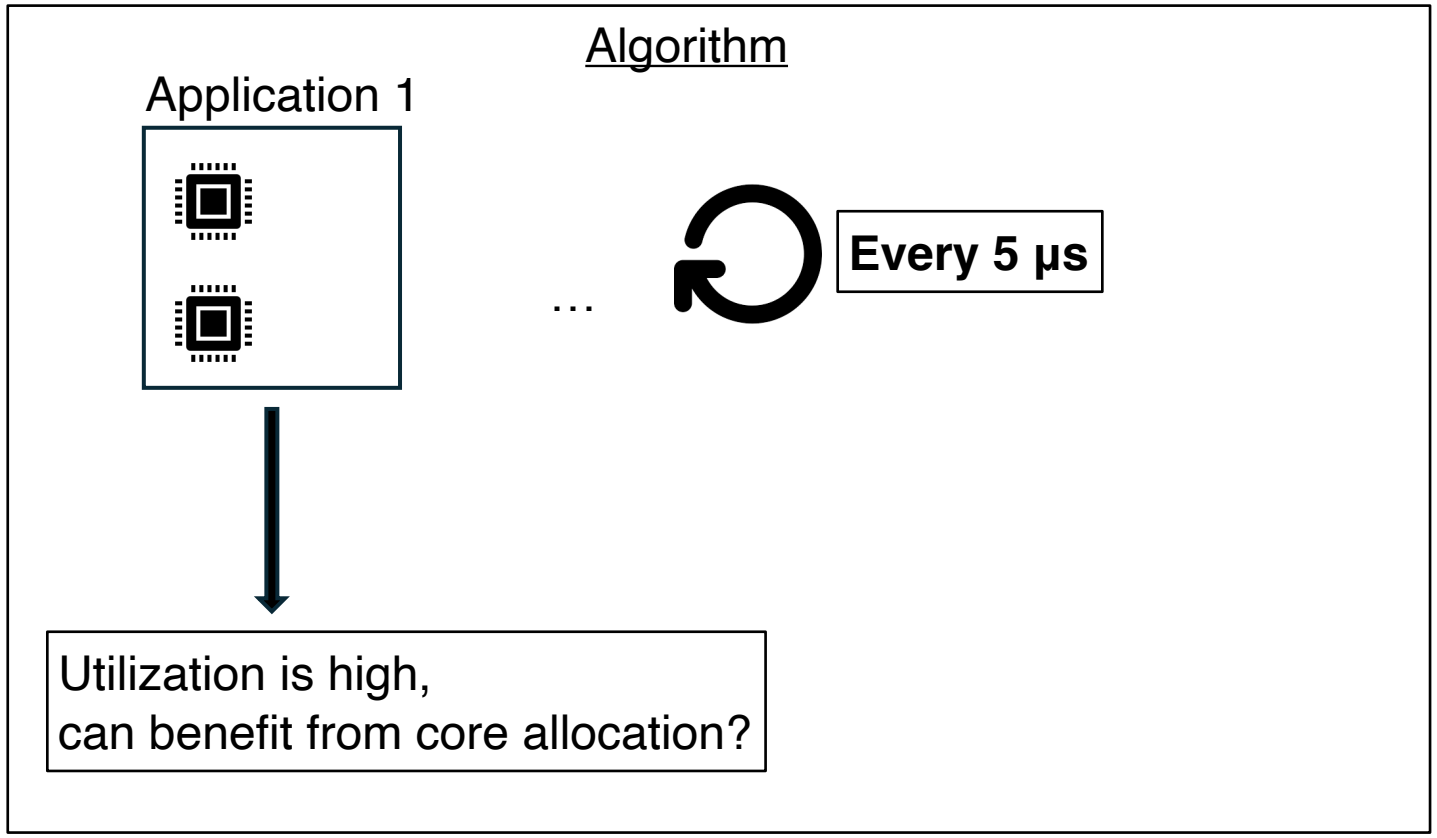

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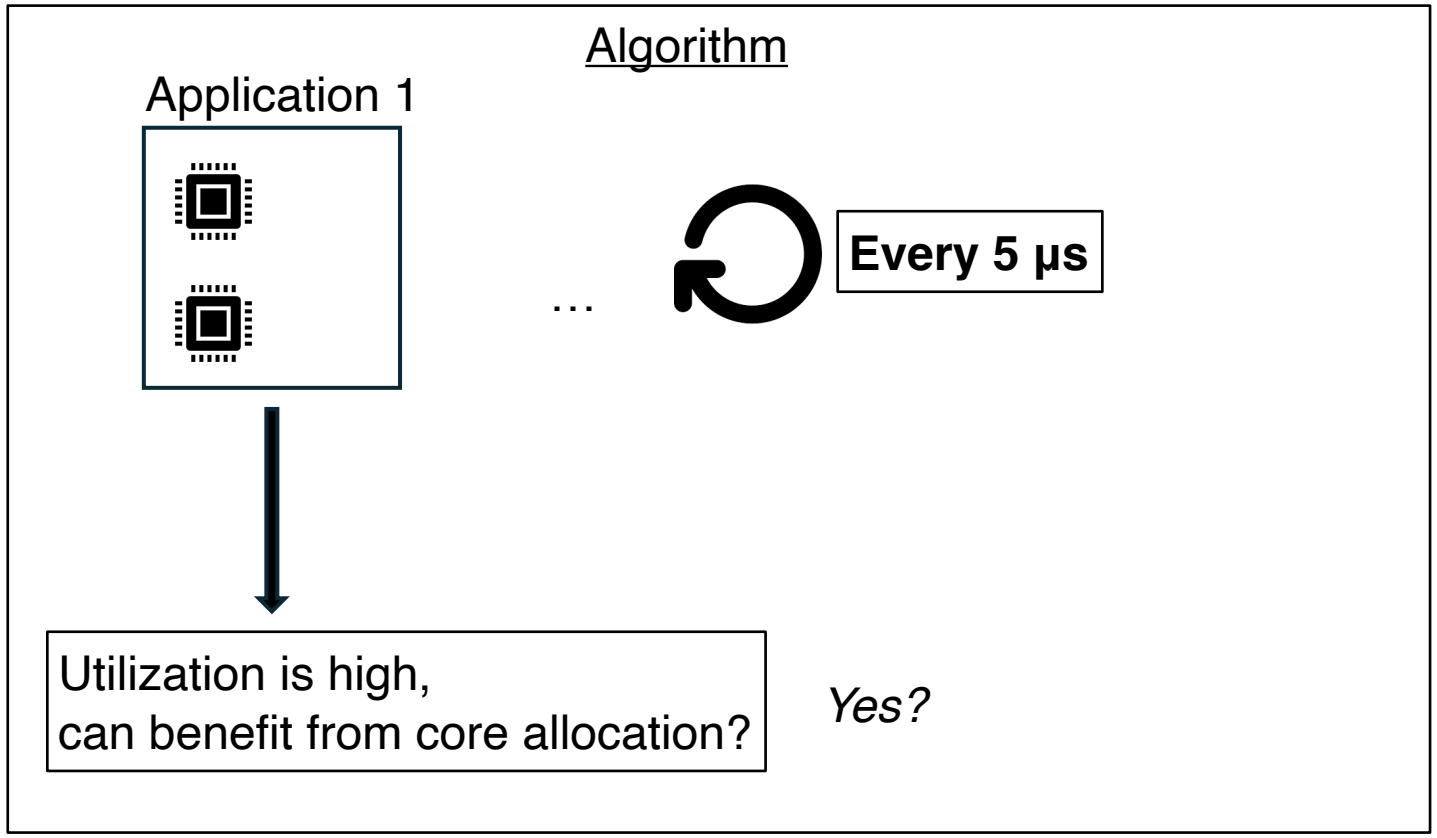

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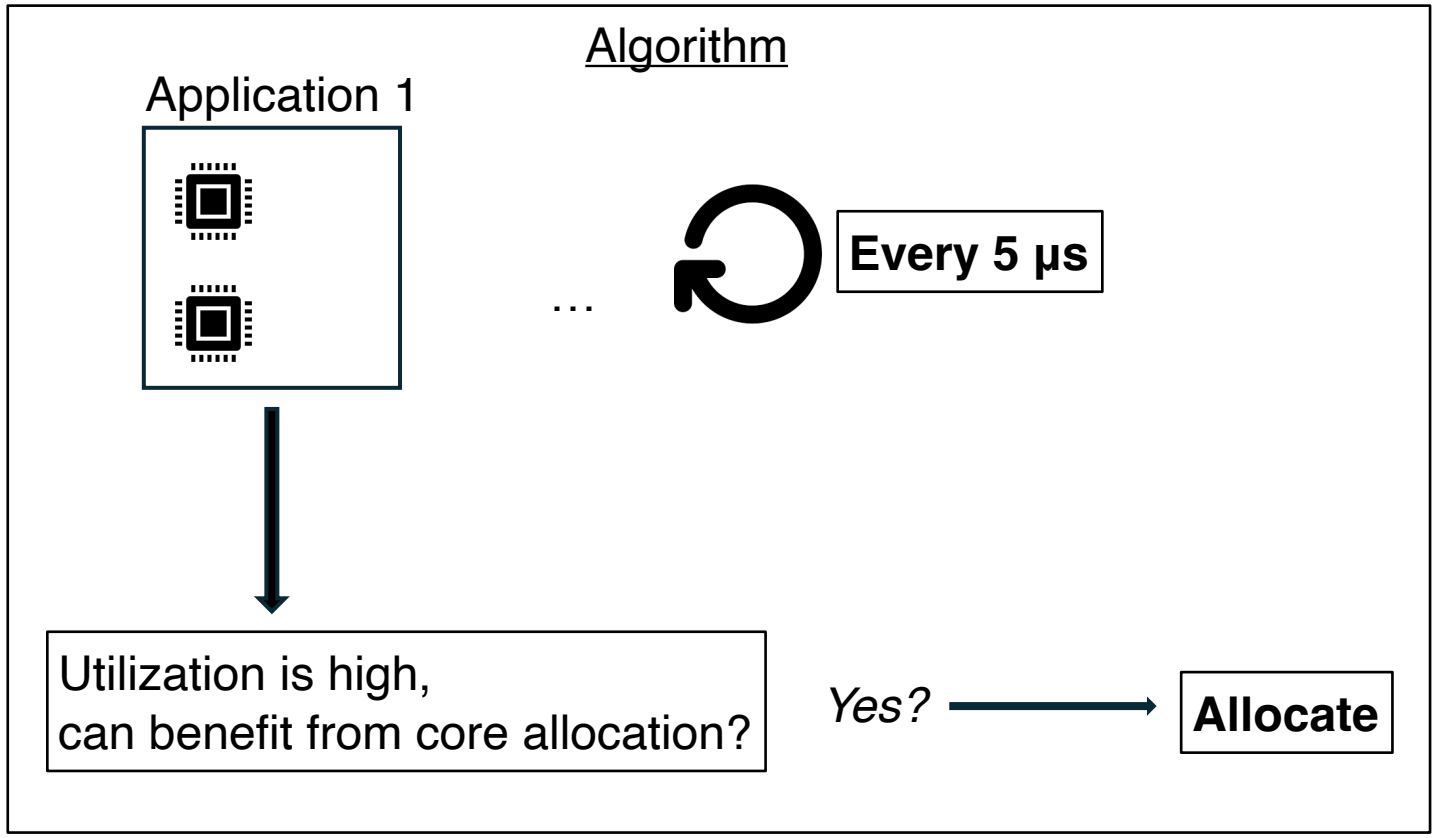

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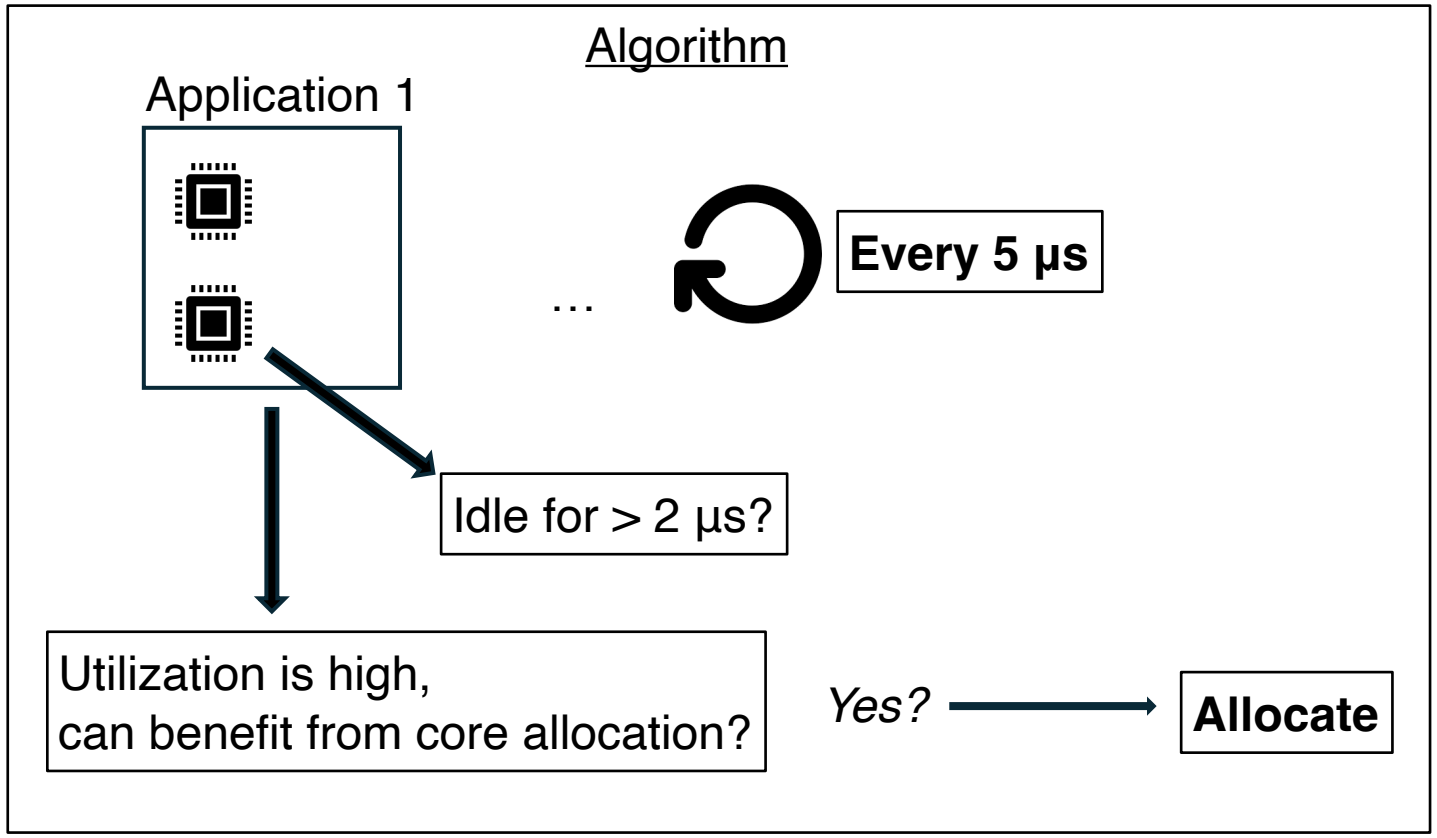

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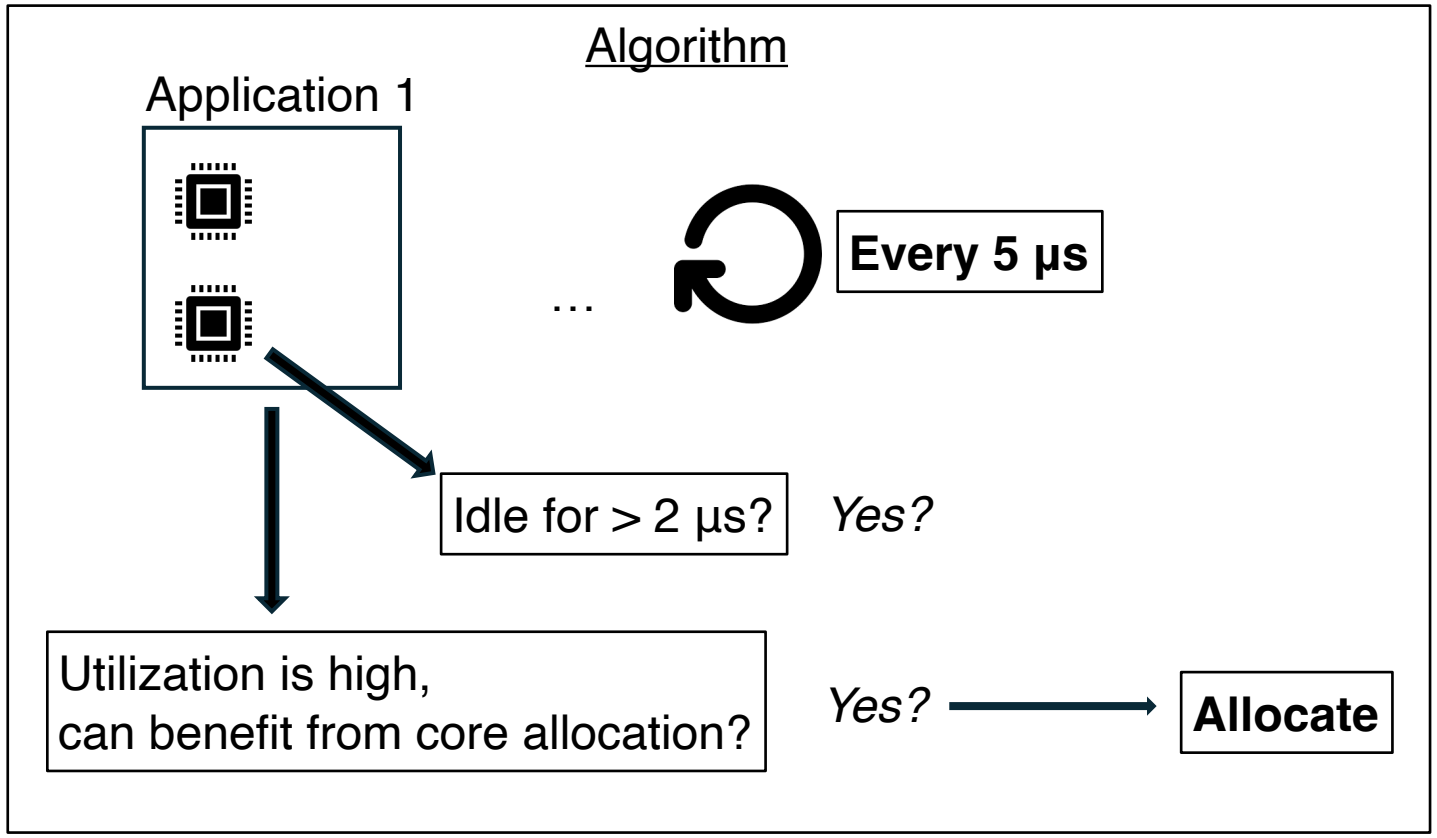

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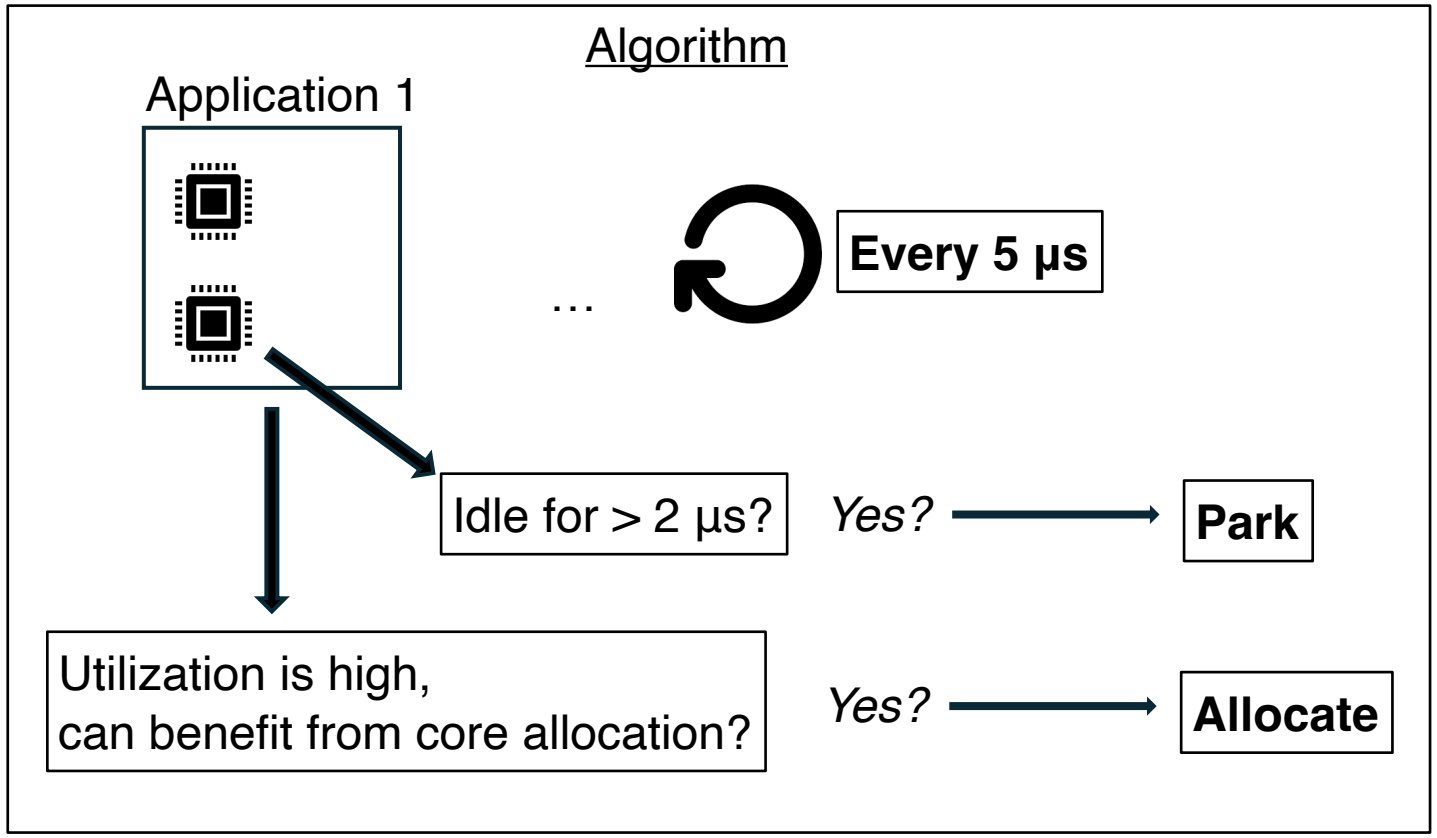

Methodology – Algorithms and Configuration

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Compare 2 policies

- **Static + Breakwater:** Maximum cores are statically allocated for the application
- **Shenango + Breakwater:** Cores dynamically allocated based on Shenango's policy

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Basic Evaluation Configuration

- **Trace Duration:** 200 microseconds
- **RTT:** 20 microseconds
- **Maximum cores available for app:** 20
- **Service time of requests:** 1microsecond to 5 microseconds

Methodology - Performance Queries

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Throughput Query: Given the load on a server, can **x** requests or lower be done over the entire trace **T**?

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Latency Query: Given the load on a server, can the maximum delay over the entire trace **T** be **y** microseconds or higher?

Latency Results

Latency Results

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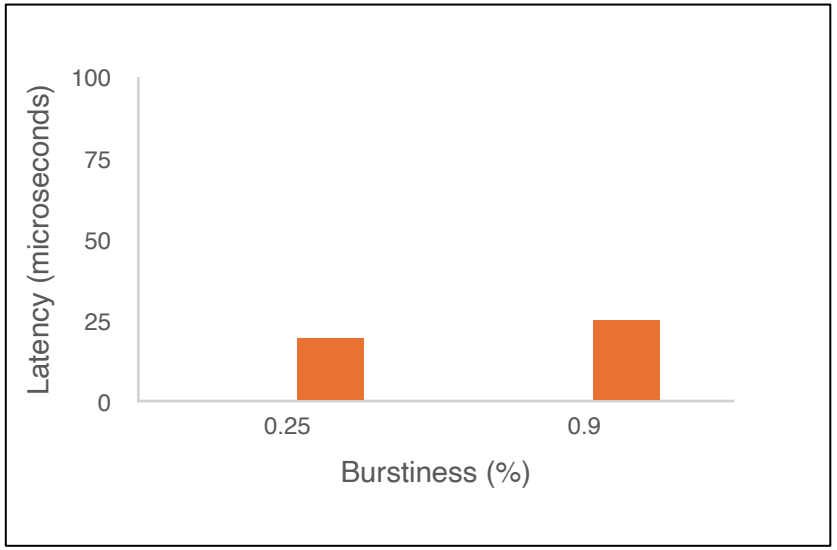
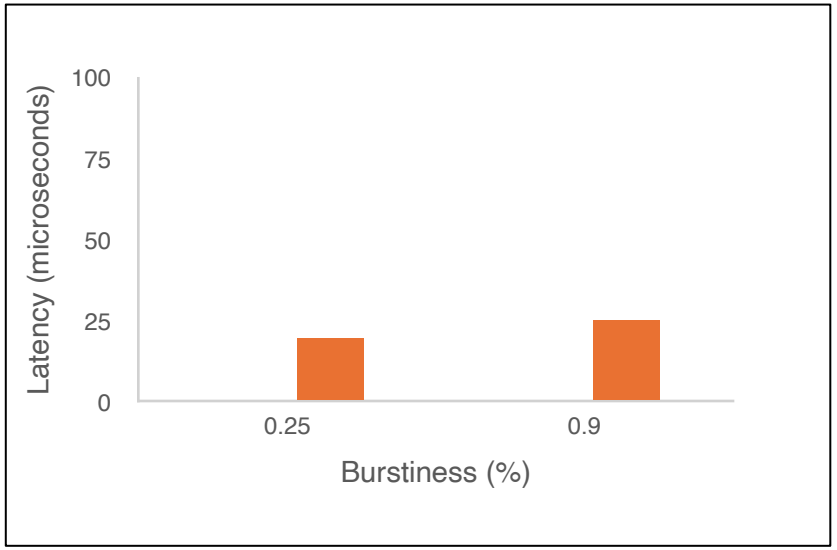
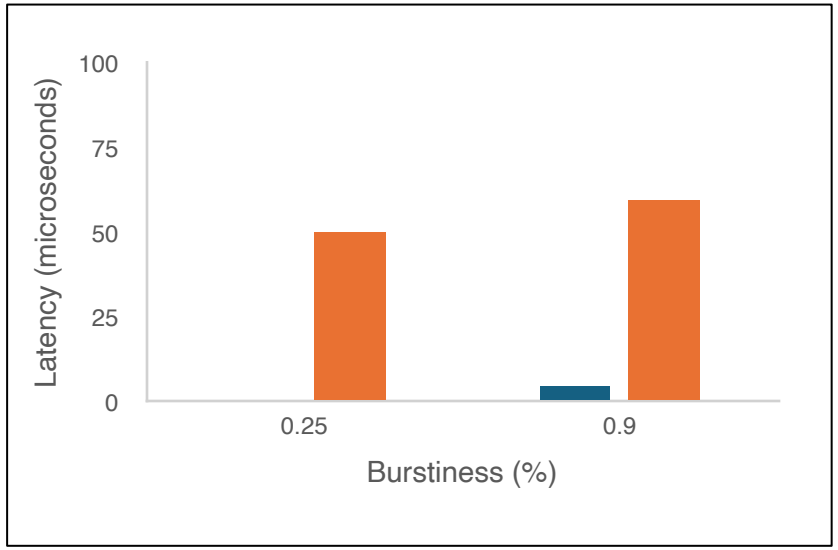


Low Load

Static+Breakwater Shenango+Breakwater

Latency Results





Low Load

High Load

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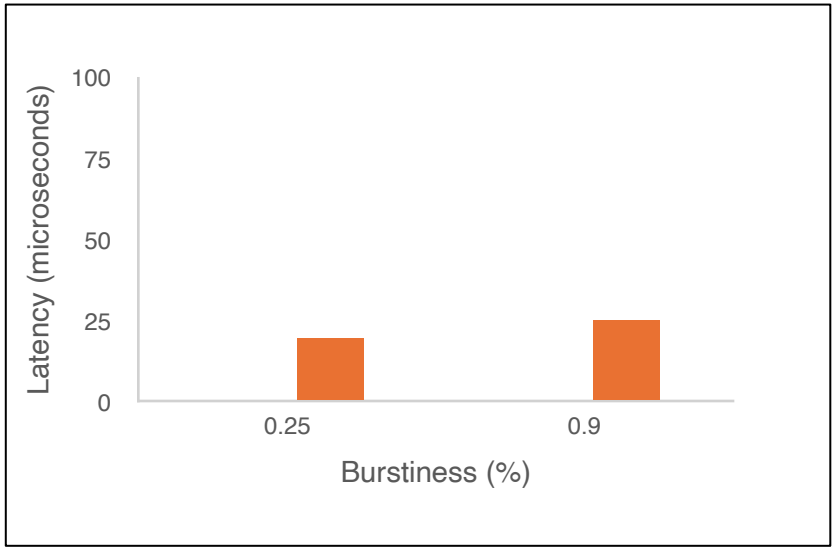
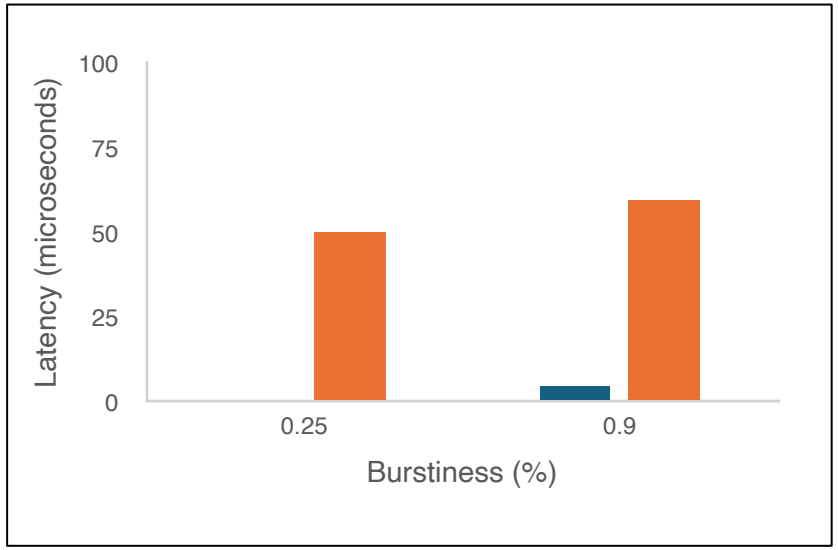
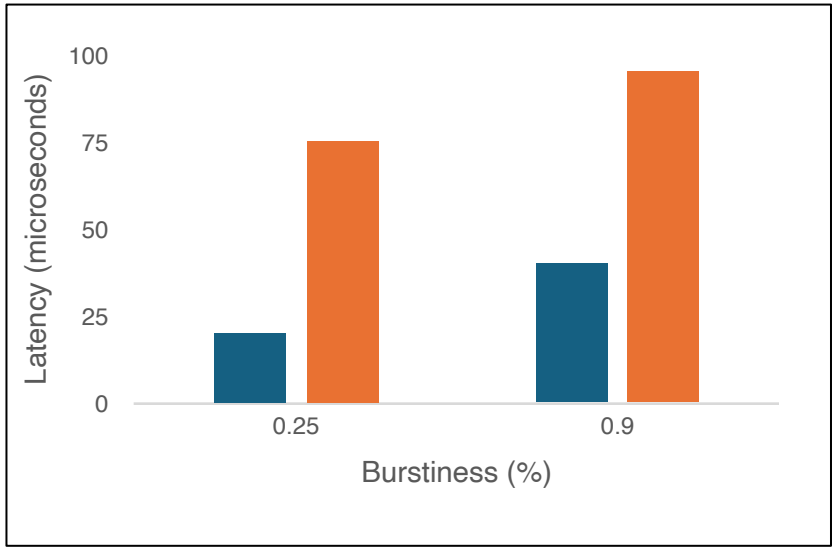
Latency Results







Low Load

High Load

Overload

Static+Breakwater Shenango+Breakwater

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- Use simulation with similar configurations to find traces that exhibit non-trivial worst-case behavior
- Traces eventually found would be hard to get without knowledge of performance guarantees provided by our tool

CoreSync: Use partial proportionality to maintain credits available to clients based on number of cores allocated (ICNP 2025)

Conclusion

- Existing models are limited in analyzing performance tradeoffs in multi-controller servers in datacenters.
- We present a modular **performance verification** framework built on an SMT solver to provide non-trivial worst-case performance guarantees.
- Our tool is evaluated on *Shenango*, a core allocation algorithm, and *Breakwater*, an overload control algorithm, for establishing bounds on Throughput and Latency.

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Thank You!