Lablel	Design Requirement Description	Stimulus Generation	Functional Covarage	Functionality Check
FIFO_1	when rst_n is asserted the data_out signal will be zero and wr_ack flag will be low, overflowflag will be low, full flag will be low, empty flag will be high, almostfull flag will be low, almostempty flag will be low, underflow flag will be low	Directed at the start of simulation	$wr_en_cp that cover the value of wr_en in 2 bins 1- zero : that cover the zero value of wr_en 2- one : that cover the one value of wr_en $rd_en_cp that cover the value of rd_en in 2 bins 1- zero : that cover the zero value of rd_en 2- one : that cover the one value of rd_en $underflow_cp that cover the value of underflow in 2 bins 1- zero : that cover the zero value of underflow 2- one : that cover the one value of underflow $wr_ack_cp that cover the value of wr_ack in 2 bins 1- zero : that cover the zero value of wr_ack 2- one : that cover the one value of wr_ack $overflow_cp that cover the value of overflow in 2 bins 1- zero : that cover the zero value of overflow 2- one : that cover the one value of overflow $full_cp that cover the value of full in 2 bins 1- zero : that cover the zero value of full 2- one : that cover the one value of full $empty_cp that cover the value of empty in 2 bins 1- zero : that cover the zero value of empty 2- one : that cover the one value of empty $almostempty_cp that cover the value of almostempty in 2 bins 1- zero : that cover the zero value of almostempty 2- one : that cover the one value of almostempty $cross_wr_ack that cover the all crossing between wr_en_cp & rd_en_cp & wr_ack_cp ignoring the crossing of {wr_en_cp.zero} and { wr_ack_cp.one} $cross_overflow that cover the all crossing between wr_en_cp & rd_en_cp & overflow_cp ignoring the crossing of {wr_en_cp.zero} and { overflow_cp.one} $cross_underflow that cover the all crossing between wr_en_cp & rd_en_cp & underflow_cp ignoring the crossing of {rd_en_cp.zero} and {underflow_cp.one} $cross_full that cover the all crossing between wr_en_cp & rd_en_cp & full_cp ignoring the crossing of {rd_en_cp.one} and {full_cp.one} $cross_empty that cover the all crossing between wr_en_cp & rd_en_cp & empty_cp $cross_almostempty that cover the all crossing between wr_en_cp & rd_en_cp & almostempty_cp $cross_almostfull that cover the all crossing between wr_en_cp & rd_en_cp & almostfull_cp	A checker in the scoreboard class and assertion in the design file to make sure the output is correct
FIFO_2	verify when wr_en is high and rd_en is low - the data_in will stored in the FIFO untill it will be fill -underflow flag still zero - verify when the FIFO Is empty the empty flag will be high - verify whan only one element is stored the almostempty flag will be high - verify when it remain only one element to be stored the almostfull flag will be high - verify when fifo is filled the full flag will be high - verify when the FIFO is full and wr_en is high the overflow flag will be high	Randomized using FIFO_Transaction Class		A checker in the scoreboard class and assertion in the design file to make sure the output is correct
FIFO_3	verify when rd_en is high and wr_en is low - the data_out will get the elemnt from FIFO memory -overflow flag still zero - verify when it remain only one element to be stored the almostfull flag will be high - verify when the FIFO Is empty the empty flag will be high - verify whan only one element is stored the almostempty flag will be high - verify when FIFO does not have any element the empty flag will be high - verify when the FIFO is empty and rd_en is high the underflow flag will be high	Randomized using FIFO_Transaction Class		A checker in the scoreboard class and assertion in the design file to make sure the output is correct
FIFO_4	verify the read and write operation and check all the flag - verify when it remain only one element to be stored the almostfull flag will be high - verify when the FIFO Is empty the empty flag will be high - verify whan only one element is stored the almostempty flag will be high - verify when FIFO does not have any element the empty flag will be high - verify when the FIFO is empty and rd_en is high the underflow flag will be high - verify when the FIFO is full and wr_en is high the overflow flag will be high	Randomized using FIFO_Transaction Class		A checker in the scoreboard class and assertion in the design file to make sure the output is correct