Please select related courses which you have done relevant to Full Chip	Design. *
Digital Logic Design/ Digital Electronics	
Analog Electronics / Analog Integrated Circuit	
☐ Very Large Scale Integration (VLSI)	
☐ Verilog/VHDL (coursework/certification)	
Programming Courses(C/C++/Python/Java etc)	
Other:	

Skill And Interest
Select one option for the following questions. Select N/A if you do not have any knowle
HDL Knowledge *
Verilog
SystemVerilog
☐ VHDL
☐ None
Other:
Programming Knowledge *
□ c
□ C++
Python

□ c
C++ -
Python
☐ Java
Others
□ None

☐ Java	
Others	
None	
Which department/s within the Full Chip Design suits you most? *	
Select based on your interest and knowledge. If you do not have any idea about the work/department please select "No Idea". The final decision will be made by the department only after careful evaluation of each candidates	
RTL Design	
Digital verification	
Analog Mixed Signal Modeling and Validation	
Electronic Design Automation (EDA)	
☐ No Idea	
₽	
If you have selected any department on the last question, briefly specify your	

	RTL Design
	Digital verification
	Analog Mixed Signal Modeling and Validation
	Electronic Design Automation (EDA)
	No Idea
If yo	ou have selected any department on the last question, briefly specify your sons.
You	r answer
Sta	to your reasons to join the Soming dust a laborate
318	te your reasons to join the Semiconductor Industry. *
You	ır answer
You	ir answer
	ny do you want to join Ulkasemi? *
Wi	

	If you have selected any department on the last question, briefly specify your reasons.
	Your answer
	State your reasons to join the Semiconductor Industry.*
	Your answer I
	Why do you want to join Ulkasemi? *
	Your answer
,	Where do you want to see yourself in next five and ten years? Write your goals for both. *
	Your answer

Expertise Assessment	
Please state your expertise on what you know in HDL and programming language based on your selection in last section	
[HDL] Select based on you knowledge on Verilog *	
☐ Beginner	
☐ Intermediate	
☐ Expert	
□ N/A	
[HDL] Select based on you knowledge on SystemVerilog *	
_	
Beginner	
☐ Intermediate	
Expert	The same

Please state your expertise on what you know in HDL and programming language based on your selection in last section	
[HDL] Select based on you knowledge on Verilog * Beginner Intermediate Expert N/A	
[HDL] Select based on you knowledge on SystemVerilog * Beginner Intermediate Expert N/A	

Please state your expertise selection in last section	on what you know in HDL and programming language based on your
selection in last section**	Lyou knowledge on Verilog *
[HDL] Select based or	
Beginner	
Intermediate	
[HDL] Select based on	
Decine	You knowledge on SystemVerilog *
Intermediate	
Eynert	You knowledge on SystemVerilog *
	you knowledge on SystemVerilog *
[HDL] Select based on	voji knowledge op.VHDI *

	Expert	
	–	
	□ N/A	
	[UDI]Salasti	
	[HDL] Select based on you knowledge on VHDL *	
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	Degillier	
	Intermediate	
	The internate	
		the second secon
	Expert	
	N/A ,	
	The state of the s	
	In-	
	[Programming Knowledge] Select based on you knowledge on C *	
	Beginner	
	Intermediate	
Photo Control of the		
	Expert	
	□ N/A	

	Intermediate
	□ Expert
1/1/1/	CALIFOLISH
	VA N/A
1999	A product the state of the state of the state of the production of the state of the
1,319,797	[Programming Knowledge] Select based on you knowledge on C++*
10.377000,774.74	☐ Beginner
19 May 19 19 19 19 19 19 19 19 19 19 19 19 19	✓ Intermediate
	☐ Expert
19, 1990, 114 LA	N/A
Sec. 9/29/2011/11/11/11	
	[Programming Knowledge] Select based on you knowledge on Python *
	☐ Beginner
	Intermediate
	Expert
A PROPERTY OF THE PROPERTY OF	□ N/A
	[Programming Knowledge] Select based on you knowledge on Java *
THE STATE OF THE S	☐ Beginner

	Transfer and the second
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	Please mention which offer programming language p_{θ} force and the experimentary tree of years, θ and were θ/θ^{-1}
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✓ Intermediate	
☐ Expert	
□ N/A	
[Programming Knowledge] Select based on you knowledge on Java *	
Beginner	
Intermediate	
Expert	
N/A	
[Programming Knowledge] State for other knowledge if you know *	
Please mention which other programming language you know and the expertise level of yours, If not answer N/A	
Your Inswer	
Back Next Page 4 of 9	

The name and photo associated with your Google account will be recorded when you upload files and submit this form. Your email is not part of your response.

Section 1: Analog and Digital Circuits

Question 1 (5 min)

Is the circuit combinational logic or sequential logic? Explain in a simple fashion what the relationship is between the inputs and outputs. What would you call this circuit?



Your answer

Guidelines for Question 2-8

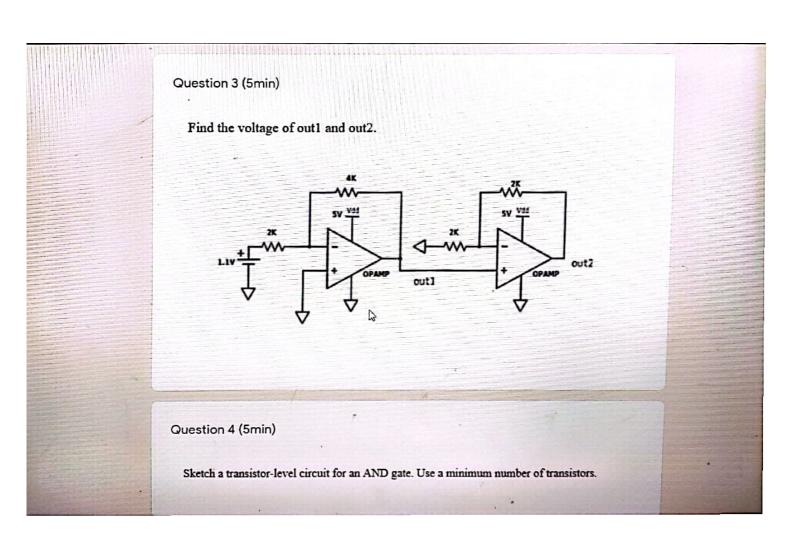
Please write the answers of following questions in extra pages and take snap of them and put all snaps in a single PDF file and upload them at the end of last section

Question 2 (10 min)

Find v1, v2, and v3 in the circuit.

Guidelines for Question 2-8 **Please write the answer's of following questions in extra pages and take snap of them and put all snaps in a single PDF file and upload them at the end of last section** Guestion 2 (10 min) Find v1, v2, and v3 in the circuit. 6 \(\Omega \) 10 \(\nu \) \$\frac{3i}{4} \(\Omega \) \$\frac{3i}{4} \(\Omega \) \$\frac{3}{4} \(\Omega \)

Question 3 (5min)



Your answer

Question 10 (15 min)

Write a program in any programming language to calculate and print the Electricity bill of a given customer. The unit consumed by the user should be taken from the keyboard and display the total amount to pay to the customer. The charge are as follow:

Unit	Charge/unit
upto 199	@1.20
200 and above but less than 400	@1.50
400 and above that less than 600	@1.80
600 and above	@2.00

If bill exceeds tk 400 then a surcharge of 15% will be charged and the minimum bill should be of tk 100/2 Sample Input:

800

Sample output:

unit Consumed :800

Amount Charges @tk 2.00 per unit: 1600.00

Surcharge Amount: 240.00

Net Amount Paid By the Customer: 1840.00

Your answer

Question 11 (5 min)

Question (1 (6 mln)

"Please also write a short description based on your output"

What will be the output of the following code:

```
#include <stdio.h>
int main()
int a = 15; b;
b = (a++) + (a++);
a = (b++) + (b++);
printf("a=*d b=*d", a, b);
return (0);
}
```

Section 2: Hardware Description Language

Question 12 (20 min)

Write an HDL code for the following specifications. Write a linear testbench to verify the design.

Input: clk, reset_n, A, B

Output : AEQB, AGTB, ALTB

The block has an active low asynchronous reset and works on the posedge of clock. The block takes two 4 bit numbers A,B and compares them. There are 3 single bit outputs and they are 1 in the following conditions otherwise 0.

AEQB i.e. A equals B

AGTB i.e. A greater than B

ALTB i.e. A less than B

Your answer

Please submit your answer script (PDF) here *

Scan all your answers from the answer script and upload them (in order) as a single PDF file.

Click	After	Submitting	g
	Te	est	

Implement a full adder using a 3 to 8 decoder. Write down the boolean expression for carry and sum only

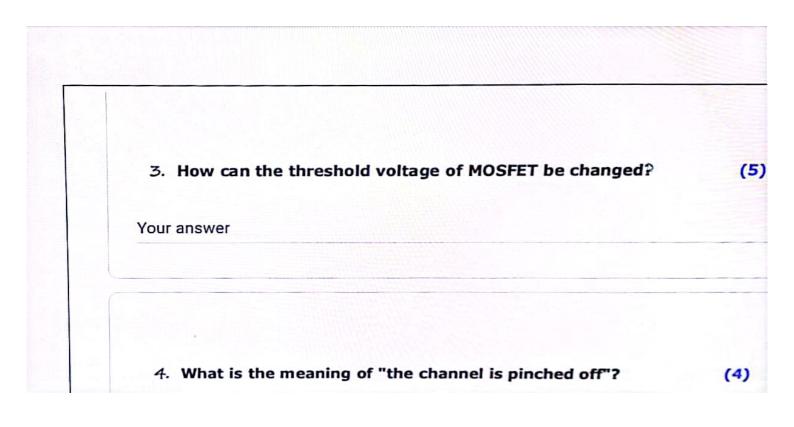
Your answer

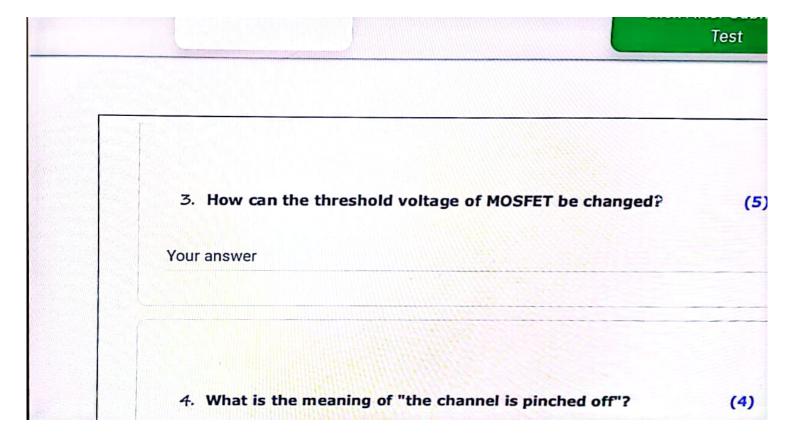
Name the two forms of Boolean expression? Find that two forms of Boolean expression from the following truth table. (5)

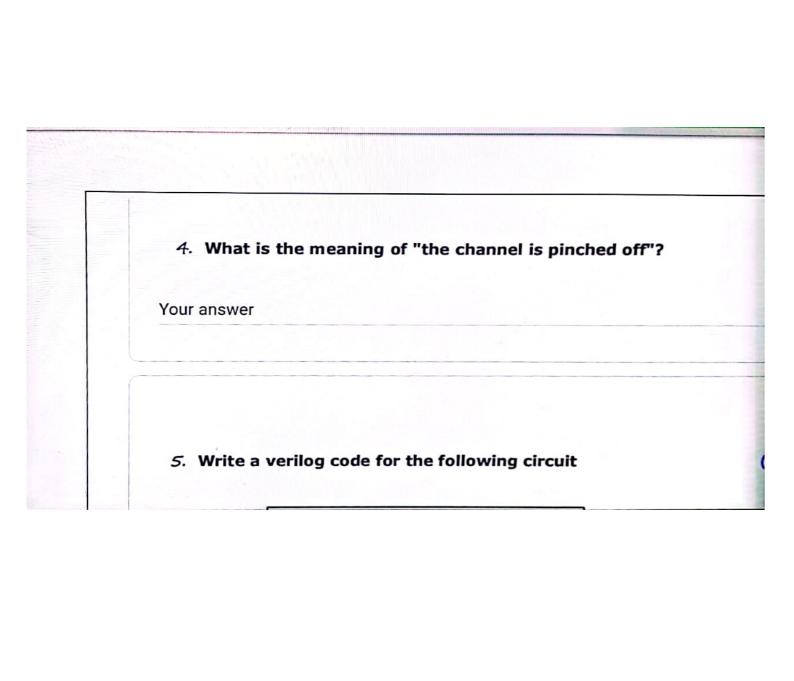
expression from the following traditionic.

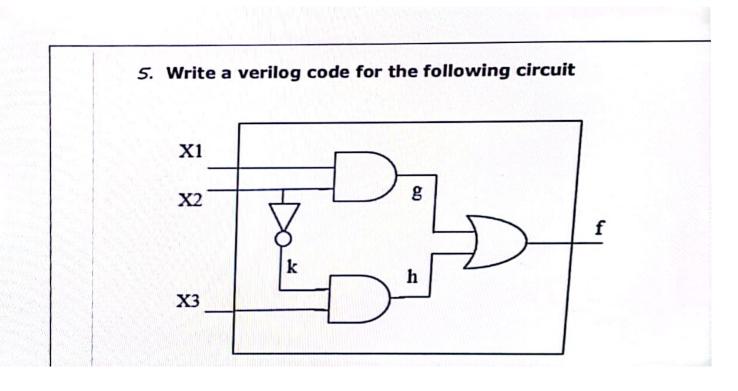
(2)

Output	С	В	Α
, 1	0	0	0
0	1	0	0
1	0	1	0
0	1	1	0
0	0	0	1
1	1	0	1
0	0	1	1
1	1	1	1

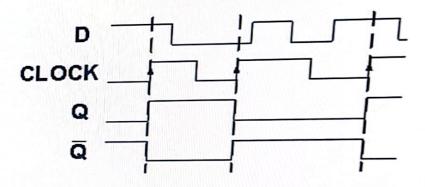








6. Write a verilog code that can generate the following timing diagram (5)



7. Observe the truth table. Write down a verilog code for the circuit that generates the following truth table (5)

Input		01	utput	
x	Y	z	А	В
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1

В	A	z	Y	X
0	0	0	0	0
1	0	1	0	0
1	0	0	1	0
0	1	1	1	0
1	0	0	0	1
0	1	1	0	1
0	1	0	1	. 1
1	1	1	1	1

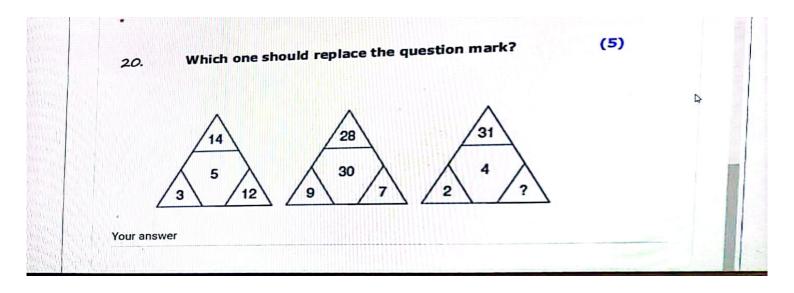
```
o. Fillu tile value ol ont-i Atlieli pelect-n alin pelect-t
          module pnr (
          input [2:0] a, b, c,
          input [1:0] select,
          output reg [2:0] out,
          );
           always @ (a, b, c, select) begin
            case(select)
               2'b01
                       : out=a;
               2'b10
                      : out=b;
               2'b11 : out=c;
               default : out =0;
            endcase
           end
          endmodule
```

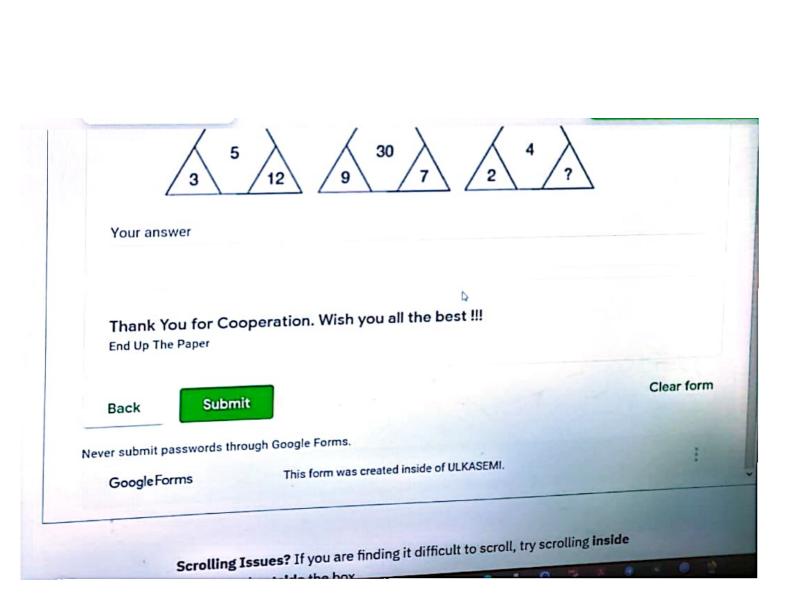
19. If 9th March 2011 was Sunday, what was the day of the week on 1st

(4)

March 2008?

19. If 9th March 2011 was Sunday, what was the day of the week on 1st March 2008?	
Your answer	۵
•	-
20. Which one should replace the question mark? (5)	
28 31	2





```
8. Find the value of out=? When select=0 and select=1
                                                                          (5)
         module pnr (
         input [2:0] a, b, c,
         input [1:0] select,
         output reg [2:0] out,
         );
          always @ (a, b, c, select) begin
            case(select)
              2'b01
                      : out=a;
              2'b10
                     : out=b;
              2'b11 : out=c;
              default : out =0;
            endcase
```

9. Calculate the frequency of the following code

`timescale 1ns/100ps module gen1; reg a; initial a = 0; always #2 a = ~a; endmodule

10. Find the output of the following program (4)

```
{
for (int i=1;i<=4;i++)
        switch (i)
case 1:
        printf("a/n");
        break;
case 2:
        printf("b/n");
        break;
case 3:
        printf("c/n");
        break;
case 4:
        printf("\nd");
        break;
```

Find the output of the following code

```
#include <iostream>
using namespace std;
int main()
{
   int i, j, k;
   int n = 5;
   for (k = 1; k <= n; k++)
   {
      for(j = 1; j <= n-k; j++)
            cout << '';
      for (i = 1; i <= 2*k-1; i++)
            cout << "*";
      cout << endl;
   }
   return 0;
}</pre>
```

12. Write a program to find the factors of a given number

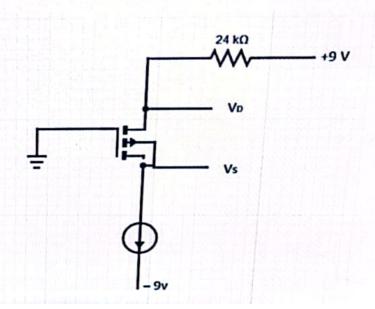
(Example: 1,2,3,6 are the factors of number 6)

Your answer

- 13. A gas station has the following price list
 - a. Diesel 80 tk/ltr
 - b. Petrol 100 tk/ltr
 - c. Compressed gas 50 tk/cc

Write a code to calculate the final price to pay of bought amoun

14. The transistor parameters are $V_{TN} = 0.6 \text{ V}$ and $n = 0.2 \text{ mA} / V_2$, find V_S and V_D .



4

16. The power dissipated across the 1 Ω is 2.25 W. If the open circuit voltage between a & b is 6 V, then R = ? (5)

