(a) Hardware architecture of the convolutional layer
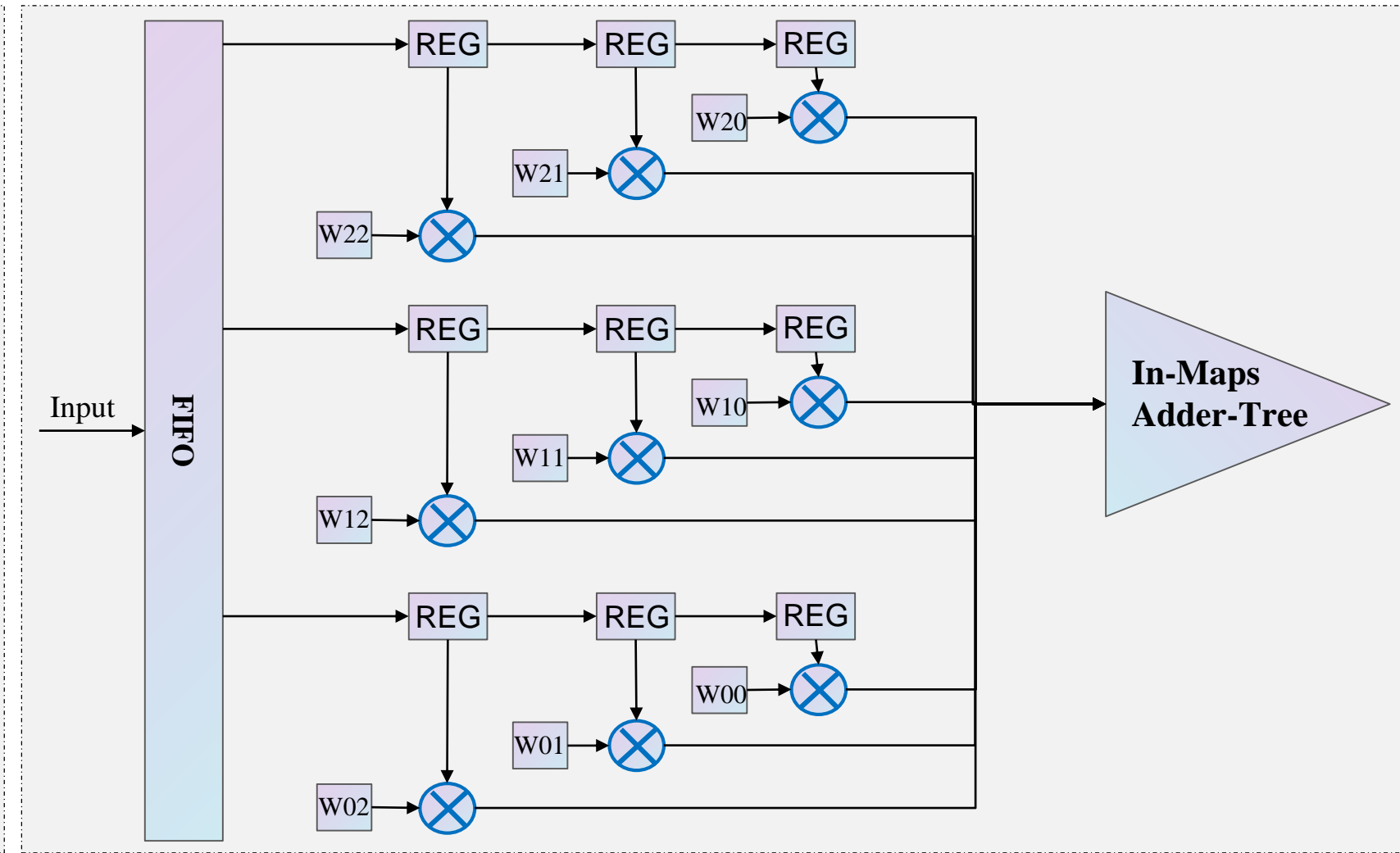
(b) Architecture of processing element in a convolutional unit using 3×3 kernel size