54S/74S89
54LS/74LS89 (Preliminary data)

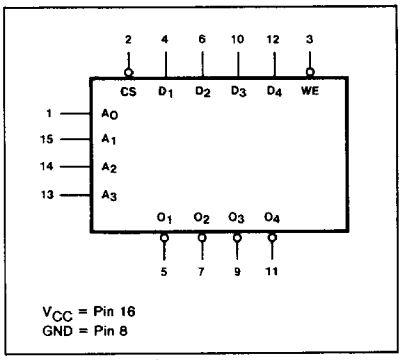
DESCRIPTION

The "89" is a 64-Bit high-speed Read/Write Random Access Memory for use as a "scratch pad" memory with non-destructive read-out. Memory cells are organized in a matrix to provide 16 words of four bits each. Four buffered Address (A_0-A_3) inputs are decoded on the chip to select one of the sixteen memory words for read or write operations. Four buffered Data inputs (D_1-D_4) and four open-collector data outputs are provided for versatile memory expansion. Data at the outputs is inverted from the data which was written into the memory. When the write mode is selected the outputs are the complement of the data inputs.

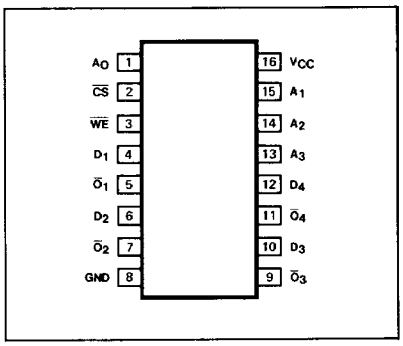
FEATURES

- **16-words by 4-bit memory**
- **On-chip address decoding**
- **Inverted data at outputs**
- **Open collector outputs for easy expansion**

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +70°C	MILITARY RANGES V_{CC}=5V±10%; T_A=−55°C to +125°C
Plastic DIP	N74S89N • N74LS89N	
Ceramic DIP	N74S89F • N74LS89F	S54S89F • S54LS89F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE[a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0-A_3	Address inputs	I_{IH} (μA) I_{IL} (μA)		25/10[a] −150/−100[a]	20 −100
$\overline{CS}$	Chip Select (active LOW) enable input	I_{IH} (μA) I_{IL} (μA)		25/10[a] −150/−100[a]	20 −400
$\overline{WE}$	Write Enable (active LOW) input	I_{IH} (μA) I_{IL} (μA)		25/10[a] −150/−100[a]	20 −400
D_1 - D_4	Data inputs	I_{IH} (μA) I_{IL} (μA)		25/10[a] −150/−100[a]	20 −400
$\overline{O}_1$-$\overline{O}_4$	Data (inverting) outputs	I_{OH} (μA) I_{OL} (mA)		+100 16	+100 12/24[a]

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "89" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A one-of-sixteen address decoder selects a single word which is specified by the four Address inputs (A_0-A_3). A READ operation is initiated after the address lines are stable when the Write Enable ($\overline{WE}$) input is HIGH and the Chip Select-Memory Enable ($\overline{CS}$) input is LOW. Data is read at the outputs inverted from the data which was written into the memory.

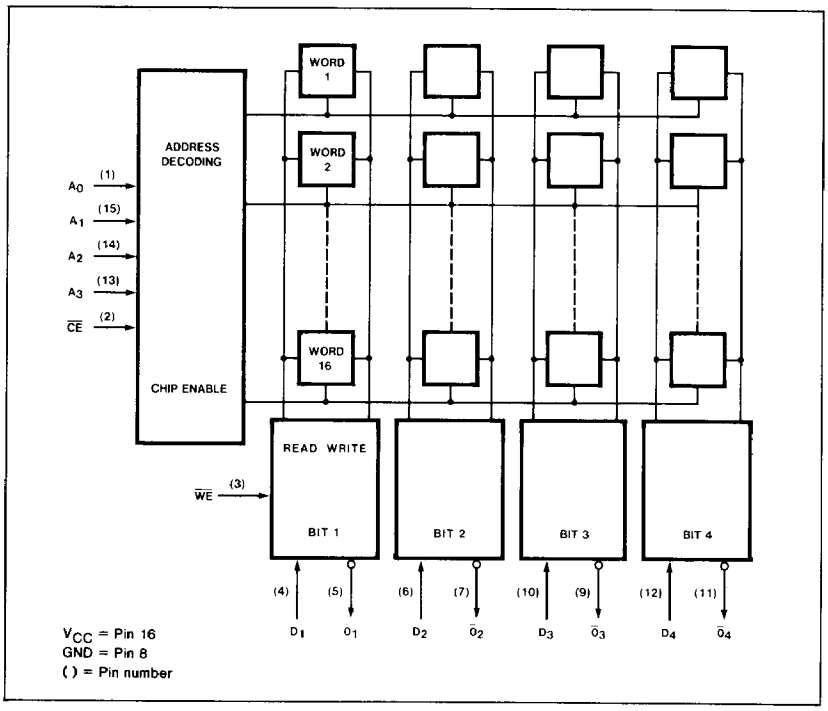
A WRITE operation requires that the $\overline{WE}$ and $\overline{CS}$ inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected the outputs are the complement of the data inputs. The selected memory cells are transparent to changes in the data during the WRITE mode. Therefore, data must be stable one setup time before the LOW-to-HIGH transition of $\overline{CE}$ or $\overline{WE}$.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{CS}$	$\overline{WE}$	D_n	$\overline{O}_n$
Write	L	L	L	H
	L	L	H	L
Read	L	H	X	$\overline{Data}$
Inhibit Writing	H	L	L	H
	H	L	H	L
Store-Disable Outputs	H	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
$\overline{Data}$ = Read complement of data from addressed word location

BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[b]

PARAMETER	TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	V_{CC} = Min, I_{OL} = 16mA	Mil				0.5			V
		Com				0.45			V
	V_{CC} = Min	I_{OL} = 12mA						0.4	V
		I_{OL} = 24mA						0.5[c]	V
I_{CC} Supply Current	V_{CC} = Max	Mil				120		45	mA
		Com				105		37	mA

See BIPOLAR & MOS MEMORY DATA MANUAL for 54S/74S89 AC Characteristics

NOTES

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications

c. This parameter for Commercial Range only.