CONTENTS

Project Name: *BCD to Decimal converter & Decimal Adder Circuit using74HC283, 74HC47.*

Objective:

Our objective is to make a BCD to decimal converter decimal adder circuit using 74HC283 which is a high-speed Si-gate CMOS device component, 74HC47 which is a BCD Decoder & a combinational circuit that converts decimal to BCD in order to represent in the Seven Segment Display.

Usage:

The goal of BCD is to make it simpler to convert human numbers into values that a machine can understand. BCD can automate some tasks and systems for humans and make these processes operate with greater efficiency. The BCD-Adder is used in the computers and the calculators that perform arithmetic operation directly in the decimal number system. The BCD-Adder accepts the binary-coded form of decimal numbers. The Decimal-Adder requires a minimum of nine inputs and five outputs.

Theory:

The digital systems handle the decimal number in the form of binary coded decimal numbers (BCD). A BCD Adder Circuit that adds two BCD digits and produces a sum digit also in BCD. BCD numbers use 10 digits, 0 to 9 which are represented in the binary form 0 0 0 0 to 1 0 0 1, i.e. each BCD digit is represented as a 4-bit binary number. When we write BCD number say 526, it can be represented as

5	2	6
↓	↓	↓
0 1 0 1	0 0 1 0	0 1 1 0

Here, we should note that BCD cannot be greater than 9.

The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added.

Let us consider additions of 3 and 6 in BCD.

	6	0	1	1	0 ← BCD for 6
+	3	0	0	1	1 ← BCD for 3
	9	1	0	0	1 ← BCD for 9

The addition is carried out as in normal binary addition and the sum is 1 0 0 1, which is BCD code for 9. So, it's okay to add 2 decimal number up to 9 + 9 = 18.

Let us consider addition of 6 and 8 in BCD

	6	0	1	1	0	← BCD for 6
+	8	1	0	0	0	← BCD for 8
	14	1	1	1	0	← Invalid BCD number

The sum 1 1 1 0 is an invalid BCD number. This has occurred because the sum of the two digits exceeds 9. Whenever this occurs the sum has to be corrected by the addition of six (0110) in the invalid BCD number, as shown below

	6	0	1	1	0	← BCD for 6
+	8	1	0	0	0	← BCD for 8
	14	1	1	1	0	← Invalid BCD number
		+ 0	1	1	0	← Add 6 for correction
0	0	0	1	0	1	0	0	← BCD for 14
		1				4		

After addition of 6 carry is produced into the second decimal position.

Sum equal 9 or less with carry 1.

Let us consider addition of 8 and 9 in BCD

	8					1	0	0	0	← BCD for 8
+	9					1	0	0	1	← BCD for 9
	17	0	0	0	1	0	0	0	1	← Incorrect BCD result

In this, case, result (0001 0001) is valid BCD number, but it is incorrect. To get the correct BCD result correction factor of 6 has to be added to the least significant digit sum, as shown below

	8					1	0	0	0	← BCD for 8
+	9					1	0	0	1	← BCD for 9
	17		0	0	0	1	0	0	0	1	← Incorrect BCD result
		+	0	0	0	0	0	1	1	0	← Add 6 for correction
			0	0	0	1	0	1	1	1	← BCD for 17

So, in order to complete the project, it is needed to convert BCD input into decimal output. Then then represent it into decimal number & Addition those BCD number into binary formation. Then represent the binary number into BCD again. After that, the BCD result is again converter into decimal in order to display it in the Seven segment display.

Required Components:

1. 74LS47 (BCD to 7-Segment Decoder).
2. 74HC283 (4-bit binary full adder with fast carry).
3. 4081 (2-input AND gate).
4. 4075 (3-input OR gate).
5. Seven Segment Display (Common Anode).
6. Red LED's.
7. Resisters (220***Ω***).
8. Logic State.
9. Connectors.

74LS47 (BCD to 7-Segment Decoder):

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 mA. Auxiliary inputs provided blanking, lamp test and cascade-able zero-suppression functions.

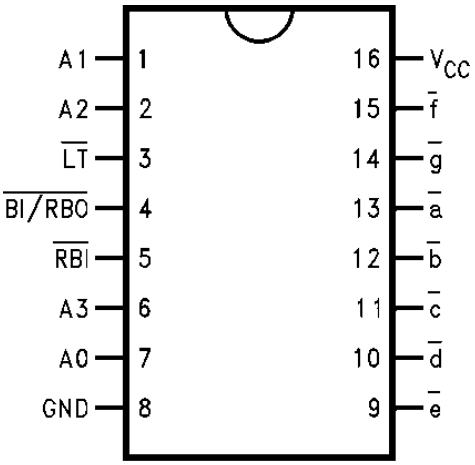


Fig. 1: Pin configuration of 74LS47.

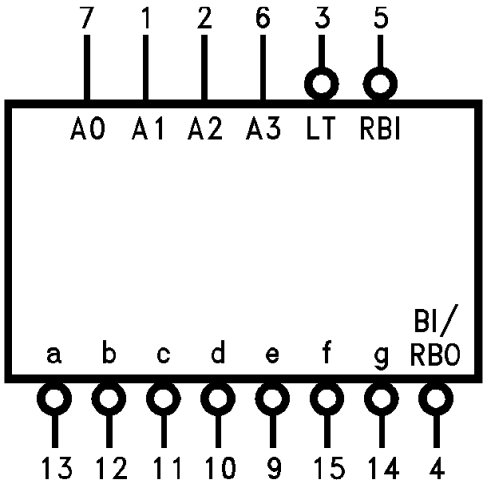


Fig. 2: Logic Symbol of 74LS47.

The internal logic diagram is following for the IC 47LS47 using primary & secondary gates.

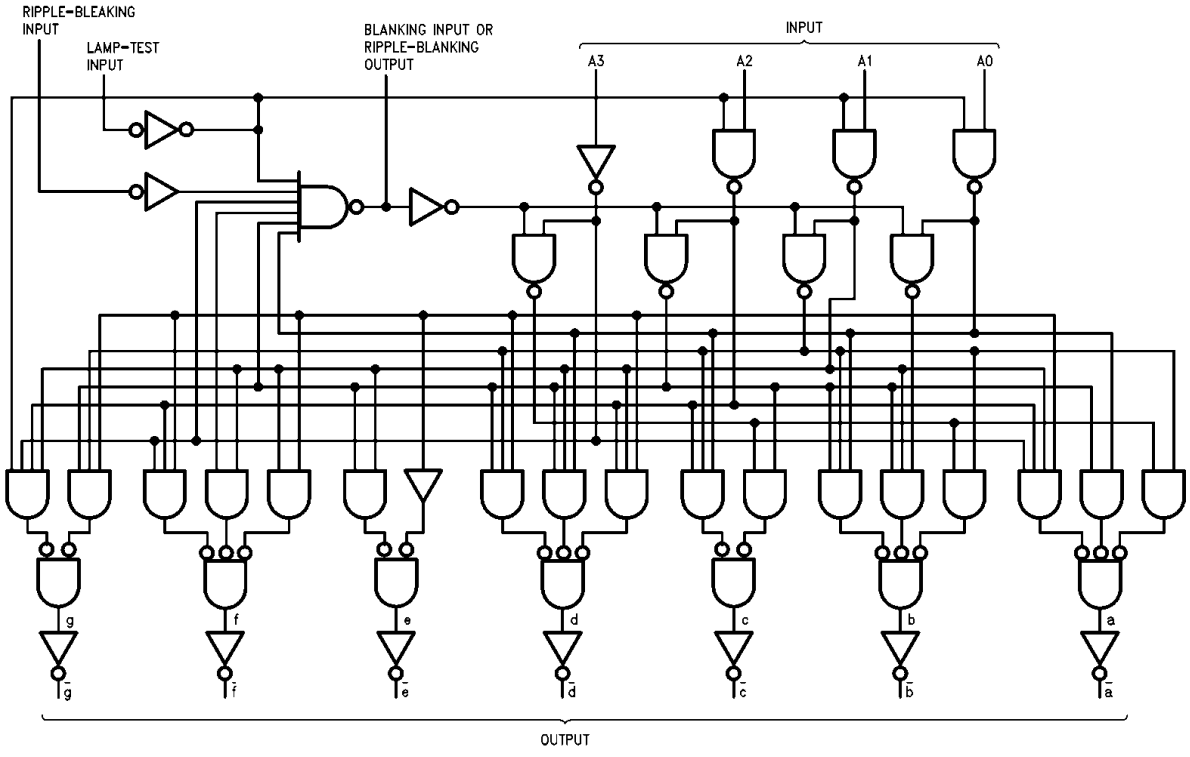


Fig. 3: Logic Diagram of 74LS47.

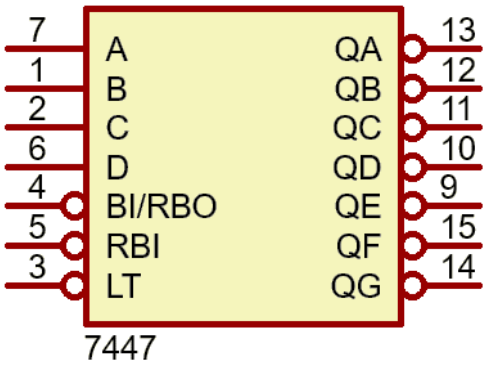


Fig. 4: Simulation Diagram of 74LS47.

Here, Input pin is A,B,C,D & output pin is QA-QG (8 pins). There are also 3 active low pins in the chip. They are, LT (Light Test), RBI (Ripple Blink Input) & RBO (Ripple Blink Output).

LT : HIGH for no operation & LOW for test all the lights are in working state.

RBI : HIGH for no operation & if using multiple chips, then MSB RBI is LOW & others are connected with the previous RBO.

RBO : HIGH for no operation & if using multiple chips, then LSB RBO is HIGH & others are connected to the next RBI.

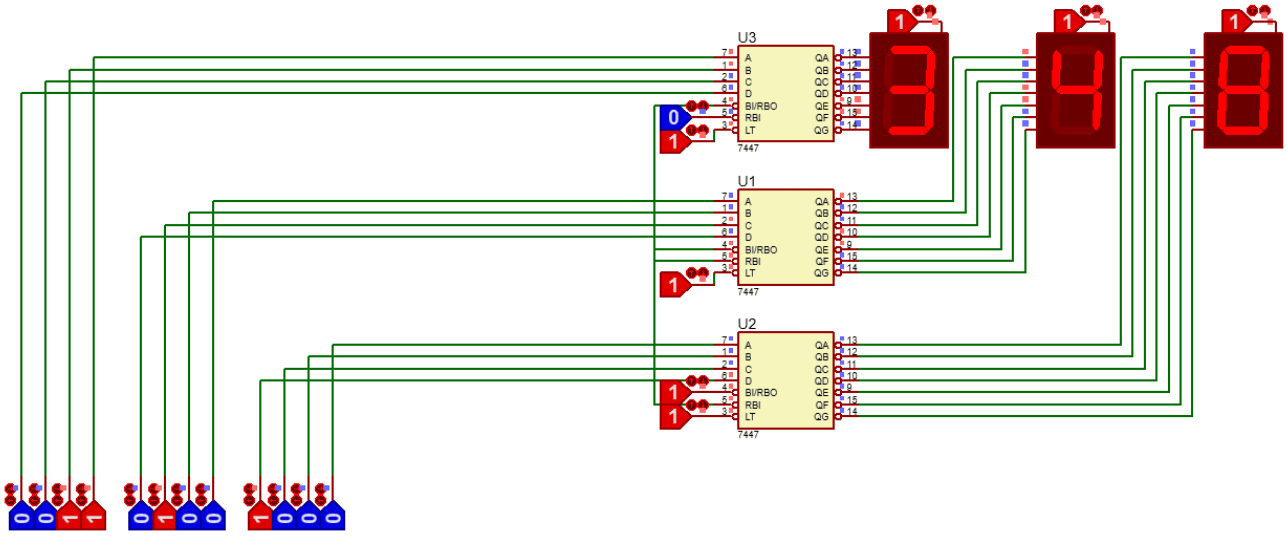


Fig. 5: BCD to Decimal conversion using 74LS47.

The following Circuit is the BCD to Decimal converter using 74HC47 or 74LS47 chip. It is the half part of the project.

***74HC283 (4-bit binary full adder with fast carry)*:**

The 74HC283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs ($\boldsymbol{\Sigma}_1$ to $\boldsymbol{\Sigma}_4$) and the out-going carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \boldsymbol{\Sigma}_1 + 2\,\boldsymbol{\Sigma}_2 + 4\boldsymbol{\Sigma}_3 + 8\,\boldsymbol{\Sigma}_4 + 16C_{OUT}$$

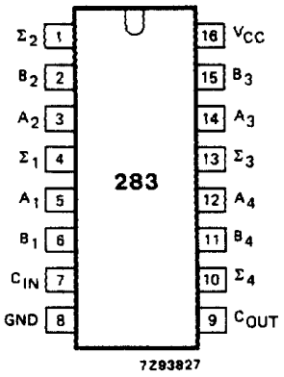


Fig. 6: Pin configuration of 74HC283.

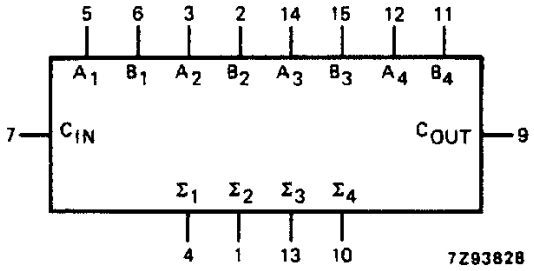


Fig. 7: Logic Symbol of 74HC283.

Due to the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results $\boldsymbol{\Sigma}_1$ to $\boldsymbol{\Sigma}_4$ and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can be assigned arbitrarily to pins 5, 6, 7, etc.

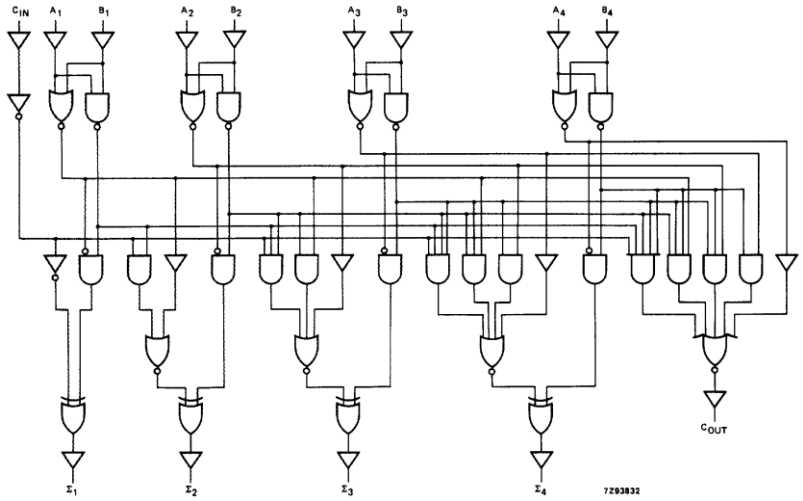


Fig. 8: Logic Diagram of 74HC283.

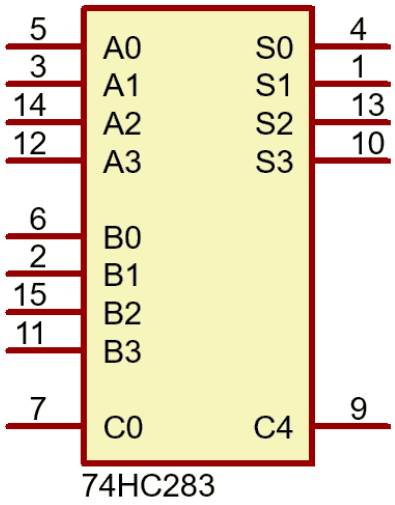


Fig. 9: Simulation Diagram of 74HC283.

Here, Input pins are A0-A3 (BCD number-1), B0-B3 (BCD number-2) & C0 (Carry in). And output pin is S1-S3 (4 pins of Binary number) & C4 (Carry out). So, the chip add two BCD number & output the addition in Binary.

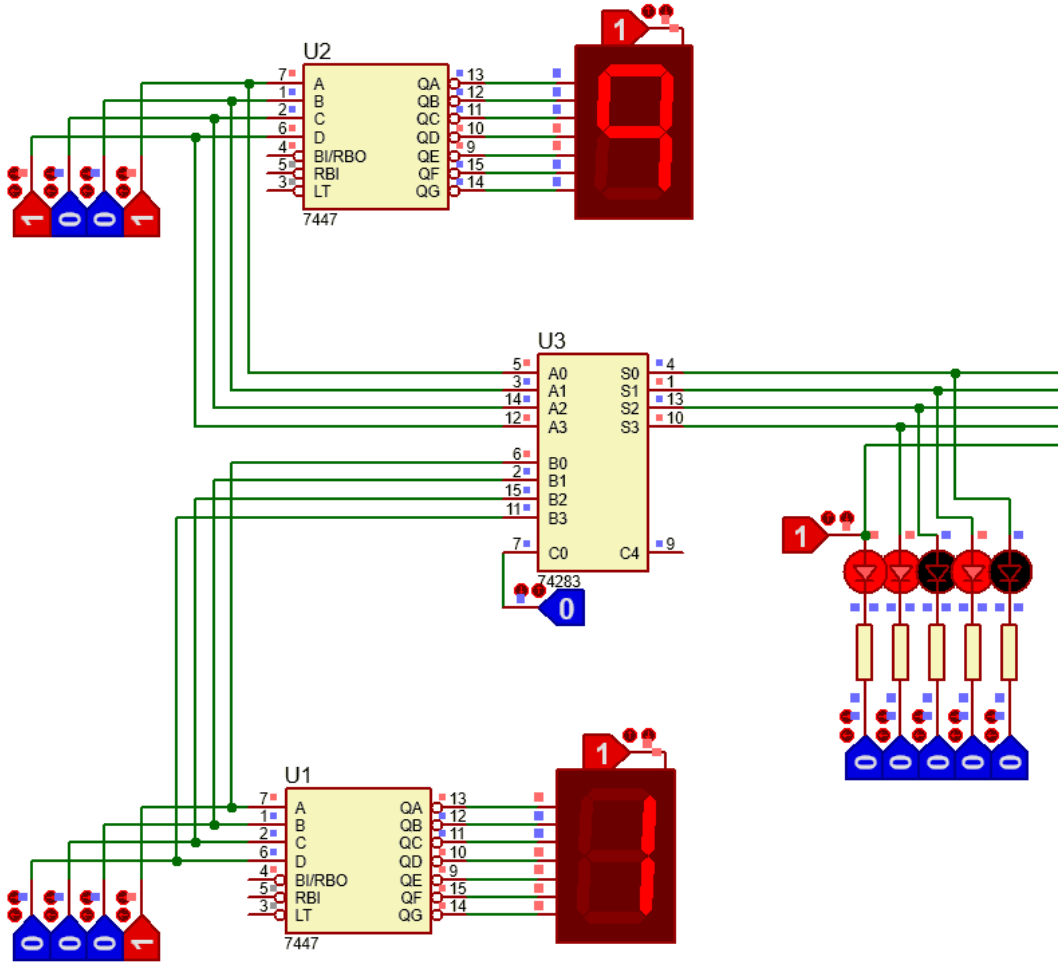


Fig. 10: BCD adder & representation in Binary format.

The following Circuit add 2 number & represent it in binary. For the following example, BCD numbers are 9 & 1. Addition of those 2 numbers is 10. Which is represent in the 4 RED LEDs from the right. Which is, 1010 in binary is equivalent to 10 in decimal. There is also a carry for further calculation in decimal format.

Seven Segment Display (Common Anode):

The emission of photons from a 7-segment display occurs when the diode junction of each segment is forward biased by an external voltage allowing current to flow across its junction, and in Electronics we call this process electroluminescence. The actual color of the visible light emitted by an LED, ranging from blue to red to orange, is decided by the spectral wavelength of the emitted light which itself is dependent upon the mixture of the various impurities added to the semiconductor materials used to produce it.

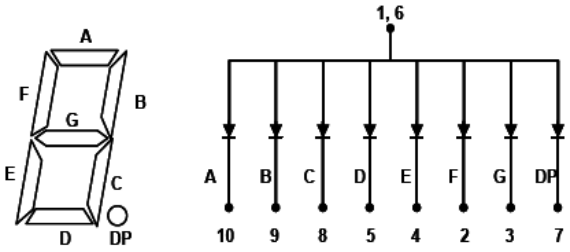


Fig. 11: Logic Diagram of 4075

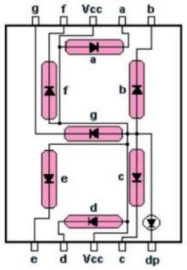


Fig. 12: Pin Configuration.

The main advantage of light emitting diodes is that because of their small die size, several of them can be connected together within one small and compact package producing what is generally called a **7-segment Display**.

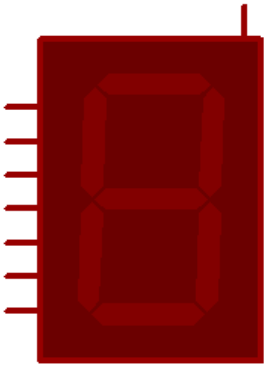


Fig. 13: Simulation Diagram of 74HC283.

For the project, Common Anode display is needed. Because the display is connected with the output pin of 74HC47. Whose output pins are active LOW.

4081 (2-input AND gate):

The CD4071BC and CD4081BC quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs protected against static discharge with diodes to VDD and VSS.

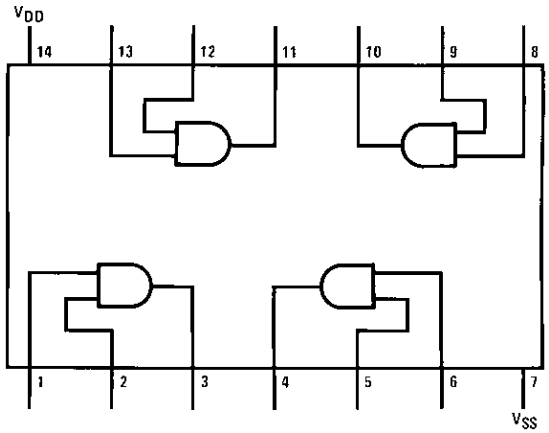


Fig. 14: Logic Diagram of 4081.

4075 (3-input OR gate):

The 74HC/HCT4075 are high-speed Si-gate CMOS devices and are pin compatible with the “4075” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT4075 provide the 3-input OR function.

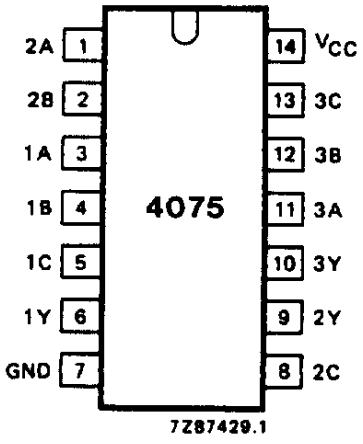


Fig. 15: Pin Configuration of 4075.

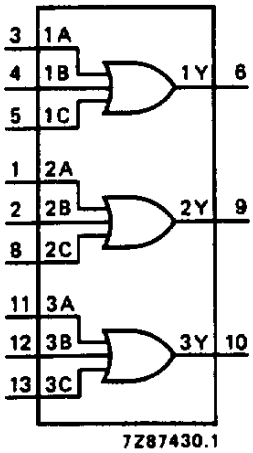
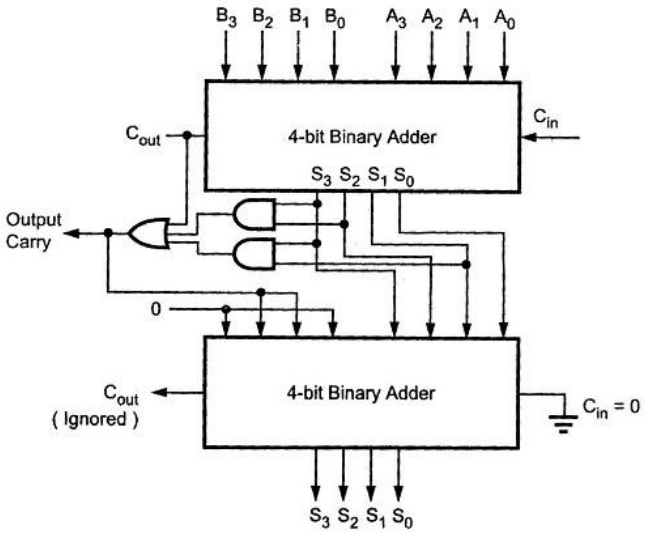


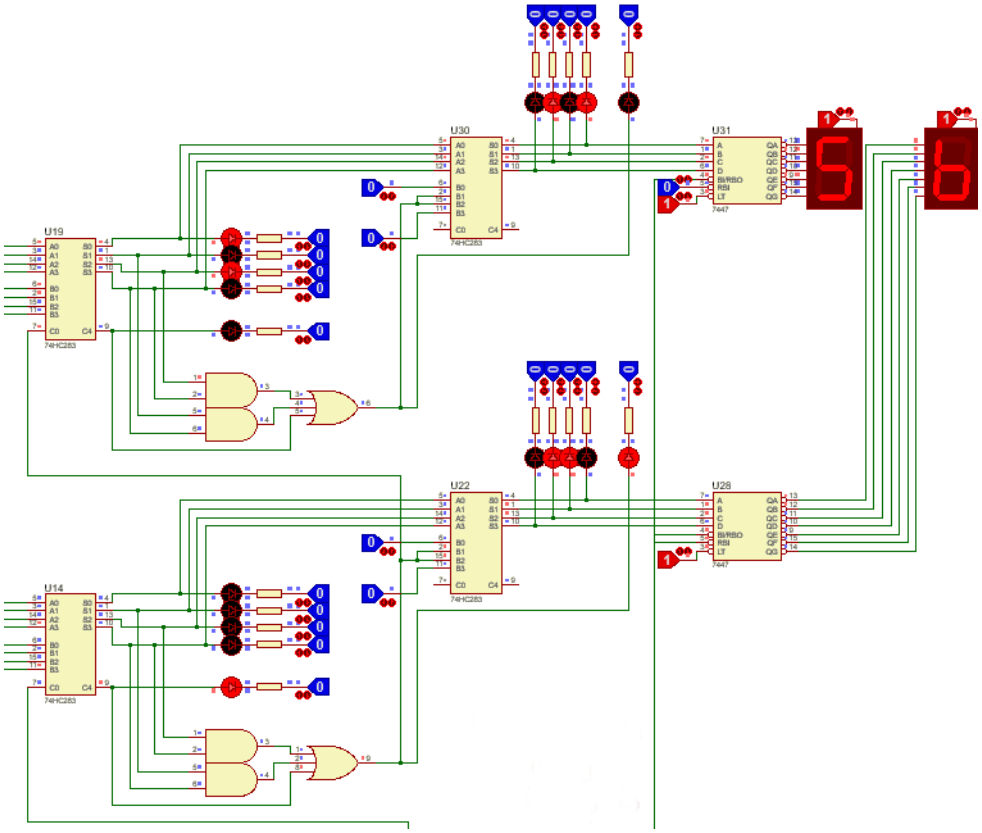
Fig. 16: Logic Diagram of 4075.

4-bit Binary to BCD conversion:

So far in the project, 2 BCD input is added in the form of 4-bit binary number. In order to display the number, we again need to convert the binary number into BCD format. For this, the following circuit is been implemented.



By using ripple carry, it is possible to combine the BCD conversion & ripple display output. Which is shown in the below circuit.



Here, the BCD input is 18 & 38. The result will be 56 (0101 0110 in BCD). But with ripple carry & input rotation property, it is possible to pass the carry out to the next adder using the combinational circuit using 2 input AND-gate & 3 input OR-gate.

Circuit Diagram:

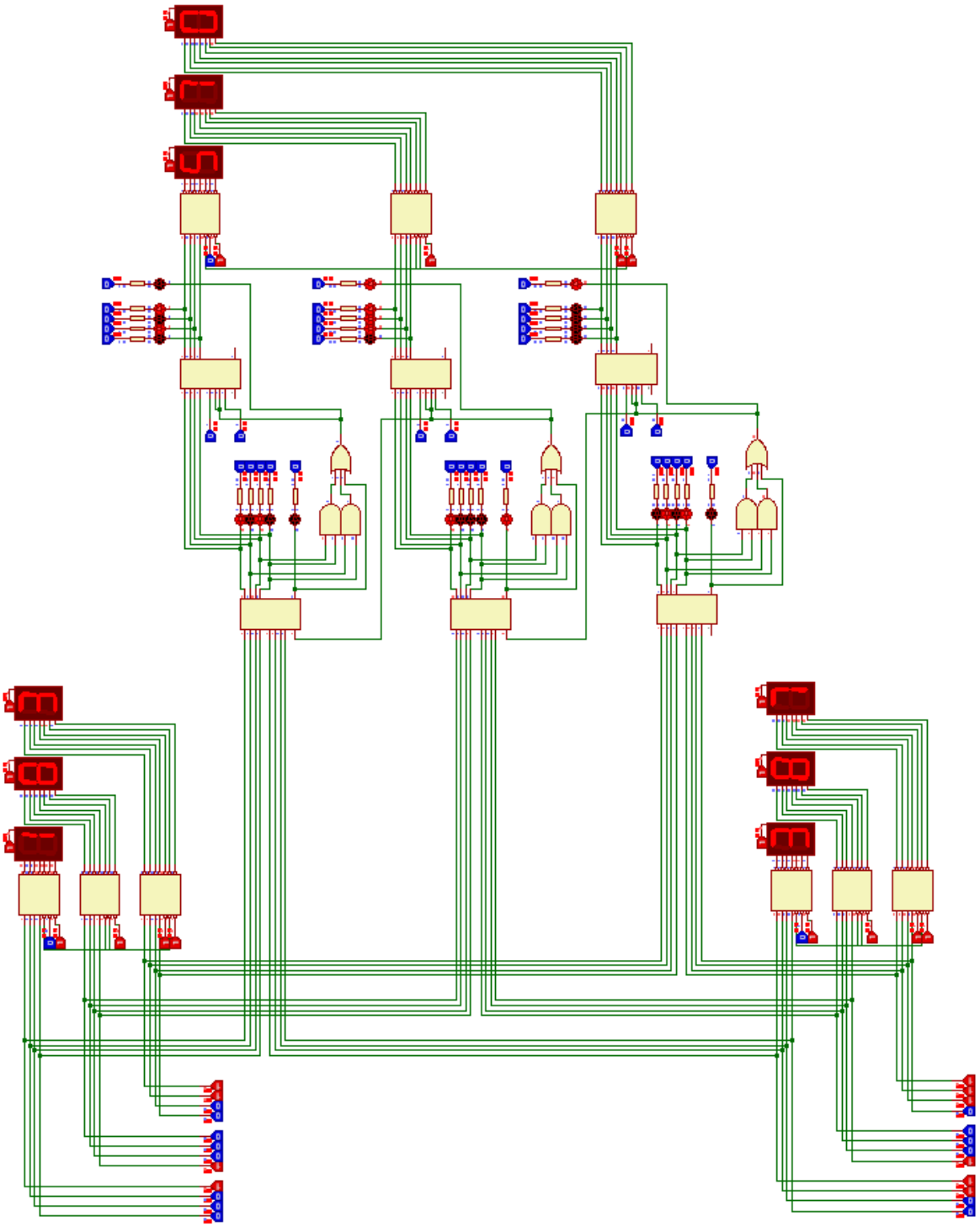
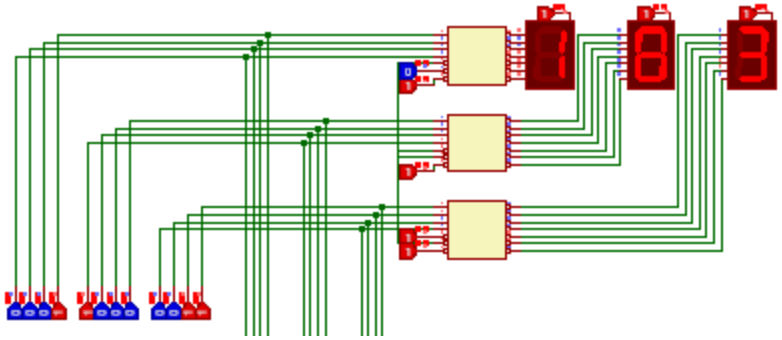


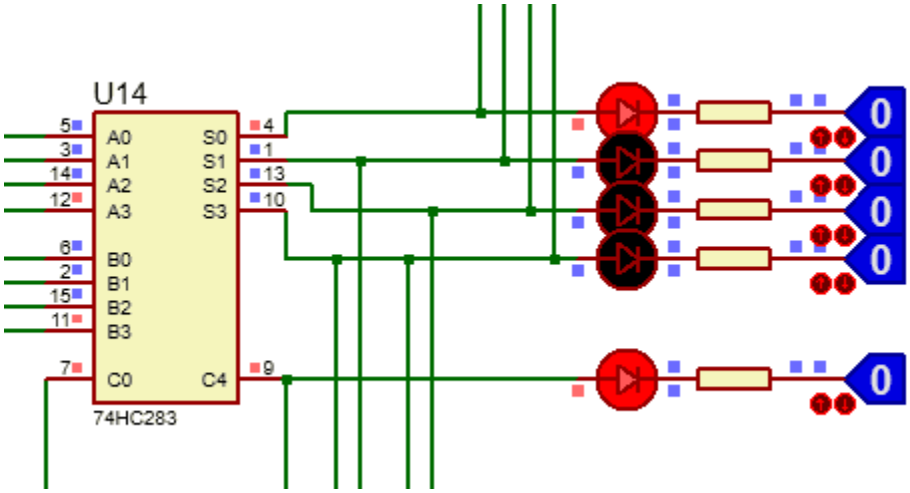
Fig. 16: BCD to Decimal Converter & Decimal Adder.

Circuit working Process:

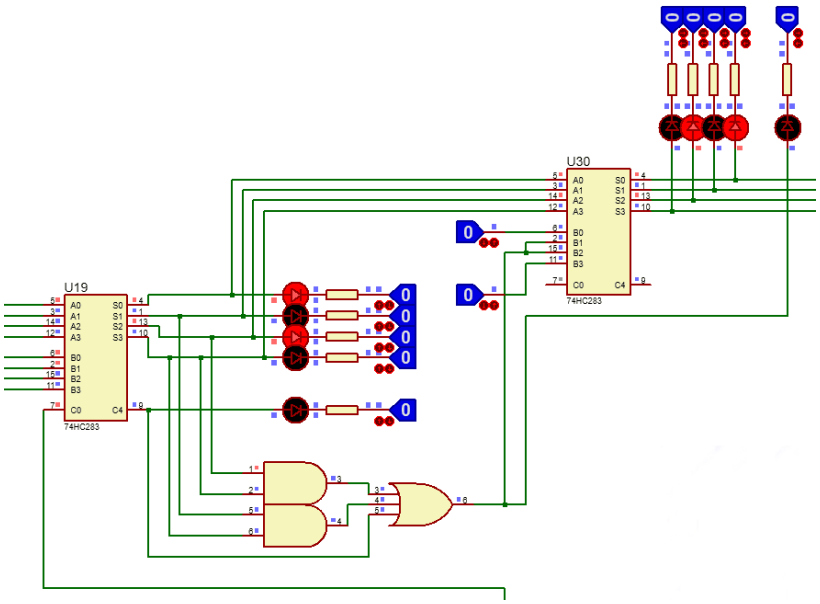
In the circuit diagram, the first part converts the BCD input into Decimal output.



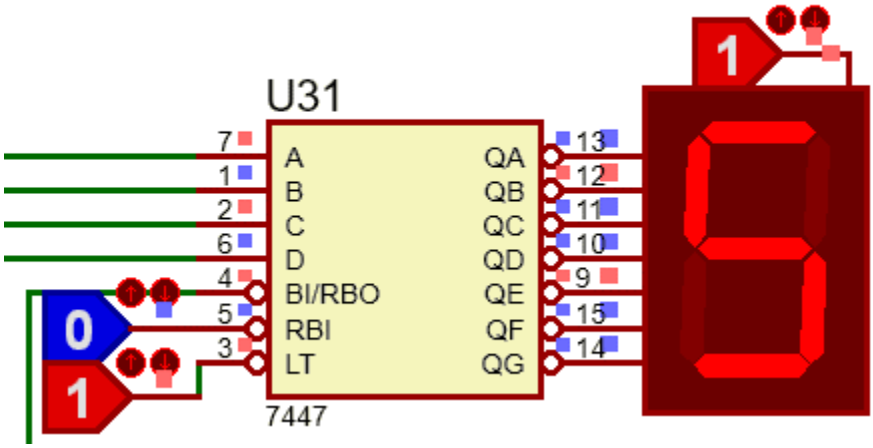
Then the next part add two BCD input & represent it into Binary output including carry.



Then in the next step convert the Binary output into BCD output.



In the last step the BCD output is passes to the 74HC47 chip in order to display.



Conclusion:

Here, in the project two 3-digit decimal number is added to made up to the result also in decimal. The following adder add up to 999. And as there is only combinational circuit, it is possible to make a adder up to any digit we want, we can make. Adder circuit is the building block of Arithmetic & Logic Unit (ALU). So, the circuit will be the very handy tool to demonstrate the part of internal architecture in a computer.

References:

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3. https://www.igelectronics.com/products/c2597b9bd1/1726810000000139001
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7. https://www.datasheetq.com/datasheet_download/131811/1/NXP/4075
8. https://www.electronics-tutorials.ws/blog/7-segment-display-tutorial.html