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Efficient and scalable designs for ternary quantum reversible multiplexer and demultiplexer systems

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Abstract

In recent years, ternary reversible logic has become a promising paradigm for advancing low-power, high-performance quantum digital systems that preserve information and are energy efficient. This paper focuses on two primary objectives: first, the efficient realization of ternary reversible 3×1 multiplexers and 1×3 demultiplexers using quantum gates, specifically 1-qutrit Shift and 3-qutrit Controlled Feynman gates, and second, the design of generalized $n \times 1$ multiplexers and $1 \times n$ demultiplexers. The proposed 9×1 multiplexer we propose in this study has demonstrated notable improvements in terms of quantum cost (20%), depth (18%), number of constant inputs (60%), and garbage outputs (30%), while the proposed 1×9 demultiplexer shows a 20% reduction in quantum cost, a 18% reduction in depth, a 33% reduction in constant inputs, and a 50% reduction in garbage outputs, compared to the most efficient existing designs. These optimizations represent an important step forward in the development of more efficient ternary and quantum reversible logic circuits, advancing the scalability of quantum systems.

Keywords Qutrit · Quantum computation · Ternary reversible logic · Scalable circuit design · Multiplexer circuit · Demultiplexer circuit

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1 Introduction

In recent years, reversible computation has emerged as a compelling alternative to conventional irreversible logic, gaining significant attention from researchers. Unlike traditional computing, where operations typically result in information loss, reversible computation ensures that every operation is bijective, meaning that it can be executed both forward and backward without loss of data [3]. This property makes it possible to fully reconstruct input states from output states, achieving an information-preserving computational paradigm. Quantum computing is inherently based on reversible computation [33, 41]. This reversibility is crucial in decreasing energy dissipation, as stated by Landauer's principle, which asserts that losing a single bit of information results in a minimum energy dissipation of $kT \ln 2$ joules, where k is Boltzmann's constant and T is absolute temperature [3, 25]. The use of reversible gates in quantum computing reduces energy loss, enabling efficient, low-power, and high-performance circuit design. Recent breakthroughs in quantum circuit design, such as binary linear code decoding techniques [42], categorical quantum circuit frameworks [4], and the realization of arbitrary reversible logic gates [39], have significantly contributed to the development of highly efficient quantum architectures. Experimental implementations of universal quantum gate sets have been successfully demonstrated across different physical platforms, including atomic-scale quantum systems [1], superconducting qubits [9, 36], and linear optics-based systems [10, 40], and with various physical structures [21].

The hardware cost of any digital system is heavily influenced by the choice of numerical radix [14, 17, 18]. Multi-valued quantum computing, particularly ternary logic, presents distinct advantages over conventional binary-based approaches by optimizing qudit (quantum digit) utilization and reducing the overall quantum resource requirements. Unlike binary systems, multi-valued logic (MVL) allows for a more compact representation of quantum information, leading to enhanced circuit efficiency. Among various MVL approaches, ternary quantum logic stands out due to its superior noise resilience [8] and its optimal radix efficiency, which is determined by examining the width and depth of the number representation [16, 23].

Hurst [16] demonstrated that the complexity (C) of a circuit designed to process a specific quantity of data (N) can be expressed using the following equation:

$$C = K(R \cdot d) \tag{1}$$

where R represents the number of basis states, d denotes the number of signals, and K is a proportional coefficient. The number of signals can be calculated as $d = \log_R N$. According to this formulation, the circuit complexity (C) obtains its minimum value when R is approximately equal to $e \approx 2.718$. Since R must be an integer in practical implementations, $R = 3$ (ternary logic) emerges as the closest optimal choice.

For the special case of binary logic ($R = 2$), the proportional coefficient K is given by:

$$K = \frac{50}{\log_2 N} \tag{2}$$

When $R \neq 2$, the general equation for circuit complexity can be rewritten as:

$$C = 50R\frac{\ln(2)}{\ln(R)} \tag{3}$$

According to this analysis, it becomes evident that ternary logic ($R = 3$) offers a more efficient computational structure than binary logic, leading to reduced circuit complexity and optimized performance [7].

Recent studies have further highlighted the compactness and efficiency of ternary quantum computers, showing that they require 37% fewer resources compared to their binary counterparts [13]. The advantages of quantum ternary logic extend beyond circuit compactness, encompassing enhanced security in quantum communication systems [2, 5], greater efficiency in quantum information processing [11], higher data storage density [6], improved fault tolerance [24], and lower interconnection complexity with decreased power consumption [6, 29].

In quantum computing, the fundamental unit of information in ternary logic is known as a qutrit. The concept of ternary reversible logic has been extensively explored as a foundation for designing efficient quantum computing architectures, enabling lower energy dissipation [32]. Due to its potential advantages, ternary reversible logic continues to attract significant research interest, particularly in the design of quantum circuits [15, 28, 38, 43].

Multiplexer and demultiplexer circuits are fundamental components in computers, arithmetic logic units, communication systems, memory architectures, and signal converters [12]. It is important to note that, unlike multiplexers and demultiplexers in classical communication systems–which transmit multiple signals over a single physical medium using distinct wavelengths, time slots, or other physical dimensions–the circuits presented in this work operate purely as logic-level components. They deterministically route ternary data based on selector values, preserving reversibility and information throughout the computation. This work presents an innovative approach to designing ternary quantum reversible multiplexer and demultiplexer circuits, focusing on improving efficiency over existing designs [20, 37]. The objective of this study is to optimize quantum ternary circuits by minimizing four critical parameters: quantum cost, depth, constant inputs, and garbage outputs. These parameters directly impact circuit efficiency and are defined as follows:

- Quantum Cost: The total number of 1-qutrit Shift gates and 2-qutrit Muthukrishnan–Stroud gates required for circuit design. A lower quantum cost indicates a more optimized and resource-efficient design [12, 26].
- Depth: The number of sequential time steps required to execute the circuit. One or more gates acting on disjoint qutrits can operate in parallel within a single time step [34, 37].
- Constant Inputs: Input values that remain fixed at 0, 1, or 2 to facilitate the synthesis of the intended logic function. An increased number of constant inputs expands the circuit size, affecting design complexity [12, 30].
- Garbage Outputs: Unused outputs introduced to maintain reversibility in quantum circuits. While necessary for preserving information, excessive garbage outputs can contribute to higher information loss, reducing overall efficiency [12, 27].

Table 1 Truth table of GF3 addition operation [19]

$\oplus$	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Table 2 Truth table of GF3 multiplication operation [19]

$\odot$	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

In quantum ternary logic, optimizing these factors is crucial for constructing efficient circuits. It should be noted that, the quantum cost refers to the total cost of the circuit, calculated based on the number of 1-qutrit Shift gates and 2-qutrit Muthukrishnan-–Stroud (M–S) gates. When the circuit is evaluated using 1-qutrit Shift gates and 2-qutrit Muthukrishnan-–Stroud gates, each assigned a cost of 1, the total quantum cost becomes numerically equal to the total number of gates, or the quantum size. If different cost values are assigned to different gates, the quantum cost and quantum size may differ. The proposed ternary circuits offer improvements in terms of quantum cost, depth, the number of constant inputs, and the number of garbage outputs compared to existing approaches [20, 37]. Our proposed multiplexer lowers quantum cost by 20%, reduces depth by 18%, reduces constant inputs by 60%, and decreases garbage outputs by 30%. The demultiplexer achieves a 20% reduction in quantum cost, a 18% reduction in depth, 33% fewer constant inputs, and 50% fewer garbage outputs compared to the most efficient existing designs presented in [37].

This paper is organized as follows: Sect. 2 provides an overview of ternary Galois fields and reversible logic gates, presenting the foundational concepts. Section 3 presents the proposed scalable designs for ternary quantum reversible multiplexers and demultiplexers. In Sect. 4, the assessment of the proposed circuits is discussed, comparing them with existing designs. Finally, Sect. 5 summarizes the key findings of this work.

2 Preliminaries

2.1 Ternary logic and galois field 3

The Galois Field in ternary logic is defined by the set $Q = \{0, 1, 2\}$, along with the operations of addition ($\oplus$) and multiplication ($\odot$) [19]. These operations, as shown in Tables 1 and 2, are performed modulo 3 and are both associative and commutative. Moreover, multiplication is distributive over addition. The properties of addition and multiplication within this algebraic structure are described as follows:

Addition ($\oplus$):

$$Z(0) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad Z(+1) = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \quad Z(+2) = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$$
$$Z(12) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \quad Z(01) = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad Z(02) = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$

Fig. 1 Representation of 1-qutrit permutative transforms [31]

Fig. 2 Symbolic representation of ternary shift gates [37]

- (A1) *Associative Law*: $a \oplus (b \oplus c) = (a \oplus b) \oplus c$.
- (A2) *Commutative Law*: $a \oplus b = b \oplus a$.
- (A3) *Identity Element*: There exists an element 0 such that $a \oplus 0 = a$ for all a.
- (A4) *Additive Inverse*: For every a, there exists an element $-a$ such that $a \oplus (-a) = 0$.

Multiplication ($\odot$):

- (M1) *Associative Law*: $a \odot (b \odot c) = (a \odot b) \odot c$.
- (M2) *Commutative Law*: $a \odot b = b \odot a$.
- (M3) *Identity Element*: There exists an element 1 (distinct from 0) such that $a \odot 1 = a$ for all a.
- (M4) *Multiplicative Inverse*: For any $a \neq 0$, there exists an element a^{-1} such that $a \odot a^{-1} = 1$.

These properties establish the foundational algebraic structure of GF(3), ensuring consistent and predictable behavior for the operations of addition and multiplication.

2.2 Ternary shift gates

In ternary quantum logic, any transformation of a qutrit is represented by a 3×3 unitary matrix, as illustrated in Fig. 1 [31]. These matrices correspond to 1-qutrit Shift gates which are 1-input, 1-output operations, where the output is the Z-transform of the input. As can be observed, in the $Z(0)$ transformation, each column corresponds to one of the states $|0\rangle$, $|1\rangle$, and $|2\rangle$, forming what is referred to as the elementary state. The $Z(+1)$ transformation shifts the qutrit states of $Z(0)$ forward by 1, while the $Z(+2)$ transformation shifts them forward by 2. For the $Z(12)$ transformation, the qutrit states $|1\rangle$ and $|2\rangle$ from the elementary state $Z(0)$ are swapped. Similarly, the $Z(01)$ transformation exchanges the qutrit states $|0\rangle$ and $|1\rangle$, and the $Z(02)$ transformation swaps $|0\rangle$ and $|2\rangle$. These transformations collectively form a set of 1-qutrit Shift gates. Figure 2 provides a graphical representation of these gates. For each gate, the output P is derived by applying the Z-transformation (where $Z \in \{+1, +2, 01, 02, 12\}$) to the input A.

The functional relationship between the input and output states for these gates is summarized in Table 3. Table 4 describes the inverse gates corresponding to these

Table 3 Truth table of ternary shift gates [31]

Input(A)	Z(0)=A	Z(+1)=A+1	Z(+2)=A+2	Z(12)=2A	Z(01)=2A+1	Z(02)=2A+2
0	0	1	2	0	1	2
1	1	2	0	2	0	1
2	2	0	1	1	2	0

Table 4 Inverse gates of ternary shift gates [31]

Gates	Z(+1)	Z(+2)	Z(12)	Z(01)	Z(02)
Inverse gates	Z(+2)	Z(+1)	Z(12)	Z(01)	Z(02)

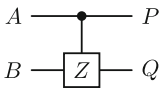


Fig. 3 Symbolic representation of ternary Muthukrishnan and Stroud (M-S) gate [37]

ternary 1-qutrit Shift gates, ensuring that each transformation can be reversed. Specifically, the inverse of $Z(+1)$ is $Z(+2)$, and vice versa, as they cyclically shift the states in opposite directions. For the swapping transformations, $Z(01)$, $Z(02)$, and $Z(12)$, each gate is its own inverse, as applying the same swap twice restores the original state. As fundamental elements of ternary quantum reversible logic, these gates are compatible with liquid ion-trap quantum technology [22]. Moreover, their simplicity is reflected in their quantum cost, which is minimal and quantified as 1.

2.3 Ternary Muthukrishnan-–Stroud gates

Muthukrishnan and Stroud (2000) introduced a novel family of 2-qutrit multiple-valued quantum gates and provided a detailed demonstration of their implementation within ion-trap systems [32]. The symbolic representation of a 2-qutrit Muthukrishnan–Stroud (M–S) gate is illustrated in Fig. 3.

In terms of functionality, the inputs to this gate are denoted as A and B, while the outputs are represented as P and Q. Specifically, the gate operation defines $P = A$ and Q as the Z-transform of B when $A = 2$; otherwise, $Q = B$. The Z-transform, in this context, is defined as $Z = \{+1, +2, 01, 02, 12\}$.

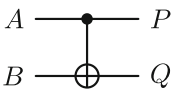
One of the notable aspects of this gate is its quantum cost, which is a measure of the resources required for its implementation. The quantum cost of this gate is minimal, quantified as a value of 1.

2.4 Ternary controlled Feynman gate

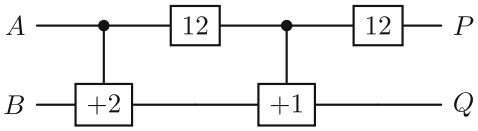
Khan and Perkowski (2006) introduced a 2-qutrit Feynman gate, the symbolic representation of the ternary Feynman gate is depicted in Fig. 4a . This gate takes two inputs, A and B, and produces two outputs, P and Q. The operation of the gate is defined such that $P = A$ and $Q = A \oplus B$ [20, 37].

A detailed realization of this gate using ternary Muthukrishnan-–Stroud and 1-qutrit Shift gates is presented in Fig. 4b . As can be observed in this realization, the behavior of the gate is conditional on the value of input A: If $A = 2$, a $(+2)$ transformation is applied to B; if $A = 1$, a $(+1)$ transformation is applied to B, and if $A = 0$, no transformation is applied to B.

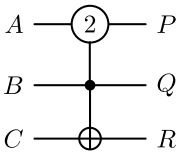
To preserve the value of input A, the second 1-qutrit (12) gate, functioning as the inverse of the first 1-qutrit (12) gate, is employed. This ensures that A is restored to



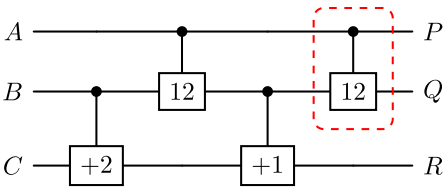
(a) Circuit representation for the Feynman gate.



(b) The realization using M-S and Shift gates.



(a) Circuit representation for the controlled Feynman gate.



(b) The realization using M-S and Shift gates.

Fig. 4 Ternary quantum reversible Feynman gate [37]

Fig. 5 Ternary quantum reversible Controlled Feynman gate [37]

its original value at the output. The quantum cost of this realization is quantified as 4, reflecting the number of primitive quantum operations required for implementation.

In addition to the ternary Feynman gate, a ternary Controlled Feynman gate is also introduced. This gate takes three inputs, A, B and C, and produces three outputs, P, Q and R. The operation of the gate is defined such that $P = A$, $Q = B$ and $R = B \oplus C$, if $A = 2$. Otherwise, $R = C$. The graphical representation of this gate is shown in Fig. 5a , and its realization using Muthukrishnan-–Stroud gates is detailed in Fig. 5b . The quantum cost of this gate is 4. It is noteworthy that in scenarios where the input B does not need to be preserved at the output, the second 2-qutrit Muthukrishnan-–Stroud gate (enclosed in the red-dotted box in Fig. 5b) can be omitted. This optimization reduces the quantum cost of the gate to 3, and in this case, the output Q is defined as $2B$ if $A = 2$.

3 Proposed approaches for multiplexer and demultiplexer synthesis

In this section, we propose a novel and scalable design for a ternary quantum reversible 3×1 multiplexer, which serves as the basis for constructing higher-order ternary quantum reversible multiplexers, including $n \times 1$ and 9×1 configurations. Additionally, we introduce a scalable ternary quantum reversible 1×3 demultiplexer, which is further utilized to design and develop $1 \times n$ and 1×9 demultiplexers.

Our approach leverages ternary 1-qutrit Shift gates and Controlled Feynman gates to enable efficient design within ternary quantum computing frameworks. The design focuses on optimizing key performance metrics, including reducing the overall quantum cost and depth, minimizing the number of constant inputs, and decreasing the number of garbage outputs. These optimizations contribute to the feasibility and resource efficiency of the proposed designs in scalable quantum systems.

3.1 Proposed design of ternary quantum reversible multiplexer circuits

In classical digital logic, a multiplexer is a combinational circuit that selects one of several input signals and forwards it to a single output line based on control signals (selectors). It is important to note that unlike multiplexers in classical communication systems that operate over physical domains such as time slots, frequencies, or wavelengths, the multiplexers presented in this work operate purely at the logic level. In the context of reversible quantum logic, a ternary multiplexer operates like a digital switch; it deterministically selects one of several ternary input lines ($I_0, I_1, \ldots, I_n$) and routes it to the output (O), based on the values of ternary selector(s).

In the following subsections, we introduce the design of a scalable ternary quantum reversible 3×1 multiplexer as a fundamental building block, and extend it to construct generalized $n \times 1$ multiplexers.

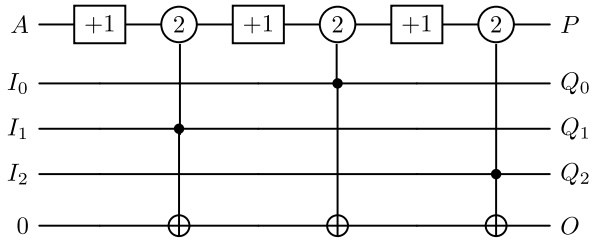
3.1.1 Scalable design of ternary quantum reversible 3 × 1 multiplexer

The following presents the design of a scalable ternary quantum reversible 3×1 multiplexer circuit. Here, the fundamental principles of ternary multiplexers are outlined. A ternary multiplexer with 3^N inputs utilizes N select lines to route one of the inputs to the target output. A ternary 3×1 multiplexer operates with three inputs I_0, I_1, and I_2, and a single selector A, which determines the input routed to the output. The selector A can take one of three values: 0, 1, or 2. When the selector $A = 0$, 1, and 2, the output corresponds to I_0, I_1, and I_2, respectively. The truth table for this operation is provided in Table 5.

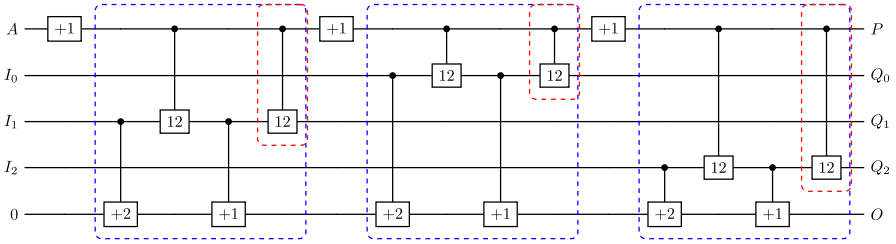
The proposed ternary quantum reversible 3×1 multiplexer circuit is illustrated in Fig. 6. As shown in Fig. 6a , the circuit employs three ternary 1-qutrit Shift gates and three ternary Controlled Feynman gates. The primary inputs are I_0, I_1, and I_2, along with one constant input initialized to 0. The selector A directs the operation, and the target output is denoted as O. Additionally, the circuit produces four garbage outputs: Q_0, Q_1, Q_2, and P. Here, P represents the selector A, while Q_0, Q_1, and Q_2 replicate the values of I_0, I_1, and I_2, respectively.

Table 5 The truth table of ternary 3 × 1 multiplexer

Selector A	Output O
0	I_0
1	I_1
2	I_2



(a) Symbol.



(b) The realization using M-S and Shift gates.

Fig. 6 Proposed ternary quantum reversible 3 × 1 multiplexer circuit

The behavior of the circuit is governed by the value of the selector A. When $A = 1$, the controlling value of the first Controlled Feynman gate is 2, resulting in $O = I_1$. Similarly, for $A = 0$ and 2, the second and third Controlled Feynman gates are activated, resulting in output $O = I_0$ and I_2, respectively.

An alternative realization of the circuit, utilizing ternary 1-qutrit Shift gates and Muthukrishnan-–Stroud (M–S) gates, is shown in Fig. 6b . This design incorporates three ternary Shift gates and twelve ternary M–S gates (the Controlled Feynman gates are highlighted in blue boxes for clarity). In this configuration, the quantum cost of the circuit is calculated as 15.

It is worth noting that restoring the input values I_0, I_1, and I_2 at the garbage outputs Q_0, Q_1, and Q_2 is not necessary. By omitting the M–S gates highlighted in red, the quantum cost can be reduced by 12. Likewise, the circuit depth is also reduced from 15 to 12. In both designs, the circuit maintains one constant input and generates four garbage outputs. These optimizations significantly enhance the efficiency of the proposed ternary quantum reversible multiplexer for scalable quantum computing architectures.

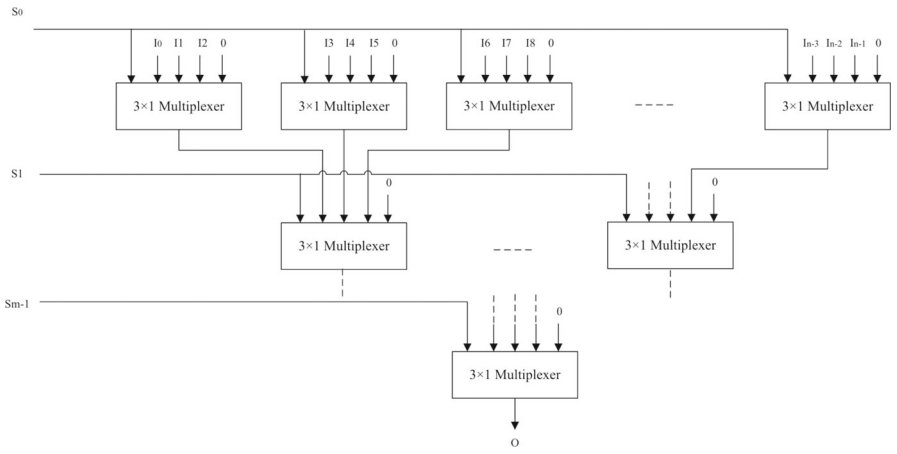


Fig. 7 Logical architecture of the proposed ternary $n \times 1$ multiplexer circuit

3.1.2 Generalized design of ternary quantum reversible $n \times 1$ multiplexer

Building upon the foundational 3×1 multiplexer, we propose a design for a ternary quantum reversible $n \times 1$ multiplexer. This generalized design extends the principles of modularity and efficiency to circuits with larger numbers of inputs and selectors. For $n = 3^m$, the circuit comprises m selector lines, one output, and n inputs. The structure relies on 3×1 multiplexers, organized to route the inputs to the target output. Figure 7 illustrates the logical structure of the proposed $n \times 1$ multiplexer.

The selector lines are applied hierarchically from top to bottom, with each successive stage of multiplexers controlled by a different selector. The final (lowest-level) multiplexer, which produces the single output, is controlled by the most significant selector, while the earlier (higher-level) stages are progressively controlled by less significant selectors.

The total number of 3×1 multiplexers, denoted as M, required for the circuit can be determined using the following equation, where n represents the total number of inputs to the multiplexer:

$$M = \frac{n-1}{2} \tag{4}$$

Each 3×1 multiplexer in the generalized design operates as an independent decision-making unit, activated by specific combinations of selector values. The selectors in each row determine the active multiplexer and the input to be routed to the next stage.

The quantum cost, the depth, the number of constant inputs, and garbage outputs of the proposed $n \times 1$ multiplexer can be determined according to Equations 5, 6, 7 and 8, respectively.

$$\text{Quantum Cost } = 12M = 12\left(\frac{n-1}{2}\right) \tag{5}$$

$$\text{Depth } = 9M = 9\left(\frac{n-1}{2}\right) \tag{6}$$

$$\text{The number of constant inputs } = M = \left(\frac{n-1}{2}\right) \tag{7}$$

$$\text{The number of garbage outputs } = 3M + m = 3\left(\frac{n-1}{2}\right) + m \tag{8}$$

To further optimize the circuit, ternary 1-qutrit Shift gates can be combined within 3×1 multiplexers, reducing the overall resource requirements. By optimizing these gate combinations, the total quantum cost is reduced to:

$$\text{Optimized Quantum Cost} = 9M + 3m \tag{9}$$

Here, M denotes the number of 3×1 multiplexers, and m represents the number of selector layers, which is given by $m = \log_3(n)$.

To clarify the derivation of the optimized quantum cost expression in Equation 9, we note that the total number of 3×1 multiplexers required to construct the circuit is $M = \frac{n-1}{2}$, based on the logical structure with n inputs in Fig. 7. Each multiplexer requires 9 M-S gates, resulting in a cost of $9\,M = \frac{9(n-1)}{2}$.

While each multiplexer could also include 3 ternary Shift gates, we optimize the design by sharing these gates across each layer. The circuit contains $m = \log_3(n)$ selector layers, and only 3 Shift gates are needed per layer. Therefore, the total cost from Shift gates is $3m$.

Combining these two contributions, the optimized quantum cost simplifies to:

$$\frac{9(n-1)}{2} + 3\log_3(n) \tag{10}$$

This generalized design offers significant flexibility and scalability, making it suitable for a wide range of applications in quantum information processing. Its modular nature allows for straightforward adaptations to different input sizes and selector configurations. Moreover, the emphasis on minimizing quantum cost ensures that the design remains efficient, even for large-scale design.

As an example, the proposed 3×1 multiplexer can be extended to design a 9×1 multiplexer. This circuit requires nine inputs I_0 to I_8, two selectors A and B, and one output O. Table 6 provides the truth table for this circuit. The output O is determined by the value of the selectors A and B, which directs the inputs to the output.

Based on the above table and the 3×1 multiplexer in Fig. 6, we propose a 9×1 multiplexer circuit. The realization of this circuit, as depicted in Fig. 8, uses twelve ternary 1-qutrit Shift gates and twelve Controlled Feynman gates, leading to a quantum cost of 48. This cost is achieved by adopting the realization of Controlled Feynman gates without the last M-S gate in Fig. 5b . This optimization is possible because the outputs Q_0 to Q_8 are treated as garbage outputs and are not used in further computation. In a typical Controlled Feynman gate, the final M-S gate is used to restore the input. Here, omitting the final M-S gate has no impact on circuit functionality of

Table 6 The truth table of a ternary 9 × 1 multiplexer

Selectors AB	Output O
00	I_0
01	I_1
02	I_2
10	I_3
11	I_4
12	I_5
20	I_6
21	I_7
22	I_8

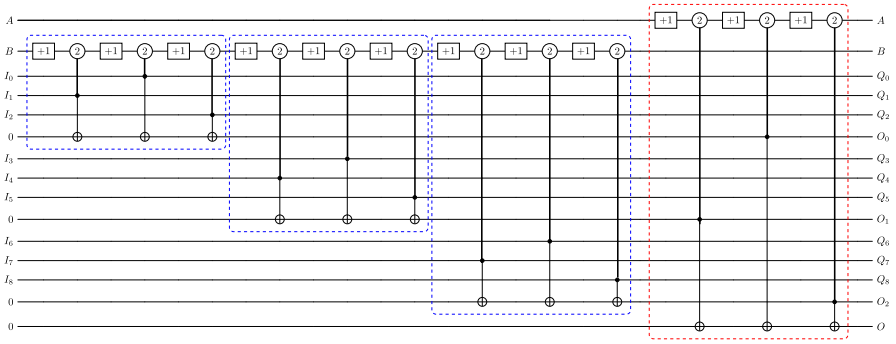


Fig. 8 Proposed ternary quantum reversible 9 × 1 multiplexer circuit

the target output O. This allows for a reduction in quantum cost without violating the principles of reversible computation.

In this specific example of a 9 × 1 multiplexer, selector B is the least significant and controls the three 3 × 1 multiplexers. Selector A, being more significant, controls the second-level multiplexer, determining which of the outputs from the first stage is routed to the final output. This control flow is also visually reflected in Fig. 8.

Further improvements can be made by combining 1-qutrit Shift gates to optimize the circuit further. As illustrated in Fig. 9, an optimized realization of the 9 × 1 multiplexer employs six ternary 1-qutrit Shift gates alongside 12 Controlled Feynman gates, significantly reducing the overall quantum cost to 42. This reduction is achieved through a meticulous reorganization of some ternary 1-qutrit Shift gates, in the first level (blue boxes), which streamlines the operation of this circuit. The optimized design still requires four constant inputs (set to 0) , produces 14 garbage outputs, and has a circuit depth of 36.

The scalability of the 9 × 1 multiplexer is a key feature of this design. By using modular 3 × 1 multiplexers, the circuit allows for a straightforward and structured expansion. Each 3 × 1 multiplexer operates as a building block, activated by the specific states of selectors A and B. This modular approach not only simplifies the

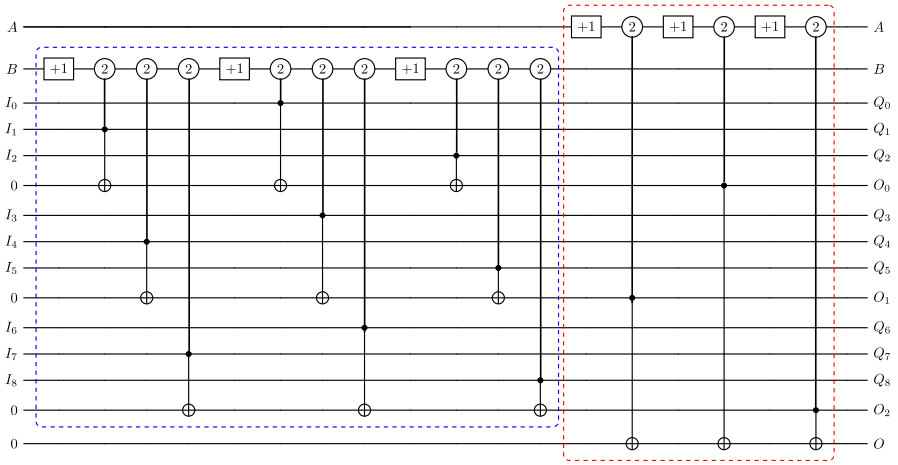


Fig. 9 Proposed optimized ternary quantum reversible 9 × 1 multiplexer circuit

design process, but also ensures that the quantum cost remains manageable, even as the circuit scales to larger configurations.

This design also offers versatility for various applications in quantum computing, where efficient reversible circuits are essential. By maintaining a balance between quantum cost and functional output, the proposed 9 × 1 multiplexer provides a robust solution for more complex logical operations. The use of optimized gates ensures that resource utilization remains efficient while minimizing quantum cost.

3.2 Proposed design of ternary quantum reversible demultiplexer circuits

In classical digital logic, a demultiplexer is a combinational circuit that takes a single input and routes it to one of several output lines based on control signals (selectors). Unlike demultiplexers in classical communication systems—which decode signals multiplexed across a shared channel via frequency, time, or wavelength separation—the demultiplexers in this paper are logic circuits operating deterministically based on control signals. In the context of reversible quantum logic, a ternary demultiplexer operates as a digital distributor: it deterministically directs the single ternary input (I) to one of several outputs ($O_0, O_1, \ldots, O_n$) based on the values of ternary selector(s), while preserving reversibility.

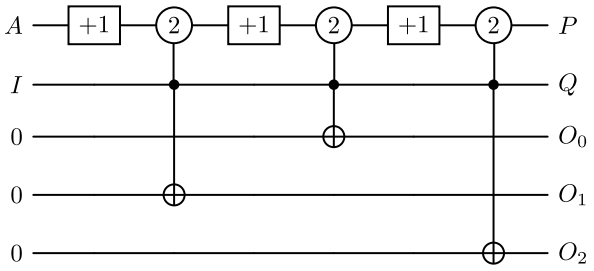
In the following subsections, we present a scalable design starting from the fundamental ternary 1 × 3 demultiplexer and extend it to an optimized 1 × n configuration with minimal quantum cost, depth, constant inputs, and garbage outputs.

3.2.1 Scalable design of ternary quantum reversible 1 × 3 demultiplexer

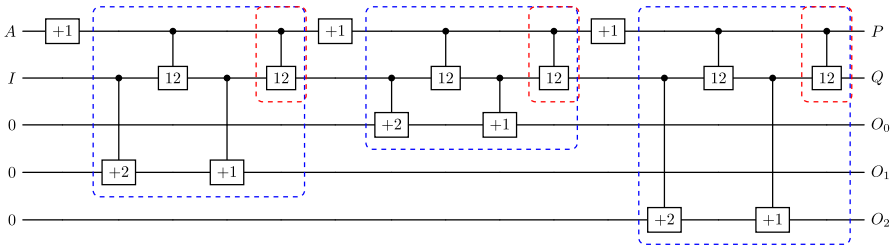
The following introduces the design of a ternary quantum reversible 1 × 3 demultiplexer, which performs the inverse operation of a multiplexer. A ternary demultiplexer with 3^N outputs utilizes N select lines to route the input to one of the output lines. In

Table 7 The truth table of a ternary 1 × 3 demultiplexer

Selector A	Outputs O_0	O_1	O_2
0	I	0	0
1	0	I	0
2	0	0	I



(a) Symbol.



(b) The realization using M-S and Shift gates.

Fig. 10 Proposed ternary quantum reversible 1 × 3 demultiplexer circuit

the case of a 1 × 3 demultiplexer, the selector A determines the output that receives the input I, respectively. Specifically, when $A = 0, 1$, or 2, the corresponding output O_0, O_1, or O_2 is set equal to I. The operational truth table for a 1 × 3 ternary demultiplexer is presented in Table 7.

The proposed ternary quantum reversible 1 × 3 demultiplexer circuit is shown in Fig. 10. The realization in Fig. 10a utilizes three ternary 1-qutrit Shift gates and three ternary Controlled Feynman gates. The circuit operates with a single primary input I and requires three constant inputs, each initialized to 0. The selector A serves as the control input, while the target outputs are O_0, O_1, and O_2. Additionally, the circuit generates two garbage outputs: P and Q. Here, P replicates the selector A, and Q indicates the value of the input I.

The behavior of the circuit is governed by the value of the selector A. When $A = 1$, the first Controlled Feynman gate, configured with a controlling value of 2, routes the input I to O_1. Similarly, when $A = 0$ and 2, the second and third Controlled Feynman gates are activated, directing the input I to O_0 and O_2, respectively. This selective

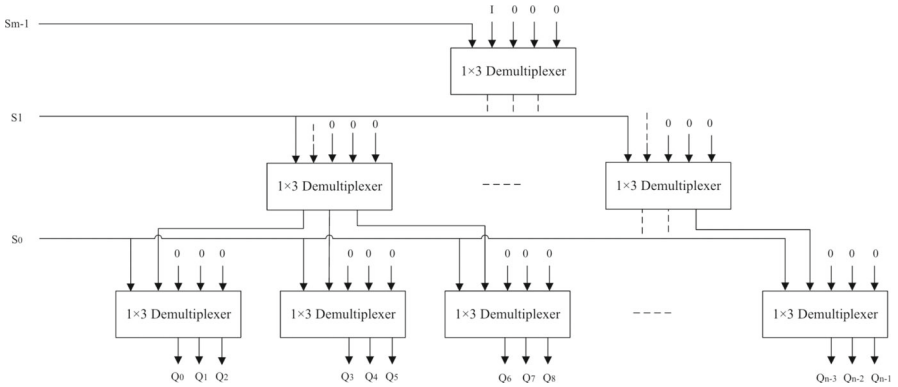


Fig. 11 Logical architecture of the proposed ternary $1 \times n$ demultiplexer circuit

operation ensures that only one output is activated for any given value of the selector A.

An alternative realization of the circuit, using ternary 1-qutrit Shift gates and Muthukrishnan-–Stroud (M–S) gates, is depicted in Fig. 10b . This design employs three ternary 1-qutrit Shift gates and twelve ternary M–S gates. To highlight their functionality, the Controlled Feynman gates are shown enclosed in blue boxes. In this configuration, the quantum cost of the circuit is calculated as 15.

It is noteworthy that restoring the value of the input I at the garbage output Q is not necessary. In the circuit shown in Fig. 10, the selector A activates only one of the Controlled Feynman gates, depending on its value (0, 1, or 2). The input I is routed exclusively through the active gate to its corresponding output O_0, O_1, or O_2, while the remaining gates remain inactive. As a result, the value of I is not passed through multiple Controlled Feynman gates nor reused elsewhere in the circuit. Since Q is a garbage output and not used in further computation, restoring the original input value at that point serves no functional purpose. Therefore, the last M–S gate in each Controlled Feynman block in Fig. 10b (as indicated by the red boxes) can be omitted, reducing the quantum cost from 15 to 12 and the circuit depth from 12 to 9, without affecting the correctness of the circuit. Despite the applied optimization, the circuit still require three constant inputs and generates two garbage outputs.

3.2.2 Generalized design of ternary quantum reversible $1 \times n$ demultiplexer

The ternary quantum reversible 1×3 demultiplexer can be generalized to construct a $1 \times n$ demultiplexer, where $n = 3^m$. The generalized design includes one input (I), m selector lines, and n outputs. The circuit is composed of 1×3 demultiplexers arranged. Figure 11 illustrates the logical structure of the proposed $1 \times n$ demultiplexer. It is worth mentioning that the selector lines in the demultiplexer are arranged hierarchically from top to bottom, with each stage governed by a different selector. The lowest-level demultiplexers, which produce the output signals, are controlled by the least significant selector, while the higher-level stages are successively driven by more significant selectors.

The number of 1×3 demultiplexers required for this proposed design is denoted by D and is determined using Equation 11, where n represents the total number of output lines.

$$D = \frac{n-1}{2} \tag{11}$$

The quantum cost, the depth, the required number of constant inputs, and the amount of produced garbage outputs for the proposed $1 \times n$ demultiplexer can be calculated using Equations 12, 13, 14, and 15, respectively. These equations provide a comprehensive framework to assess the resource demands and efficiency of the design.

$$\text{Quantum Cost } = 12D = 12\left(\frac{n-1}{2}\right) \tag{12}$$

$$\text{Depth } = 9D = 9\left(\frac{n-1}{2}\right) \tag{13}$$

$$\text{The number of constant inputs } = 3D = 3\left(\frac{n-1}{2}\right) \tag{14}$$

$$\text{The number of garbage outputs } = D - 1 + (m+1) = \left(\frac{n-1}{2}\right) - 1 + (m+1) \tag{15}$$

Optimizations can be applied to reduce the total number of gates required, leading to minimizing the total quantum cost. By combining ternary 1-qutrit Shift gates within 1×3 demultiplexers, the optimized quantum cost of the proposed ternary quantum reversible $1 \times n$ demultiplexer is given by:

$$\text{Optimized Quantum Cost} = 9D + 3m \tag{16}$$

where D represents the number of 1×3 demultiplexers required, and m shows the number of selectors in the demultiplexer circuit, which is equal to $\log_3(n)$.

To derive the optimized quantum cost expression presented in Equation 16, we can consider that the total number of 1×3 demultiplexers used in the circuit is given by $D = \frac{n-1}{2}$, based on the hierarchical configuration shown in Fig. 11, where n denotes the number of output lines. Each demultiplexer requires 9 M-S gates, leading to a total cost contribution of $9D = \frac{9(n-1)}{2}$.

Although each demultiplexer could include 3 ternary 1-qutrit Shift gates, the design is optimized by reusing Shift gates across selector layers. Since there are $m = \log_3(n)$ selector levels, only 3 Shift gates per layer are required, resulting in an additional cost of $3m$.

By combining the costs from the M-S and shared Shift gates, the total optimized quantum cost could be simplifies to:

$$\frac{9(n-1)}{2} + 3\log_3(n) \tag{17}$$

Table 8 The truth table of a ternary 1×9 demultiplexer

Selectors AB	Outputs Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
00	I	0	0	0	0	0	0	0	0
01	0	I	0	0	0	0	0	0	0
02	0	0	I	0	0	0	0	0	0
10	0	0	0	I	0	0	0	0	0
11	0	0	0	0	I	0	0	0	0
12	0	0	0	0	0	I	0	0	0
20	0	0	0	0	0	0	I	0	0
21	0	0	0	0	0	0	0	I	0
22	0	0	0	0	0	0	0	0	I

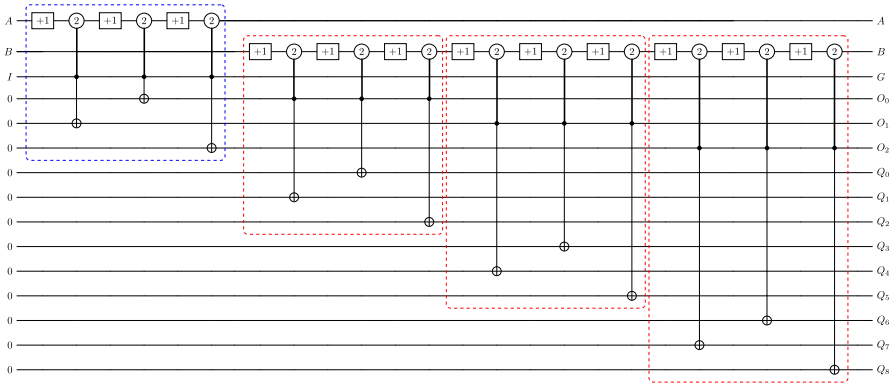


Fig. 12 Proposed ternary quantum reversible 1×9 demultiplexer circuit

This modular and efficient approach allows for straightforward scalability of the $1 \times n$ demultiplexer, making it suitable for larger configurations. Each 1×3 demultiplexer in the design functions as an independent unit, activated by specific combinations of the m selectors. The proposed structure ensures that the input I is routed efficiently to one of the n outputs.

As an example, the proposed 1×3 demultiplexer can be extended to design a 1×9 demultiplexer, which requires one input I, two selectors A and B, and nine outputs Q_0 to Q_8. Table 8 provides the truth table for this circuit. The selectors determine which output receives the target input I in 1×9 demultiplexer.

As can be observed in Fig. 12, the proposed design consists of four 1×3 demultiplexers. When selector $A = 0$, the input I is routed to the outputs O_0 and then to Q_0 to Q_2 by the first 1×3 demultiplexer based on the value of B. Similarly, $A = 1$ or 2 activates the third or fourth 1×3 demultiplexer, respectively, routing the input to the corresponding outputs Q_3 to Q_8. This arrangement enables efficient routing of the input to the desired output.

The realization of this circuit uses twelve ternary 1-qutrit Shift gates and twelve Controlled Feynman gates, resulting in a quantum cost of 48. This cost is achieved by

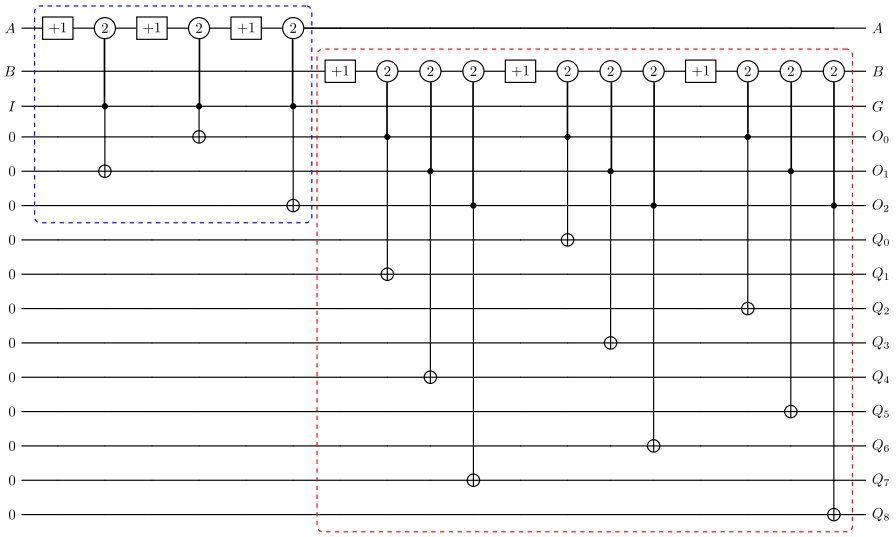


Fig. 13 Proposed optimized ternary quantum reversible 1×9 demultiplexer circuit

using the realization of Controlled Feynman gates without the last M-S gate in Fig. 5b, as the input I and constant inputs in the first demultiplexer do not need to be restored at the garbage outputs. The number of garbage outputs is 6, which includes the outputs corresponding to the input I, the selectors A and B, and the constant inputs required for the operation of the first demultiplexer circuit. A total of 12 constant inputs, initialized to 0, are required.

Further optimization is possible by adopting an alternative realization, as shown in Fig. 13. This optimized design reduces the quantum cost to 42 by employing 12 Controlled Feynman gates and only 6 ternary 1-qutrit Shift gates, while maintaining the same number of constant inputs and garbage outputs. This reduction is achieved by merging in the number of the ternary 1-qutrit Shift gates within the 1×3 demultiplexers and optimizing the overall gate configuration.

The scalability of the 1×9 demultiplexer is a significant advantage. By using 1×3 demultiplexers as modular building blocks, the design can be extended to handle larger configurations. Each 1×3 demultiplexer functions as an independent unit, activated by specific combinations of selectors A and B. This modular approach simplifies the design process and ensures that the circuit remains efficient and manageable, guaranteeing that the circuit is well-suited for large-scale quantum systems. By balancing quantum cost and functional output, the proposed 1×9 demultiplexer provides a reliable and scalable solution for complex reversible computing tasks.

4 Results and evaluation

In this section, we present a comprehensive analysis of our proposed ternary quantum reversible multiplexer and demultiplexer circuits. The primary objective of this

analysis is to assess their efficiency in comparison with the existing designs in the literature [20, 37]. Specifically, we evaluate our proposed circuits with respect to three critical design parameters: quantum cost, depth, the number of garbage outputs, and the number of constant inputs, all of which are discussed in detail in Sect. 1. These parameters play a significant role in determining the efficiency of quantum reversible circuit designs, as minimizing them contributes to enhanced circuit performance and reduced resource consumption.

Our evaluation is structured into two key comparisons: The first focuses on the proposed ternary quantum reversible multiplexer, while the second examines the ternary quantum reversible demultiplexer. We provide a detailed comparative analysis of our designs against existing designs presented in [20, 37].

The proposed circuits were evaluated using QuTiP-MRL, a custom simulation framework developed for multiple-valued reversible logic. This platform extends the QuTiP (Quantum Toolbox in Python) library and enables simulation, gate-level evaluation, and correctness checking of ternary and other multiple-valued quantum circuits. Details of the simulation environment are presented in [35], while scripts simulating all ternary quantum circuits discussed in this paper are available in the online repository [1].

4.1 Evaluation of the ternary quantum reversible multiplexer

Table 9 presents an evaluation of our proposed ternary quantum reversible 3×1 and $n \times 1$ multiplexer circuits based on key performance metrics: quantum cost, depth, garbage outputs, and constant inputs. As these scalable and generalized designs are introduced for the first time, no existing counterparts are available for direct comparisons. As can be observed, the proposed 3×1 multiplexer achieves a quantum cost of 12, requires only one constant input, and generates four garbage outputs, exhibits a circuit depth of 9. Based on this circuit, we proposed an $n \times 1$ multiplexer with a quantum cost of $9\left(\frac{n-1}{2}\right) + 3\log_3(n)$. This expression is derived in detail in Sect. 3.1.2, where the cost contributions from M-S gates and shared Shift gates are analyzed and simplified. The design requires $\frac{n-1}{2}$ constant inputs, produces $3\left(\frac{n-1}{2}\right) + \log_3(n)$ garbage outputs, and has a circuit depth of $9\left(\frac{n-1}{2}\right)$.

Table 10 shows that our proposed approach for ternary quantum reversible 9×1 multiplexer design achieves notable improvements across all four critical parameters, quantum cost, depth, garbage outputs, and constant inputs, when compared with the best ternary quantum reversible multiplexer designs in the literature, reported in [37]. In particular, our multiplexer exhibits a quantum cost of 42, marking a 20% reduction in comparison with the 53 quantum cost of [37], and an even more significant improvement over the 102 quantum cost of the design in [20]. Furthermore, the circuit depth is reduced to 36, achieving an 18% improvement over the depth of 44 reported in [37]. Additionally, our design drastically minimizes the number of constant inputs, reducing them to just 4, a remarkable 60% improvement over the 10 required in [37]. Similarly, the number of garbage outputs is decreased to 14, reflecting a 30% reduction compared to the 20 garbage outputs in [37]. The substantial reductions in these

[1] https://github.com/foselab/QuTiP-MRL/tree/main/examples

Table 9 Result assessment of our proposed ternary quantum reversible multiplexer designs

	Quantum Cost	Depth	Constant Inputs	Garbage Outputs
3×1 Multiplexer	12	9	1	4
$n \times 1$ Multiplexer	$9\left(\frac{n-1}{2}\right) + 3(\log_3(n))$	$9\left(\frac{n-1}{2}\right)$	$\frac{n-1}{2}$	$3\left(\frac{n-1}{2}\right) + (\log_3(n))$

Table 10 Comparison between ternary quantum reversible 9 × 1 multiplexer designs

	Proposed 9 × 1 multiplexer	Improvement percentage	[37]	[20]
Quantum cost	42	20%	53	102
Depth	36	18%	44	75
Constant input number	4	60%	10	11
Garbage output number	14	30%	20	21

values underscore the superior efficiency of our multiplexer architecture, offering a more optimized and scalable solution for reversible computing applications.

4.2 Evaluation of the ternary quantum reversible demultiplexer

Table 11 provides an assessment of our proposed ternary quantum reversible 1×3 and $1 \times n$ demultiplexer circuits, evaluating their performance based on key parameters. According to the results, the proposed 1×3 demultiplexer has a quantum cost of 12, exhibits a circuit depth of 9, requires 1 constant input, and produces 4 garbage outputs. Similarly, the proposed $1 \times n$ demultiplexer is characterized by a quantum cost of $9\left(\frac{n-1}{2}\right) + 3\log_3(n)$ (as derived in Sect. 3.2.2) with $3(\frac{n-1}{2})$ constant inputs, a circuit depth of $9\left(\frac{n-1}{2}\right)$, and $9\left(\frac{n-1}{2}\right) - 1 + (\log_3(n) + 1)$ garbage outputs.

Since these scalable and generalized designs are introduced for the first time as well, there are no existing designs available for direct comparison.

The performance of our proposed ternary quantum reversible 1×9 demultiplexer is summarized in Table 12, which compares our design with its counterparts in [20, 37]. As depicted in the table, our 1×9 demultiplexer design significantly optimizes key performance metrics, including quantum cost, depth, constant input requirements, and garbage output generation. Specifically, our 1×9 demultiplexer requires only 12 constant inputs and produces 6 garbage outputs, representing a substantial reduction compared to the design presented in [37], which requires 18 constant inputs and generates 12 garbage outputs. In addition, our approach achieves a notable improvement in quantum cost, reducing it to 42, which marks a 20% decrease compared to the 53 quantum cost of [37] and an even more significant reduction relative to the 102 quantum cost of the design in [20]. It also achieves a depth of 36, which reflects an 18% improvement over the 44-depth design in [37] and a substantial reduction from the 75-depth design in [20].

These improvements underscore the efficiency of our proposed architecture, as the lower quantum cost directly translates to a more resource-efficient design. Additionally, reducing circuit depth, constant inputs and garbage outputs makes it a more optimized solution for ternary logic-based reversible quantum computing applications. The considerable enhancements achieved in our design demonstrate its superiority over existing alternatives in [20, 37], reinforcing its potential for advancing the field of reversible computing and its applications in low-power, high-performance computing systems.

Overall, these findings indicate that our proposed ternary quantum reversible 9×1 multiplexer and 1×9 demultiplexer are more efficient than their counterparts in [20, 37], as reversible circuits are generally more effective when the important parameters are decreased.

5 Conclusion

This paper has introduced a novel scalable ternary quantum reversible 3×1 multiplexer circuit, using ternary 1-qutrit Shift gates and Controlled Feynman gates. The proposed

Table 11 Result assessment of our proposed ternary quantum reversible demultiplexer designs

	Quantum Cost	Depth	Constant Inputs	Garbage Outputs
1×3 Demultiplexer	12	9	3	2
$1 \times n$ Demultiplexer	$9\left(\frac{n-1}{2}\right) + 3(\log_3(n))$	$9\left(\frac{n-1}{2}\right)$	$3\left(\frac{n-1}{2}\right)$	$9\left(\frac{n-1}{2}\right) + \log_3(n)$

Table 12 Comparison between ternary quantum reversible 1 × 9 demultiplexer designs

	Proposed 1 × 9 demultiplexer	Improvement percentage	[37]	[20]
Quantum cost	42	20%	53	102
Depth	36	18%	44	75
Constant input number	12	33%	18	19
Garbage output number	6	50%	12	13

design has been effectively extended and demonstrated its adaptability for a larger $n \times 1$ configuration. Subsequently, we demonstrated the implementation of a ternary quantum reversible 9×1 multiplexer and compared its performance with existing designs. Additionally, we have presented a scalable realization of a 1×3 demultiplexer, which serves as the foundational architecture for our proposed ternary quantum reversible $1 \times n$ and 1×9 demultiplexer circuits. The proposed designs significantly reduce quantum cost, depth, the number of constant inputs, and the number of garbage outputs compared to existing approaches. Since minimizing these parameters is essential for enhancing the efficiency of reversible circuits, it can be concluded that our multiplexer and demultiplexer designs outperform their existing counterparts, making them a highly optimized solution for reversible logic applications. These advancements contribute to the development of highly efficient, scalable, reversible logic circuits. The proposed circuits enhance security by minimizing information loss, which is crucial for secure quantum computing and quantum cryptographic applications. Future research may explore the integration of our proposed circuits into complex digital systems, including quantum computing and energy-efficient circuit applications. Moreover, we will aim to experimentally validate the proposed circuits and investigate their practical applications in quantum computing. The demonstrated efficiency and scalability of our designs open new possibilities for high-performance ternary and quantum reversible logic, further advancing the field of low-power digital design and computation.

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Data Availability No datasets were generated or analyzed during the current study.

Declarations

Conflict of interest The authors declare no Conflict of interest.

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