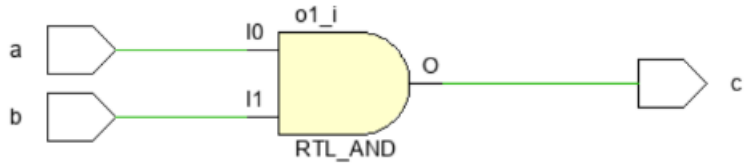
AND GATE IMPLEMENTATION

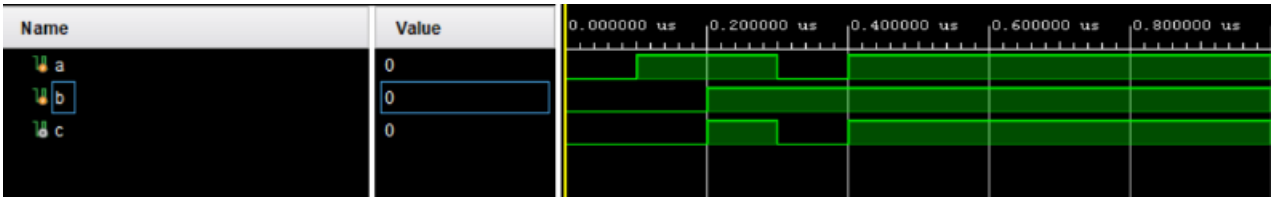
VERILOG CODE:

```
module myANDgate(
input a,
input b,
output c
    );
 and o1(c,a,b);
endmodule
```

RTL:



WAVEFORM:



TEST BENCH CODE:

```
module test1;

	// Inputs
	reg a;
	reg b;

	// Outputs
	wire c;

	// Instantiate the Unit Under Test (UUT)
	MyANDgate uut (
		.a(a),
		.b(b),
		.c(c)
	);

	initial begin
		// Initialize Inputs
		a = 0;
		b = 0;

		// Wait 100 ns for global reset to finish
		#100;
		a = 1;
		b = 0;
// Wait 100 ns for global reset to finish
		#100;
	    a = 1;
		b = 1;
// Wait 100 ns for global reset to finish
#100;
a = 0;
b = 1;

// Wait 100 ns for global reset to finish
#100;
a = 1;
b = 1;

// Wait 100 ns for global reset to finish
#100;


// Add stimulus here
end
endmodule
```