Name	Value
X	1
Y	1
CIN	1
S	1
COUT	1

| 0 ns | 200 ns | 400 ns | 600 ns | 800 ns |

7 Cells   5 I/O Ports   10 Nets

```verilog
module FULLADDER(
    input X,
    input Y,
    input CIN,
    output S,
    output COUT
    );
    xor g1 (S, X, Y, CIN);
    and g2 (t1, CIN, X);
    and g3 (t2, CIN, Y);
    and g4 (t3, X, Y);
    or g5 (COUT, t1, t2, t3);
    endmodule
```

```verilog
module FULLADDER_testbench;
reg X;
reg Y;
reg CIN;
wire S;
wire COUT;
FULLADDER uut (
.X(X),
.Y(Y),
.CIN(CIN),
.S(S),
.COUT(COUT)
);
initial begin
X = 0;
Y = 0;
CIN = 0;
#100;
X = 0;
Y = 0;
CIN = 1;
#100;
X = 0;
Y = 1;
CIN = 0;
#100;
X = 0;
Y = 1;
CIN = 1;
#100;
X = 1;
Y = 0;
CIN = 0;
#100;
X = 1;
Y = 0;
CIN = 1;
#100;
X = 1;
Y = 1;
CIN = 0;
#100;
X = 1;
Y = 1;
CIN = 1;
#100;
end
endmodule
```