LAB 03

DECODER 2-2-4:

VERILOG CODE:

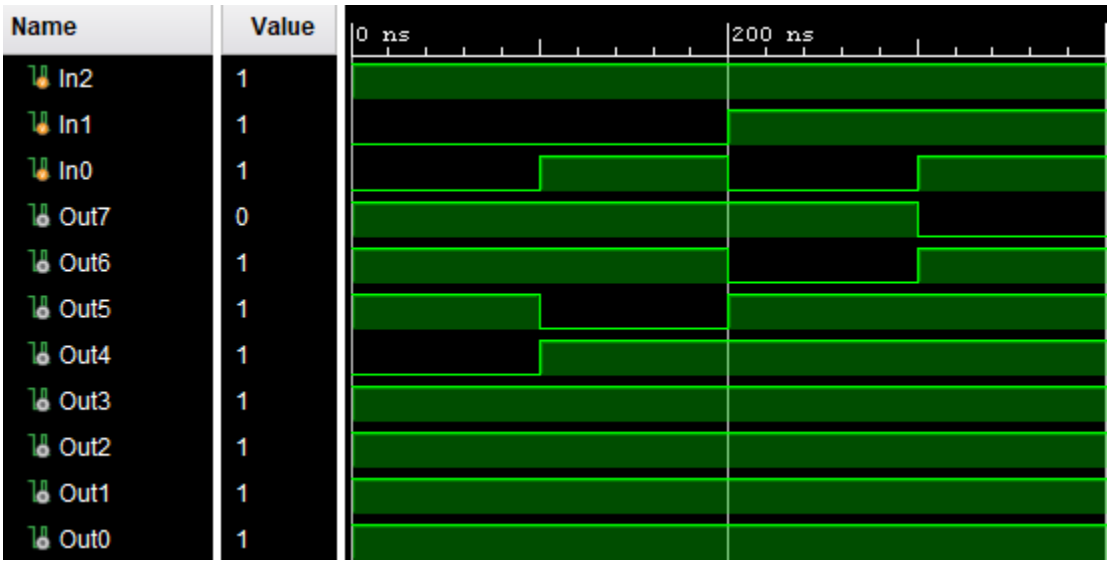
```
module Decoder224(
    input En,
    input In1,
    input In0,
    output Out3,
    output Out2,
    output Out1,
    output Out0
    );
    assign Out3 = ~(En & In1 & In0 );
    assign Out2 = ~(En & In1 & (~In0));
    assign Out1 = ~(En & (~In1) & In0);
    assign Out0 = ~(En & (~In1) & (~In0));

endmodule
```

DECODER 3-2-8:

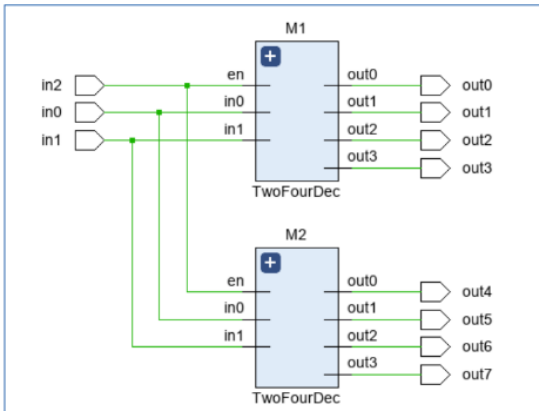
VERILOG CODE:

```
module Decoder328(
    input In2,
    input In1,
    input In0,
    output Out7,
    output Out6,
    output Out5,
    output Out4,
    output Out3,
    output Out2,
    output Out1,
    output Out0
    );
    Decoder224 I1 (~In2,In1,In0,Out3,Out2,Out1,Out0);
    Decoder224 I2 (.En(In2),.In1(In1),.In0(In0),.Out3(Out7),.Out2(Out6),.Out1(Out5),.Out0(Out4));
endmodule
```

WAVEFORM:



RTL:



TESTBENCH CODE:

```
module decoder328_testbench;
      reg In2;
      reg In1;
      reg In0;
      wire Out7;
      wire Out6;
      wire Out5;
      wire Out4;
      wire Out3;
      wire Out2;
      wire Out1;
      wire Out0;
Decoder328 uut(
    .In2(In2),
    .In1(In1),
    .In0(In0),
    .Out7(Out7),
    .Out6(Out6),
    .Out5(Out5),
     .Out4(Out4),
    .Out3(Out3),
    .Out2(Out2),
    .Out1(Out1),
    .Out0(Out0)

);
```

```
initial begin
In2=1;
In1 = 0;
In0 = 0;

#100;
In2=1;
In1 = 0;
In0 = 1;

#100;
In2=1;
In1 = 1;
In0 = 0;


#100;
In2=1;
In1 = 1;
In0 = 1;


#100;
end
endmodule
```

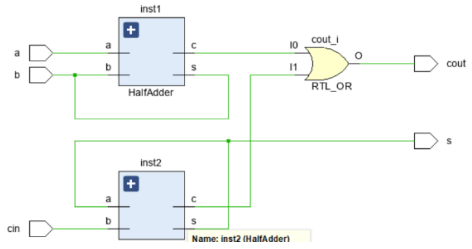
FULL ADDER:

```
module FullAdder(
    input A,
    input B,
    input Cin,
    output S,
    output Cout
    );

   HalfAdder g1 (.A(A),.B(B),.S(B),.C(p));
   HalfAdder g2 (.A(S),.B(Cin),.S(S),.C(q));
   assign cout = p | q ;
endmodule
```

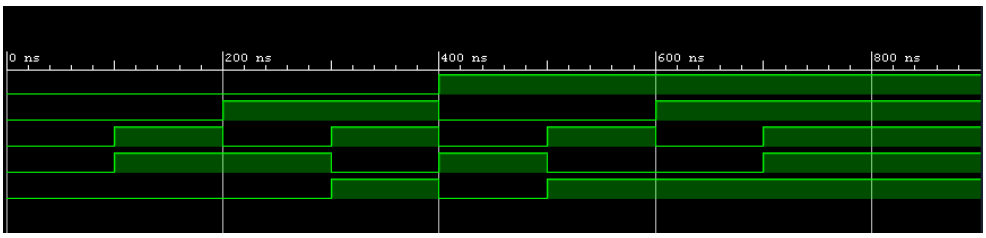
Test bench:

```
module fulladder_tb;
// Inputs
reg a;
reg b;
reg cin;


// Outputs
wire s;
wire cout;
// Instantiate the Unit Under Test (UUT)
FullAdder2 uut (
.a(a),
.b(b),
.s(s),
.cin(cin),
.cout(cout)
);
initial begin
// Initialize Inputs
a = 0;
b = 0;
cin = 0;

// Wait 100 ns for global reset to finish
#100;
a = 0;
b = 1;
cin = 0;

// Wait 100 ns for global reset to finish
#100;
a = 1;
b = 0;
cin = 1;

// Wait 100 ns for global reset to finish
#100;
a = 1;
b = 1;
cin = 1;

// Wait 100 ns for global reset to finish
#100;

// Add stimulus here
end
endmodule
```

RTL:



WAVEFORM:

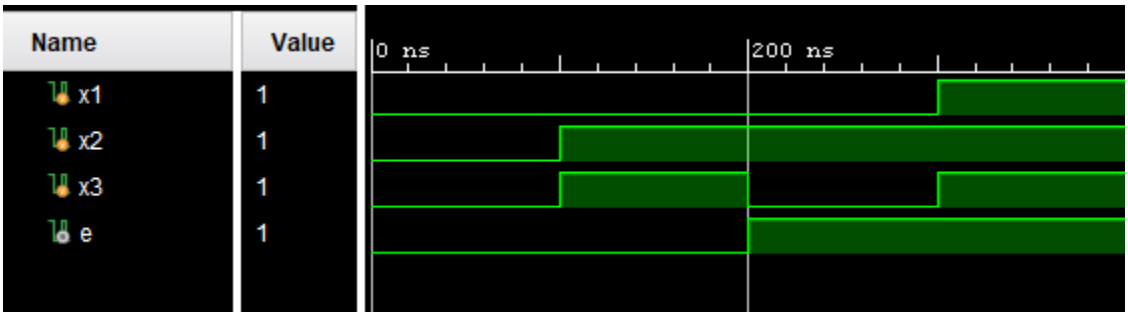


LAB04

DATA FLOW LEVEL

VERILOG CODE:

WAVEFORM:



TEST BENCH CODE:

```
module LAB4_DATAFLOW_testbench;
      reg x1;
      reg x2;
      reg x3;
      wire e;

LAB4_DATAFLOW uut(
    .x1(x1),
    .x2(x2),
    .x3(x3),
    .e(e)


);
initial begin
x1=0;
x2 = 0;
x3 = 0;

#100;
x1=0;
x2 = 1;
x3 = 1;

#100;
x1=0;
x2 = 1;
x3 = 0;


#100;
x1=1;
x2 = 1;
x3 = 1;


#100;
End
```