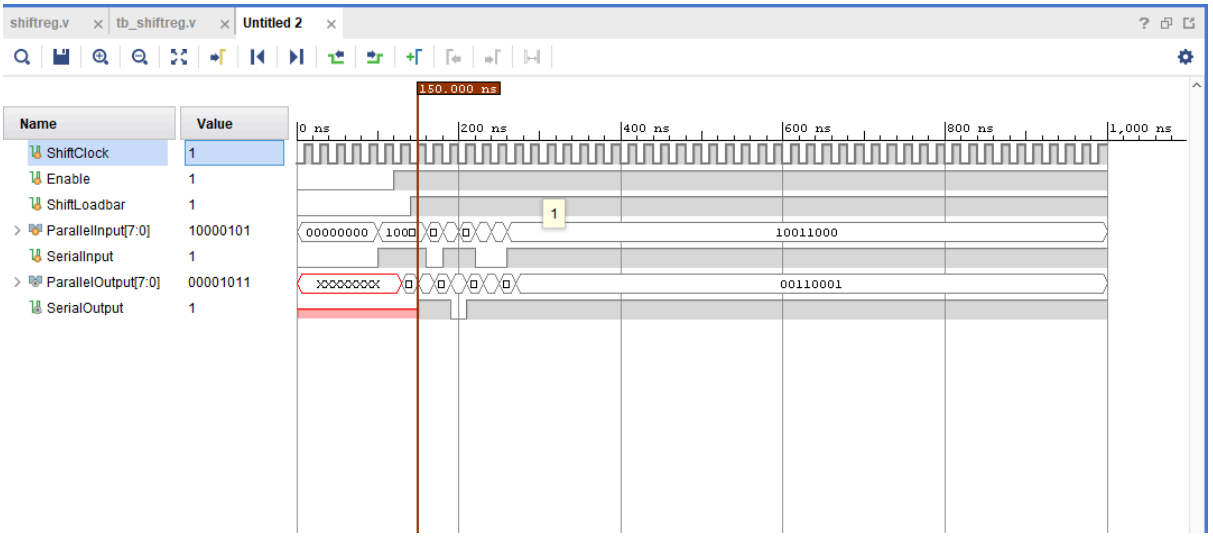
```
22
23      module tb_shiftreg;
24          reg ShiftClock;
25          reg Enable;
26          reg ShiftLoadbar;
27          reg [7:0] ParallelInput;
28          reg SerialInput;
29          wire [7:0] ParallelOutput;
30          wire SerialOutput;
31
32          shiftreg uut(
33              ShiftClock,
34              Enable,
35              ShiftLoadbar,
36              ParallelInput,
37              SerialInput,
38              ParallelOutput,
39              SerialOutput
40              );
41          always
42          #10 ShiftClock = ~ShiftClock;
43
44          initial begin
45              ShiftClock = 0;
46              Enable = 0;
47              ShiftLoadbar = 0;
48              ParallelInput = 0;
49              SerialInput = 0;
50              #100;
51
52              ParallelInput = 8'b10000101;
53              SerialInput = 1;
54
55              #20;
56
57              Enable = 1;
58
59              #20;
60
61              ShiftLoadbar = 1;
62
63              #20;
64              ParallelInput = 8'b11110101;
65              SerialInput = 0;
66
67              #20;
68              ParallelInput = 8'b00000000;
69              SerialInput = 1;
70
71              #20;
72              ParallelInput = 8'b11111111;
73
```

```
74          #20;
75          ParallelInput = 8'b10001111;
76          SerialInput = 0;
77
78          #20;
79          ParallelInput = 8'b10101010;
80
81          #20;
82          ParallelInput = 8'b10011000;
83          SerialInput = 1;
84      end
85
86
87  endmodule
88
```



```
23  module shiftreg(
24      input ShiftClock,
25      input Enable,
26      input ShiftLoadbar,
27      input [7:0] ParallelInput,
28      input SerialInput,
29      output wire [7:0] ParallelOutput,
30      output reg SerialOutput
31      );
32      reg [7:0] ShiftRegister;
33
34      always@(posedge ShiftClock)
35
36      begin
37          if (Enable)
38          begin
39              if (!ShiftLoadbar)
40                  ShiftRegister<=ParallelInput;
41
42              else
43              begin
44                  ShiftRegister=ParallelInput;
45                  {SerialOutput,ShiftRegister} <= ShiftRegister<<1;
46                  ShiftRegister[0] <= SerialInput;
47
48              end
49          end
50      end
51    assign ParallelOutput=ShiftRegister;
52  endmodule
53
```