COMPUTER SYSTEM ARCHITECTURE

(Course code: AECD04)

B.Tech III Semester

Regulation: IARE BT-23

Prepared by:

Mr. N Rajasekhar Reddy

Assistant Professor & Dean – Computer Center

Department of Computer Science and Engineering

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

DUNDIGAL, HYDERABAD - 500 043

Course Outcomes

The course should enable the students to:	
CO 1	Understand the organization and levels of design in computer architecture and To understand the concepts of programming methodologies.
CO 2	Describe Register transfer languages, arithmetic micro operations, logic micro operations, shift micro operations address sequencing, micro program example, and design of control unit.
CO 3	Understand the Instruction cycle, data representation, memory reference instructions, input-output, and interrupt, addressing modes, data transfer and manipulation, program control. Computer arithmetic: Addition and subtraction, floating point arithmetic operations, decimal arithmetic unit.
CO 4	Knowledge about Memory hierarchy, main memory, auxiliary memory, associative memory, cache memory, virtual memory Input or output Interface, asynchronous data transfer, modes of transfer, priority interrupt, direct memory access.
CO 5	Explore the Parallel processing, pipelining-arithmetic pipeline, instruction pipeline Characteristics of multiprocessors, inter connection structures, inter processor arbitration, inter processor Communication and synchronization

MODULE-III

Micro Programmed Control And Input – Output Organization

Course Outcomes

CO 1	Describe Register transfer languages, arithmetic micro operations, logic micro operations, shift micro operations address sequencing, micro program example, and design of control unit.
CO 2	Classify the functionalities of various micro operations such as arithmetic, logic and shift micro operations.
CO 3	Describe the Control unit and Control memory operations.
CO 4	Knowledge about address sequencing in Control memory
CO 5	Explore the micro program example and design of control unit

Contents

Micro Programmed Control:

- Control memory
- Address sequencing
- Design of control unit
- Hardwired Control
- Micro Programmed Control

Control Memory

- Major Components of a digital system are CPU , Memory and I/O Devices.
- The major digital components of CPU are CU ,ALU and Registers.
- The function of control unit is to initiate sequence of micro operations.
- There are two ways to implement control unit:

1. Hardwired Control unit
2. Micro programmed Control Unit

Control Memory

Hardwired Control unit:

- When the control signals are generated by hardware using conventional logic design techniques then it is called hardwired control unit.
- Hardwired control implemented with fixed instructions , fixed logic blocks of arrays , encoders , decoders etc.
- The characteristics of Hardwired control logic are high speed operation , expensive , relatively complex and no flexibility to add new instructions.

Micro programmed CU:

- The main principle of microprogramming is an elegant and systematic method for controlling the micro operation sequence in a digital computer.
- Micro programmed control unit contains variable number of instructions.
- Easy to implement and add new instructions.

Control Memory

- The Control variable at any given time can be represented by a string of 1's and 0's called a Control Word.
- **Microprogram**

  - Program stored in memory that generates all the control signals required to execute the instruction set correctly.
  - Consists of microinstructions .
- **Microinstruction**

  - It Specifies one or more micro operations for the system.
  - Contains a control word and a sequencing word .
  - Control Word - All the control information required for one clock cycle
  - **Sequencing Word** - Information needed to decide the next microinstruction address .
- **Control Memory**.

-Storage in the microprogrammed control unit to store the microprogram.

Control Memory

- **Writeable Control Memory(Writeable Control Storage: WCS)**
  - CS whose contents can be modified
  - Allows the microprogram can be changed
  - Instruction set can be changed or modified .
- **Dynamic Microprogramming**
  - Computer system whose control unit is implemented with a microprogram in WCS .
  - Microprogram can be changed by a systems programmer or a user .
- **Sequencer (Microprogram Sequencer)**
  - A Microprogram Control Unit that determines the Microinstruction Address to be executed in the next clock cycle .

Control Memory

- In-line Sequencing
- Branch
- Conditional Branch
- Subroutine
- Loop
- Instruction OP-code mapping

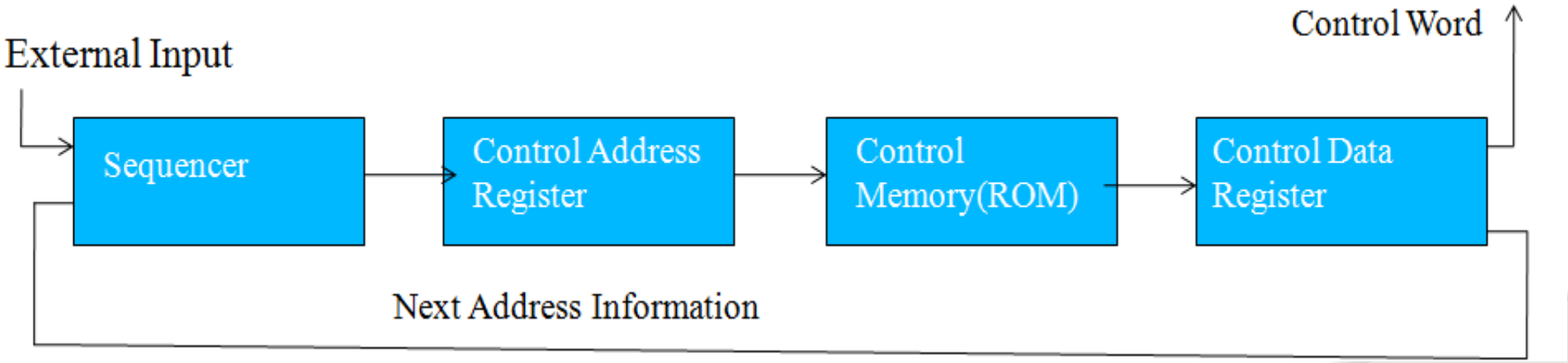


Fig : Micro programmed Control Unit

Address Sequencing

- Microinstructions are stored in control memory in groups, with each group specifying a routine.

- Each computer instruction has its own micro program routine in control memory to generate the micro operations that execute the instruction.

- The hardware that controls the address sequencing of the control memory must be capable of sequencing the microinstructions within a routine and be able to branch from one routine to another.

Address Sequencing

- This address is usually the address of the first microinstruction that activates the instruction fetch routine.

- The fetch routine may be sequenced by incrementing the control address register through the rest of its microinstructions.

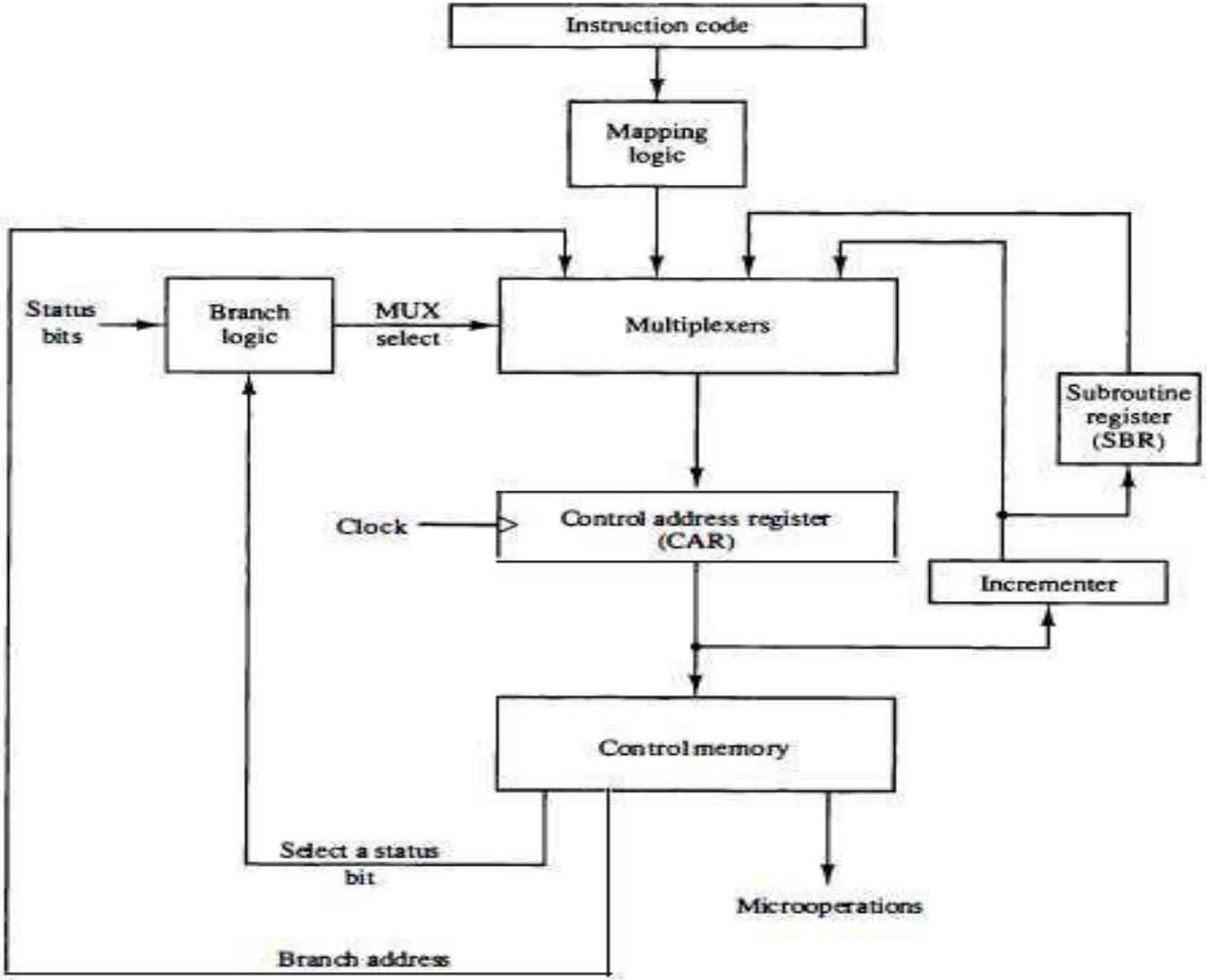
- At the end of the fetch routine, the instruction is in the instruction register of the computer

Address Sequencing

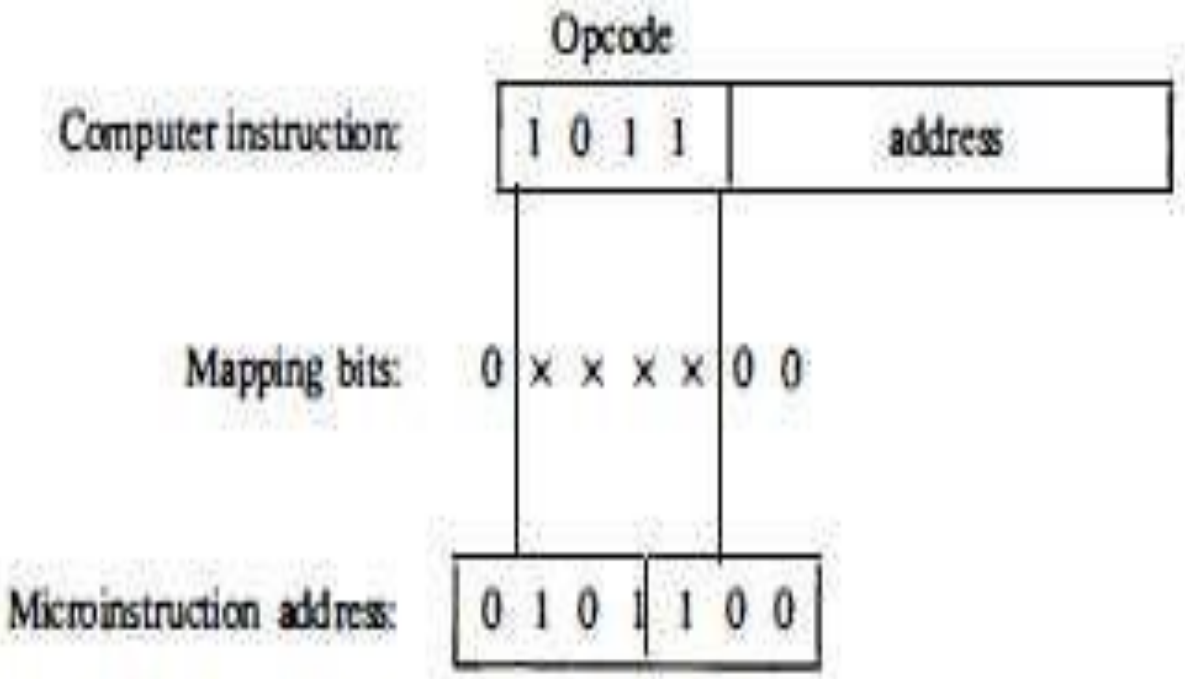
The address sequencing capabilities required in a control memory are:

- 1. Incrementing of the control address register.
- 2. Unconditional branch or conditional branch, depending on status bit conditions.
- 3. A mapping process from the bits of the instruction to an address for control memory

Address Sequencing



Address Sequencing



Address Sequencing

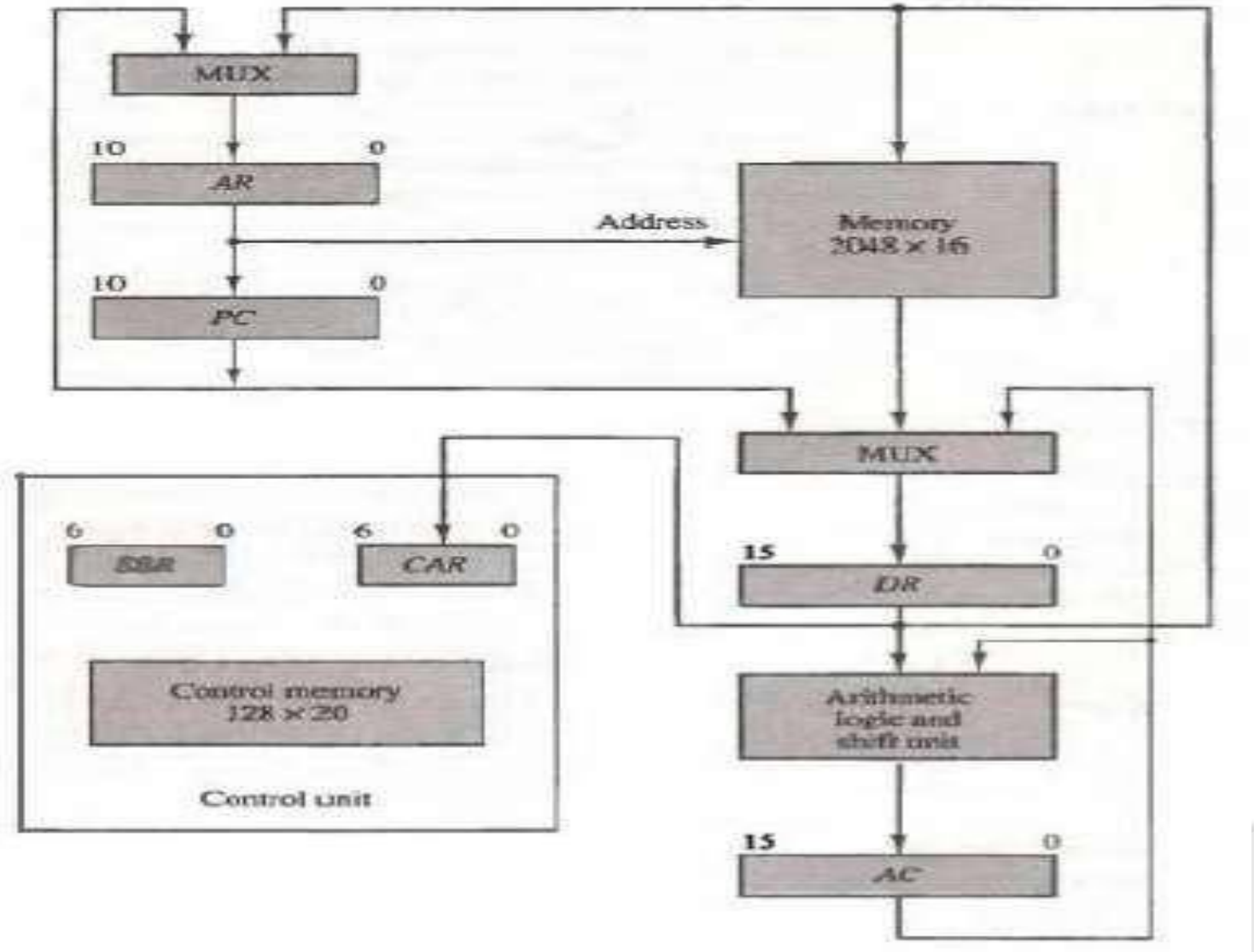
- **Subroutines**

- Subroutines are programs that are used by other routines to accomplish a particular task. A subroutine can be called from any point within the main body of the micro program.
- Frequently, many micro programs contain identical sections of code. Microinstructions can be saved by employing subroutines that use common sections of microcode.
- For example, the sequence of microoperations needed to generate the effective address of the operand for an instruction is common to all memory reference instructions.

Address Sequencing

- This sequence could be a subroutine that is called from within many other routines to execute the effective address computation.
- Micro programs that use subroutines must have a provision for storing the return address during a subroutine call and restoring the address during a subroutine return.

Address Sequencing



Design of Control Unit

- The bits of the microinstruction are usually divided into fields, with each field defining a distinct, separate function.

- The various fields encountered in instruction formats provide control bits to initiate microoperations in the system, special bits to specify the way that the next address is to be evaluated, and an address field for branching.

- The number of control bits that initiate micro operations can be reduced by grouping mutually exclusive variables into fields and encoding the k bits in each field to provide 2' micro operations.

Design of Control Unit

- Figure 2.18 shows the three decoders and some of the connections that must be made from their outputs.

- Each of the three fields of the microinstruction presently available in the output of control memory are decoded with a 3 x 8 decoder to provide eight outputs.

- As shown in Figure 2.18 outputs 5 and 6 of decoder f1 are connected to the load input of AR so that when either one of these outputs is active, information from the multiplexers is transferred to AR.

Design of Control Unit

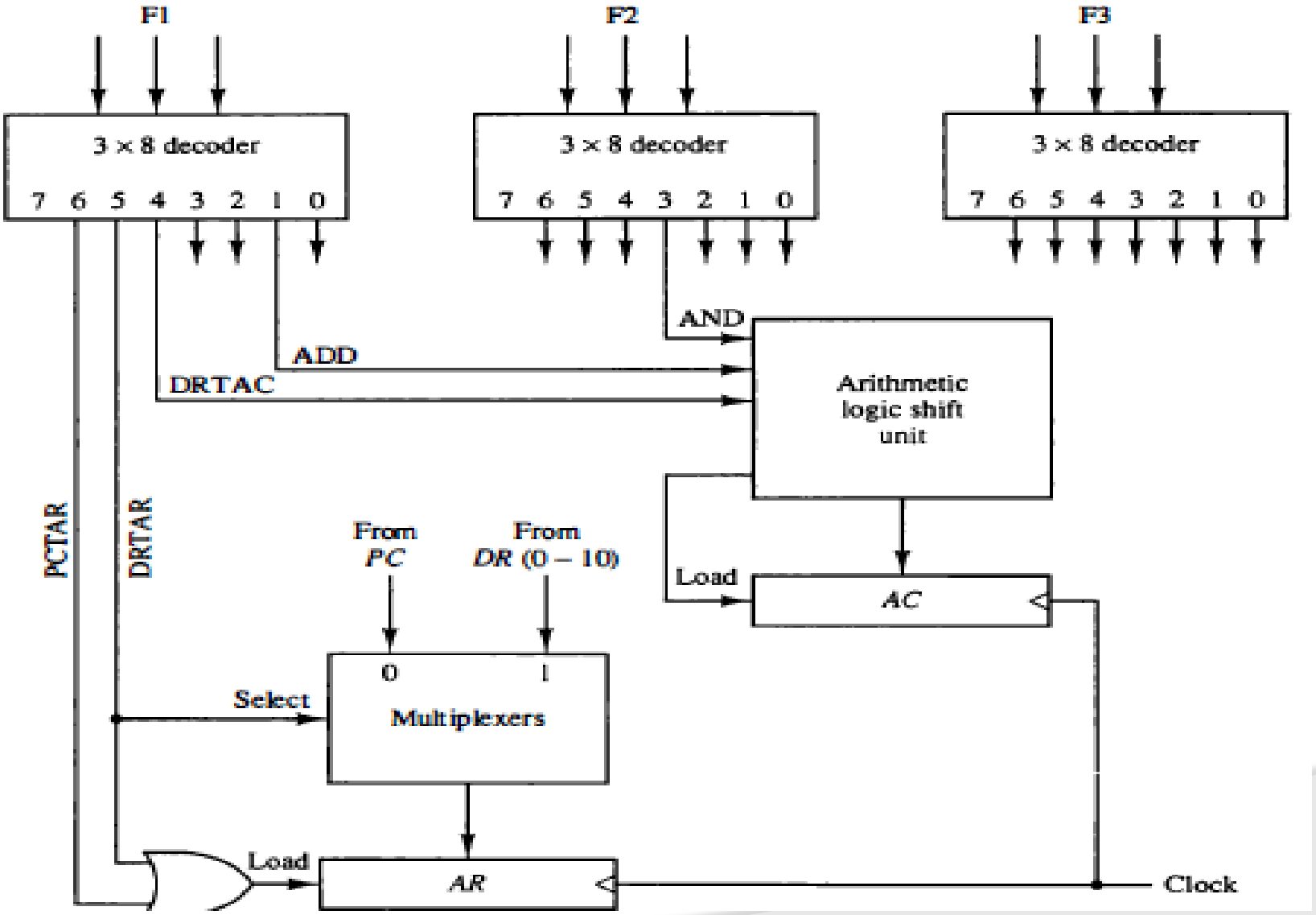
TABLE 7-4 Input Logic Truth Table for Microprogram Sequencer

BR Field		Input			MUX 1		Load *SBR*
		I_1	I_0	T	S_1	S_0	L
0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0
0	1	0	1	0	0	0	0
0	1	0	1	1	0	1	1
1	0	1	0	x	1	0	0
1	1	1	1	x	1	1	0

Design of Control Unit

- The multiplexers select the information from DR when output 5 is active and from PC when output 5 is inactive, as shown in Figure 2.18. The other outputs of the decoders that are associated with an AC operation must also be connected to the arithmetic logic shift unit in a similar fashion.

Design of Control Unit



Design of Control Unit

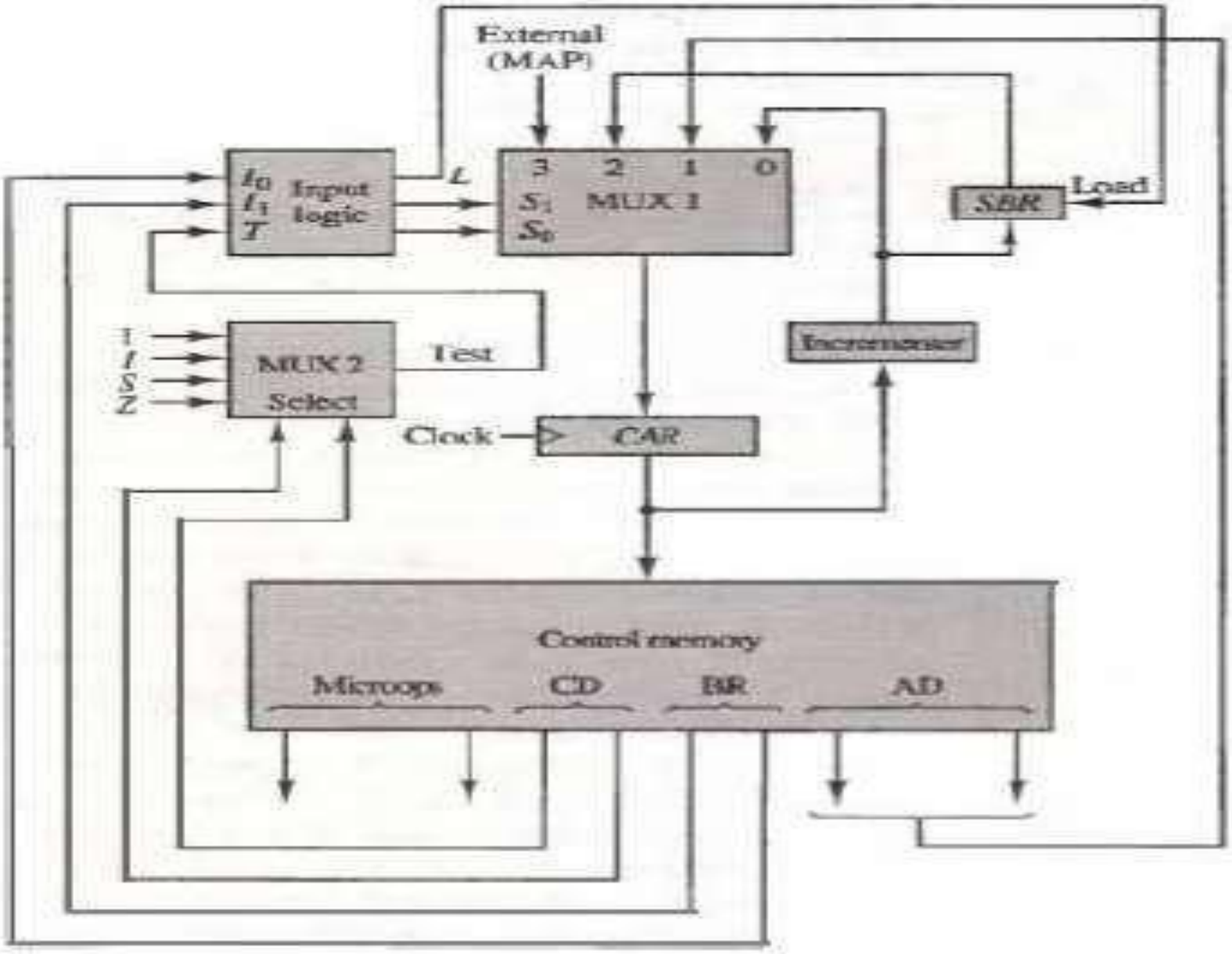
- A microprogram sequencer can be constructed with digital Functions to suit a particular application.
- However, just as there are large ROM units available in integrated circuit packages, so are general-purpose sequencers suited for the construction of microprogram control units.
- To guarantee a wide range of acceptability, an integrated circuit sequencer must provide an internal organization that can be adapted to a wide range of applications.
- The block diagram of the microprogram sequencer is shown in Fig.

Design of Control Unit

- The control memory is included in the diagram to show the interaction between the sequencer and the memory attached to it.

- There are two multiplexers in the circuit. The first multiplexer selects an address from one of four sources and routes it into a control address register CAR .

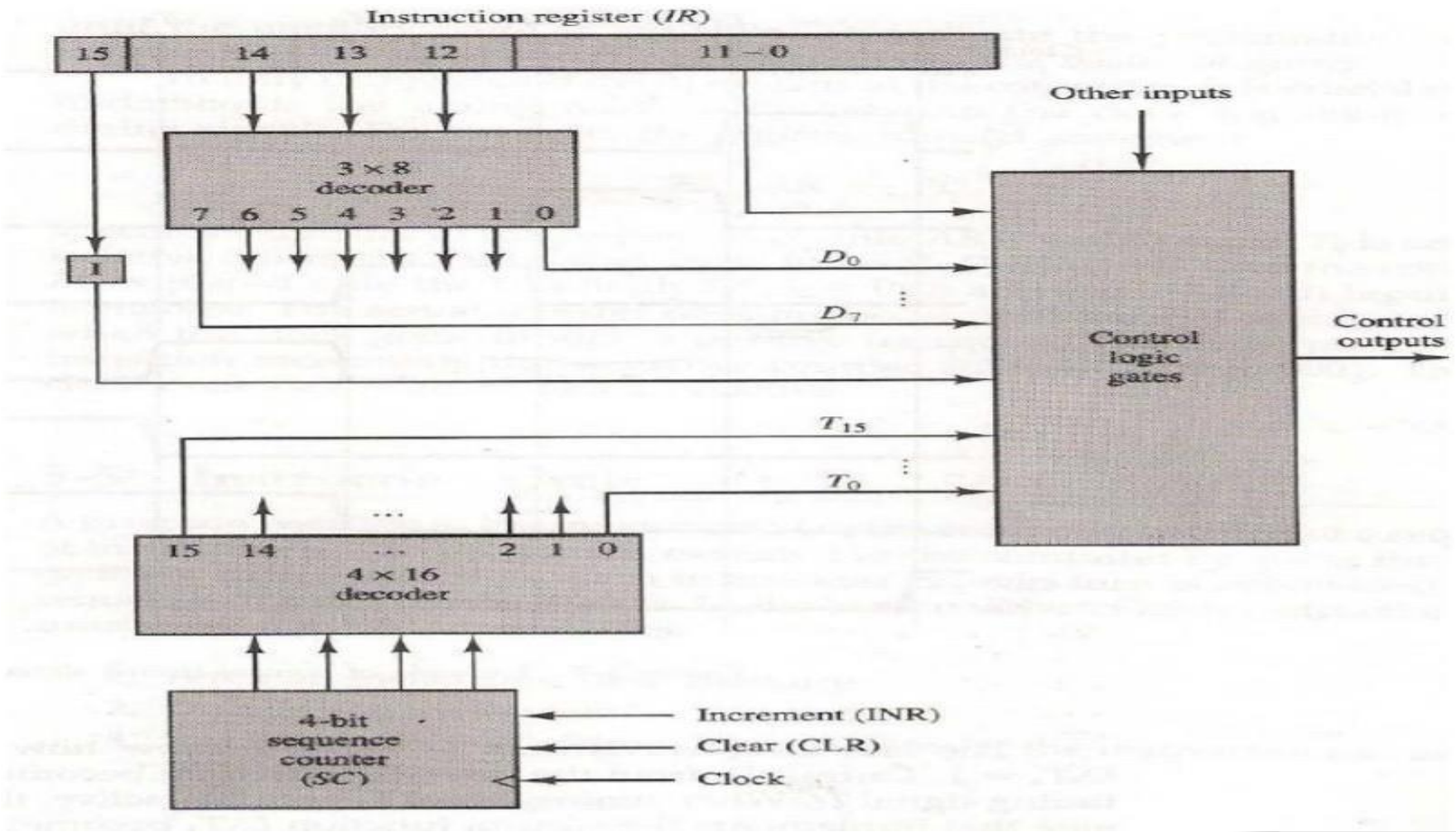
Design of Control Unit



Design of Control Unit

- The input logic circuit in Fig. has three inputs, l0, l1, and T, and three outputs, S0, S1, and L. Variables So and S, select one of the source addresses for CAR .
- Variable L enables the load input in SBR. The binary values of the two selection variables determine the path in the multiplexer.
- For example, with S1 So = 10, multiplexer input number 2 is selected and establishes a transfer path from SBR to CAR. Note that each of the four inputs as well as the output of MUX 1 contains a 7-bit address.

Hardwired Control



The block diagram of the Hardwired Control Unit

Hardwired Control

The control unit of basic computers consists of two decoders, a sequence counter and a number of control logic gates.

- An instruction read from memory is placed in the instruction register (IR). It is divided into three parts:
  - The I bit
  - The operation code and
  - Bits 0 through 11.
- The operation code in bits 12 through 14 are decoded with a 3*8 decoder. The eight outputs of the decoder are designated by the symbols D0 through D7.
- Bit 15 of the instruction is transferred to a flip-flop designated by the symbol I.
- Bits 0 through 11 are applied to the control logic gates.

Hardwired Control

An instruction read from memory is placed in the **instruction register (IR)**.

- The instruction register is divided into three parts: the I bit, operation code, and address part.
- First 12-bits (0-11) to specify an address, next 3-bits specify the operation code (opcode) field of the instruction and last left most bit specify the addressing mode I.

I = 0 for direct address

I = 1 for indirect address

- First 12-bits (0-11) are applied to the control logic gates.
- The operation code bits (12 – 14) are decoded with a 3 x 8 decoder.
- The eight outputs (D0 through D7) from a decoder goes to the control logic gates to perform specific operation.

Hardwired Control

- Last bit 15 is transferred to a I flip-flop designated by symbol I
- The 4-bit sequence counter SC can count in binary from 0 through 15.
- The counter output is decoded into 16 timing pulses T0 through T15.
- The sequence counter can be incremented by INR input or clear by CLR input synchronously.

Micro Programmed Control

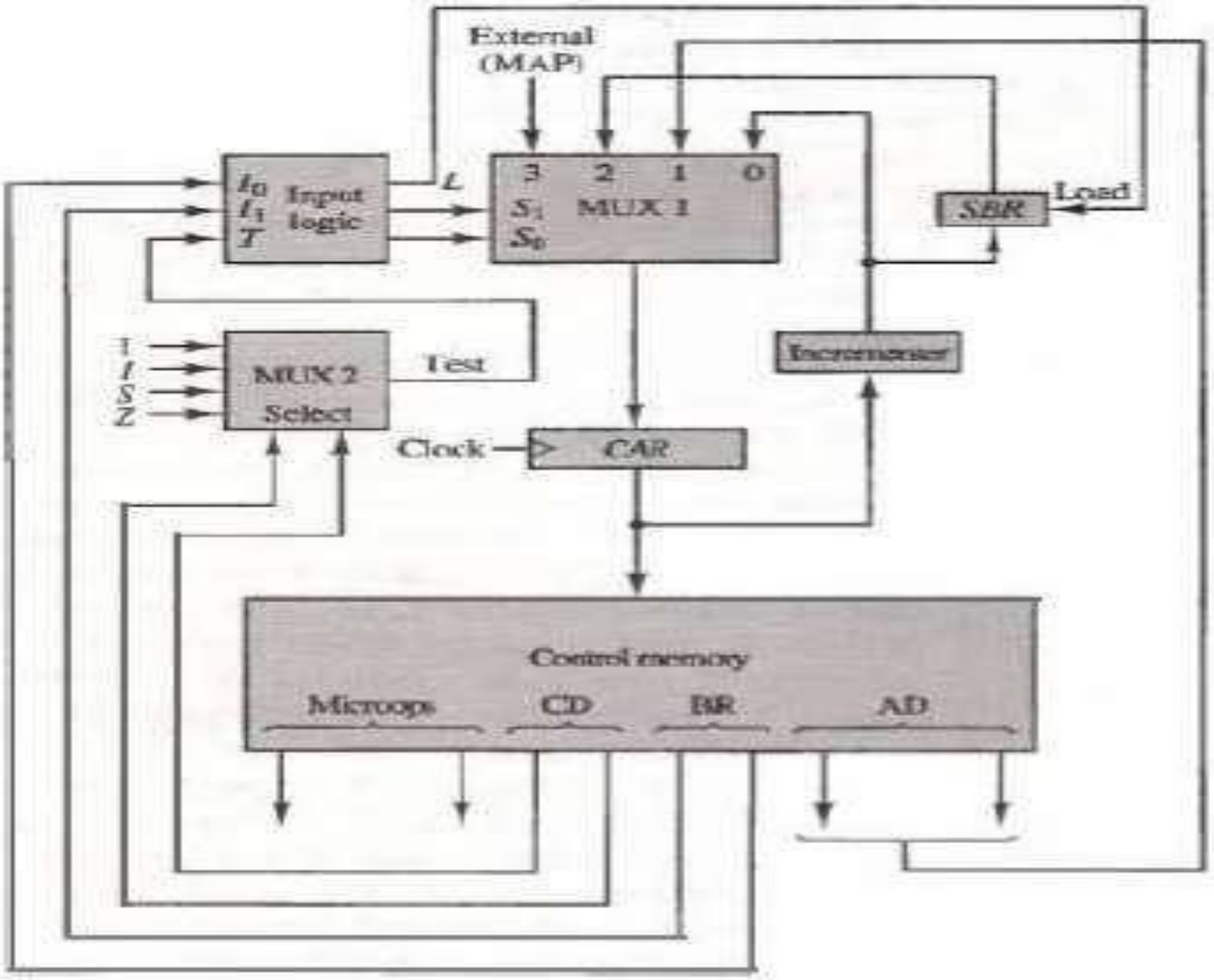
- A micro program sequencer can be constructed with digital functions to suit a particular application.

- To guarantee a wide range of acceptability, an integrated circuit sequencer must provide an internal organization that can be adapted to a wide range of applications.

- The control memory is included in the diagram to show the interaction between the sequencer and the memory attached to it.
- The binary values of the two selection variables determine the path in the multiplexer.

- For example, with S1, So = 10, multiplexer input number 2 is selected and establishes a transfer path from SBR to CAR. Note that each of the four inputs as well as the output of MUX 1 contains a 7-bit address.

Micro Programmed Control



Differences Between Hardwired Control Micro programmed Control

Hardwired Control	Micro-programmed Control
The control logic is implemented with gates, flip-flops, decoders and other digital circuits.	The control information is stored in a control memory. The control memory is programmed to initiate the required sequence of micro operations.
The advantage is that it can be optimized to produce a fast mode of operation.	Compared with the hardwired control operation is slow.
Requires changes in the wiring among the various components if the design has to be modified or changed.	Required changes or modifications can be done by updating the microprogram in control memory.