MODULE 4 (CSA)

PART-A

Q1) Describe The Role Of Each Level in the Memory Hierarchy (cache,main memory, auxiliary memory,and virtual memory)and discuss how they work together to optimize system performance.Which level do you think most critical for improving speed,and why?

A. **1. Cache Memory**

Role:

- Cache memory is the fastest type of memory, located close to the CPU. It stores frequently accessed data and instructions to reduce the average time to access data from the main memory.
- There are typically multiple levels of cache (L1, L2, L3), with L1 being the smallest and fastest, integrated directly within the CPU core, and L3 being larger and slower, shared among multiple cores.

How It Works:

- When the CPU needs data, it first checks the cache. If the data is found (cache hit), it is accessed quickly.
- If the data is not found (cache miss), it is fetched from the main memory and placed in the cache for future use.

2. Main Memory (RAM)

Role:

- Main memory, or RAM, is where the active working set of data and instructions for running programs are stored. It is slower than cache memory but offers larger storage capacity.
- RAM is volatile, meaning it loses its data when the power is turned off.

How It Works:

- The CPU accesses data from RAM when it is not available in the cache.
- RAM acts as a bridge between the fast cache memory and the slower auxiliary memory, providing reasonably fast access to data for running programs.

3. Auxiliary Memory (Secondary Storage)

Role:

- Auxiliary memory includes hard drives (HDDs) and solid-state drives (SSDs). It provides large, persistent storage for data and programs.
- It is much slower than RAM and cache but offers a significantly larger capacity.

How It Works:

- Data and programs are stored in auxiliary memory when not in active use.
- When data is needed, it is loaded from auxiliary memory into RAM, and from there, potentially into the cache if it becomes frequently accessed.

4. Virtual Memory

Role:

- Virtual memory is a technique that allows the computer to use a portion of the auxiliary memory as if it were additional RAM.
- This creates the illusion of a larger main memory, enabling the execution of larger programs than would otherwise fit in RAM.

How It Works:

- The operating system divides memory into pages and manages the transfer of data between RAM and the auxiliary memory (swap space).
- When the system runs out of RAM, less frequently used data is moved to the swap space, and more needed data is brought into RAM, maintaining an efficient working set.

How They Work Together to Optimize Performance

- **Cache Memory**: Provides the fastest access to the most frequently used data, minimizing CPU wait times and enhancing performance.
- **Main Memory**: Serves as the main workspace for active data and instructions, bridging the speed gap between cache and auxiliary memory.
- **Auxiliary Memory**: Offers large, persistent storage, ensuring data and programs are preserved and available for future use.
- **Virtual Memory**: Extends the capacity of main memory, allowing the system to handle larger workloads and multitasking more effectively.

Critical Level for Improving Speed: Cache Memory

Reason:

- **Speed**: Cache memory operates at speeds close to that of the CPU, significantly reducing the time needed to access frequently used data and instructions.
- **Efficiency**: A well-designed cache system can vastly improve the efficiency of the CPU, minimizing delays caused by slower memory accesses.
- **Hit Rate**: Higher cache hit rates lead to fewer accesses to slower memory levels, directly enhancing overall system performance.

Q2) Explain The Fundamental differencesbetweenStatic RAM(SRAM)andDynamic RAM(DRAM) in terms of structure,performance,and use cases. In What Scenarios would one be preferred over the other?

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Fundamental Differences Between Static RAM (SRAM) and Dynamic RAM (DRAM)

Static RAM (SRAM) and Dynamic RAM (DRAM) are two types of semiconductor memory used in computers. They differ significantly in terms of structure, performance, and use cases.

Structure

SRAM:

- **Technology**: Uses bistable latching circuitry made up of transistors (typically six transistors per bit).
- **Storage Cells**: Each cell stores a bit of data without needing to refresh, as long as power is supplied.
- **Complexity**: More complex circuitry per bit, leading to higher density and more power consumption.

DRAM:

- **Technology**: Uses a capacitor and a transistor for each bit of data.
- **Storage Cells**: Each cell stores a bit in a capacitor, which needs to be periodically refreshed to retain data.
- **Simplicity**: Simpler cells with fewer transistors, allowing for higher density and lower cost per bit.

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Performance

SRAM:

- **Speed**: Faster access times (nanoseconds) due to simpler read/write cycles.
- **Power Consumption**: Consumes more power because all parts of the memory remain active.
- **Latency**: Lower latency, making it ideal for cache memory.

DRAM:

- **Speed**: Slower access times compared to SRAM due to the need for refreshing and more complex read/write operations.
- **Power Consumption**: Lower power consumption in idle states as only the cells being accessed are active.

- **Latency**: Higher latency, but suitable for larger storage needs.

Use Cases

SRAM:

- **Cache Memory**: Used in CPU cache (L1, L2, L3) due to its high speed and low latency.
- **Embedded Systems**: Utilized in applications requiring fast memory access and low latency.
- **Networking Devices**: Found in routers and switches for fast data processing.

DRAM:

- **Main Memory (RAM)**: Widely used as the main memory in computers and other devices due to its high density and lower cost.
- **Graphics Memory**: Used in graphics cards (GDDR) where large amounts of data are processed.
- **Mobile Devices**: Incorporated in smartphones and tablets for general-purpose memory.

Scenarios for Preference

When to Prefer SRAM:

- **High-Speed Requirements**: Applications where speed and low latency are critical, such as CPU caches and real-time processing systems.

- **Low Power Applications**: Despite higher power consumption when active, SRAM is used in scenarios where idle power consumption can be managed effectively.

When to Prefer DRAM:

- **Large Memory Requirements**: Situations where high memory capacity is needed at a lower cost, such as main system memory.
- **Cost-Sensitive Applications**: Devices that require large amounts of memory but need to keep costs low, such as consumer electronics and general computing.

Q3) When Designing a new computer system,what trade-offs must be considered when deciding how much cache memory to include versus how much main memory to allocate?How would decisions impact overall performance and cost?

A. **Trade-Offs to Consider**

1. Performance

- **Cache Memory**:
  - **Speed**: Cache memory is significantly faster than main memory. It reduces the time the CPU spends waiting for data.
  - **Hit Rate**: Higher cache sizes generally lead to higher hit rates, meaning more data requests can be served from the cache, improving overall system speed.
- **Main Memory**:

    - **Capacity**: Main memory provides a larger storage area for data and programs that are actively being used.
    - **Latency**: Accessing data from main memory is slower compared to cache memory.

2. Cost

- **Cache Memory**:
    - **Cost per Byte**: Cache memory (especially L1 and L2 caches) is much more expensive per byte than main memory because it uses faster, more complex technology like SRAM.
    - **Economics of Scale**: Increasing the cache size significantly impacts the cost of the processor.
- **Main Memory**:
    - **Cost per Byte**: Main memory (typically DRAM) is cheaper per byte compared to cache memory.
    - **Upgrade Flexibility**: It's often easier and more cost-effective to add more RAM to a system than to increase the cache size.

3. Power Consumption

- **Cache Memory**:
    - **Efficiency**: Smaller, faster memory consumes less power. However, as cache size increases, power consumption also increases.
- **Main Memory**:
    - **Higher Power Usage**: More DRAM means more power consumption overall, which can affect battery life in portable devices.

4. Complexity and Design

- **Cache Memory**:
    - **Complexity**: Implementing larger caches introduces complexity in cache coherence protocols and management.
- **Diminishing Returns**: Beyond a certain point, increasing cache size yields diminishing returns due to factors like cache coherency issues.

Main Memory:

- **Simplicity**: Increasing main memory size is generally straightforward and provides clear benefits for running larger applications and multitasking.

Q4) How Does The Operation Of SynchronousDRAM (SDRAM) Improve Performance Compared To AsynchronousDRAM? Provide Examples Of applications where SDRAM is critical.

A. **How SDRAM Improves Performance**

1. **Synchronization with CPU Clock**:
    - **SDRAM**: Operates in sync with the system clock, allowing precise timing for data transfer. This synchronization enables predictable and faster access times, reducing latency.
    - **Asynchronous DRAM**: Does not synchronize with the system clock, leading to variable access times and

increased latency due to the need for the CPU to wait for data availability.

2. **Pipelined Operation**:
   - **SDRAM**: Supports pipelining, where multiple memory operations are overlapped. This means while one data read/write is being executed, the next can be prepared, significantly increasing throughput.
   - **Asynchronous DRAM**: Typically processes one memory operation at a time, leading to slower overall performance.
3. **Burst Mode**:
   - **SDRAM**: Utilizes burst mode to transfer blocks of data sequentially after the initial address is provided. This efficient data transfer reduces overhead and increases data throughput.
   - **Asynchronous DRAM**: Transfers data one word at a time, making it less efficient for continuous data access.
4. **Predictable Timing**:
   - **SDRAM**: The synchronization with the clock ensures more predictable and consistent timing for memory operations, which is crucial for high-performance computing tasks.
   - **Asynchronous DRAM**: Variable timing due to lack of synchronization can lead to unpredictability and inefficiencies in high-speed systems.

Applications Where SDRAM is Critical

1. **High-Performance Computing**:

    - SDRAM is essential in high-performance computing environments, such as scientific simulations, financial modeling, and large-scale data processing, where fast and predictable memory access is crucial.

2. **Gaming Systems**:
    - Modern gaming consoles and high-end gaming PCs require the fast and efficient memory access provided by SDRAM to handle complex graphics and real-time processing demands.

Servers and Workstations:

- Servers and workstations benefit from SDRAM's high bandwidth and low latency, which are vital for managing multiple simultaneous tasks, virtual machines, and extensive databases.

Embedded Systems:

- SDRAM is used in embedded systems that demand high-speed data processing, such as automotive control systems, networking devices, and industrial automation.

Graphics Cards:

- Graphics cards utilize SDRAM (often in the form of GDDR - Graphics Double Data Rate) to handle the intensive data processing required for rendering high-resolution images and videos.

Q5) How Has The Advancement in non-volatile memory technologies influenced system architecture and software design?Discuss How this may affect both consumer devices and enterprise solutions?

A. Advancements in non-volatile memory (NVM) technologies have significantly influenced both system architecture and software design, with notable impacts on consumer devices and enterprise solutions.

System Architecture

1. **Unified Memory Hierarchy**: Traditional architectures have separate layers for volatile (e.g., DRAM) and non-volatile (e.g., SSDs) memory. Emerging NVM technologies like phase-change memory (PCM) and resistive RAM (RRAM) are blurring these lines, enabling a unified memory hierarchy1.
2. **Reduced Latency**: NVM technologies offer lower latency compared to traditional storage solutions, which can lead to faster data access and improved overall system performance.
3. **Energy Efficiency**: NVMs consume less power, which is crucial for battery-operated devices and data centers aiming to reduce energy consumption.

Software Design

1. **File Systems**: Traditional file systems are designed for volatile memory, but NVM requires new file systems that can handle persistent storage. This includes changes to how data is written, read, and cached1.

2. **Virtual Memory**: With faster NVM, the need for swapping data between RAM and disk storage decreases, leading to potential redesigns of virtual memory management.
3. **Application Development**: Developers can now design applications that leverage persistent memory, allowing for faster startup times and improved data persistence

Q6) Illustrate The Characteristics of some common memory technologies

A. The key characteristics of memory devices or memory system are as follows:

1. Location
2. Capacity
3. Unit of Transfer
4. Access Method
5. Performance
6. Physical type
7. Physical characteristics
8. Organization

1. Location: It deals with the location of the memory device in the computer system. There are three possible locations: CPU : This is often in the form of CPU registers and a small amount of cache Internal or main: This is the main memory like RAM or ROM. The CPU can directly access the main memory. External or secondary: It comprises secondary storage devices like hard disks, magnetic tapes. The CPU doesn’t access these devices

directly. It uses device controllers to access secondary storage devices.

2. Capacity: The capacity of any memory device is expressed in terms of: i)word size ii)Number of words

Word size: Words are expressed in bytes (8 bits). A word can however mean any number of bytes. Commonly used word sizes are 1 byte (8 bits), 2bytes (16 bits) and 4 bytes (32 bits).

Number of words: This specifies the number of words available in the particular memory device. For example, if a memory device is given as 4K x 16.This means the device has a word size of 16 bits and a total of 4096(4K) words in memory.

3. Unit of Transfer: It is the maximum number of bits that can be read or written into the memory at a time. In case of main memory, it is mostly equal to word size. In case of external memory, the unit of transfer is not limited to the word size; it is often larger and is referred to as blocks.

4. Access Methods: It is a fundamental characteristic of memory devices. It is the sequence or order in which memory can be accessed. There are three types of access methods: Random Access: If storage locations in a particular memory device can be accessed in any order and access time is independent of the memory location being accessed. Such memory devices are said to have a random access mechanism. RAM (Random Access Memory) IC's use this access method. Serial Access: If memory locations can be accessed only in a certain predetermined sequence, this access method is called serial access. Magnetic Tapes, CD-ROMs employ serial access methods. Semi random

Access: Memory devices such as Magnetic Hard disks use this access method. Here each track has a read/write head thus each track can be accessed randomly but access within each track is restricted to a serial access.

5. Performance: The performance of the memory system is determined using three parameters: Access Time: In random access memories, it is the time taken by memory to complete the read/write operation from the instant that an address is sent to the memory. For non random access memories, it is the time taken to position the read write head at the desired location. Access time is widely used to measure performance of memory devices. Memory cycle time: It is defined only for Random Access Memories and is the sum of the access time and the additional time required before the second access can commence. Transfer rate: It is defined as the rate at which data can be transferred into or out of a memory unit.

6. Physical type: Memory devices can be either semiconductor memory (like RAM) or magnetic surface memory (like Hard disks).

7. Physical Characteristics: Volatile/Non- Volatile: If a memory device continues to hold data even if power is turned off. The memory device is non-volatile else it is volatile.

8. Organization: Erasable/Non-erasable: The memories in which data once programmed cannot be erased are called Non-erasable memories. Memory devices in which data in the memory can be erased is called erasable memory. E.g. RAM(erasable), ROM(non-erasable).

Q7) Explain a privileged instruction set in memory?
A. The Instructions that can run only in Kernel Mode are called Privileged Instructions . Privileged Instructions possess the following characteristics :

(i) If any attempt is made to execute a Privileged Instruction in User Mode, then it will not be executed and treated as an illegal instruction. The Hardware traps it to the Operating System.

(ii) Before transferring the control to any User Program, it is the responsibility of the Operating System to ensure that the Timer is set to interrupt. Thus, if the timer interrupts then the Operating System regains the control. Thus, any instruction which can modify the contents of the Timer is a Privileged Instruction

iii) Privileged Instructions are used by the Operating System in order to achieve correct operation.

(iv) Various examples of Privileged Instructions include:

I/O instructions and Halt instructions
Turn off all Interrupts
Set the Timer
Context Switching
Clear the Memory or Remove a process from the Memory
Modify entries in Device-status table

Q8) Demonstrate the asynchronous bus with read and write cycles?
A: **Asynchronous Bus with Read and Write Cycles**

An asynchronous bus is a type of communication bus in which data transfer is not synchronized with a common clock. Instead, handshaking signals are used to coordinate the transfer of data between the bus master and slave. Let's walk through the read and write cycles of an asynchronous bus.

Asynchronous Read Cycle

1. **Initiate Read**:
    - The bus master places the address of the data to be read on the address bus.
    - The bus master asserts the Read Request signal (RD).
2. **Address Strobe**:
    - The bus master asserts the Address Strobe signal (AS), indicating that a valid address is present on the address bus.
3. **Data Ready**:
    - The addressed slave device decodes the address and places the requested data on the data bus.
    - The slave device asserts the Data Acknowledge signal (DAK) once the data is ready.
4. **Data Transfer**:
    - The bus master reads the data from the data bus.
    - After reading the data, the bus master deasserts the Read Request (RD) and Address Strobe (AS) signals.
5. **Completion**:
    - The slave device deasserts the Data Acknowledge signal (DAK), completing the read cycle.

Asynchronous Write Cycle

1. **Initiate Write**:
    - The bus master places the address of the data to be written on the address bus.

- The bus master places the data to be written on the data bus.
- The bus master asserts the Write Request signal (WR).

2. **Address Strobe**:
   - The bus master asserts the Address Strobe signal (AS), indicating that a valid address is present on the address bus.

Q9) Apply the modes of data transfer in memory organization to give the functionality in detail?

A. the mode of transferring information between internal storage and external I/O devices is known as I/O interface or input/output interface.

I/O Module Decisions:

Hide or reveal device properties to CPU

Support multiple or single devices

Control device functions or leave for CPU

Also, O/S decisions – e.g. Unix treats everything it can as a file

Mode of Transfer:

Data transfer between the central computer to I/O devices may be handled in a variety of modes.

1.–Programmed I/O

2.–Interrupt Initiated I/O

3.–Direct Memory Access (DMA)

Programmed I/O:

CPU requests I/O operation

I/O module performs operations.

I/O module sets status bits

CPU checks status bits periodically

I/O module does not inform CPU directly

I/O module does not interrupt CPU

Interrupt Driven I/O Basic Operation:

CPU issues read command

I/O module gets data from peripheral whilst CPU does other work

I/O module interrupts CPU

CPU requests data

I/O module transfers data

Multiple Interrupts:

Each interrupt line has a priority

Higher priority lines can interrupt lower priority lines

If bus mastering only current master can interrupt

Direct Memory Access (DMA)

Interrupt driven and programmed I/O require active CPU intervention

.Transfer rate is limited (processor to test and service the device)

.CPU is tied up for managing I/O transfer.

.Additional Module (hardware) on the bus

.DMA controller takes over from the CPU for I/ODMA is the answer.

.DMA module must use the bus only when the processor does not need it,

It must force the processor to suspend operation temporarily. This technique is called cycle stealing

Q10) Explain the necessity of an interface in memory organization?

A. Memory Interfacing When we are executing any instruction, the address of memory location or an I/O device is sent out by the microprocessor. The corresponding memory chip or I/O device is selected by a decoding circuit.

Memory requires some signals to read from and write to registers and microprocessors transmit some signals for reading or writing data.

The interfacing process includes matching the memory requirements with the microprocessor signals.Therefore, the interfacing circuit should be designed in such a way that it matches the memory signal requirements with the microprocessor's signals.

As we know, keyboards and displays are used as a communication channel with the outside world. Therefore, it is necessary that we interface the keyboard and display with the microprocessor. This is called I/O interfacing. For this type of interfacing, we use latches and buffers for interfacing the keyboards and displays with the microprocessor. But the main drawback of this interfacing is that the microprocessor can perform only one function.

When we are executing any instruction, we need the microprocessor to access the memory for reading instruction codes and the data stored in the memory. For this, both the memory and the microprocessor requires some signals to read from and write to registers.

PART-B

Q1) What is nonvolatile solid-state memory,and how does it differ from volatile memory?Provide Examples of nonvolatile solid-state memory technologies.

A. **Nonvolatile Solid-State Memory**

Nonvolatile solid-state memory is a type of memory that retains data even when the power supply is turned off. This contrasts with volatile memory, which requires power to maintain stored information.

Differences Between Nonvolatile and Volatile Memory

Nonvolatile Memory

- **Data Retention**: Retains data without a power supply.
- **Usage**: Ideal for long-term storage of data.
- **Speed**: Typically slower than volatile memory for read/write operations, but advancements are closing this gap.
- **Examples**: SSDs (Solid-State Drives), USB flash drives, and certain types of RAM like EEPROM (Electrically Erasable Programmable Read-Only Memory).

Volatile Memory

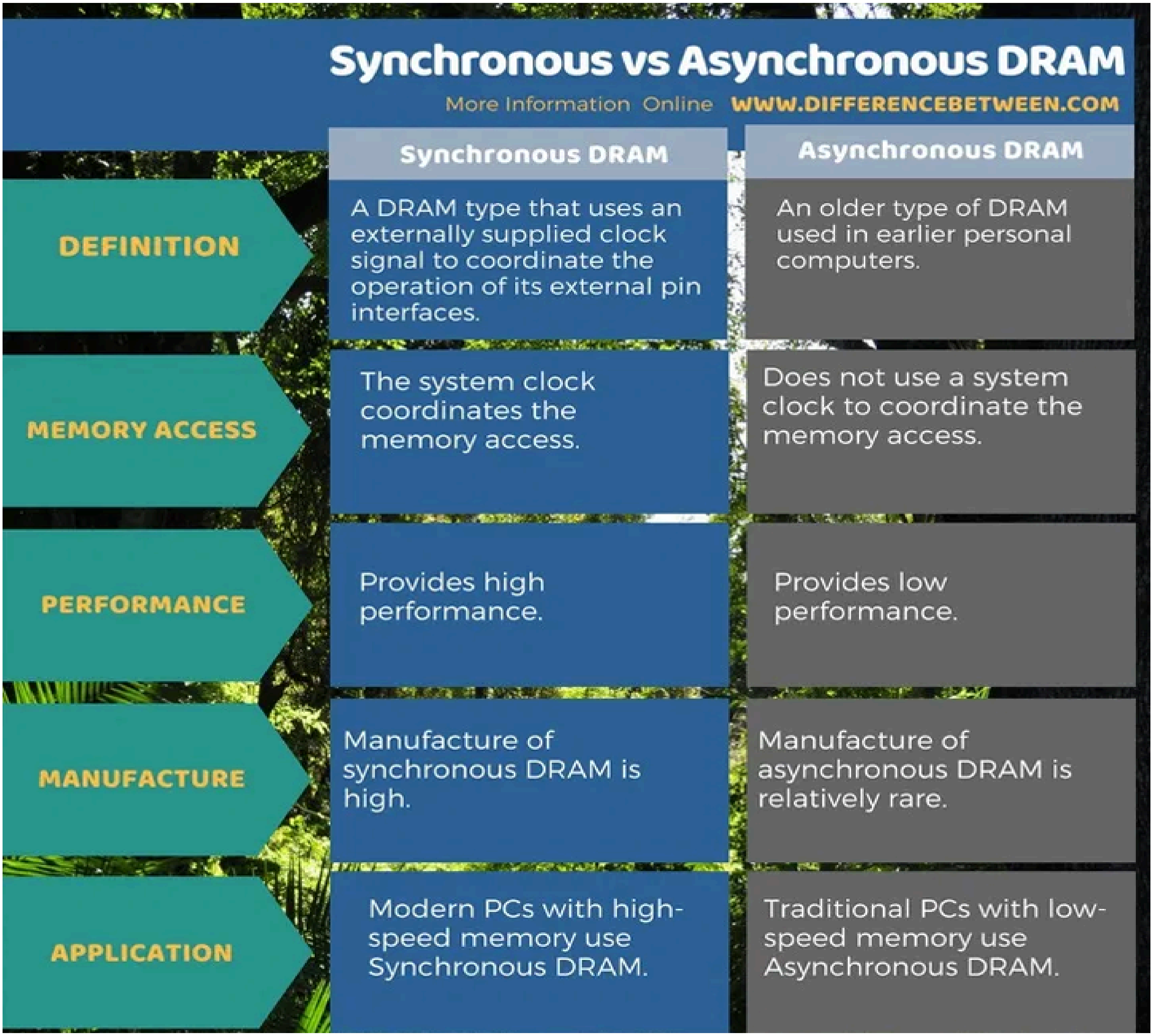
- **Data Retention**: Loses data when power is lost.
- **Usage**: Used for temporary storage to speed up processing tasks.
- **Speed**: Faster read/write operations compared to nonvolatile memory.
- **Examples**: DRAM (Dynamic Random-Access Memory) and SRAM (Static Random-Access Memory).

Examples of Nonvolatile Solid-State Memory Technologies

1. **NAND Flash Memory**
   - **Description**: Widely used in SSDs, USB flash drives, and memory cards.
   - **Features**: High-density storage, faster than traditional magnetic storage, and reliable for long-term data retention.
2. **NOR Flash Memory**
   - **Description**: Used in applications requiring fast read operations, like firmware and boot loaders.
   - **Features**: Faster read access compared to NAND but lower density and higher cost per bit.

Q2) Compare between asynchronous DRAM and synchronous RAM.

A. Synchronous DRAM uses a system clock to coordinate memory accessing while Asynchronous DRAM does not use a system clock to synchronize or coordinate memory accessing. Synchronous DRAM is faster and more efficient than asynchronous DRAM. Furthermore, synchronous DRAM provides high performance and better control than the asynchronous DRAM. Modern high-speed PCs use synchronous DRAM while older low-speed PCs used asynchronous DRAM.



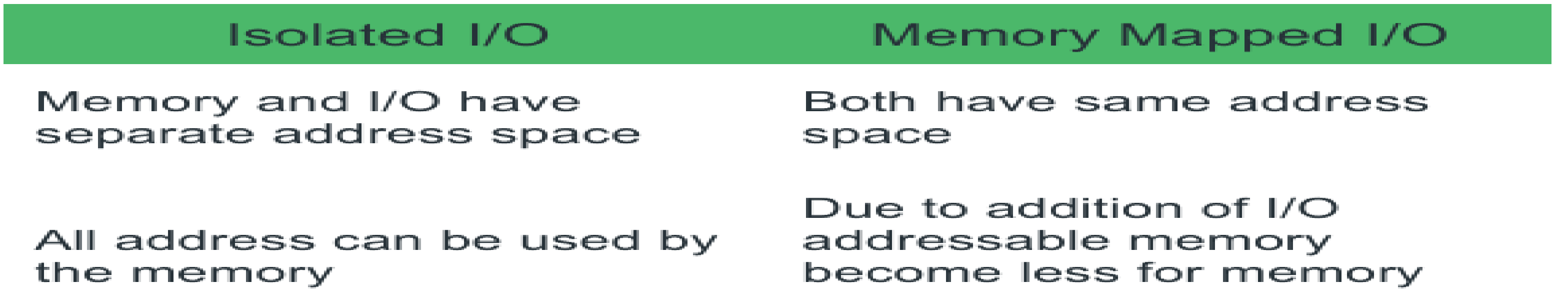
Synchronous vs Asynchronous DRAM

More Information Online WWW.DIFFERENCEBETWEEN.COM

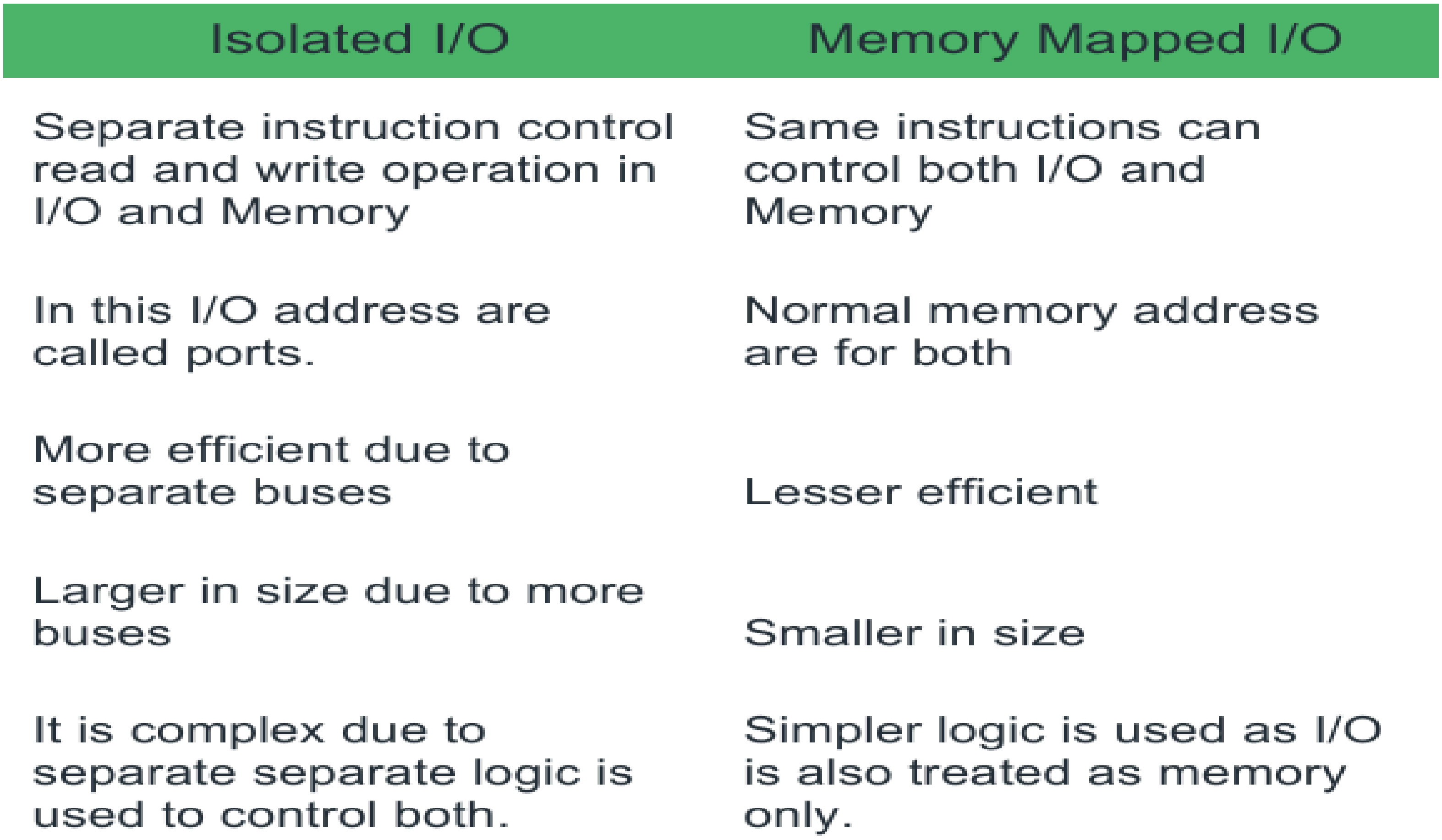
	Synchronous DRAM	Asynchronous DRAM
DEFINITION	A DRAM type that uses an externally supplied clock signal to coordinate the operation of its external pin interfaces.	An older type of DRAM used in earlier personal computers.
MEMORY ACCESS	The system clock coordinates the memory access.	Does not use a system clock to coordinate the memory access.
PERFORMANCE	Provides high performance.	Provides low performance.
MANUFACTURE	Manufacture of synchronous DRAM is high.	Manufacture of asynchronous DRAM is relatively rare.
APPLICATION	Modern PCs with high-speed memory use Synchronous DRAM.	Traditional PCs with low-speed memory use Asynchronous DRAM.

Q3) Compare isolated I/O and memory mapped I/O?

A.



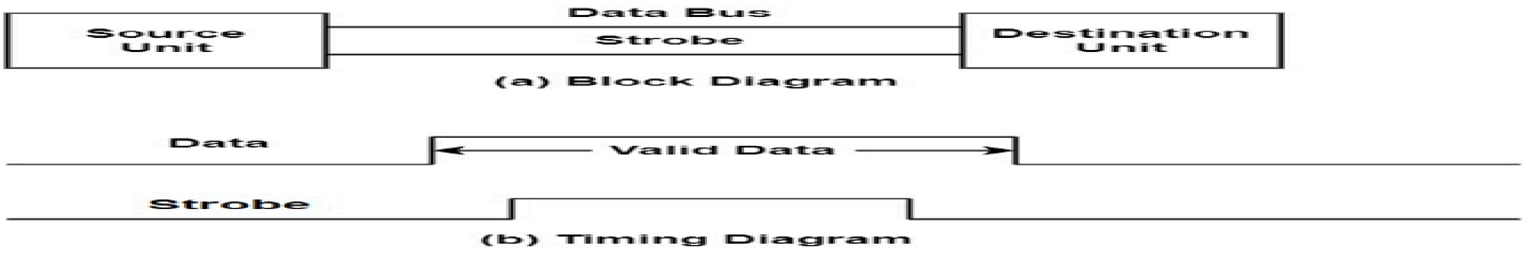
Isolated I/O	Memory Mapped I/O
Memory and I/O have separate address space	Both have same address space
All address can be used by the memory	Due to addition of I/O addressable memory become less for memory



Isolated I/O	Memory Mapped I/O
Separate instruction control read and write operation in I/O and Memory	Same instructions can control both I/O and Memory
In this I/O address are called ports.	Normal memory address are for both
More efficient due to separate buses	Lesser efficient
Larger in size due to more buses	Smaller in size
It is complex due to separate separate logic is used to control both.	Simpler logic is used as I/O is also treated as memory only.

Q4) Illustrate Strobe Control method of Asynchronous data transfer technique?

A. The strobe control technique of asynchronous data transfer operates a single control line to time each transfer. The strobe can be activated by either the source or the destination unit. The diagram shows a source-initiated transfer.

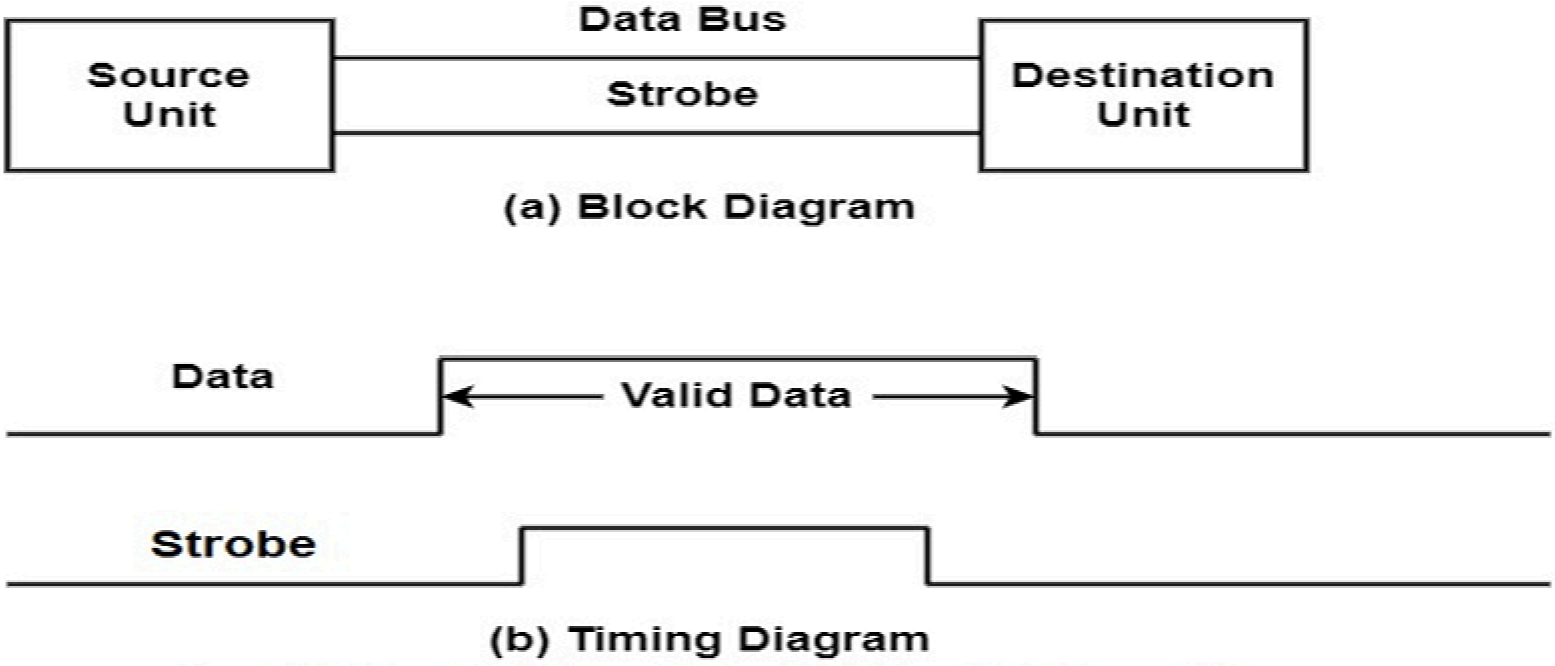


(a) Block Diagram

(b) Timing Diagram

Source-Initiated strobe for data transfer

The data bus gives the binary data from the source unit to the destination unit. Generally, the bus has multiple lines to transfer a unified byte or word. The strobe is a single line that instructs the destination unit when an accurate data word is accessible in the bus. The destination unit helps the lowering edge of the strobe pulse to send the contents of the data bus into one of its internal registers. The source deletes the data from the bus for a short period after it disables its strobe pulse. The source does not have to modify the data in the data bus. The case that the strobe signal is disabled signifies that the data bus does not include correct data. New correct data will be available only after the strobe is allowed again.



(a) Block Diagram

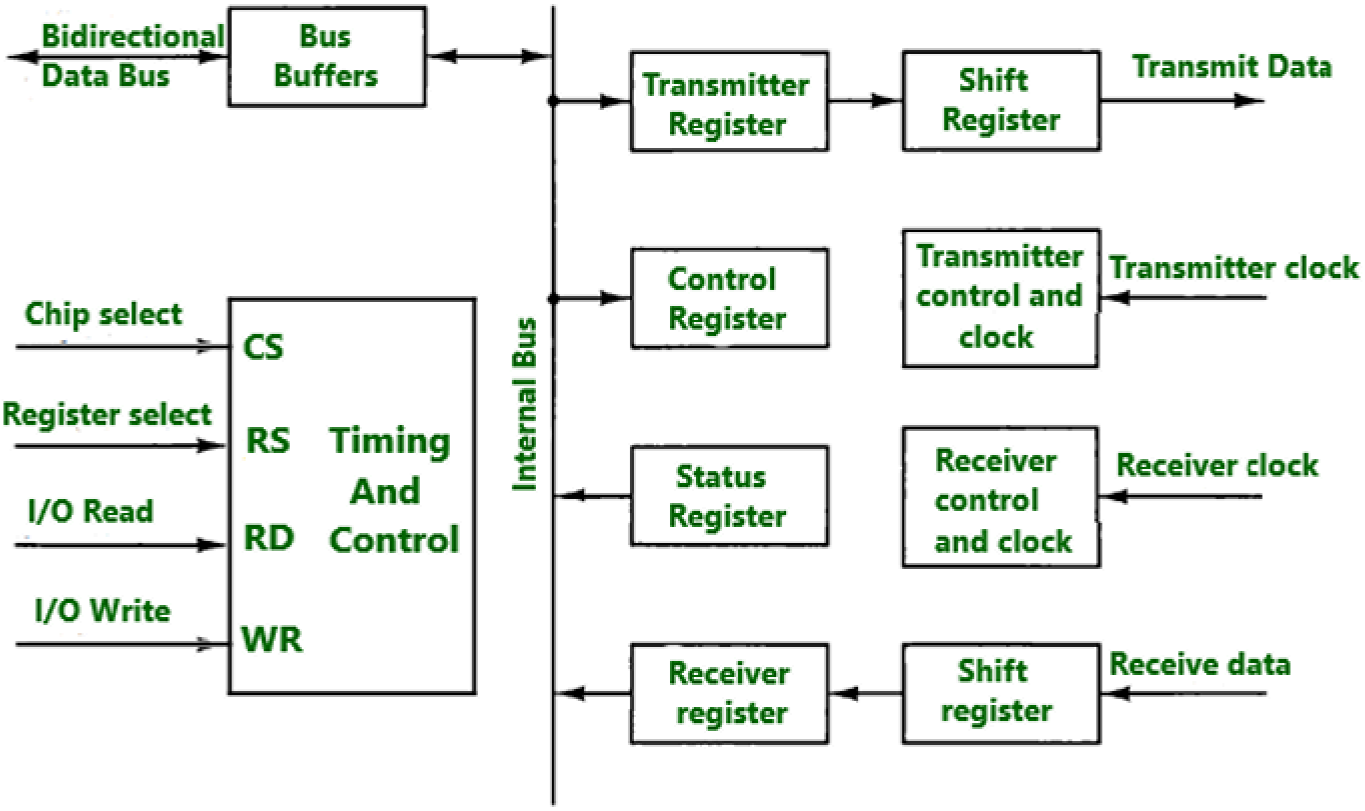
(b) Timing Diagram

Destinated-Initiated Strobe for data transfer

The falling edge of the strobe pulse can be used to produce a destination register. The destination unit then disables the strobe. The source eliminates the data from the bus after a fixed time interval. In several computers, the strobe pulse is guarded by the clock pulses in the CPU. Correspondingly, the strobe can be a memory-read control signal from the CPU to a memory unit. The destination, the CPU, starts the read operation to update the memory, which is the source, to locate a selected word into the data bus. The transfer of data between the CPU and an interface unit is the same as the strobe transfer. Data transfer between an interface and an I/O device is generally reserved by a set of handshaking lines.

Q5) Explain asynchronous communication interface with diagram?

A. It works as both a sender and a receiver. The interface is booted up for a specific mode of transfer using a control byte that is loaded into its control register. The transmitter register receives a data byte from the CPU by the data bus. This byte is sent to a shift register for serial transmission.



The receiver portion receives serial information into another shift register, and when a finalized data byte is acquired, it is moved to the receiver register. The CPU can choose the receiver register to read the byte through the data bus. The bits in the status register are utilized for input and output flags and for recording specific errors that can appear during the transmission. The CPU can read the status register to determine the status of the flag bits and to decide if any errors have appeared. The chip chooses and the read and write control lines connect with the CPU. The chip select (CS) input can select the interface by the address bus. The register select (RS) is related to the read (RD) and write (WR) controls. Two registers are write-only and two are read-only. The register selected is a service of the RS value and the RD and WR status, as recorded in the table following the diagram.

Q6) Explain How Virtual Memory uses paging to manage memory.Discuss The Benefits and potential drawbacks of this approach regarding system performance.

A. **Virtual Memory and Paging**

Virtual memory is a technique that allows a computer to use more memory than physically available by extending physical RAM onto a storage device like an SSD or HDD. Paging is one method used to implement virtual memory.

How Paging Works

1. **Division into Pages and Page Frames**:
    - **Virtual Memory**: The virtual address space of a process is divided into fixed-size blocks called **pages**.
    - **Physical Memory**: The physical memory (RAM) is divided into fixed-size blocks called **page frames**.
2. **Page Tables**:

    - A page table is maintained by the operating system, which keeps track of the mapping between virtual pages and physical page frames.
    - Each entry in the page table contains a frame number and status bits, such as whether the page is present in memory, read/write permissions, etc.

Address Translation:

- When a process accesses a virtual address, the virtual address is divided into a **page number** and an **offset.**
- The page number is used to look up the corresponding page frame in the page table.
- The offset is added to the starting address of the page frame to get the physical address.

Page Faults:

- If a page is not in physical memory, a **page fault** occurs.
- The operating system then loads the required page from the secondary storage (e.g., SSD) into a free page frame in physical memory.
- If no free page frames are available, the OS may use a page replacement algorithm to select a page to swap out to the disk.

Benefits of Paging

1. **Efficient Memory Utilization**:
    - Paging allows processes to use memory more flexibly and efficiently by only loading the necessary pages into physical memory.

  - It enables the system to run larger applications than the physical memory would otherwise allow.

2. **Isolation and Protection**:
   - Each process has its own virtual address space, which provides isolation and protection from other processes.
   - This prevents one process from accessing the memory space of another process, enhancing system security and stability.
3. **Simplified Memory Management**:
   - Paging eliminates the need for contiguous memory allocation, reducing fragmentation.
   - It simplifies memory allocation and deallocation, making it easier for the OS to manage memory.

Q7) With a block diagram, explain the direct and set associative mapping between cache and main memory?

A. **Direct Mapping and Set Associative Mapping in Cache Memory**

Understanding how cache memory maps to main memory is essential for optimizing system performance. Here, I'll explain the concepts of direct mapping and set associative mapping, along with block diagrams to illustrate each method.

Direct Mapping

Direct Mapping is the simplest form of cache memory mapping. Each block of main memory maps to exactly one cache line. This is done using a modulo operation.

Main Memory (Blocks)   Cache (Lines)

```
+--------+                    +--------+
| Block 0|---+                 | Line 0 |
+--------+   |                +--------+
| Block 1|   |                | Line 1 |
+--------+   |                +--------+
| Block 2|   |                | Line 2 |
+--------+   |                +--------+
| Block 3|   |--Modulo Mapping-->+--------+
+--------+   |                | Line 3 |
| Block 4|   |                +--------+
+--------+   |                | Line 4 |
| Block 5|   |                +--------+
+--------+---+                 | Line 5 |
|  ...   |                  |  ...   |
+--------+                    +--------+
```

Q8) Explain the I/O bus and interface modules?

A. The data bus, address bus and control bus that arise out of the processor and are intended to communicate with I/O devices are called I/O bus. The I/O bus is connected to all peripheral interfaces. To communicate with a particular device, the processor places a device address on the address bus. Each interface attached to the I/O bus contains an address decoder that monitors the address lines. When the interface detects an address to be its own, it activates the path between the bus and the device that it controls. All other peripherals are disabled. At the same time, a function code is provided to the control bus which is called I/O command. The types of I/O commands that are given out by the processor are:

1. Control Commands: This is the function code that activates the corresponding peripherals and informs them about what to do.
2. Status Commands: A status command is used to test various status conditions in the interface and the peripheral devices like BUSY, ERROR, data available or not in the buffer etc .
3. Data Output Command: A data output command causes the interface to respond by transferring the data from the processor to the peripheral. The data is sent from the CPU to the buffer of the interface after this command is provided.
4. Data Input Command: This command is sent by the CPU if the data is to be read from the peripheral. After this command is issued, the data of the peripheral are extracted into the buffer of the interface and are read by the CPU.

Q9) With a neat diagram, explain in detail the input interface circuit?

A. **Input Interface Circuit**

An input interface circuit is crucial for connecting input devices (e.g., sensors, keyboards, switches) to a microcontroller or microprocessor. It ensures that the signals from these devices are correctly interpreted and processed by the digital system.

Components of an Input Interface Circuit

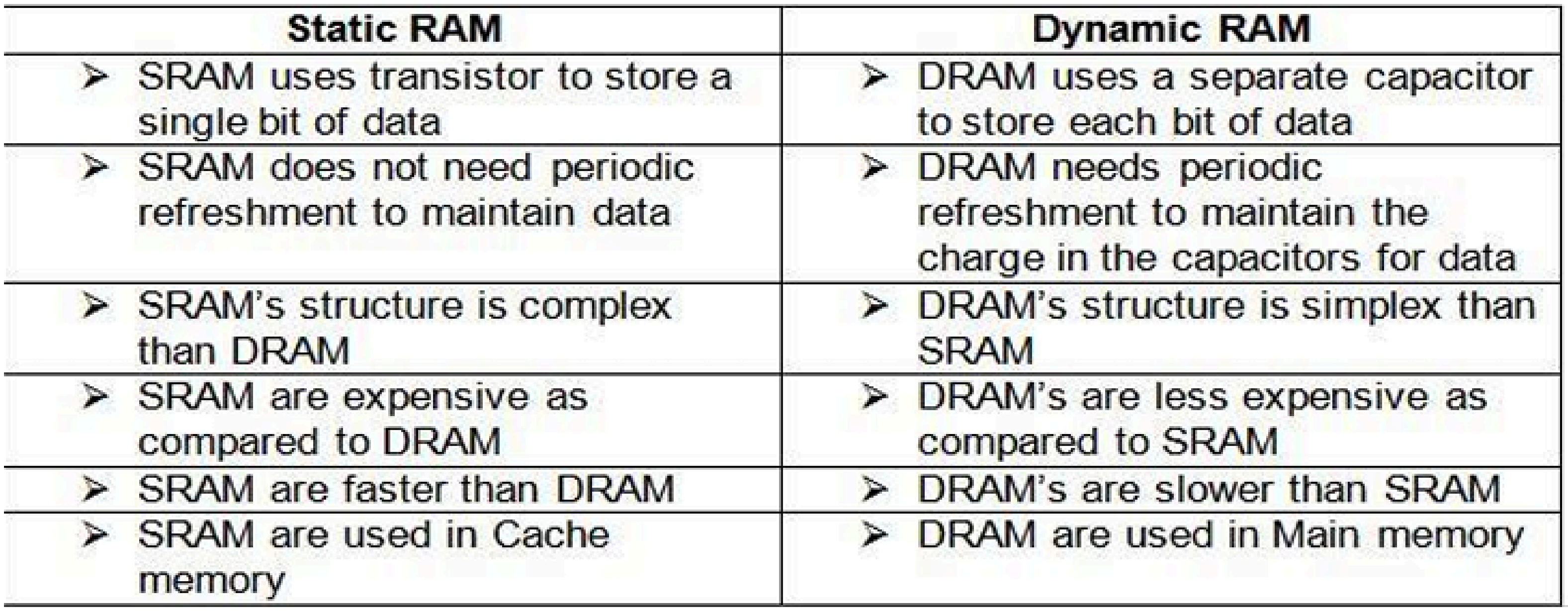
1. **Input Device**: The actual device generating the input signal (e.g., sensor, switch).

2. **Debouncing Circuit**: Removes noise and glitches from mechanical switches to ensure a clean digital signal.
3. **Signal Conditioning**: Amplifies or filters the signal to make it suitable for processing.
4. **Analog-to-Digital Converter (ADC)**: Converts analog signals from sensors into digital signals if needed.
5. **Buffer/Driver**: Isolates the input device from the microcontroller to protect against high currents or voltages.
6. **Pull-Up/Pull-Down Resistors**: Ensures a defined logic level (HIGH or LOW) when no input is present.

```
          +------------------+
     |  Input Device    |
     +--------+---------+
              |
              | (Analog or Digital Signal)
              |
      +------+------+
      |  Debouncing | (Optional, for switches)
      +------+------+
              |
     +-------+-------+
     | Signal        |
     | Conditioning   |
     +-------+-------+
              |
              | (Analog Signal, if from sensor)
              |
    +---------+---------+
    |     ADC           |
    | (Analog-to-Digital |
    |   Converter)      |
    +---------+---------+
              | (Digital Signal)
              |
              |
    +---------+---------+
    |      Buffer/      |
    |      Driver       |
    +---------+---------+
              | (Digital Signal)
              |
     +--------+--------+
     | Microcontroller |
     +-----------------+
```

Q10) Classify the differences between static and dynamic memories?

A.



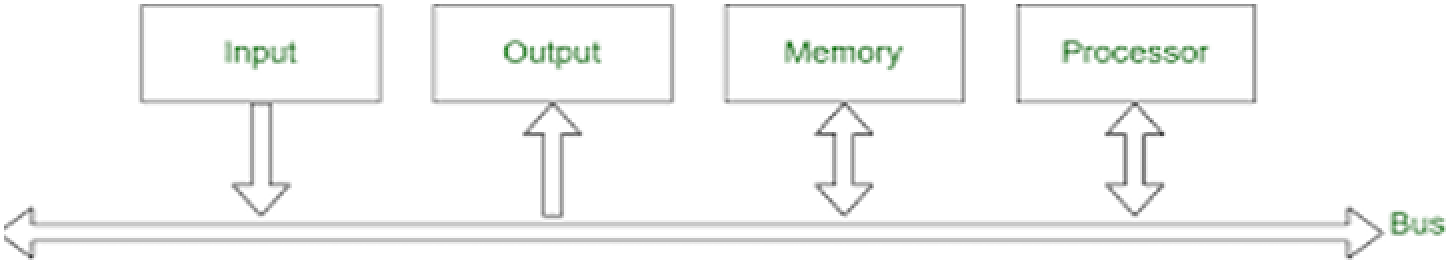
Static RAM	Dynamic RAM
➢ SRAM uses transistor to store a single bit of data	➢ DRAM uses a separate capacitor to store each bit of data
➢ SRAM does not need periodic refreshment to maintain data	➢ DRAM needs periodic refreshment to maintain the charge in the capacitors for data
➢ SRAM's structure is complex than DRAM	➢ DRAM's structure is simplex than SRAM
➢ SRAM are expensive as compared to DRAM	➢ DRAM's are less expensive as compared to SRAM
➢ SRAM are faster than DRAM	➢ DRAM's are slower than SRAM
➢ SRAM are used in Cache memory	➢ DRAM are used in Main memory

Q11) Explain the multilevel hierarchy of storage devices?

A. Described is a system and method for a multi-level memory hierarchy. Each level is based on different attributes including, for example, power, capacity, bandwidth, reliability, and volatility. In some embodiments, the different levels of the memory hierarchy may use an on-chip stacked dynamic random access memory, (providing fast, high-bandwidth, low energy access to data) and an off-chip non-volatile random access memory, (providing low power, high-capacity storage), in order to provide higher-capacity, lower power, and higher-bandwidth performance. The multi-level memory may present a unified interface to a processor so that specific memory hardware and software implementation details are hidden. The multi-level memory enables the illusion of a single-level memory that satisfies multiple conflicting constraints. A comparator receives a memory address from the processor, processes the address and reads from or writes to the appropriate memory level. In some embodiments, the memory architecture is visible to the software stack to optimize memory utilization.

Q12) Illustrate the arrangement of a single bus structure and brief about memory mapped I/O?

A. Single Bus Structure : In single bus structure, one common bus used to communicate between peripherals and microprocessor. It has disadvantages due to the use of one common bus. In the single bus structure all the units are connected in the similar type of bus rather than connecting different buses as multiple bus structures.



Single Bus Structure

Memory-mapped I/O uses the same address space to address both memory and I/O devices. The memory and registers of the I/O devices are mapped to (associated with) address values. So a memory address may refer to either a portion of physical RAM, or instead to memory and registers of the I/O device. Thus, the CPU instructions used to access the memory can also be used for accessing devices. Each I/O device monitors the CPU's address bus and responds to any CPU access of an address assigned to that device, connecting the data bus to the desired device's hardware register. To accommodate the I/O devices, areas of the addresses used by the CPU must be reserved for I/O and must not be available for normal physical memory. The reservation may be permanent, or temporary (as achieved via bank switching).

Q13) Compare synchronous and asynchronous communication?
A. Synchronous communication happens when messages can only be exchanged in real time. It requires that the transmitter and receiver are present in the same time and/or space. Examples of synchronous communication are phone calls or video meetings.

Asynchronous communication happens when information can be exchanged independent of time. It doesn’t require the recipient’s immediate attention, allowing them to respond to the message at their convenience. Examples of asynchronous communication are emails, online forums, and collaborative documents.

SYNCHRONOUS

VERSUS

ASYNCHRONOUS

COMMUNICATION

Synchronous	Asynchronous
Communicated in real-time	Is well-timed
Creates interruptions in a workday	Eliminates interruptions
Online chat sessions, Live Customer Support, Video Conferencing	Emails, Pre-recorded Videos, Social Media Posts, Blogs
The other party is actively waiting for replies	Neither expecting nor waiting for an incoming message
Too much of real time communication leads to burnout and depletes individual efficiency	Saves from unnecessary distractions & Gives time to streamline activities on personal end
Use it for discussions like code issues and routine bottlenecks in task progress	Use it when you do not need immediate response- to report a bug, resolve customer query or pitch a digital product to a client, etc.
Quick response impacts the quality of conversations & meetings, making them longer and distractive	Gives time to respond- leading to definite messages and shaping up the quality of conversations & meetings

StoryXpress

Q14)Explain about interrupt masks provided in any processor?
A. An interrupt is an event caused by a component other than the CPU. It indicates the CPU of an external event that requires immediate attention. Interrupts occur asynchronously. Maskable and non-maskable interrupts are two types of interrupts. Maskable Interrupt :
An Interrupt that can be disabled or ignored by the instructions of CPU are called as Maskable Interrupt.The interrupts are either edge-triggered or level-triggered or level-triggered.

Why are interrupt masks provided in any processor?
Interrupt masks enable the higher priority devices to come first and therefore lower priority devices come last. The interrupt enable bits as a bit vector is known as interrupt mask. Which enables / disables the devices according to the correct configuration of the mask

Q15) Explain the operation of memory hierarchy?
A. In Computer System Design, Memory Hierarchy is an enhancement to organize the memory such that it can minimize the access time. The Memory Hierarchy was developed based on a program behavior known as locality of references.The figure below clearly demonstrates the different levels of memory hierarchy:

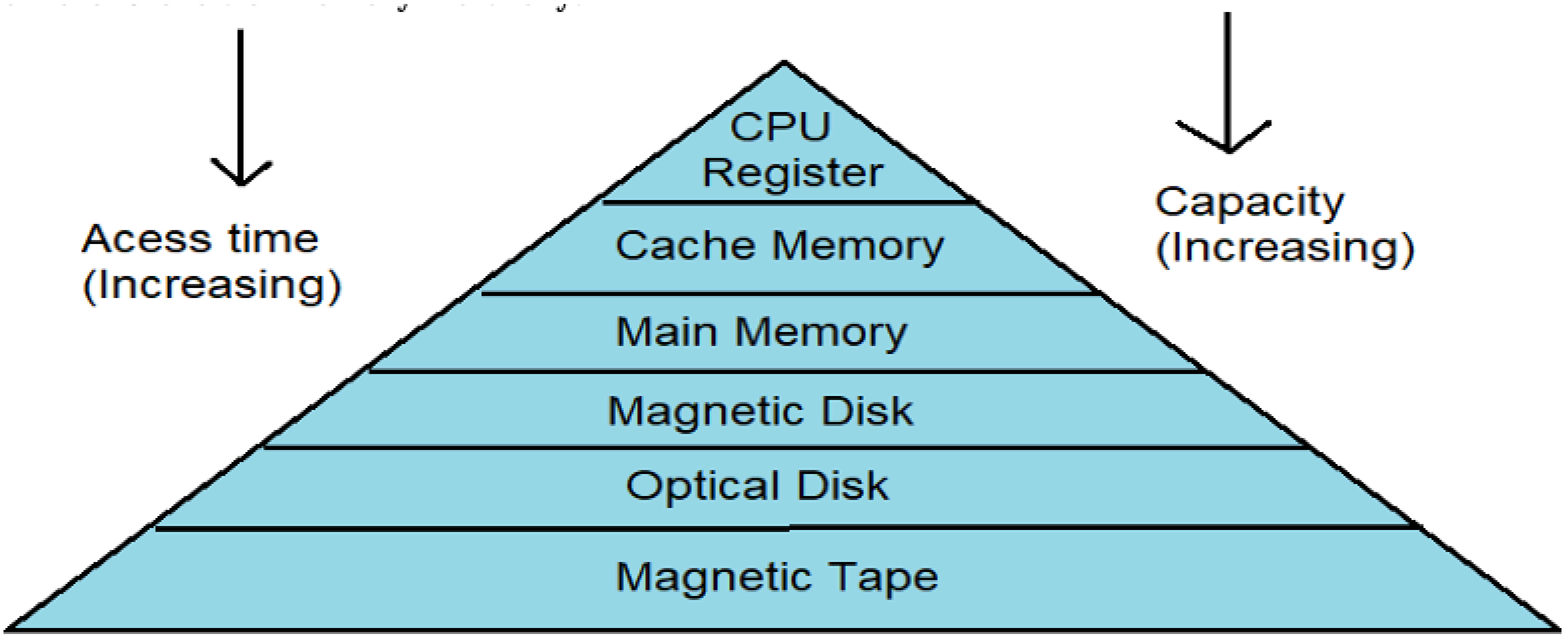


Fig:- Memory Hierarchy

This Memory Hierarchy Design is divided into 2 main types:

1. External Memory or Secondary Memory Comprising Magnetic Disk, Optical Disk, Magnetic Tape i.e. peripheral storage devices which are accessible by the processor via I/O Module.

2. Internal Memory or Primary Memory Comprising of Main Memory, Cache Memory & CPU registers. This is directly accessible by the processor.

We can infer the following characteristics of Memory Hierarchy Design from above figure:

1. Capacity: It is the global volume of information the memory can store. As we move from top to bottom in the Hierarchy, the capacity increases.

2. Access Time: It is the time interval between the read/write request and the availability of the data. As we move from top to bottom in the Hierarchy, the access time increases.

3. Performance: This enhancement was made in the form of Memory Hierarchy Design because of which the performance of the system increases. One of the most significant ways to

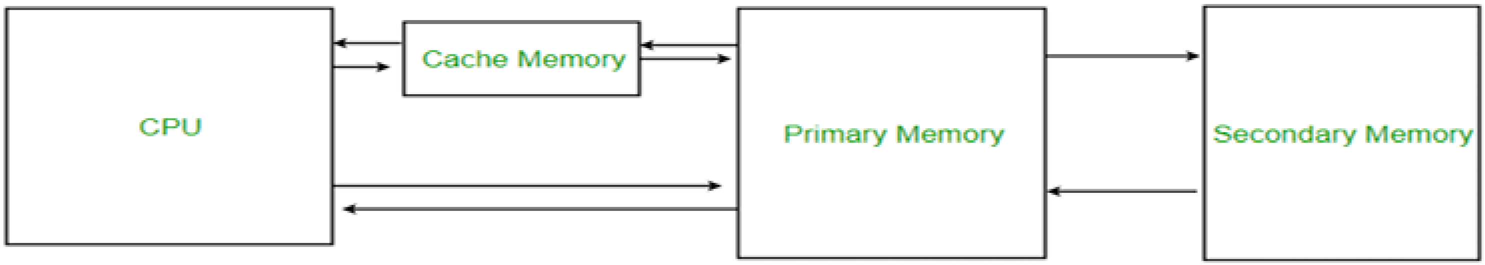
increase system performance is minimizing how far down the memory hierarchy one has to go to manipulate data.
4. Cost per bit: As we move from bottom to top in the Hierarchy, the cost per bit increases i.e. Internal Memory is costlier than External Memory

Q16)Explain any four non-volatile memory concepts with their functionality?
A. Non-volatile memory (NVM) Non-volatile memory is a very advanced storage technology. It does not use continuous power to keep the data or program files located on the computer so that it becomes an effective power saver.
Types of non-volatile memory Many other NVM types are widely used to read and write data to and from business and personal devices; each has its own advantages and disadvantages. NAND flash, the most common type used in data storage, includes several variants, such as single-level cells or one bit per multi-level cell or two bits per cell; three-level cells or three bits per cell and quad-level cells or four bits per cell, respectively.

Manufacturers kept updating NAND flash technology to reduce cost per bit. When they had difficulty in scaling two-dimensional NAND technology, which has a single layer of memory cells, they introduced 3D NAND flash memory. Technology vendors are also continuing to work on additional NVMe technologies to minimize costs, enhance efficiency, improve data storage capacity, and decrease energy usage

Q17)Model the different mapping functions in cache?

A. Cache Memory is a special very high-speed memory. It is used to speed up and synchronize with high-speed CPUs. Cache memory is costlier than main memory or disk memory but economical than CPU registers. Cache memory is an extremely fast memory type that acts as a buffer between RAM and the CPU. It holds frequently requested data and instructions so that they are immediately available to the CPU when needed. Cache memory is used to reduce the average time to access data from the Main memory. The cache is a smaller and faster memory which stores copies of the data from frequently used main memory locations. There are various different independent caches in a CPU, which store instructions and data.



Cache Performance: When the processor needs to read or write a location in main memory, it first checks for a corresponding entry in the cache. The performance of cache memory is frequently measured in terms of a quantity called Hit ratio.

Hit ratio = hit / (hit + miss) = no. of hits/total accesses

We can improve Cache performance using higher cache block size, higher associativity, reduce miss rate, reduce miss penalty, and reduce the time to hit in the cache.

Q18) Demonstrate any one feature of memory, show that leads to improved performance of computer?

A. Earlier when the computer system was designed without Memory Hierarchy design, the speed gap increased between the CPU registers and Main Memory due to large difference in access time. This results in lower performance of the system and thus, enhancement was required. This enhancement was made in the form of Memory Hierarchy Design because of which the performance of the system increases. One of the most significant ways to increase system performance is minimizing how far down the memory hierarchy one has to go to manipulate data. Memory Hierarchy is an enhancement to organize the memory such that it can minimize the access time. The Memory Hierarchy was developed based on a program behavior known as locality of references

Q19) Explain the working of 16- megabyte DRAM chip configured as 1M x 6 memory chips?

A. **Working of a 16-Megabyte DRAM Chip Configured as 1M x 6 Memory Chips**

A 16-megabyte (MB) DRAM chip can be organized in various configurations. When it is configured as 1M x 16, it means there are 1 million (1M) addresses, each capable of storing 16 bits. To understand this configuration, let's break it down into its components and the way it operates.

Basic Concepts

1. **DRAM** (Dynamic Random-Access Memory):
    - **Storage Cells**: DRAM stores each bit of data in a separate capacitor within an integrated circuit. These

capacitors need to be periodically refreshed to retain their charge.

- **Address Lines**: Used to select the specific memory location for read/write operations.
- **Data Lines**: Used to transfer data to and from the memory.

2. **Memory Organization (1M x 16)**:
   - **1M**: Indicates 1,048,576 (2^20) unique memory addresses.
   - **16**: Each address can hold 16 bits of data (2 bytes).

Block Diagram and Explanation

1. **Address Bus**:
   - **Address Lines (A0 - A19)**: 20 address lines are required to uniquely address 1,048,576 locations (2^20).
2. **Data Bus**:
   - **Data Lines (D0 - D15)**: 16 data lines are required to read/write 16 bits of data at each address.
3. **Control Signals**:
   - **Row Address Strobe (RAS)**: Selects the row in the memory matrix.
   - **Column Address Strobe (CAS)**: Selects the column in the memory matrix.
   - **Write Enable (WE)**: Indicates a write operation.
   - **Output Enable (OE)**: Indicates a read operation.

```
+------------------------+
|       DRAM           |
|                    |
       |  +---------+          |
       |  |         |         |
 Addr -->|->|   RAS   |---> Rows  |
       |  |         |         |
       |  +---------+          |
       |  +---------+          |
       |  |         |         |
       |  |   CAS   |---> Cols  |
       |  |         |         |
       |  +---------+          |
       |  +---------+          |
       |  |         |         |
  Data <->|->|   WE   |<---> Data |
       |  |         |         |
       |  +---------+          |
       +----------------------+
```

Q20) What is thrashing in the context of virtual memory? Discuss The Conditions That Thrashing suggests strategies to minimize its impact system performance.

A. **Thrashing in Virtual Memory**

Thrashing occurs when a computer's virtual memory system is overwhelmed by excessive paging and spends more time swapping pages in and out of memory than executing actual tasks. This leads to severe performance degradation.

Conditions That Cause Thrashing

1. **Insufficient Physical Memory**:

- When the system does not have enough physical memory (RAM) to hold the working set of the active processes, frequent page faults occur, causing thrashing.

2. **High Degree of Multiprogramming**:
    - Running too many processes simultaneously can lead to competition for memory, increasing the likelihood of thrashing.
3. **Large Working Sets**:
    - Processes with large working sets (the set of pages a process needs to execute efficiently) can cause more page faults if there isn't enough memory to accommodate all their pages.
4. **Poor Locality of Reference**:
    - If processes do not exhibit good locality of reference (accessing a small set of pages frequently), the system may spend more time swapping pages that are not needed immediately.