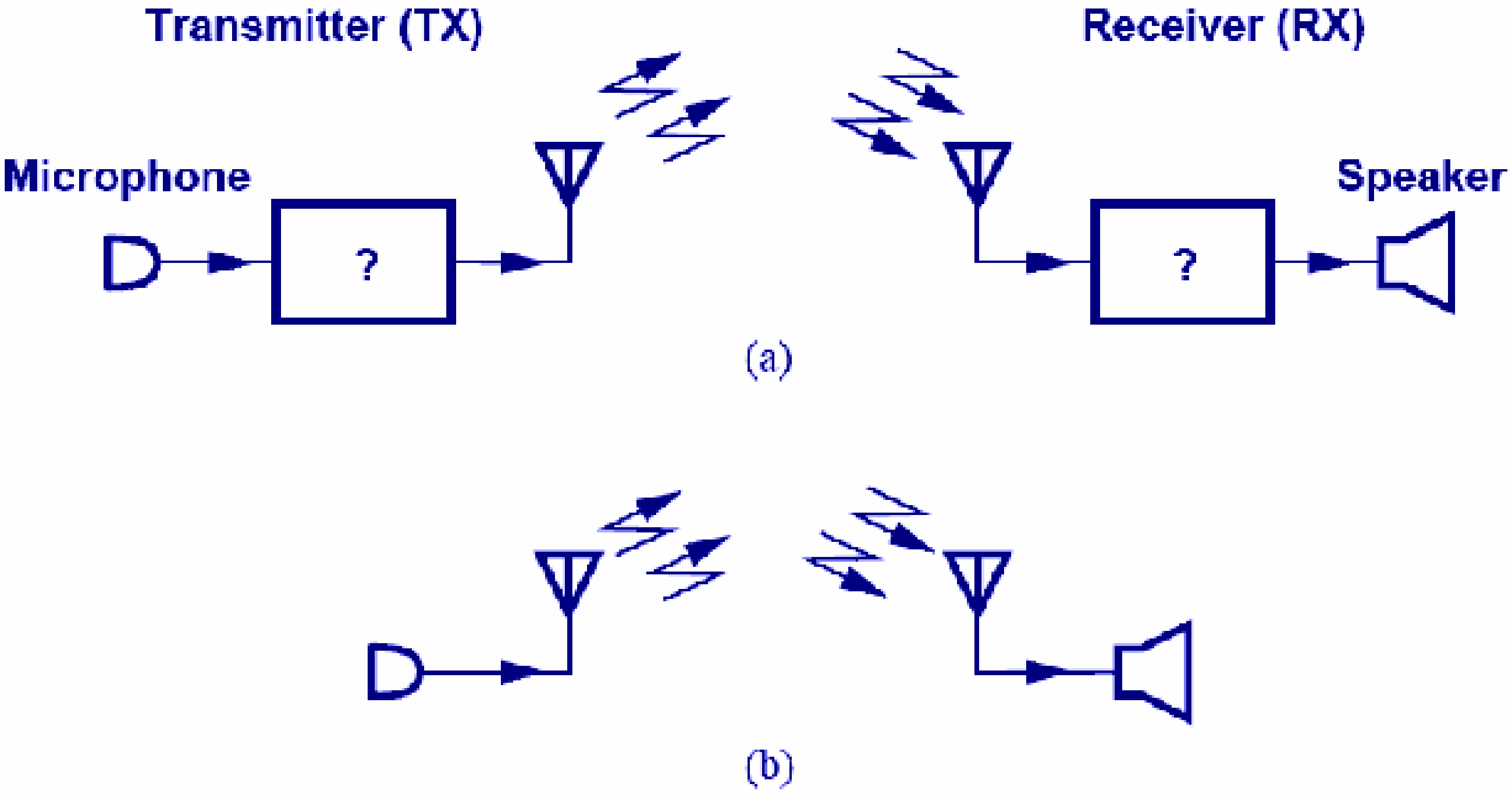
Fundamentals of Microelectronics

Chapter 1 Why Microelectronics?

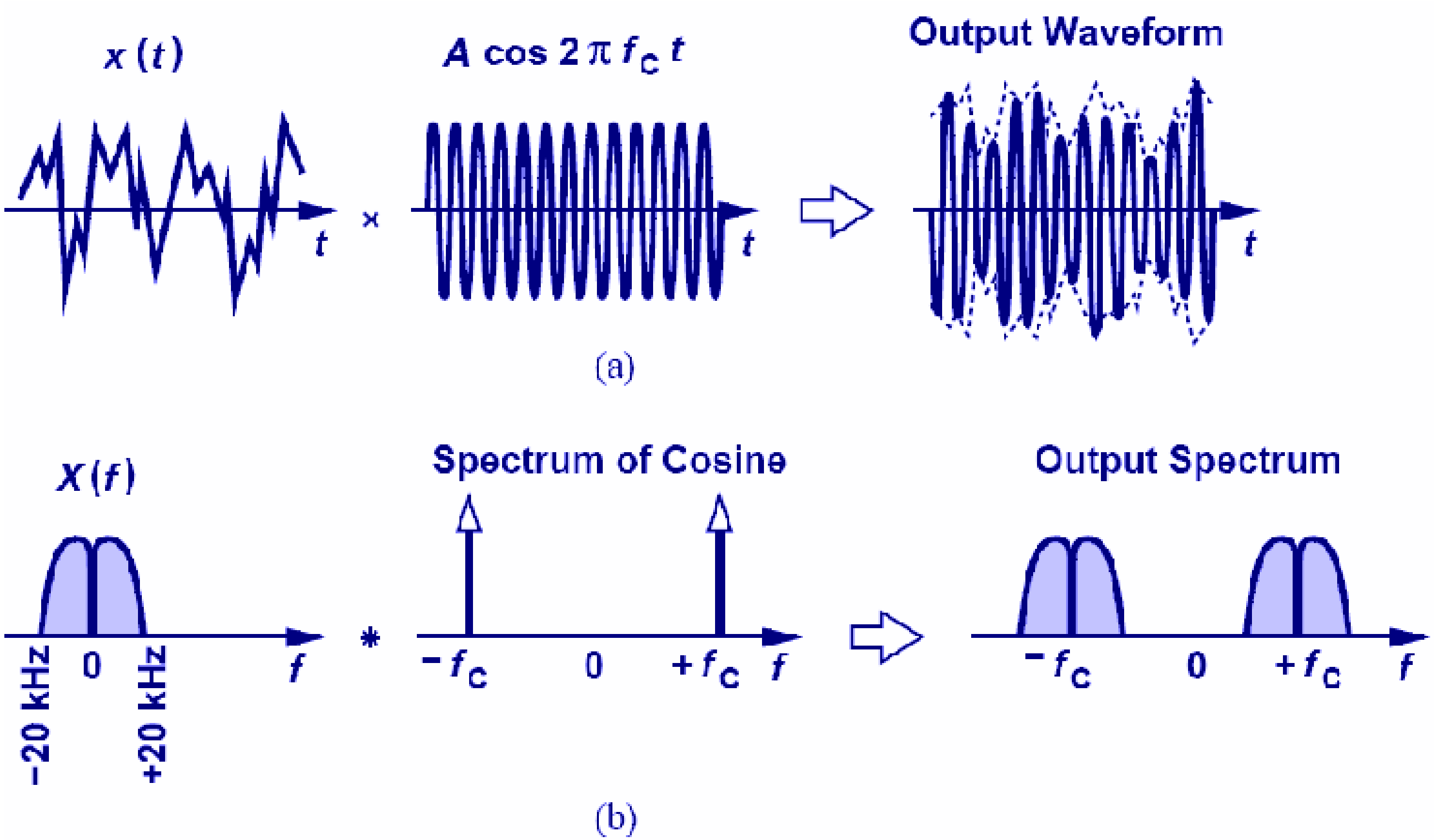
- 1.1 Electronics versus Microelectronics
- 1.2 Example of Electronic System: Cellular Telephone
- 1.3 Analog versus Digital

Cellular Technology



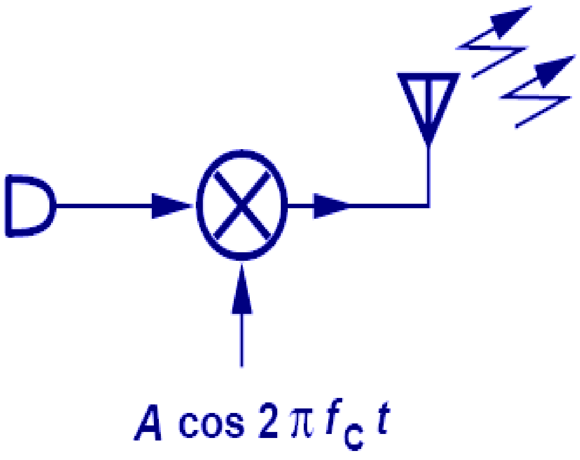
- **An important example of microelectronics.**
- **Microelectronics exist in black boxes that process the received and transmitted voice signals.**

Frequency Up-conversion



- **Voice is "up-converted" by multiplying two sinusoids.**
- **When multiplying two sinusoids in time domain, their spectra are convolved in frequency domain.**

Transmitter



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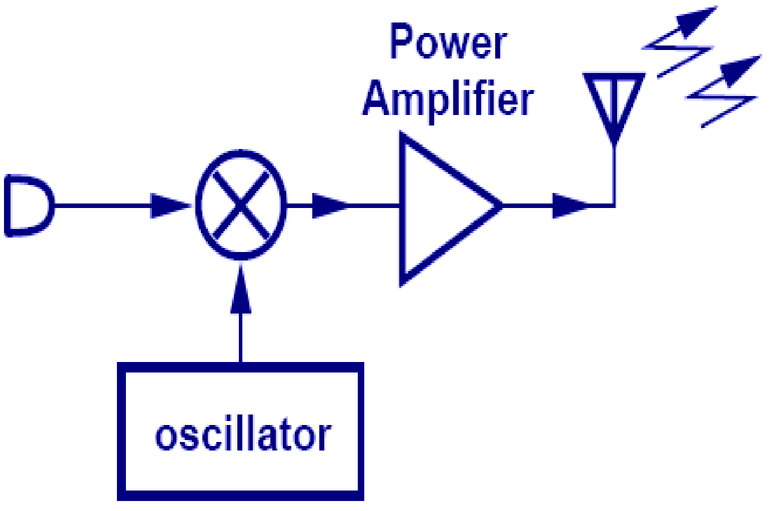
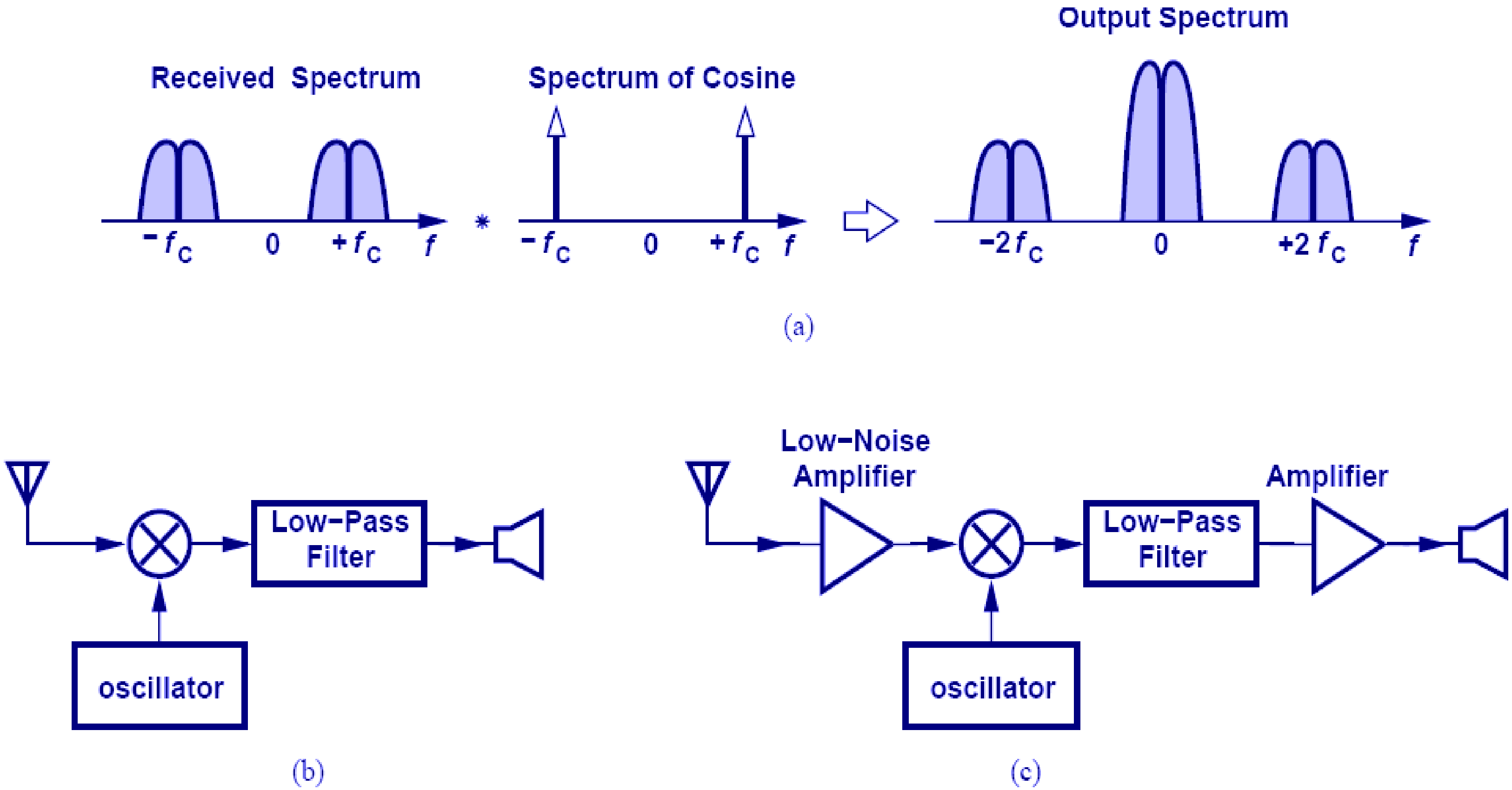


(b)

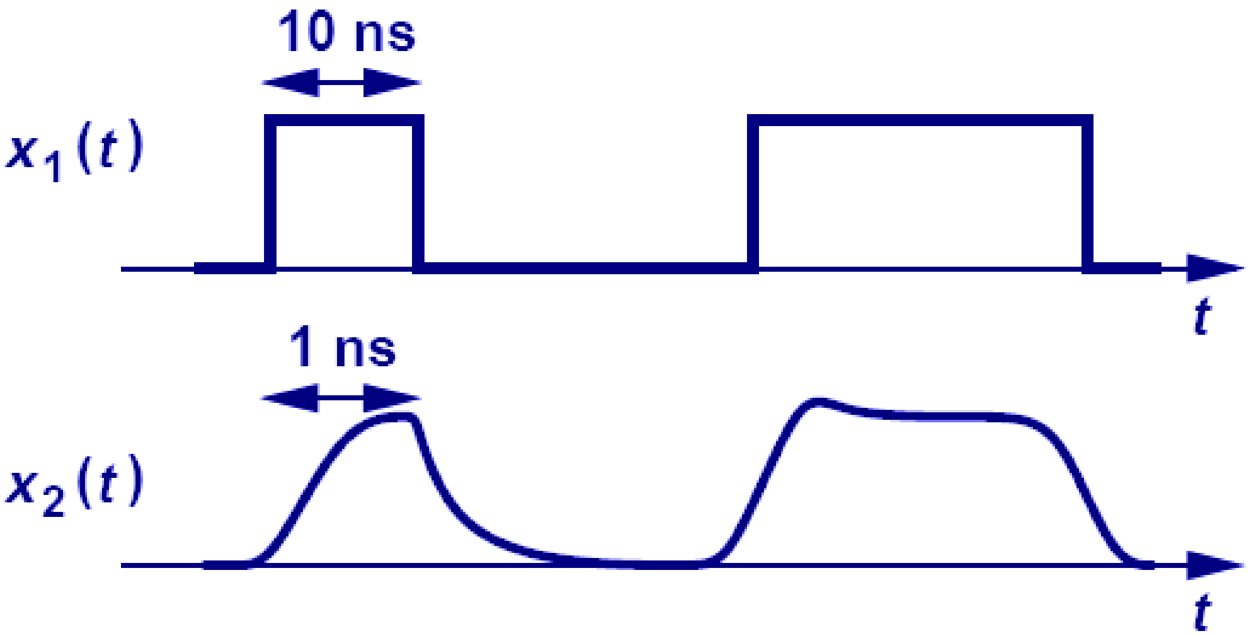
- Two frequencies are multiplied and radiated by an antenna in (a).
- A power amplifier is added in (b) to boost the signal.

Receiver



- **High frequency is translated to DC by multiplying by f_C.**
- **A low-noise amplifier is needed for signal boosting without excessive noise.**

Digital or Analog?



- $X_1(t)$ **is operating at 100Mb/s and** $X_2(t)$ **is operating at 1Gb/s.**
- **A digital signal operating at very high frequency is very "analog".**

Chapter 2 Basic Physics of Semiconductors

- 2.1 Semiconductor materials and their properties
- 2.2 PN-junction diodes
- 2.3 Reverse Breakdown

Semiconductor Physics

Semiconductors

- Charge Carriers
- Doping
- Transport of Carriers

PN Junction

- Structure
- Reverse and Forward Bias Conditions
- I/V Characteristics
- Circuit Models

- **Semiconductor devices serve as heart of microelectronics.**
- **PN junction is the most fundamental semiconductor device.**

Charge Carriers in Semiconductor

Charge Carriers in Solids		Modification of Carrier Densities		Transport of Carriers
• Crystal Structure	⇨	• Intrinsic Semiconductors	⇨	• Diffusion
• Bandgap Energy		• Extrinsic Semiconductors		• Drift
• Holes		• Doping		

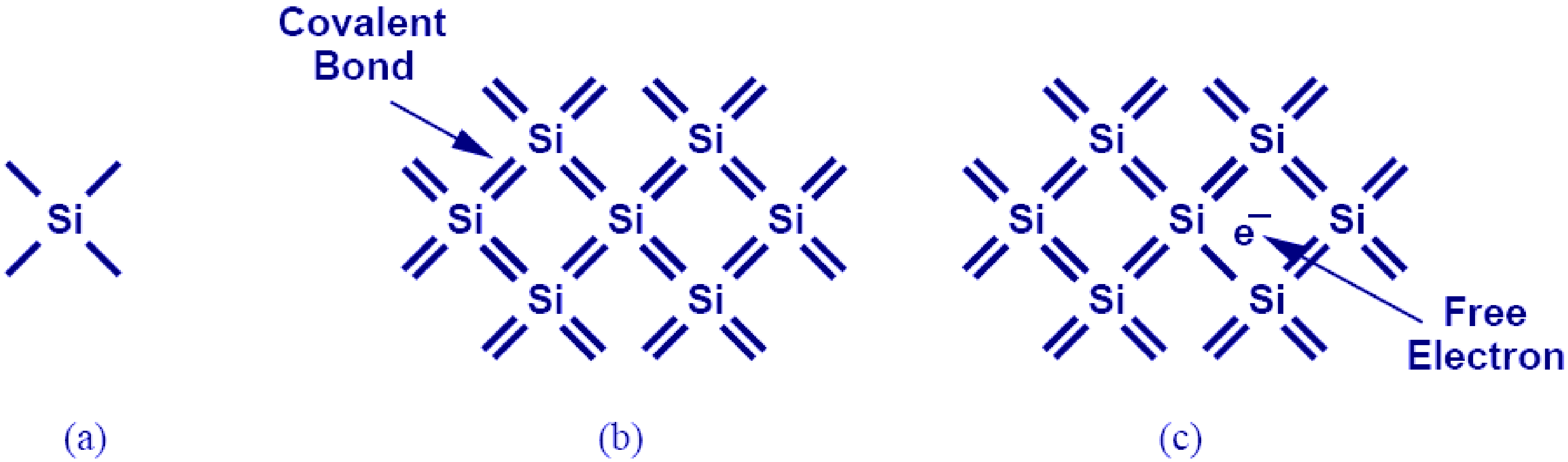
- **To understand PN junction's IV characteristics, it is important to understand charge carriers' behavior in solids, how to modify carrier densities, and different mechanisms of charge flow.**

Periodic Table

III	IV	V
Boron (B)	Carbon (C)	
Aluminum (Al)	Silicon (Si)	Phosphorous (P)
Galium (Al)	Germanium (Ge)	Arsenic (As)

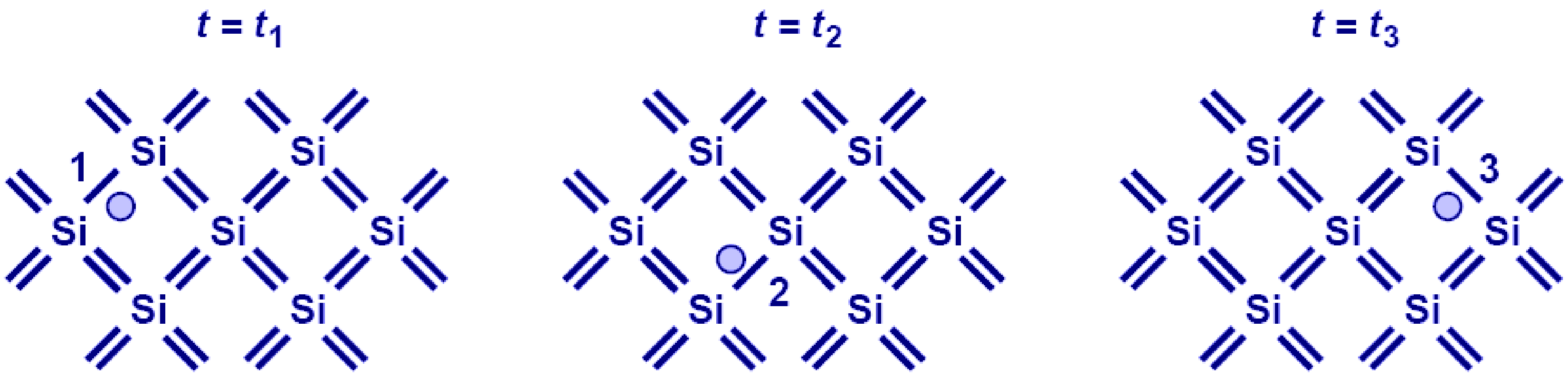
- **This abridged table contains elements with three to five valence electrons, with Si being the most important.**

Silicon



- Si has four valence electrons. Therefore, it can form covalent bonds with four of its neighbors.
- When temperature goes up, electrons in the covalent bond can become free.

Electron-Hole Pair Interaction



- With free electrons breaking off covalent bonds, holes are generated.
- Holes can be filled by absorbing other free electrons, so effectively there is a flow of charge carriers.

Free Electron Density at a Given Temperature

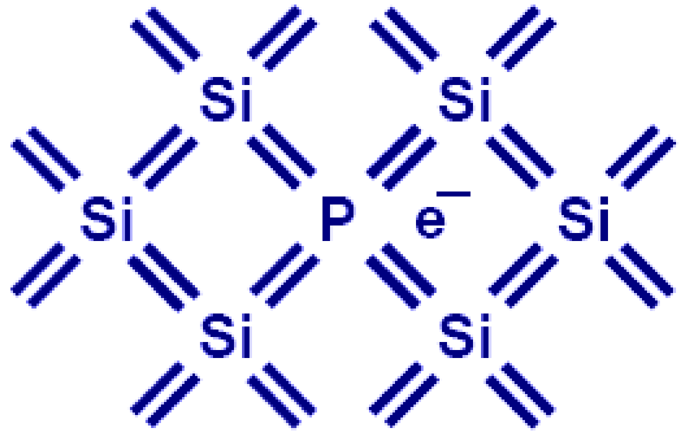
$$n_i = 5.2 \times 10^{15} T^{3/2} \exp \frac{-E_g}{2kT} \; electrons / cm^3$$

$$n_i(T = 300^0 K) = 1.08 \times 10^{10} \; electrons / cm^3$$

$$n_i(T = 600^0 K) = 1.54 \times 10^{15} \; electrons / cm^3$$

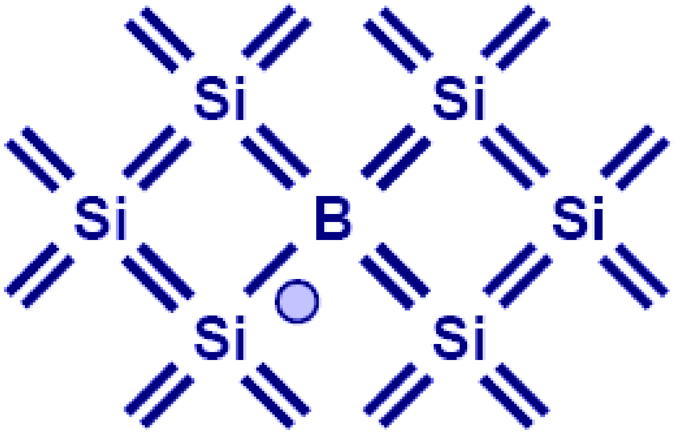
- ***E_g*, or bandgap energy determines how much effort is needed to break off an electron from its covalent bond.**
- **There exists an exponential relationship between the free-electron density and bandgap energy.**

Doping (N type)



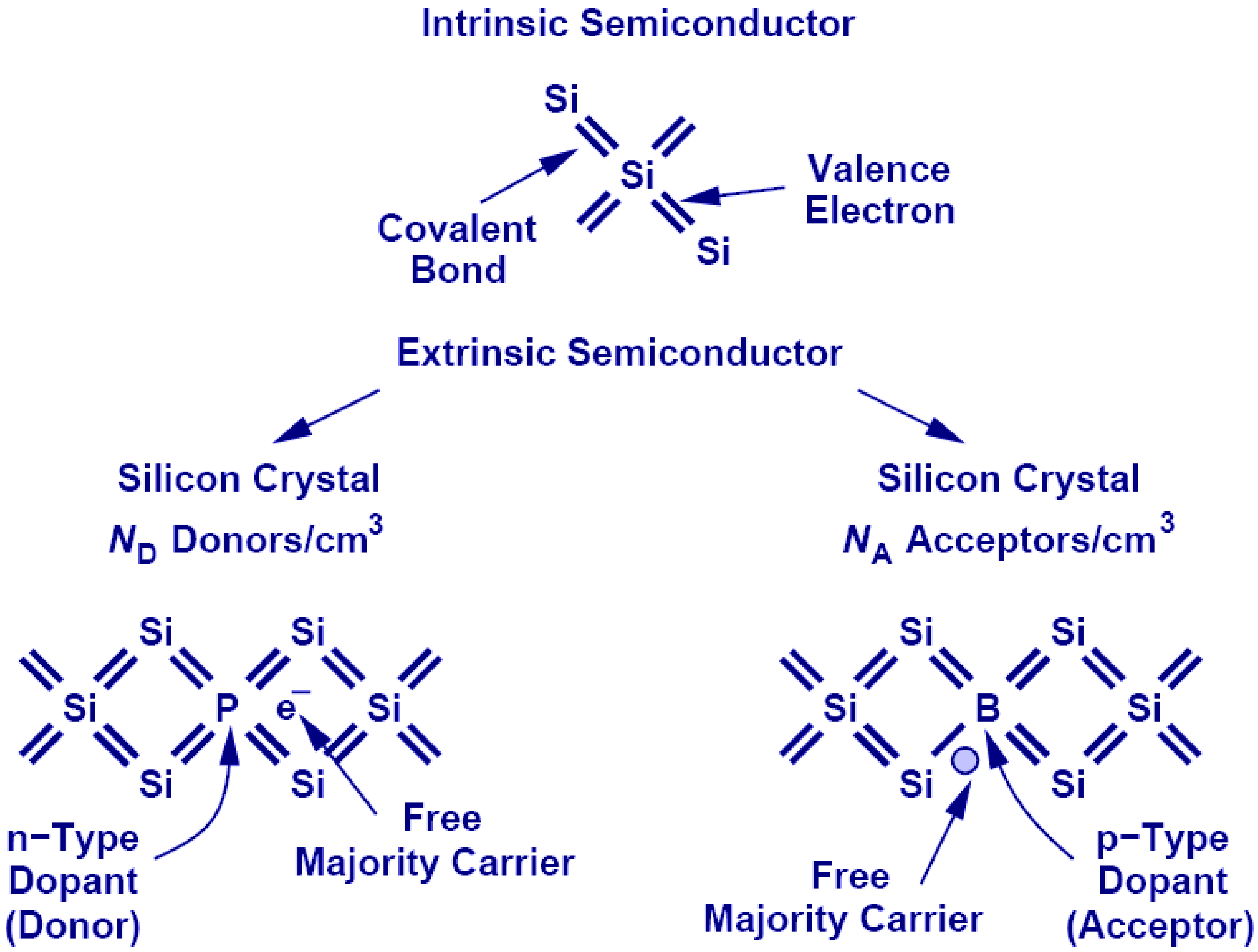
- Pure Si can be doped with other elements to change its electrical properties.
- For example, if Si is doped with P (phosphorous), then it has more electrons, or becomes type N (electron).

Doping (P type)



- **If Si is doped with B (boron), then it has more holes, or becomes type P.**

Summary of Charge Carriers



Electron and Hole Densities

$$np = n_i^2$$

Majority Carriers : $p \approx N_A$

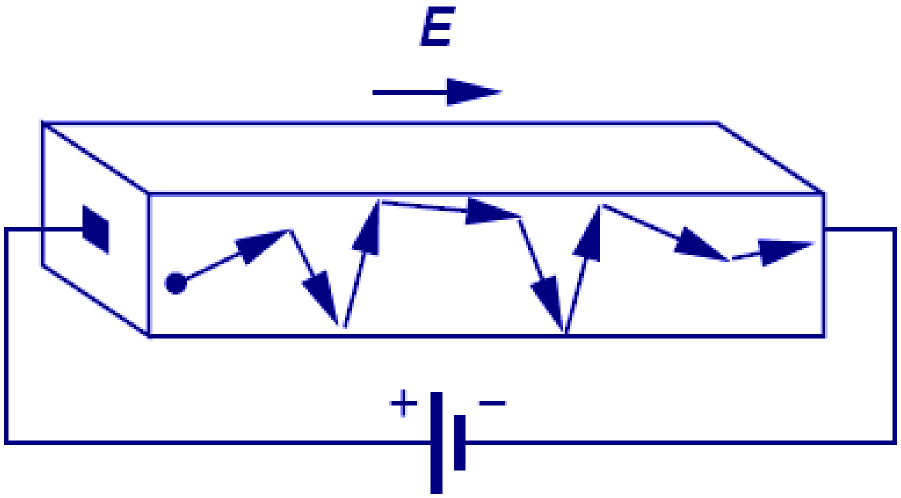
Minority Carriers : $n \approx \dfrac{n_i^2}{N_A}$

Majority Carriers : $n \approx N_D$

Minority Carriers : $p \approx \dfrac{n_i^2}{N_D}$

- **The product of electron and hole densities is ALWAYS equal to the square of intrinsic electron density regardless of doping levels.**

First Charge Transportation Mechanism: Drift

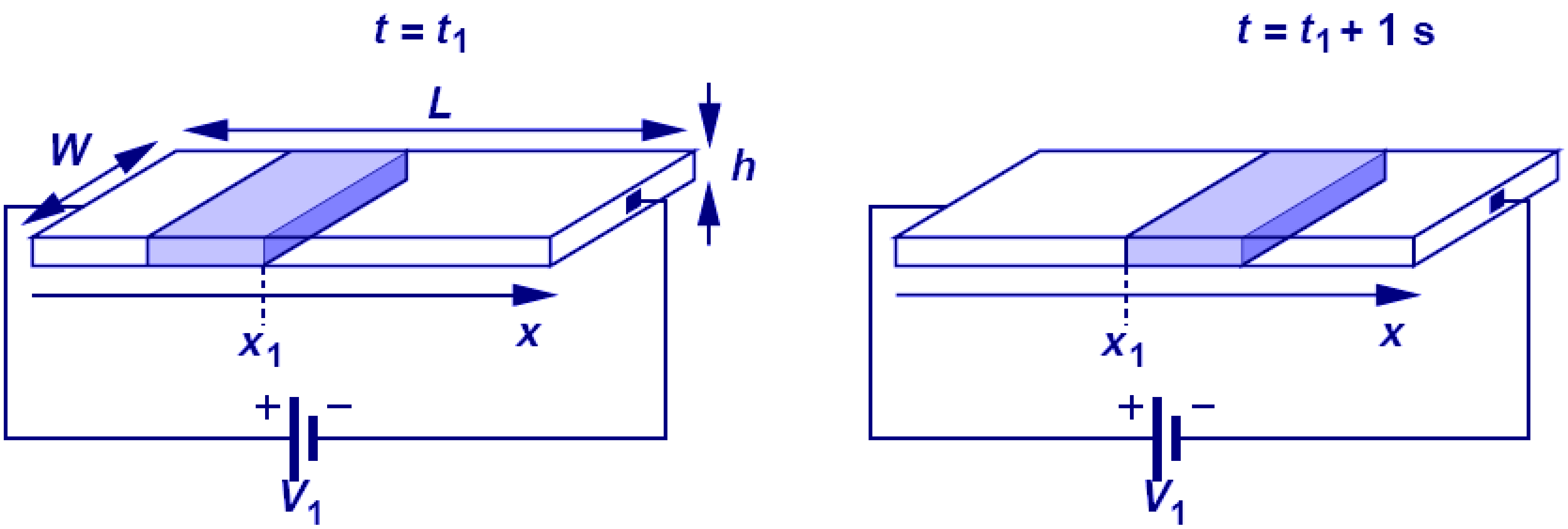


$$\vec{v}_h = \mu_p \vec{E}$$

$$\vec{v}_e = -\mu_n \vec{E}$$

- The process in which charge particles move because of an electric field is called drift.
- Charge particles will move at a velocity that is proportional to the electric field.

Current Flow: General Case



$$I = -v \cdot W \cdot h \cdot n \cdot q$$

- **Electric current is calculated as the amount of charge in *v* meters that passes thru a cross-section if the charge travel with a velocity of *v* m/s.**

Current Flow: Drift

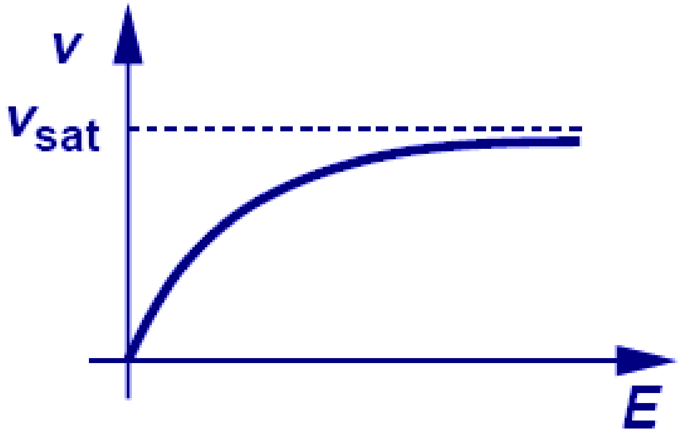
$$J_n = \mu_n E \cdot n \cdot q$$

$$J_{tot} = \mu_n E \cdot n \cdot q + \mu_p E \cdot p \cdot q$$

$$= q(\mu_n n + \mu_p p)E$$

- **Since velocity is equal to μE, drift characteristic is obtained by substituting V with μE in the general current equation.**
- **The total current density consists of both electrons and holes.**

Velocity Saturation



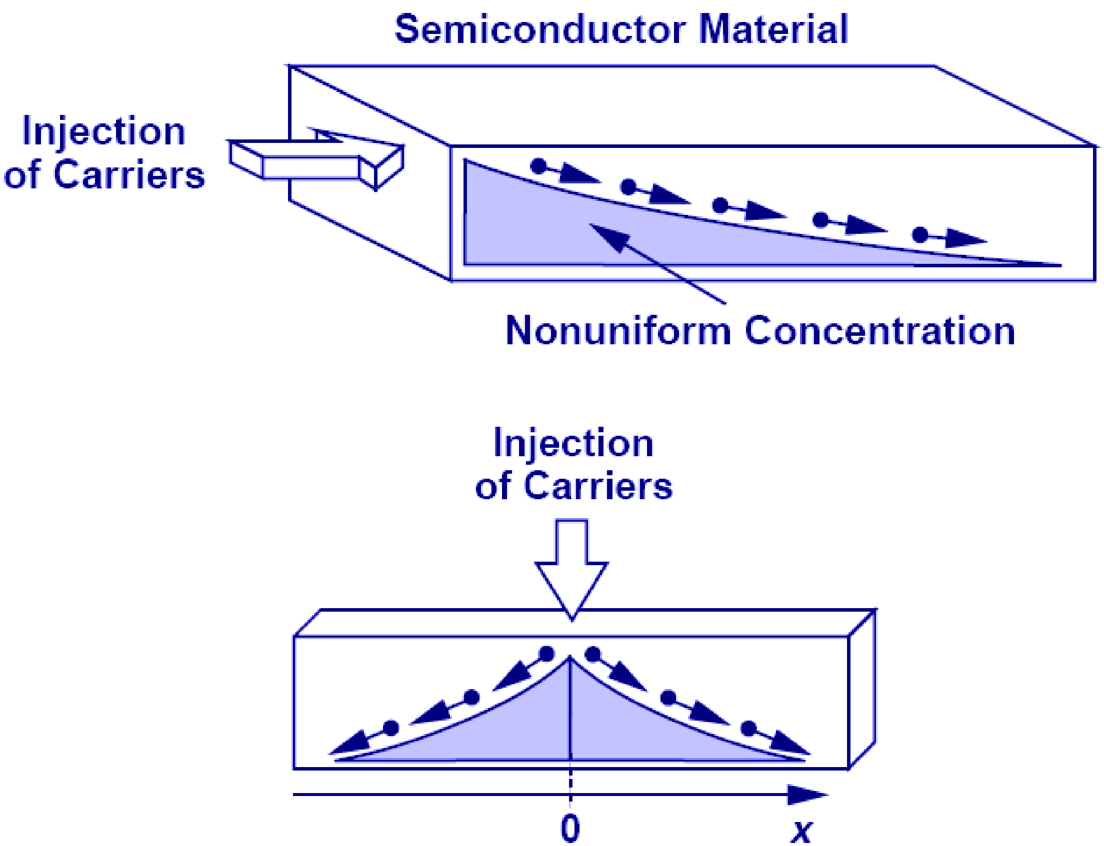
$$\mu = \frac{\mu_0}{1 + bE}$$

$$v_{sat} = \frac{\mu_0}{b}$$

$$v = \frac{\mu_0}{1 + \frac{\mu_0 E}{v_{sat}}} E$$

- A topic treated in more advanced courses is velocity saturation.
- In reality, velocity does not increase linearly with electric field. It will eventually saturate to a critical value.

Second Charge Transportation Mechanism: Diffusion



- **Charge particles move from a region of high concentration to a region of low concentration. It is analogous to an every day example of an ink droplet in water.**

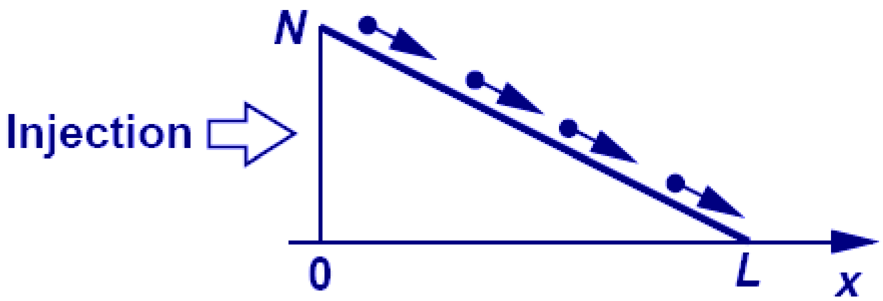
Current Flow: Diffusion

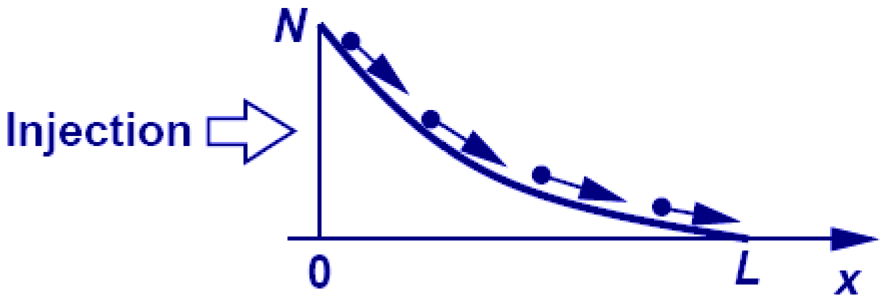
$$I = AqD_n \frac{dn}{dx} \qquad J_p = -qD_p \frac{dp}{dx}$$

$$J_n = qD_n \frac{dn}{dx} \qquad J_{tot} = q\left(D_n \frac{dn}{dx} - D_p \frac{dp}{dx}\right)$$

- **Diffusion current is proportional to the gradient of charge (dn/dx) along the direction of current flow.**
- **Its total current density consists of both electrons and holes.**

Example: Linear vs. Nonlinear Charge Density Profile





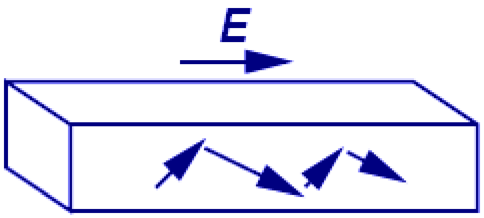
$$J_n = qD_n \frac{dn}{dx} = -qD_n \cdot \frac{N}{L}$$

$$J_n = qD \frac{dn}{dx} = \frac{-qD_n N}{L_d} \exp \frac{-x}{L_d}$$

- **Linear charge density profile means constant diffusion current, whereas nonlinear charge density profile means varying diffusion current.**

Einstein's Relation

Drift Current



$$J_n = q\,\mu_n\,E$$

$$J_p = q\,\mu_p$$

Diffusion Current

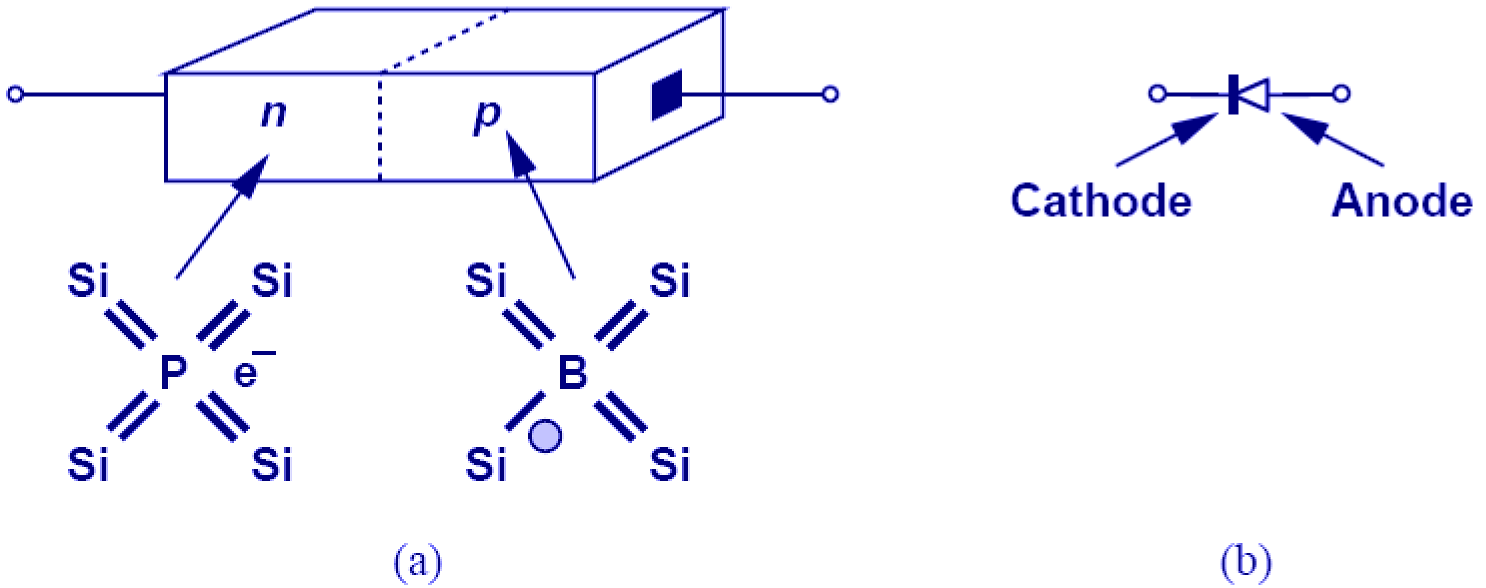
$$J_n = q\,D_n\,\frac{dn}{dx}$$

$$J_n = -\,q\,D_p\,\frac{dp}{dx}$$

$$\boxed{\frac{D}{\mu} = \frac{kT}{q}}$$

- **While the underlying physics behind drift and diffusion currents are totally different, Einstein's relation provides a mysterious link between the two.**

PN Junction (Diode)



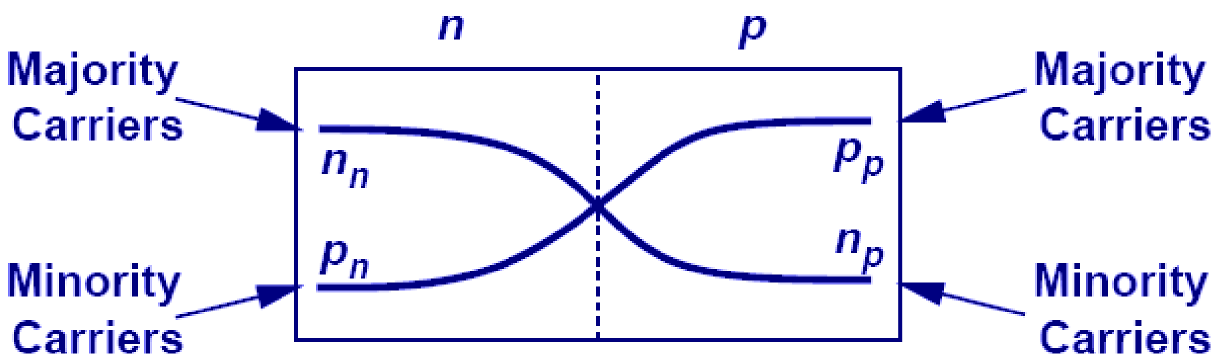
- **When N-type and P-type dopants are introduced side-by-side in a semiconductor, a PN junction or a diode is formed.**

Diode's Three Operation Regions

PN Junction in Equilibrium		PN Junction Under Reverse Bias		PN Junction Under Forward Bias
• Depletion Region • Built–in Potential	⇨	• Junction Capacitance	⇨	• I/V Characteristics

- In order to understand the operation of a diode, it is necessary to study its three operation regions: equilibrium, reverse bias, and forward bias.

Current Flow Across Junction: Diffusion



n_n : Concentration of electrons on n side

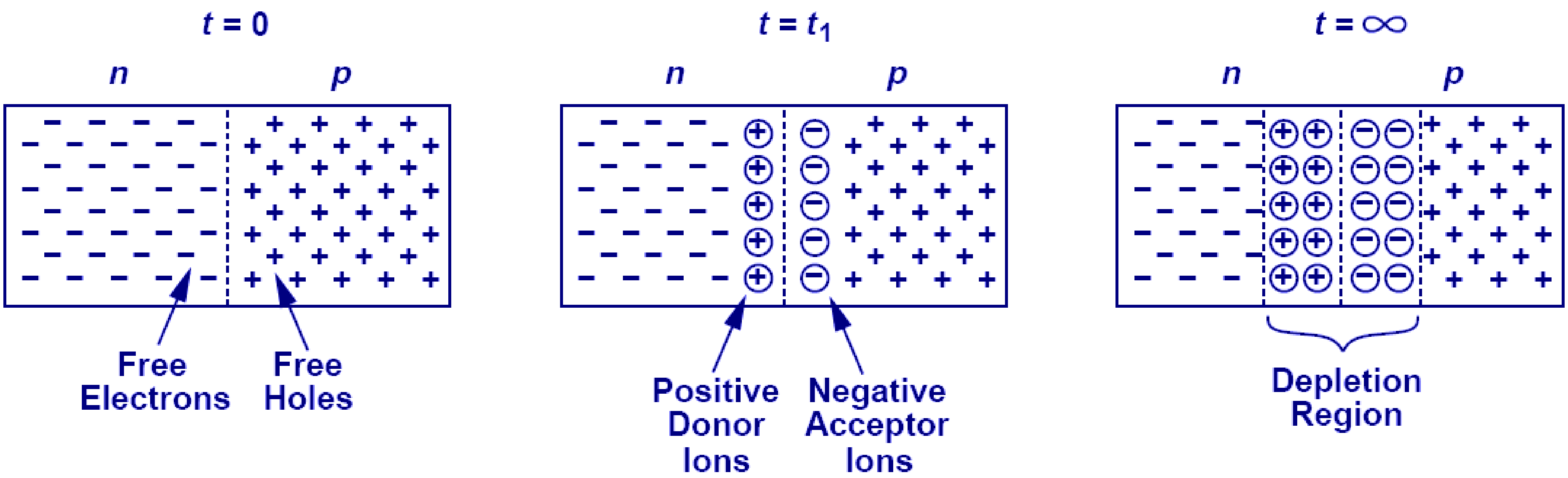
p_n : Concentration of holes on n side

p_p : Concentration of holes on p side

n_p : Concentration of electrons on p side

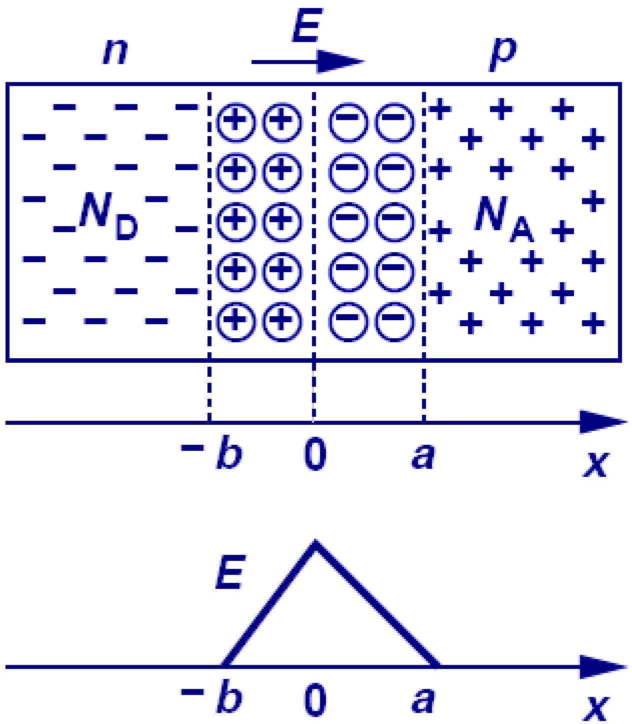
- **Because each side of the junction contains an excess of holes or electrons compared to the other side, there exists a large concentration gradient. Therefore, a diffusion current flows across the junction from each side.**

Depletion Region



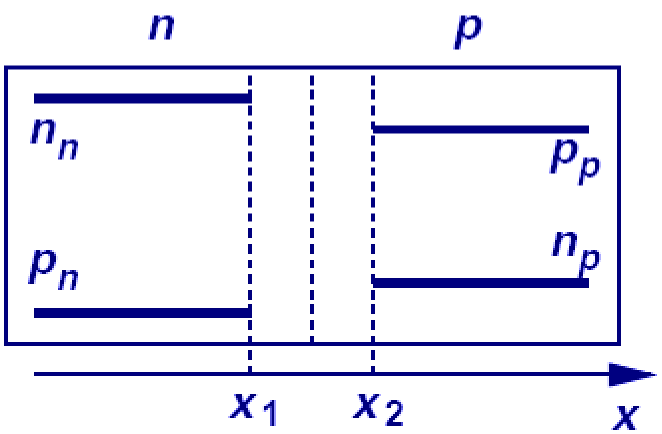
- As free electrons and holes diffuse across the junction, a region of fixed ions is left behind. This region is known as the "depletion region."

Current Flow Across Junction: Drift



- **The fixed ions in depletion region create an electric field that results in a drift current.**

Current Flow Across Junction: Equilibrium



$$I_{drift,p} = I_{diff,p}$$
$$I_{drift,n} = I_{diff,n}$$

- At equilibrium, the drift current flowing in one direction cancels out the diffusion current flowing in the opposite direction, creating a net current of zero.
- The figure shows the charge profile of the PN junction.

Built-in Potential

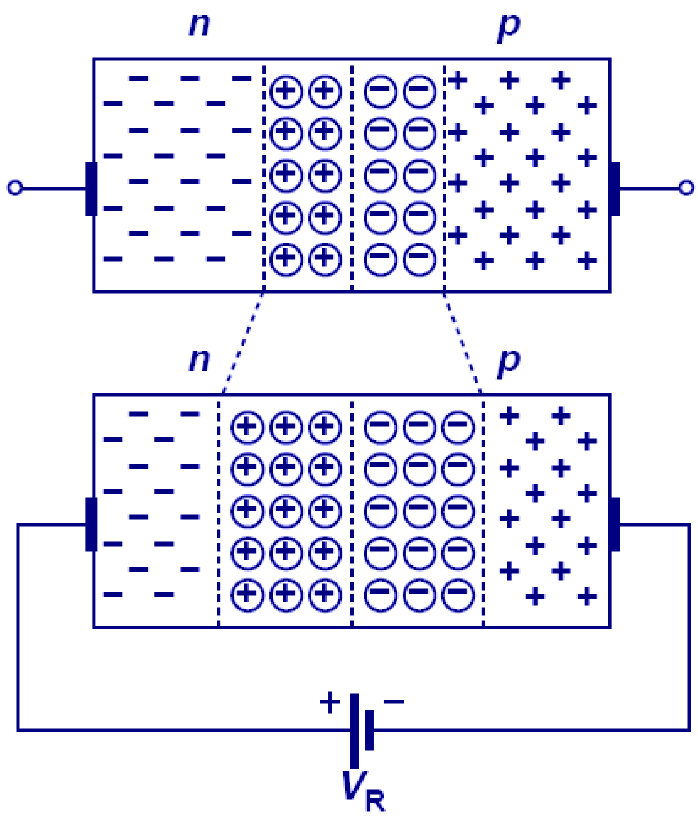
$$q\mu_p pE = -qD_p \frac{dp}{dx} \qquad -\mu_p p \frac{dV}{dx} = -D_p \frac{dp}{dx}$$

$$\mu_p \int_{x_1}^{x_2} dV = D_p \int_{p_p}^{p_n} \frac{dp}{p} \qquad V(x_2) - V(x_1) = \frac{D_p}{\mu_p} \ln \frac{p_p}{p_n}$$

$$V_0 = \frac{kT}{q} \ln \frac{p_p}{p_n}, V_0 = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

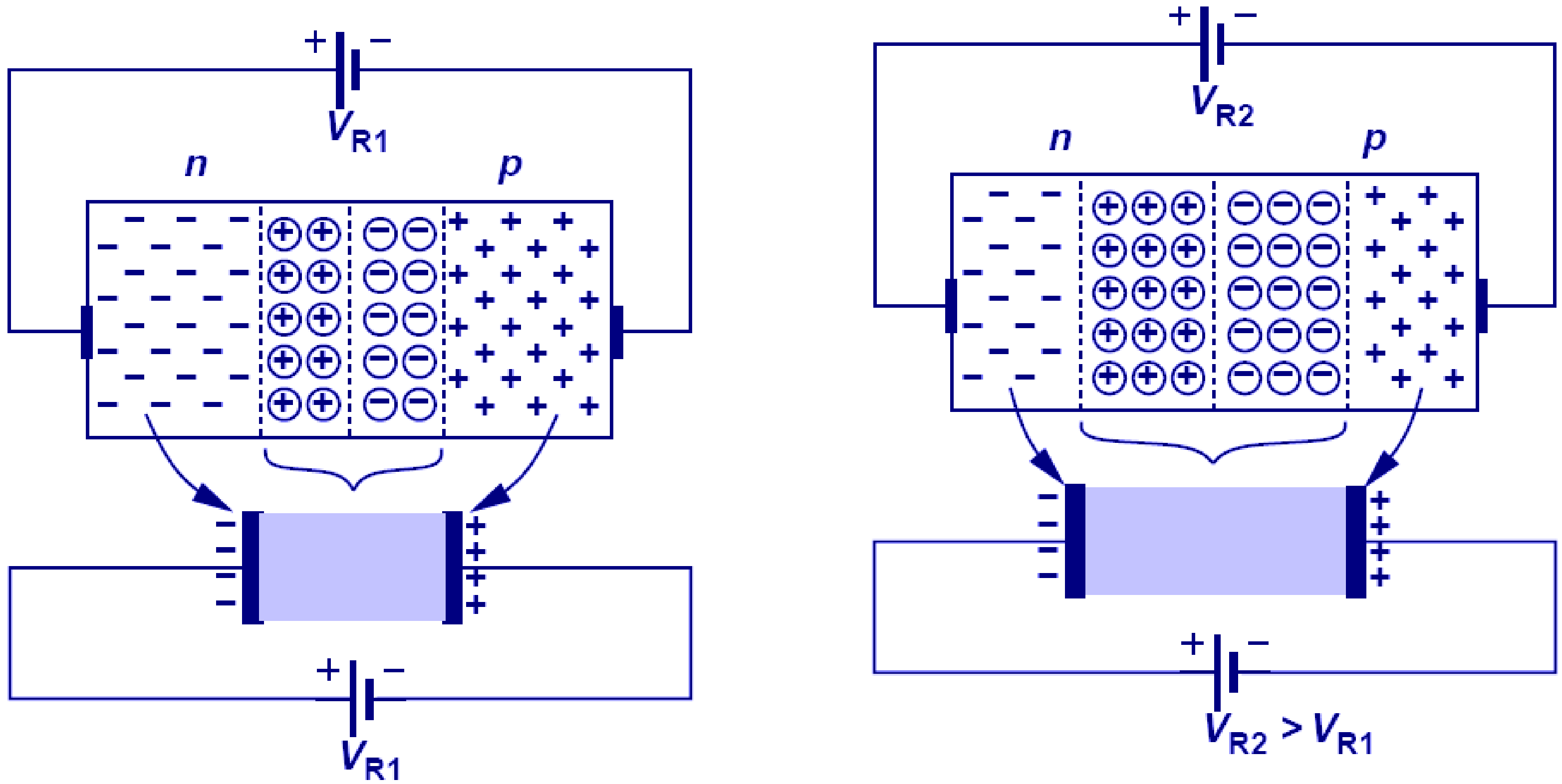
- **Because of the electric field across the junction, there exists a built-in potential. Its derivation is shown above.**

Diode in Reverse Bias



- When the N-type region of a diode is connected to a higher potential than the P-type region, the diode is under reverse bias, which results in wider depletion region and larger built-in electric field across the junction.

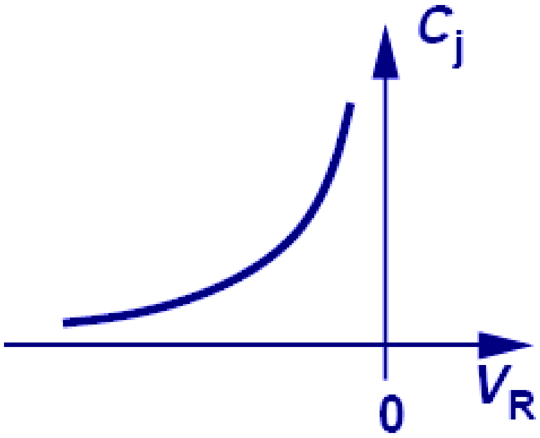
Reverse Biased Diode's Application: Voltage-Dependent Capacitor



(a) (b)

- **The PN junction can be viewed as a capacitor. By varying V_R, the depletion width changes, changing its capacitance value; therefore, the PN junction is actually a voltage-dependent capacitor.**

Voltage-Dependent Capacitance

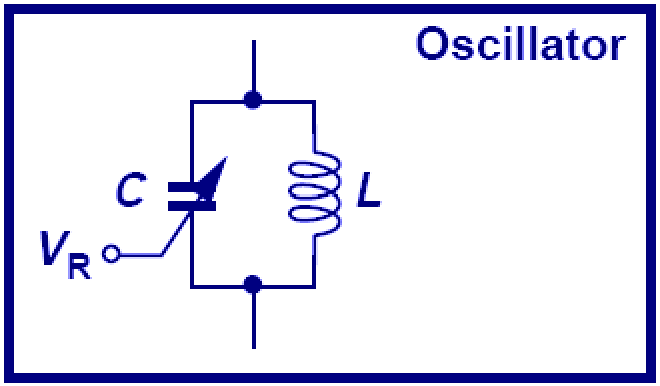


$$C_j = \frac{C_{j0}}{\sqrt{1 + \dfrac{V_R}{V_0}}}$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{V_0}}$$

- **The equations that describe the voltage-dependent capacitance are shown above.**

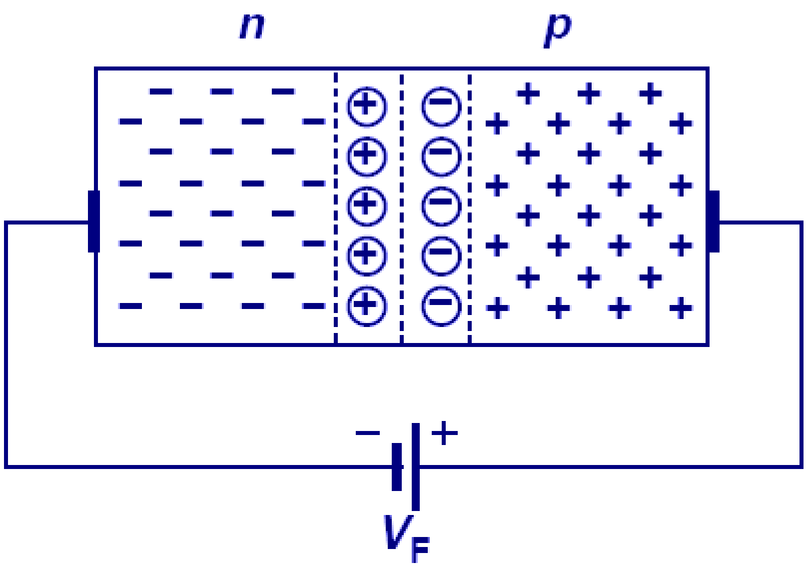
Voltage-Controlled Oscillator



$$f_{res} = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}$$

- **A very important application of a reverse-biased PN junction is VCO, in which an LC tank is used in an oscillator. By changing V_R, we can change C, which also changes the oscillation frequency.**

Diode in Forward Bias

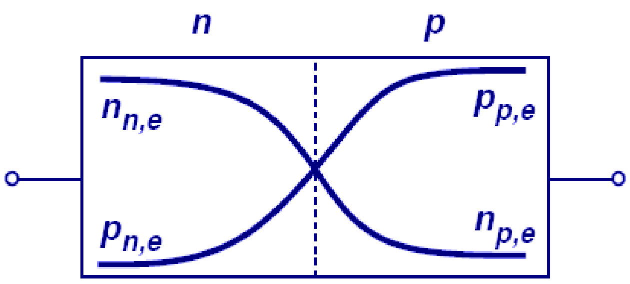


- When the N-type region of a diode is at a lower potential than the P-type region, the diode is in forward bias.
- The depletion width is shortened and the built-in electric field decreased.

Minority Carrier Profile in Forward Bias

$$p_{n,e} = \frac{p_{p,e}}{\exp\dfrac{V_0}{V_T}}$$

$$p_{n,f} = \frac{p_{p,f}}{\exp\dfrac{V_0 - V_F}{V_T}}$$



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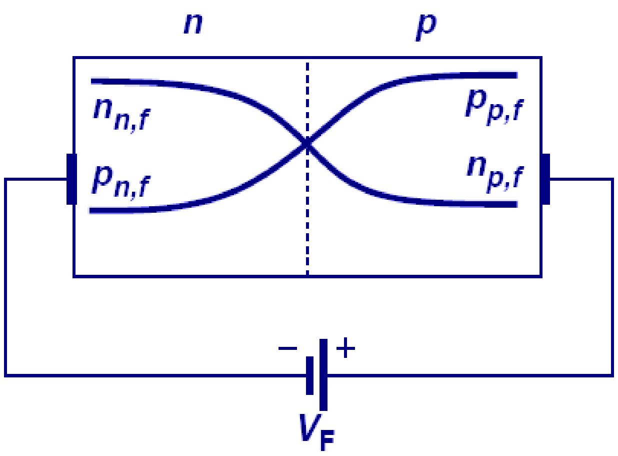


(b)

- Under forward bias, minority carriers in each region increase due to the lowering of built-in field/potential. Therefore, diffusion currents increase to supply these minority carriers.

Diffusion Current in Forward Bias

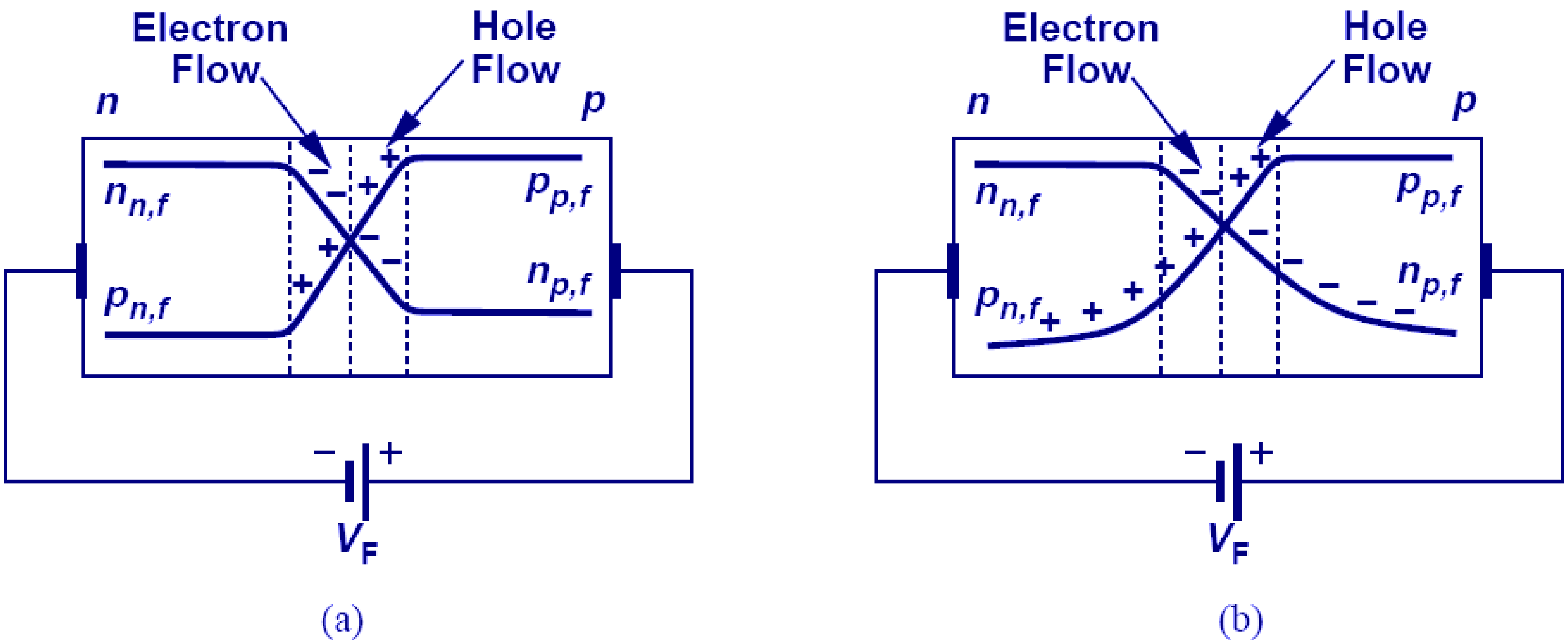
$$\Delta n_p \approx \frac{N_D}{\exp\frac{V_0}{V_T}}(\exp\frac{V_F}{V_T} - 1) \qquad \Delta p_n \approx \frac{N_A}{\exp\frac{V_0}{V_T}}(\exp\frac{V_F}{V_T} - 1)$$

$$I_{tot} \propto \frac{N_A}{\exp\frac{V_0}{V_T}}(\exp\frac{V_F}{V_T} - 1) + \frac{N_D}{\exp\frac{V_0}{V_T}}(\exp\frac{V_F}{V_T} - 1)$$

$$I_{tot} = I_s(\exp\frac{V_F}{V_T} - 1) \qquad I_s = Aqn_i^2(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p})$$

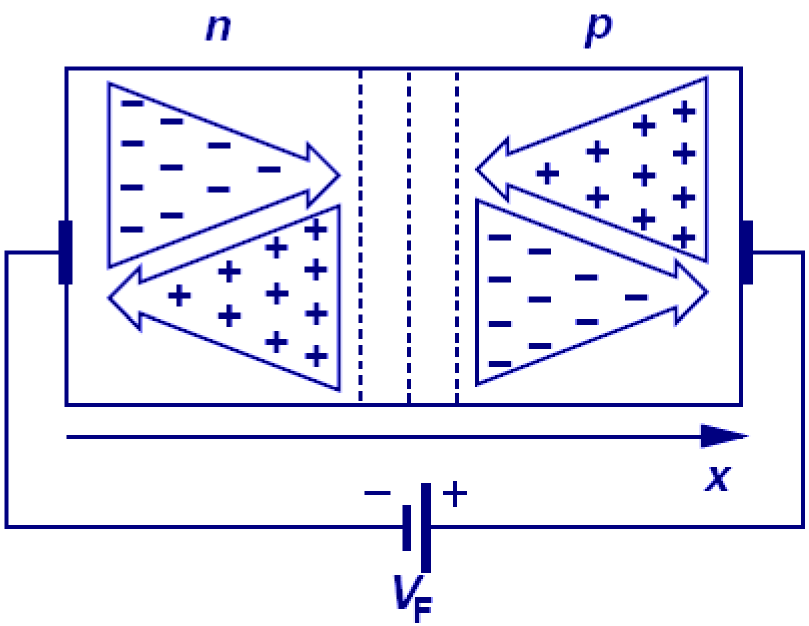
- **Diffusion current will increase in order to supply the increase in minority carriers. The mathematics are shown above.**

Minority Charge Gradient



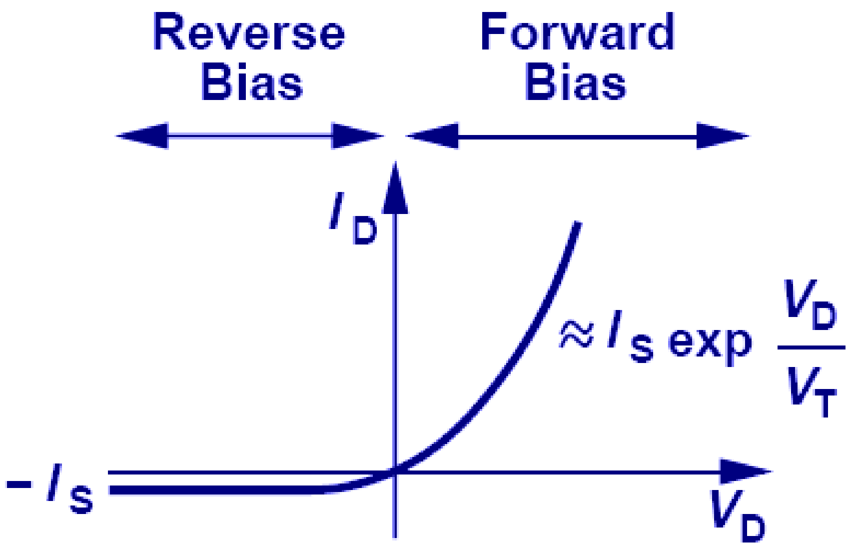
- Minority charge profile should not be constant along the x-axis; otherwise, there is no concentration gradient and no diffusion current.
- Recombination of the minority carriers with the majority carriers accounts for the dropping of minority carriers as they go deep into the P or N region.

Forward Bias Condition: Summary



- In forward bias, there are large diffusion currents of minority carriers through the junction. However, as we go deep into the P and N regions, recombination currents from the majority carriers dominate. These two currents add up to a constant value.

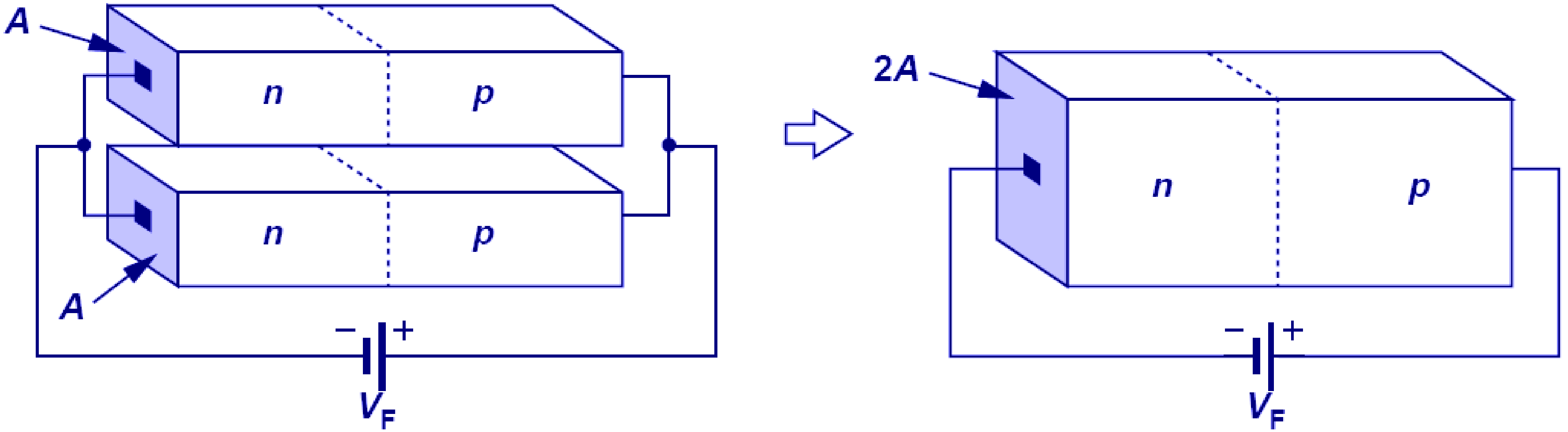
IV Characteristic of PN Junction



$$I_D = I_S\left(\exp\frac{V_D}{V_T} - 1\right)$$

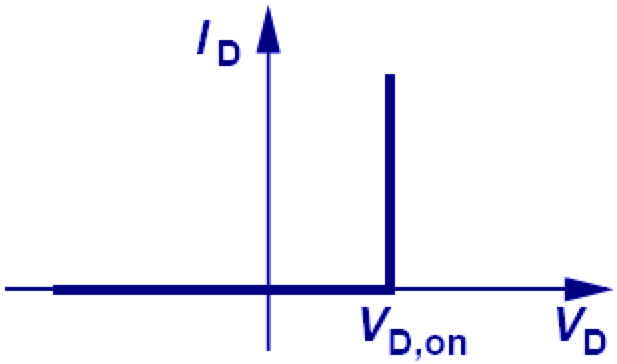
- **The current and voltage relationship of a PN junction is exponential in forward bias region, and relatively constant in reverse bias region.**

Parallel PN Junctions



- Since junction currents are proportional to the junction's cross-section area. Two PN junctions put in parallel are effectively one PN junction with twice the cross-section area, and hence twice the current.

Constant-Voltage Diode Model



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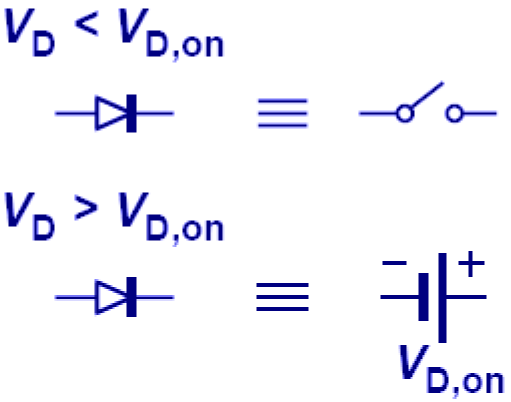
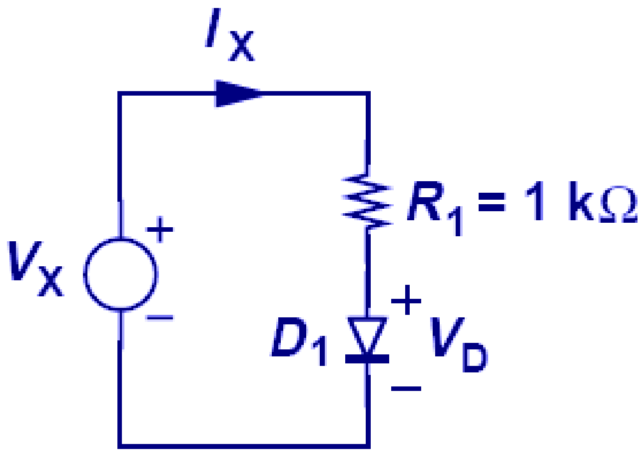


(b)

- **Diode operates as an open circuit if $V_D < V_{D,on}$ and a constant voltage source of $V_{D,on}$ if V_D tends to exceed $V_{D,on}$.**

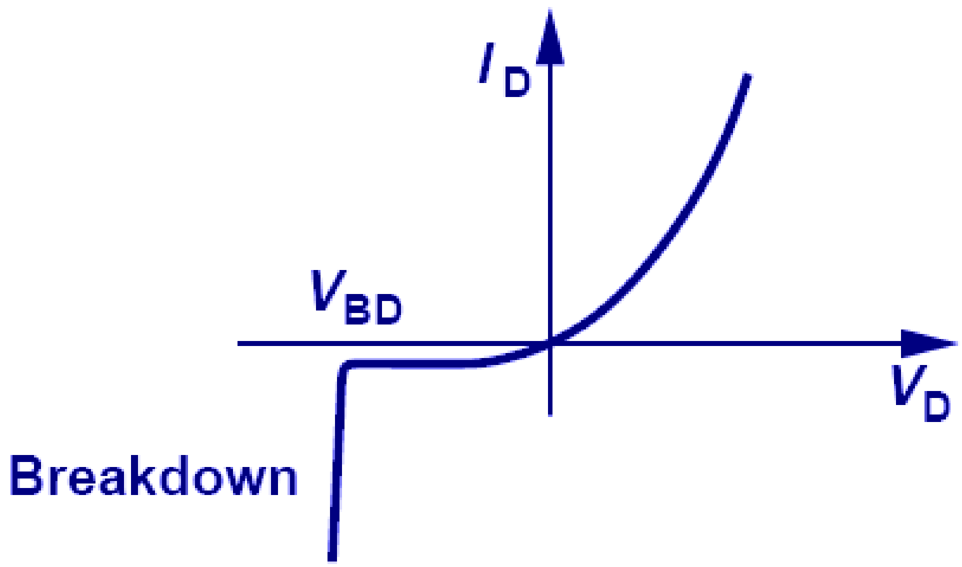
Example: Diode Calculations



$$V_X = I_X R_1 + V_D = I_X R_1 + V_T \ln\frac{I_X}{I_S}$$
$$I_X = 2.2mA \quad for \quad V_X = 3V$$
$$I_X = 0.2mA \quad for \quad V_X = 1V$$

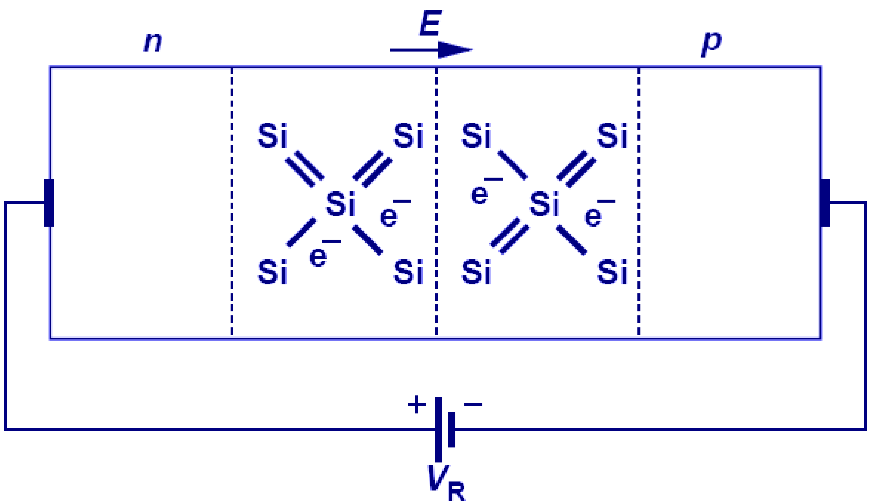
- This example shows the simplicity provided by a constant-voltage model over an exponential model.
- For an exponential model, iterative method is needed to solve for current, whereas constant-voltage model requires only linear equations.

Reverse Breakdown

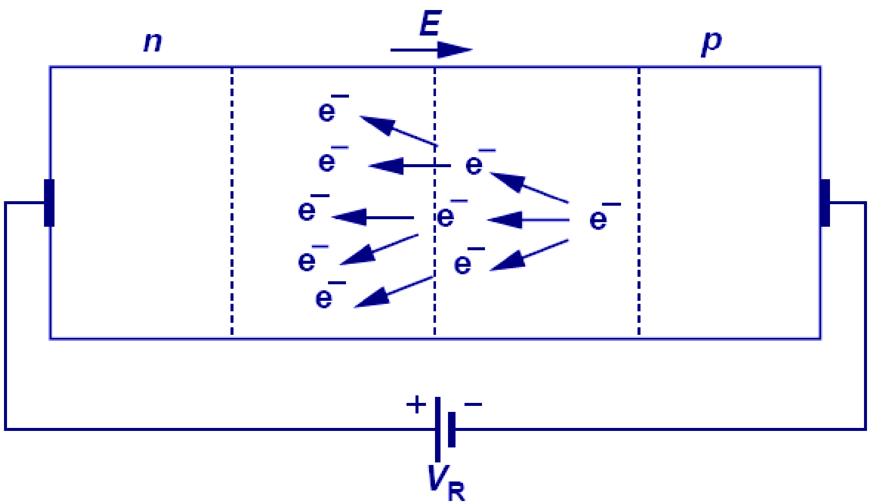


- **When a large reverse bias voltage is applied, breakdown occurs and an enormous current flows through the diode.**

Zener vs. Avalanche Breakdown



(a)



(b)

- **Zener breakdown is a result of the large electric field inside the depletion region that breaks electrons or holes off their covalent bonds.**
- **Avalanche breakdown is a result of electrons or holes colliding with the fixed ions inside the depletion region.**

Chapter 3 Diode Circuits

- 3.1 Ideal Diode
- 3.2 PN Junction as a Diode
- 3.3 Applications of Diodes

Diode Circuits

Diodes as Circuit Elements

- Ideal Diode
- Circuit Characteristics
- Actual Diode

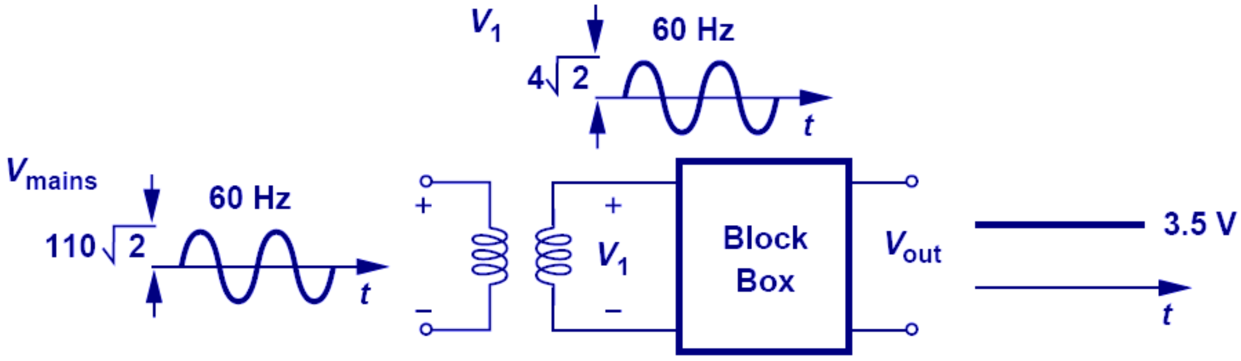
⇨

Applications

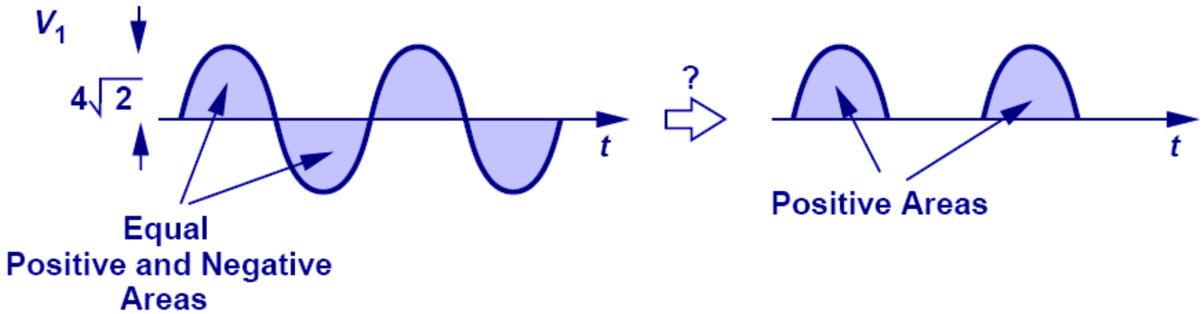
- Regulators
- Rectifiers
- Limiting and Clamping Circuits

➢ **After we have studied in detail the physics of a diode, it is time to study its behavior as a circuit element and its many applications.**

Diode's Application: Cell Phone Charger



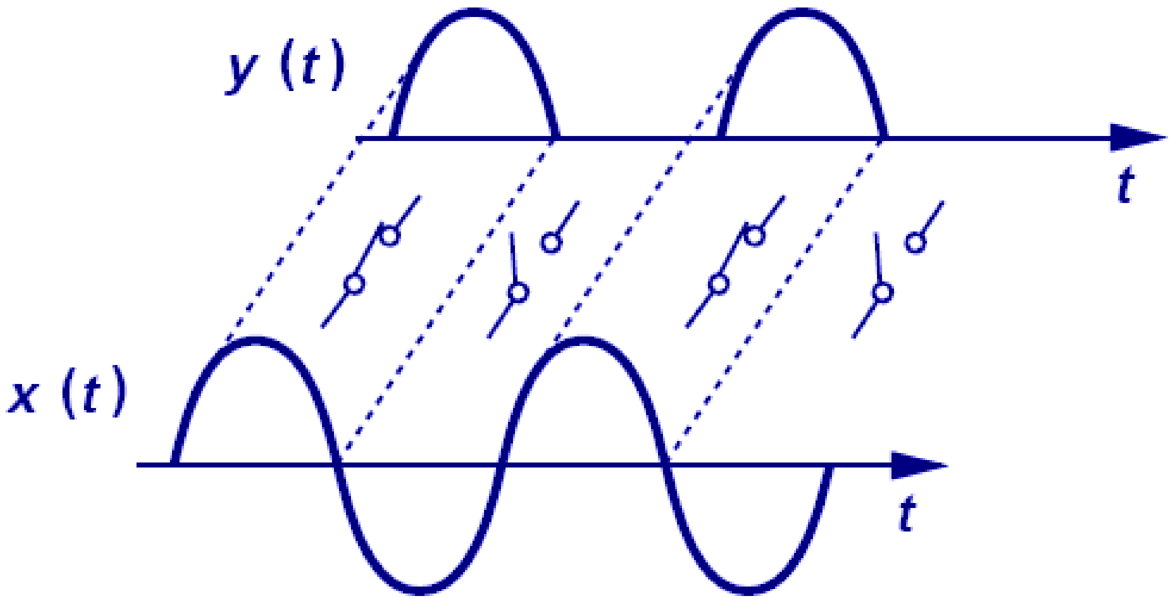
(a)



(b)

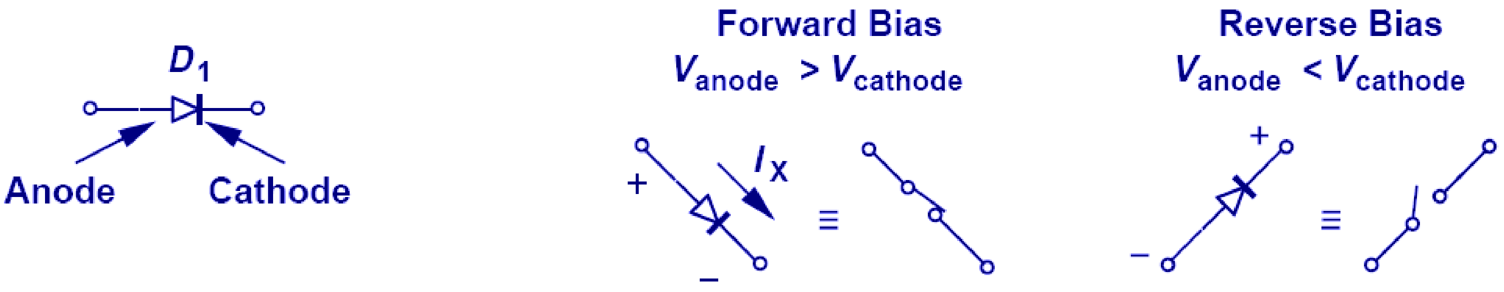
- An important application of diode is chargers.
- Diode acts as the black box (after transformer) that passes only the positive half of the stepped-down sinusoid.

Diode's Action in The Black Box (Ideal Diode)



- The diode behaves as a short circuit during the positive half cycle (voltage across it tends to exceed zero), and an open circuit during the negative half cycle (voltage across it is less than zero).

Ideal Diode



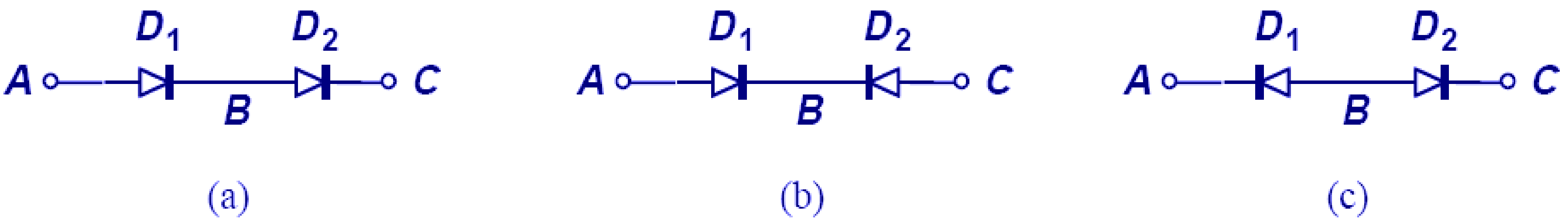
(a)

(b)

(c)

- **In an ideal diode, if the voltage across it tends to exceed zero, current flows.**
- **It is analogous to a water pipe that allows water to flow in only one direction.**

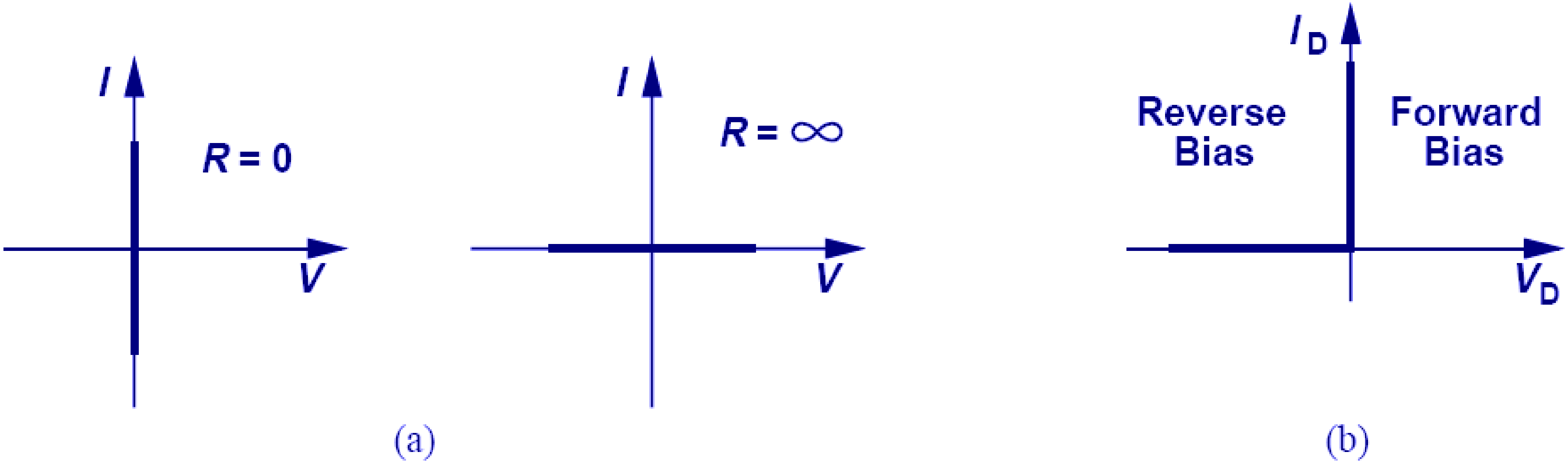
Diodes in Series



- **Diodes cannot be connected in series randomly. For the circuits above, only a) can conduct current from A to C.**

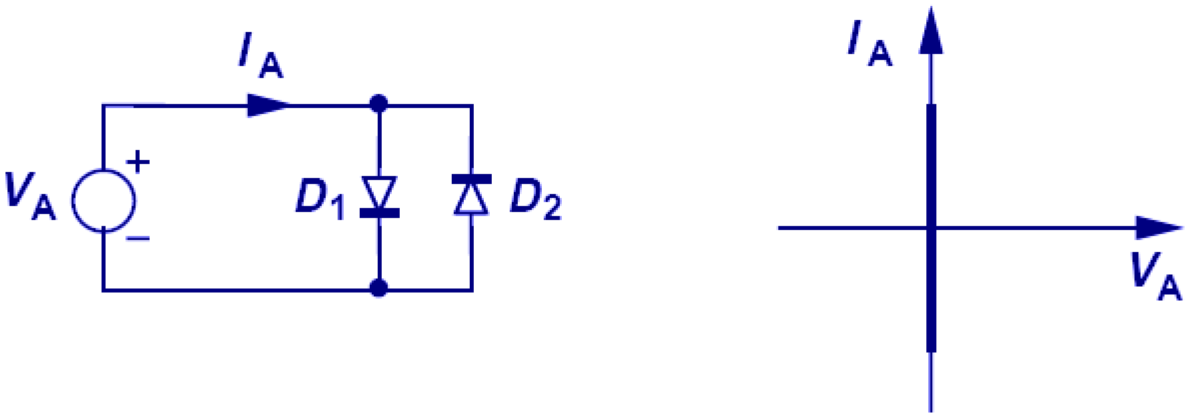
IV Characteristics of an Ideal Diode

$$R = 0 \Rightarrow I = \frac{V}{R} = \infty \qquad R = \infty \Rightarrow I = \frac{V}{R} = 0$$



- If the voltage across anode and cathode is greater than zero, the resistance of an ideal diode is zero and current becomes infinite. However, if the voltage is less than zero, the resistance becomes infinite and current is zero.

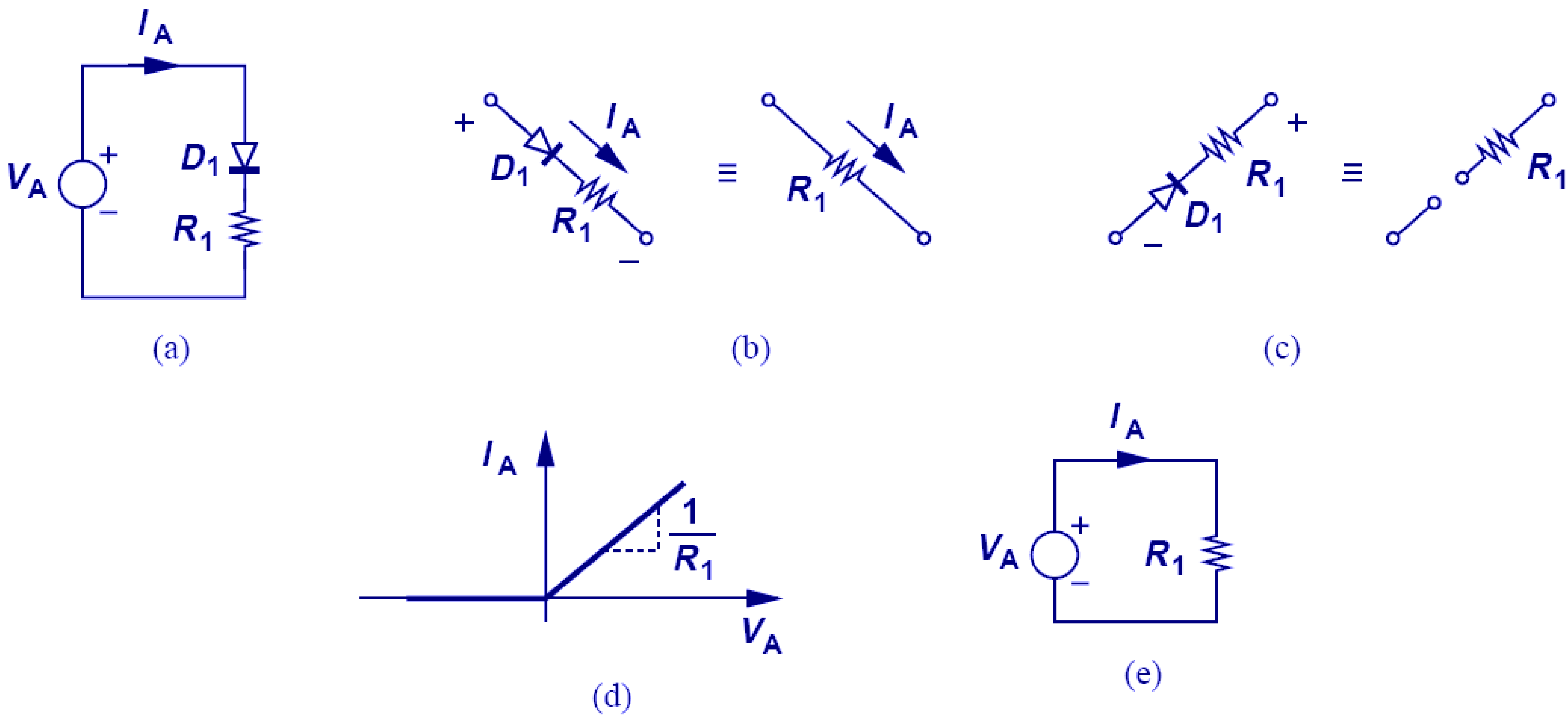
Anti-Parallel Ideal Diodes



(a) (b)

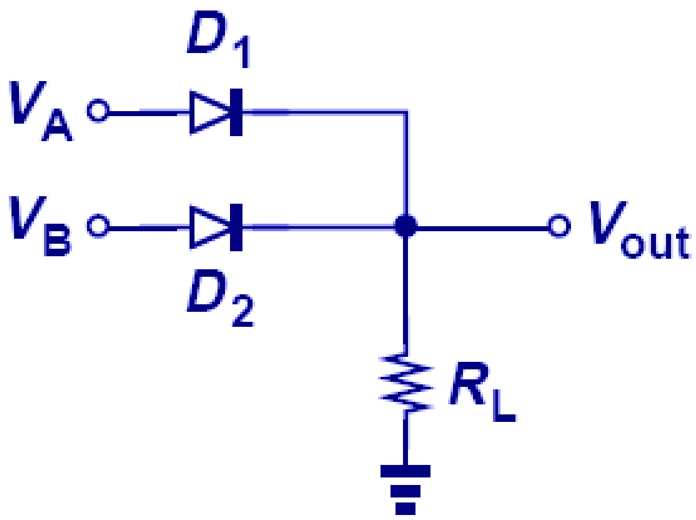
- **If two diodes are connected in anti-parallel, it acts as a short for all voltages.**

Diode-Resistor Combination



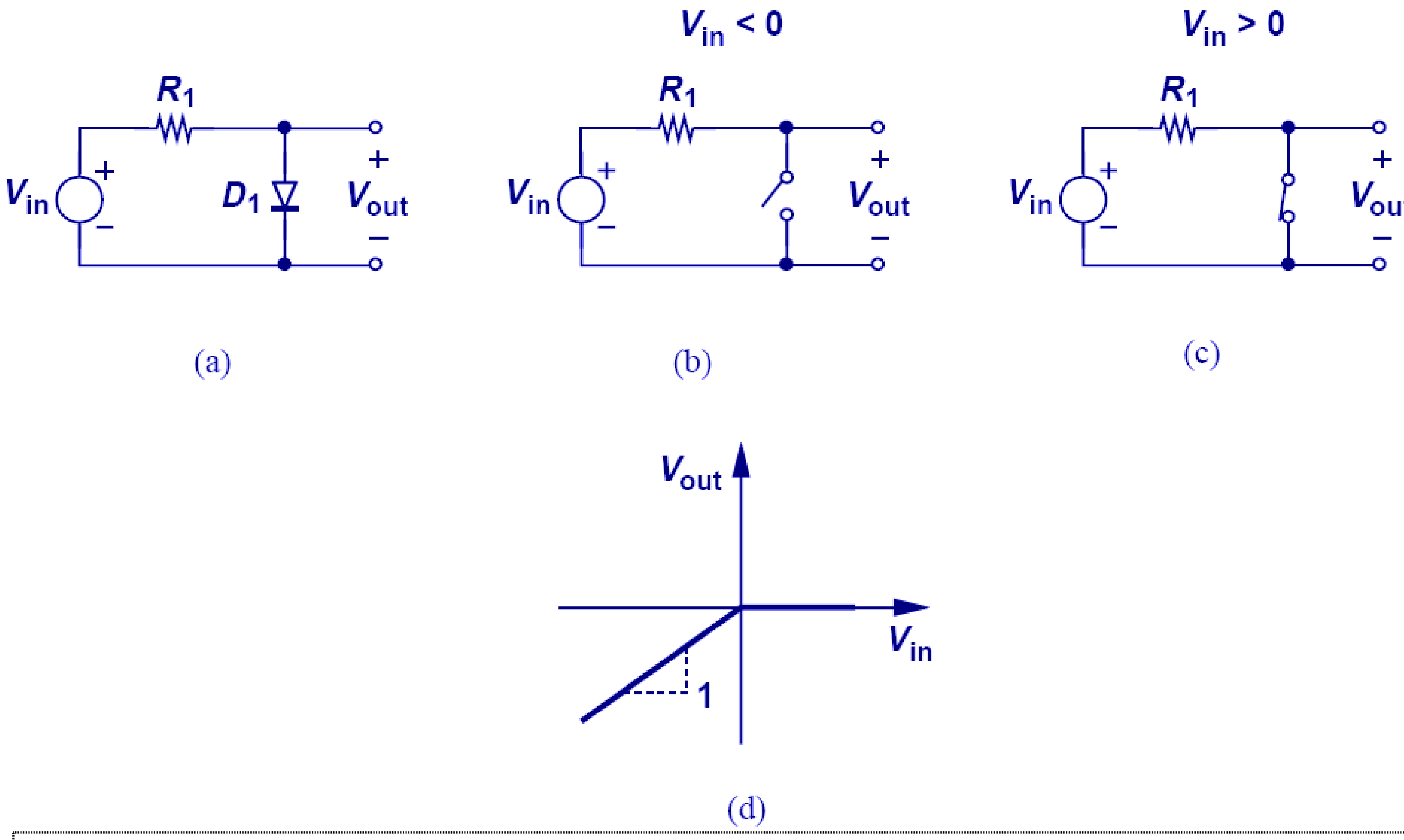
- **The IV characteristic of this diode-resistor combination is zero for negative voltages and Ohm's law for positive voltages.**

Diode Implementation of OR Gate



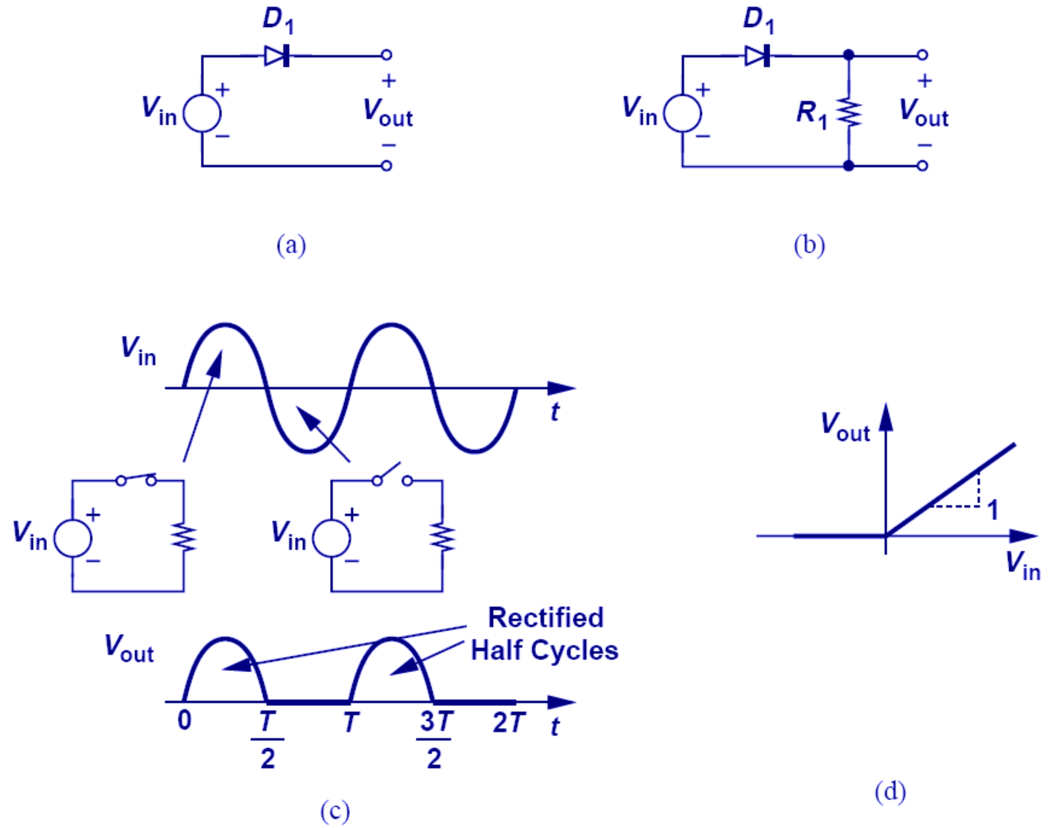
- The circuit above shows an example of diode-implemented OR gate.
- V_{out} can only be either V_A or V_B, not both.

Input/Output Characteristics



- When V_{in} is less than zero, the diode opens, so $V_{out} = V_{in}$.
- When V_{in} is greater than zero, the diode shorts, so $V_{out} = 0$.

Diode's Application: Rectifier



- A rectifier is a device that passes positive-half cycle of a sinusoid and blocks the negative half-cycle or vice versa.
- When V_{in} is greater than 0, diode shorts, so $V_{out} = V_{in}$; however, when V_{in} is less than 0, diode opens, no current flows thru R_1, $Vout = I_{R1}R_1 = 0$.

Signal Strength Indicator

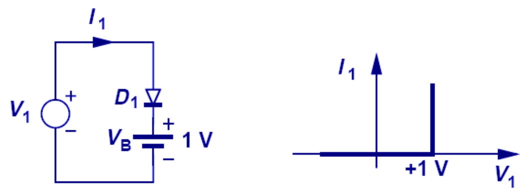
$$V_{out} = V_p \sin \omega t = 0 \qquad for \quad 0 \le t \le \frac{T}{2}$$

$$V_{out,avg} = \frac{1}{T}\int_0^T V_{out}(t)dt = \frac{1}{T}\int_0^{T/2} V_p \sin \omega t dt$$

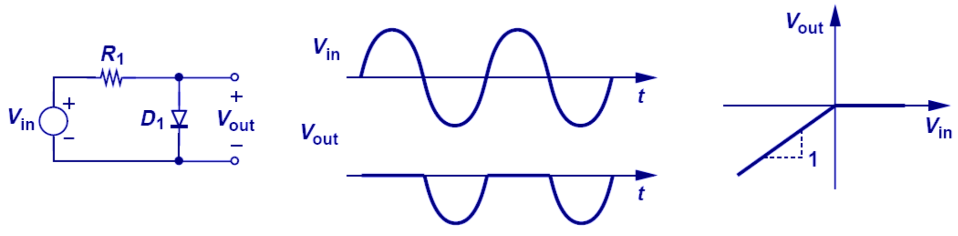
$$= \frac{1}{T}\frac{V_p}{\omega}\left[- \cos \omega t\right]_0^{T/2} = \frac{V_p}{\pi} \qquad for \quad \frac{T}{2} \le t \le T$$

- **The averaged value of a rectifier output can be used as a signal strength indicator for the input, since $V_{out,avg}$ is proportional to V_p, the input signal's amplitude.**

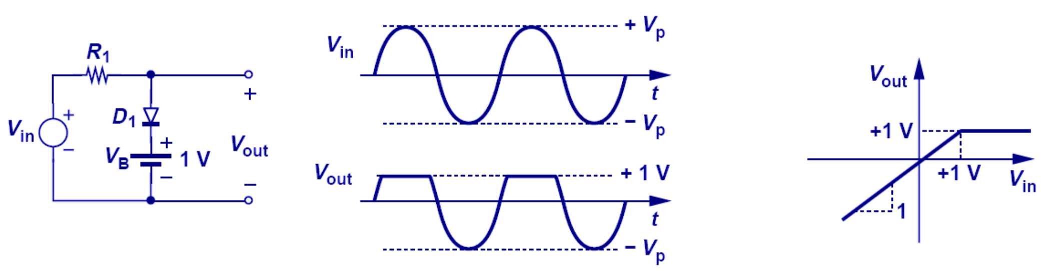
Diode's application: Limiter



(a)



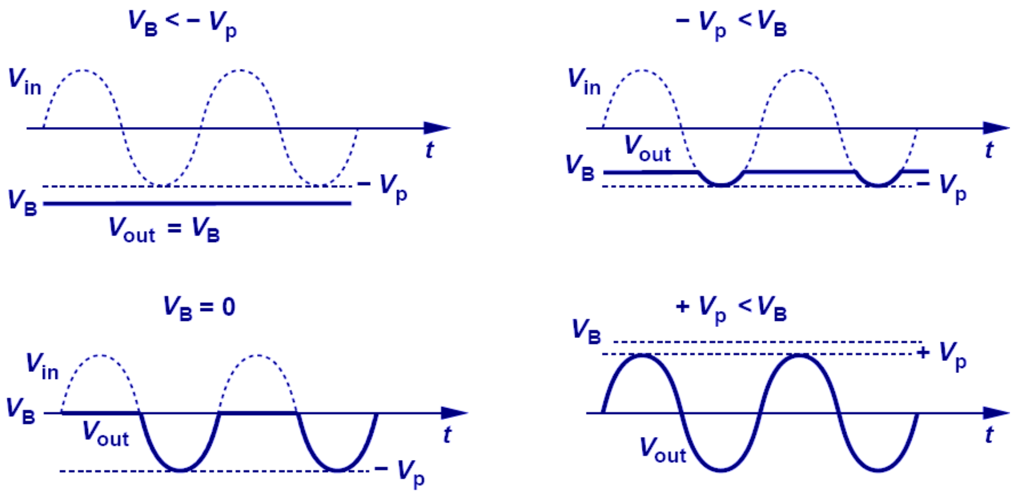
(b)



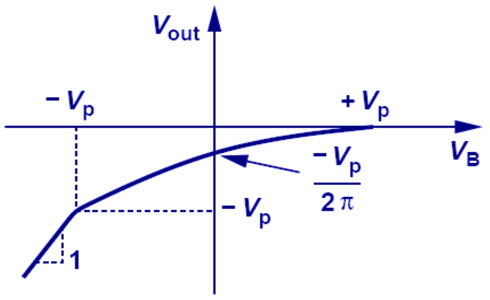
(c)

- The purpose of a limiter is to force the output to remain below certain value.
- In a), the addition of a 1 V battery forces the diode to turn on after V_1 has become greater than 1 V.

Limiter: When Battery Varies



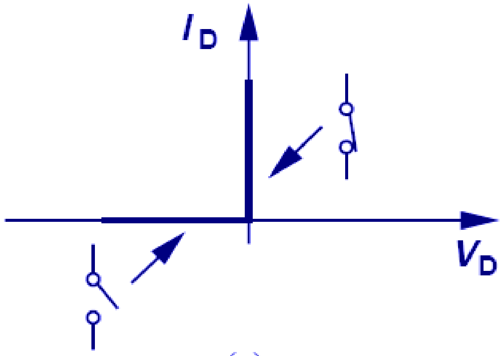
(a)



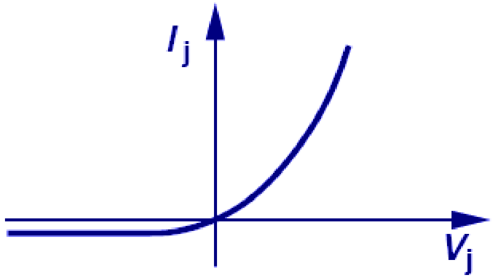
(b)

- An interesting case occurs when V_B (battery) varies.
- Rectification fails if V_B is greater than the input amplitude.

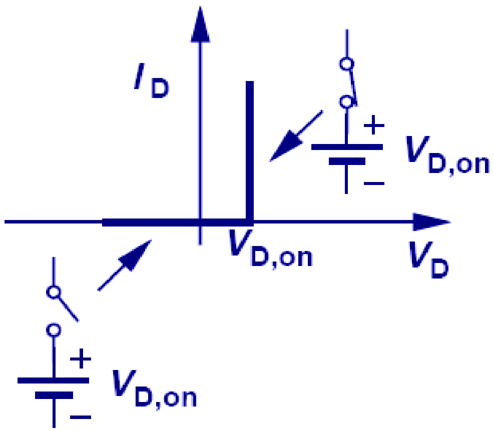
Different Models for Diode



(a)



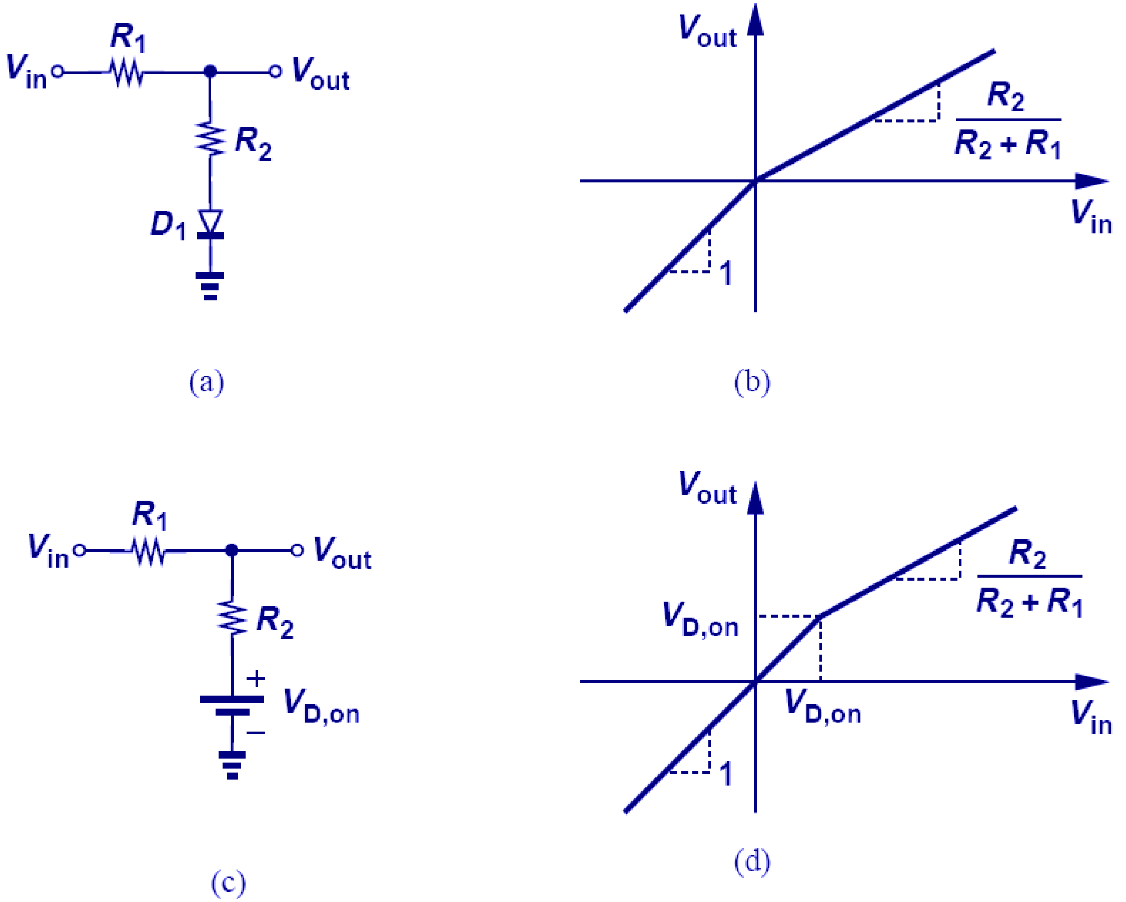
(b)



(c)

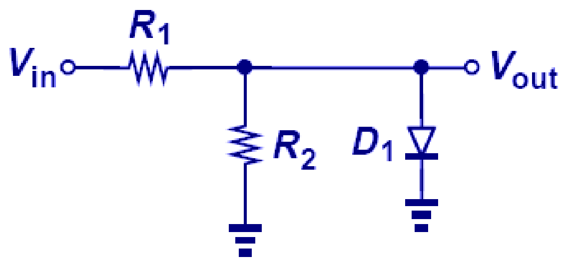
- **So far we have studied the ideal model of diode. However, there are still the exponential and constant voltage models.**

Input/Output Characteristics with Ideal and Constant-Voltage Models

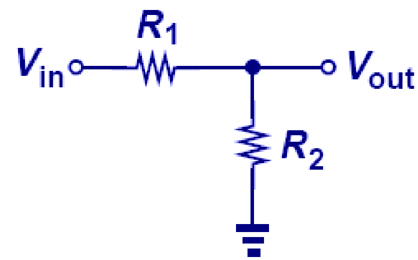


- **The circuit above shows the difference between the ideal and constant-voltage model; the two models yield two different break points of slope.**

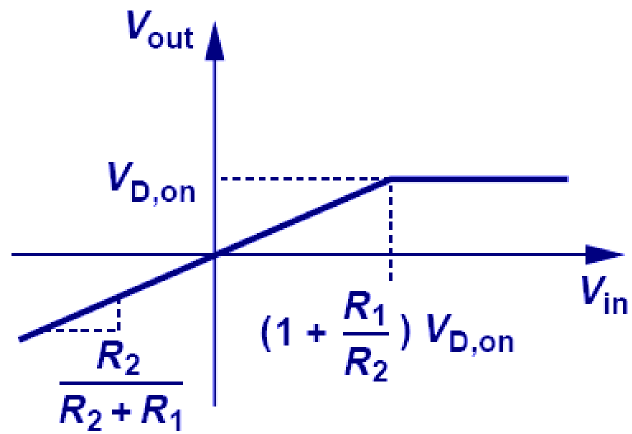
Input/Output Characteristics with a Constant-Voltage Model



(a)



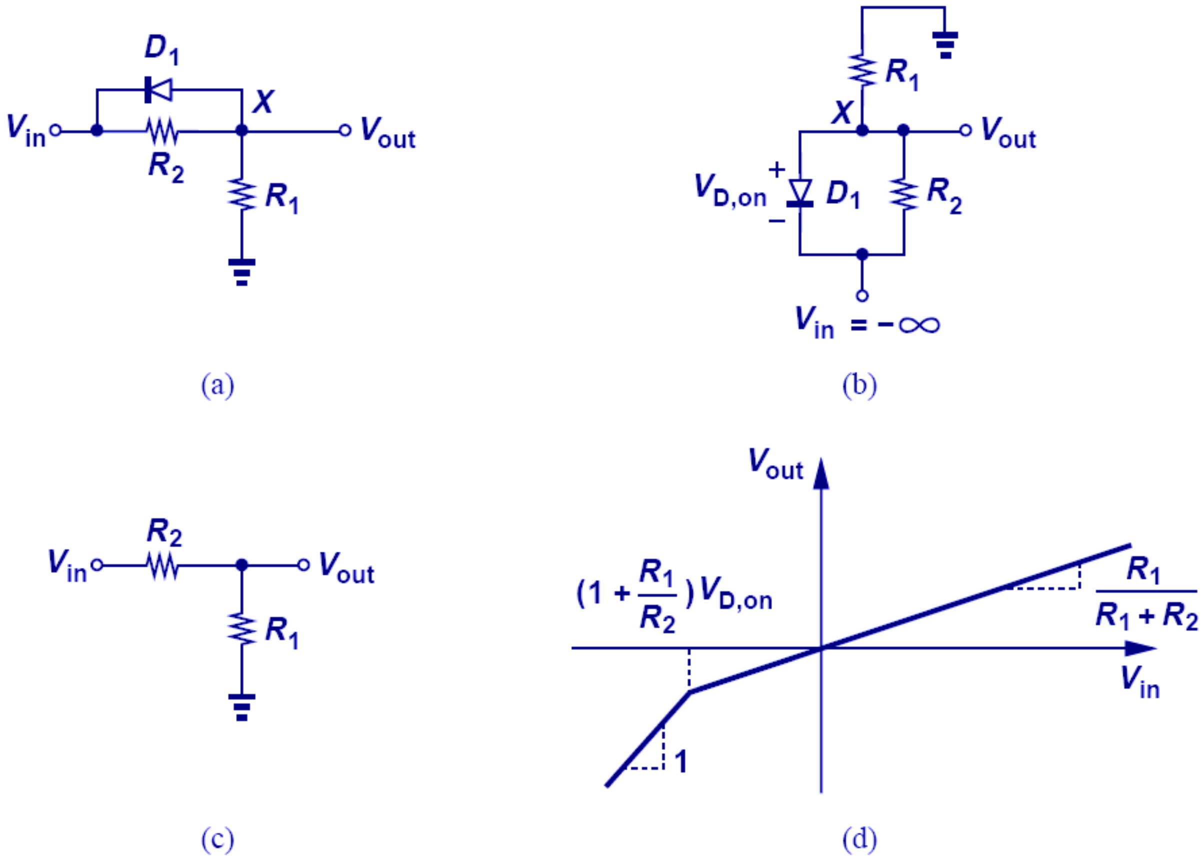
(b)



(c)

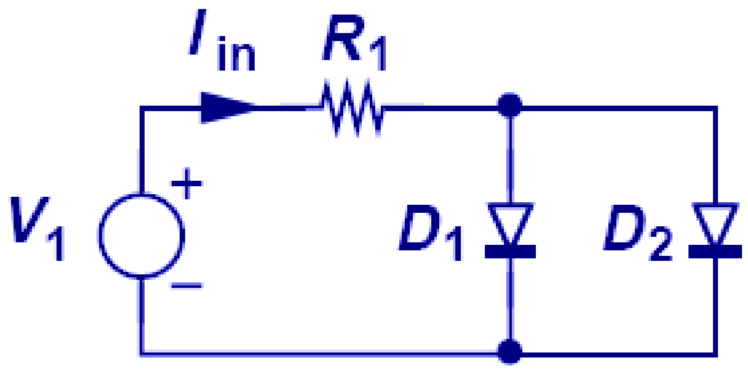
- **When using a constant-voltage model, the voltage drop across the diode is no longer zero but $V_{d,on}$ when it conducts.**

Another Constant-Voltage Model Example



- In this example, since Vin is connected to the cathode, the diode conducts when Vin is very negative.
- The break point where the slope changes is when the current across R1 is equal to the current across R2.

Exponential Model

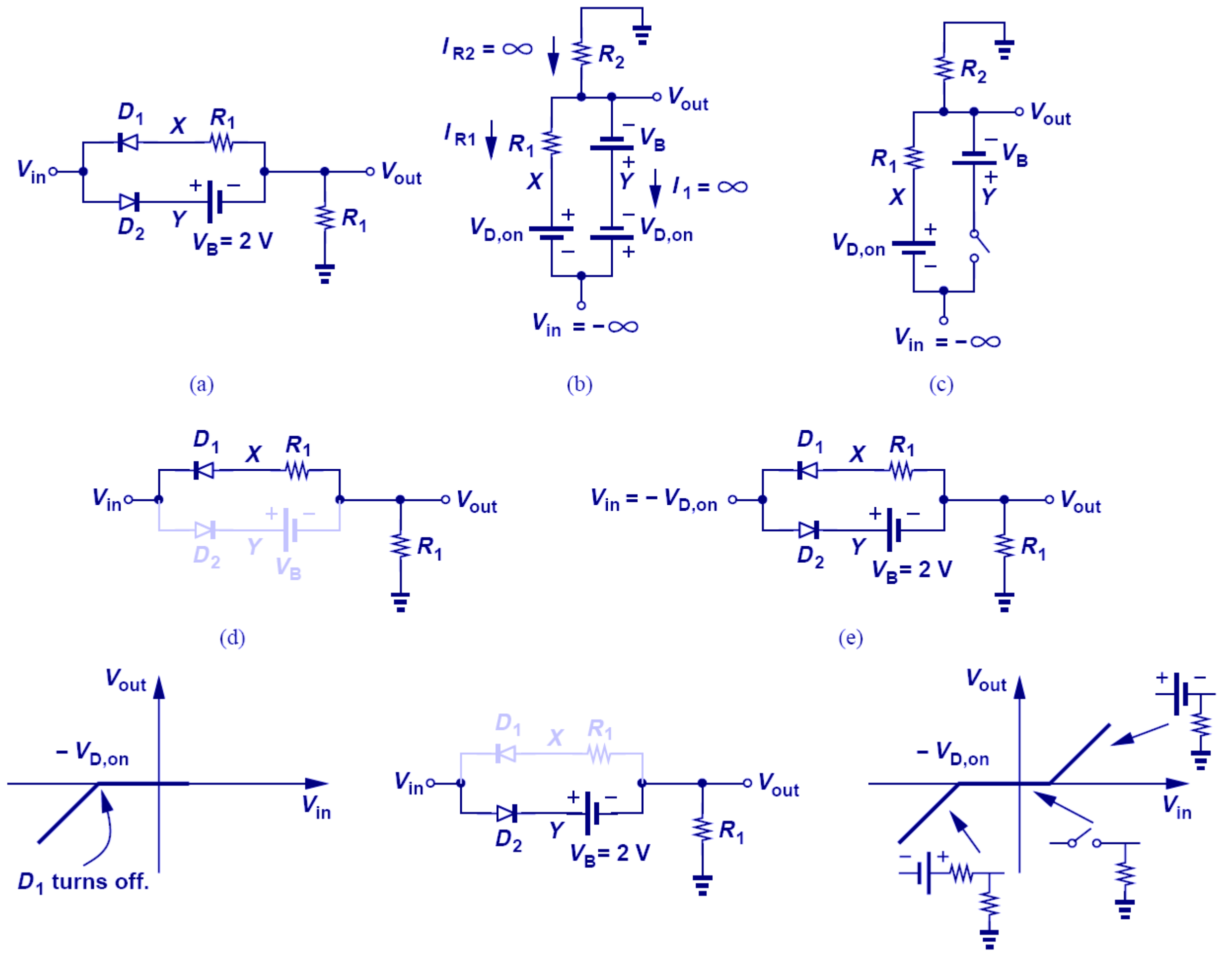


$$I_{D1} = \frac{I_{in}}{1 + \frac{I_{s2}}{I_{s1}}}$$

$$I_{D2} = \frac{I_{in}}{1 + \frac{I_{s1}}{I_{s2}}}$$

- **In this example, since the two diodes have different cross-section areas, only exponential model can be used.**
- **The two currents are solved by summing them with I_{in}, and equating their voltages.**

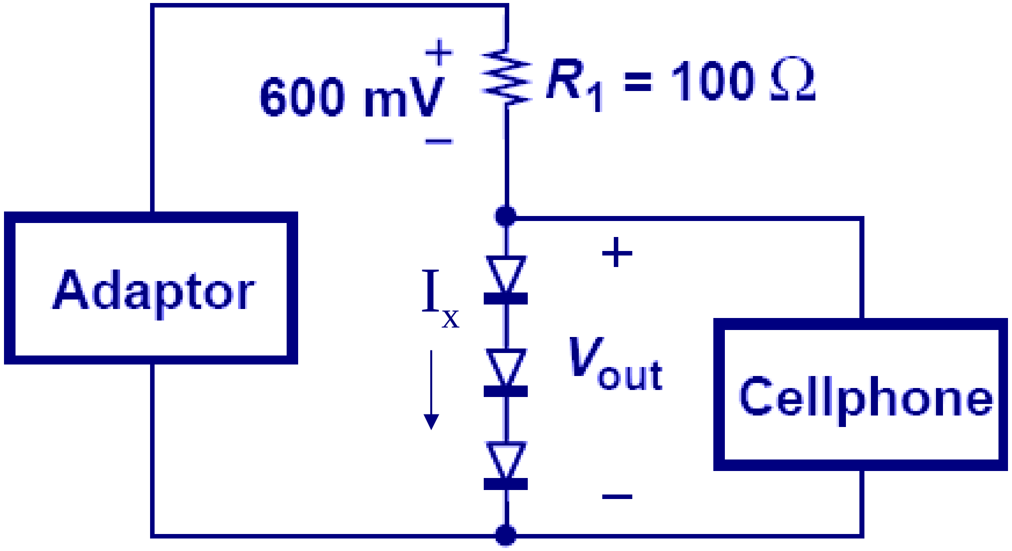
Another Constant-Voltage Model Example



(a) (b) (c) (d) (e) (f) (g) (h)

- **This example shows the importance of good initial guess and careful confirmation.**

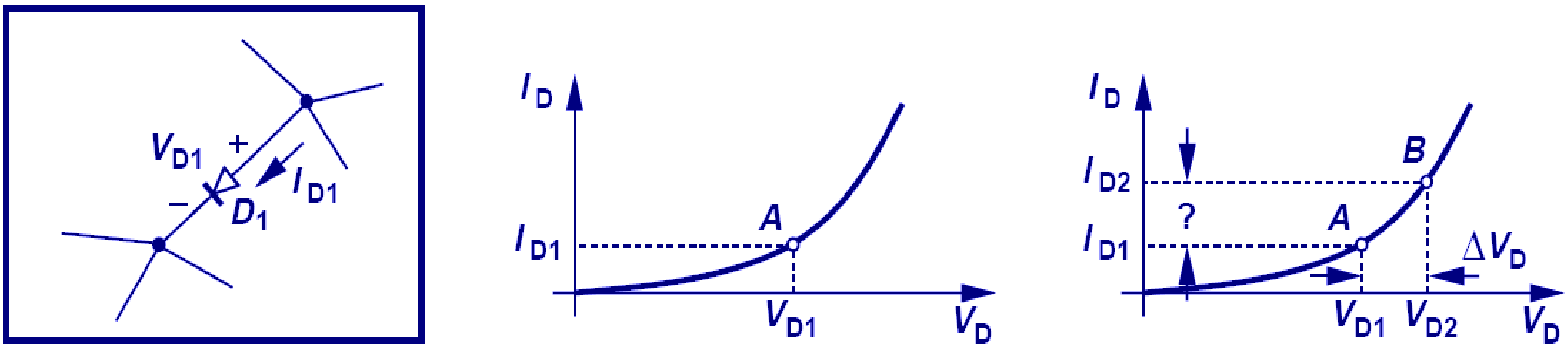
Cell Phone Adapter



$$V_{out} = 3V_D$$
$$= 3V_T \ln \frac{I_X}{I_s}$$

- $V_{out} = 3\ V_{D,on}$ **is used to charge cell phones.**
- **However, if Ix changes, iterative method is often needed to obtain a solution, thus motivating a simpler technique.**

Small-Signal Analysis

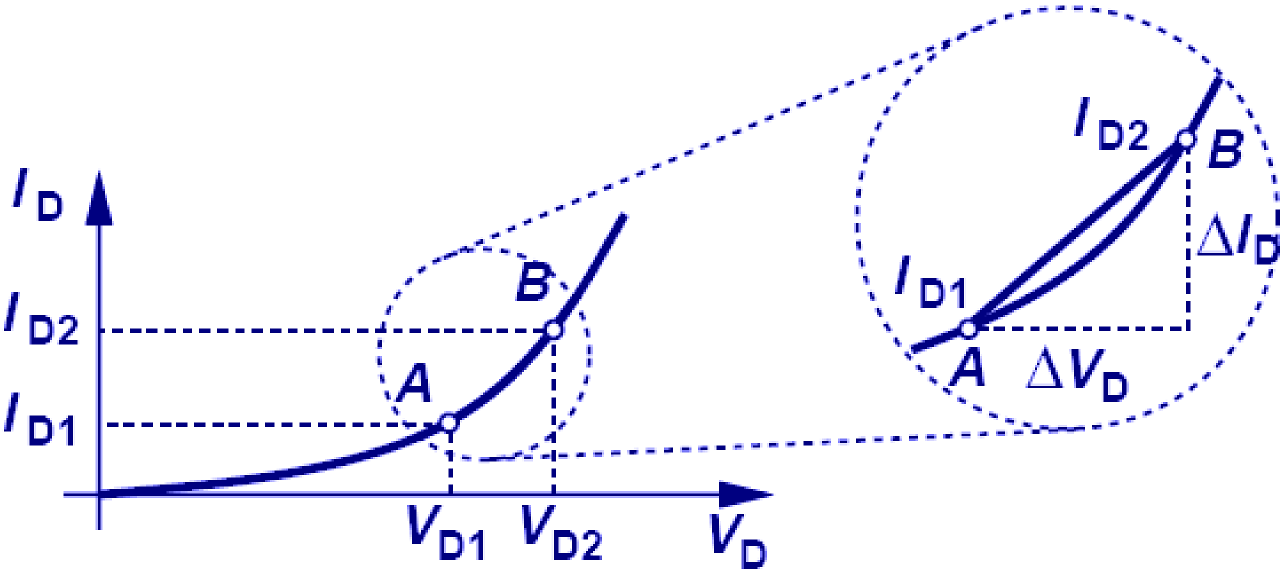


(a) (b) (c)

$$\Delta I_D = \frac{\Delta V}{V_T} I_{D1}$$

- **Small-signal analysis is performed around a bias point by perturbing the voltage by a small amount and observing the resulting linear current perturbation.**

Small-Signal Analysis in Detail



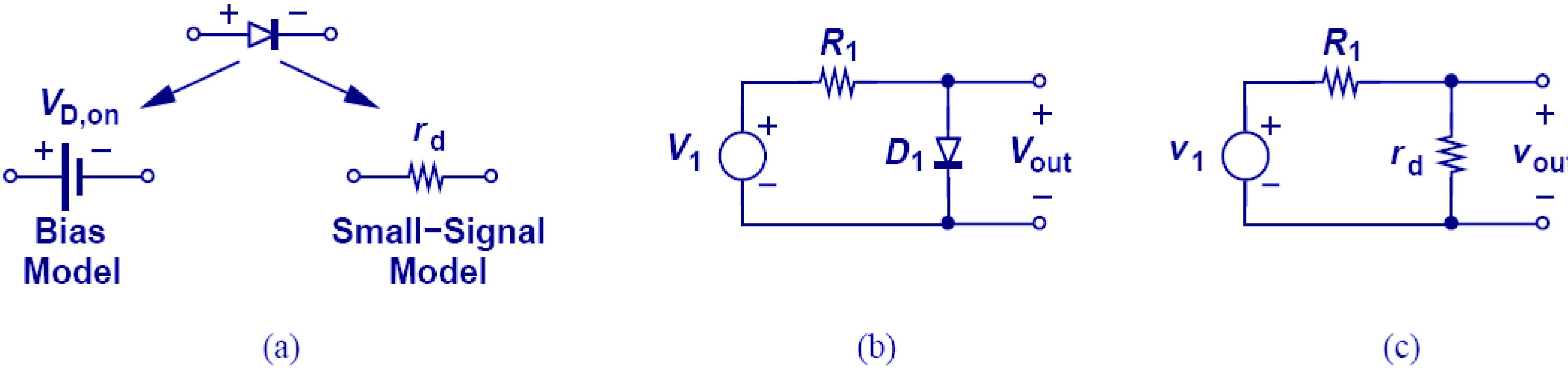
$$\frac{\Delta I_D}{\Delta V_D} = \frac{dI_D}{dV_D}\Big|_{VD=VD1}$$

$$= \frac{I_s}{V_T} \exp \frac{I_{D1}}{V_T}$$

$$= \frac{I_{D1}}{V_T}$$

- If two points on the IV curve of a diode are close enough, the trajectory connecting the first to the second point is like a line, with the slope being the proportionality factor between change in voltage and change in current.

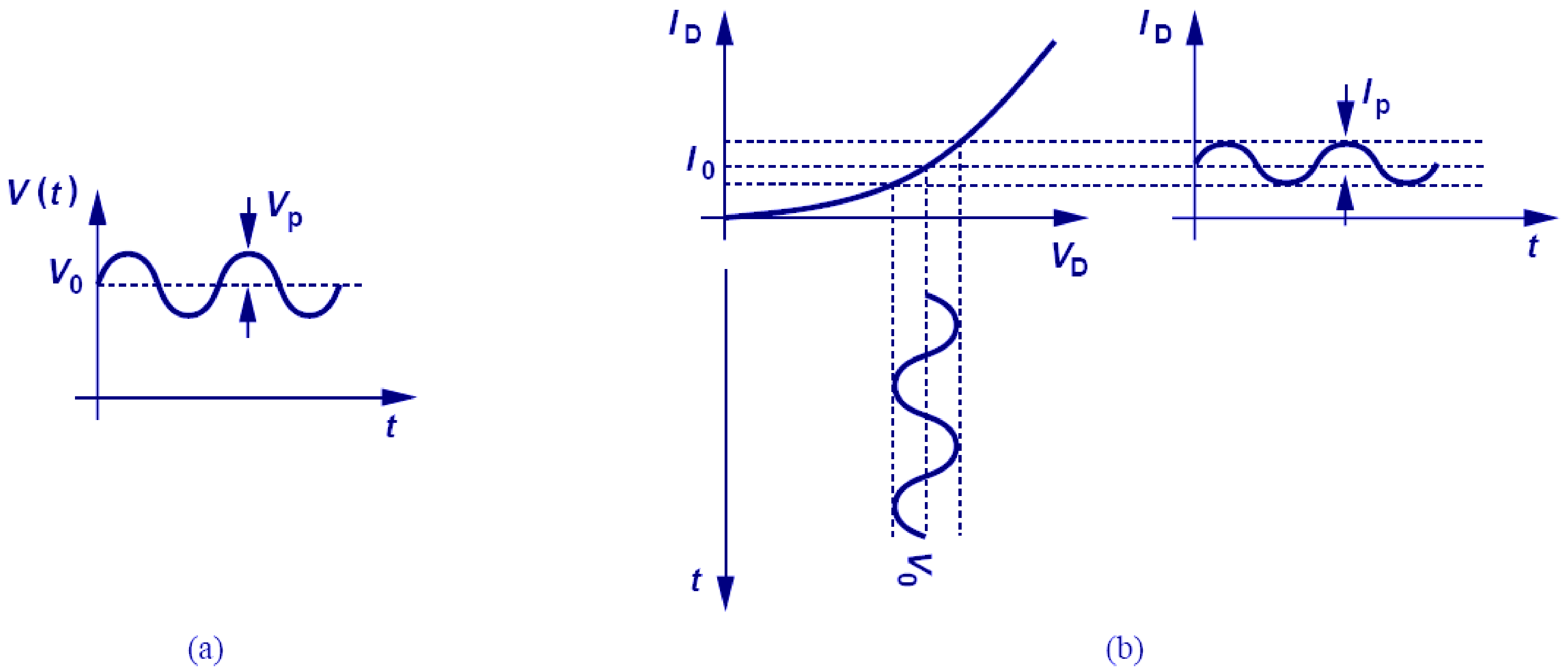
Small-Signal Incremental Resistance



$$r_d = \frac{V_T}{I_D}$$

- Since there's a linear relationship between the small signal current and voltage of a diode, the diode can be viewed as a linear resistor when only small changes are of interest.

Small Sinusoidal Analysis

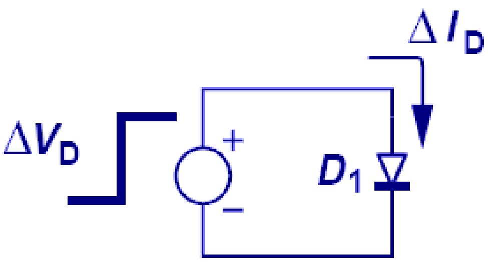


$$V(t) = V_0 + V_p \cos \omega t$$

$$I_D(t) = I_0 + I_p \cos \omega t = I_s \exp \frac{V_0}{V_T} + \frac{V_T}{I_0} V_p \cos \omega t$$

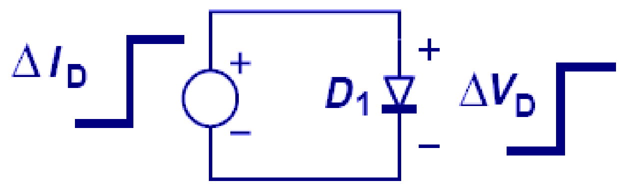
- **If a sinusoidal voltage with small amplitude is applied, the resulting current is also a small sinusoid around a DC value.**

Cause and Effect



(a)

$$\Delta I_D = \frac{\Delta V_D}{r_d} = \Delta V_D \frac{I_{D1}}{V_T}$$

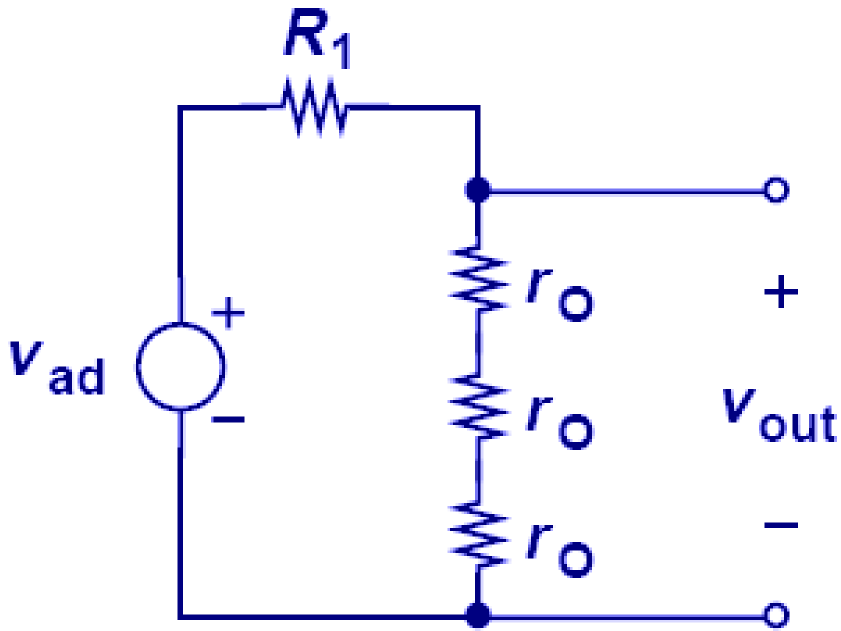


(b)

$$\Delta V_D = \Delta I_D\ r_d = \Delta I_D \frac{V_T}{I_{D1}}$$

- **In (a), voltage is the cause and current is the effect. In (b), the other way around.**

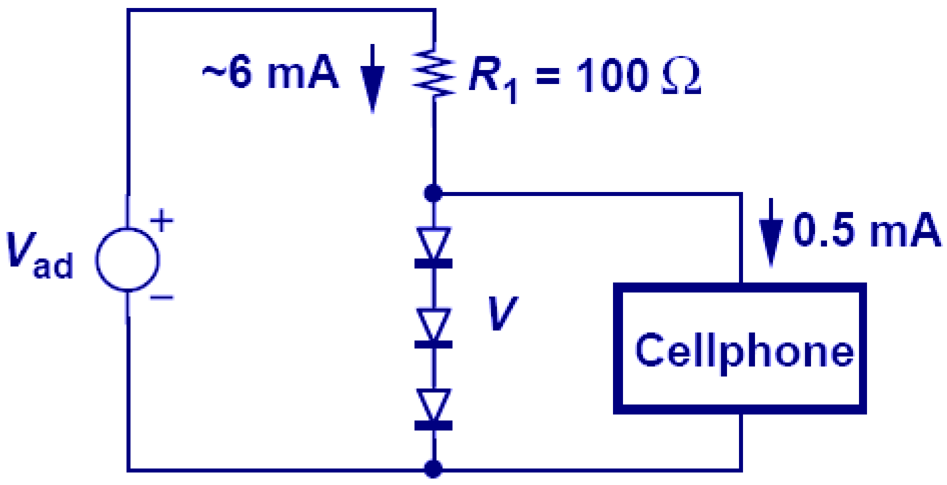
Adapter Example Revisited



$$v_{out} = \frac{3r_d}{R_1 + 3r_d} v_{ad}$$
$$= 11.5mV$$

- With our understanding of small-signal analysis, we can revisit our cell phone charger example and easily solve it with just algebra instead of iterations.

Simple is Beautiful



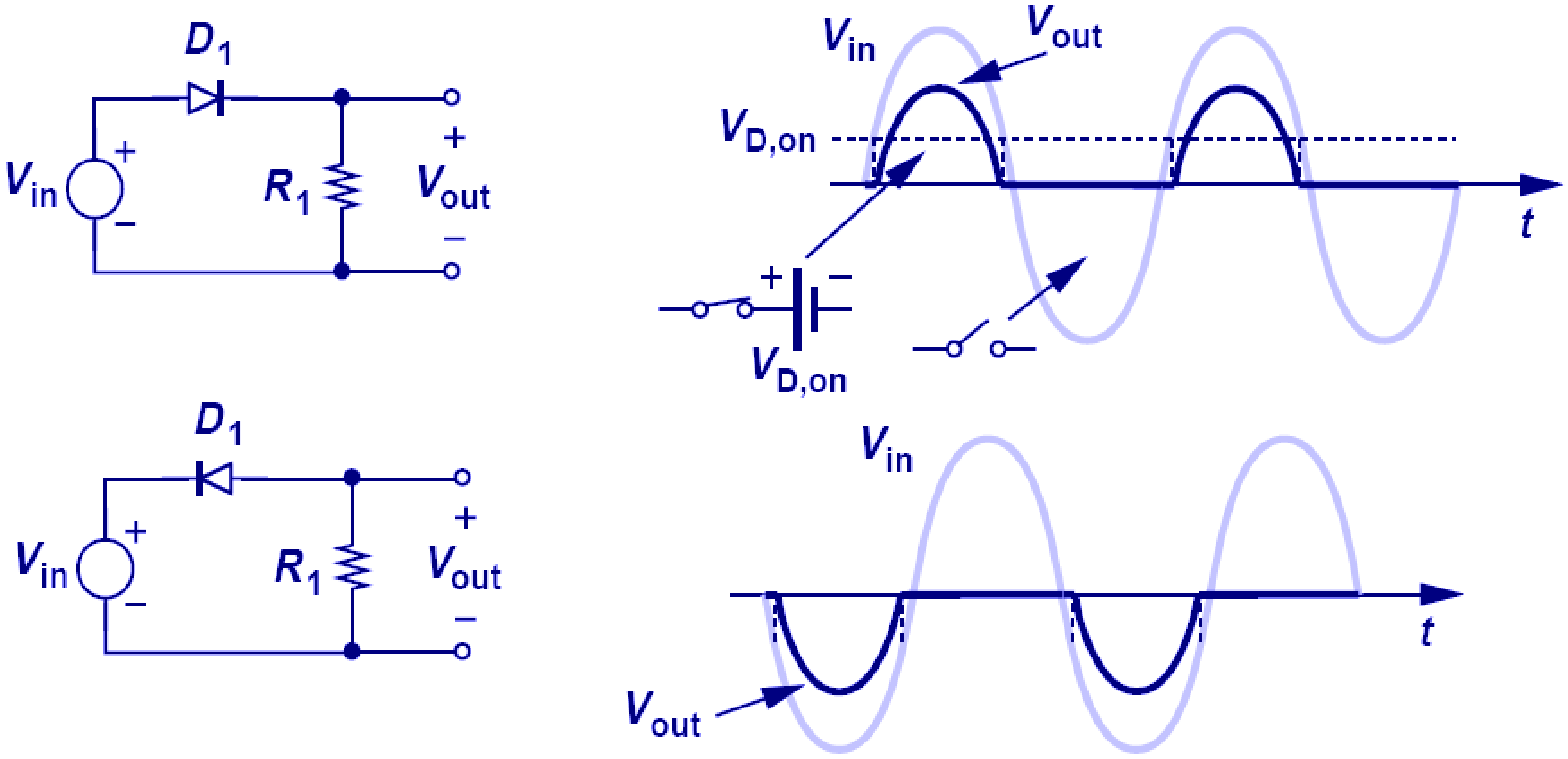
$$
\begin{aligned}
\Delta V_{out} &= \Delta I_D \cdot (3r_d) \\
&= 0.5mA(3 \times 4.33\Omega) \\
&= 6.5mV
\end{aligned}
$$

- **In this example we study the effect of cell phone pulling some current from the diodes. Using small signal analysis, this is easily done. However, imagine the nightmare, if we were to solve it using non-linear equations.**

Applications of Diode

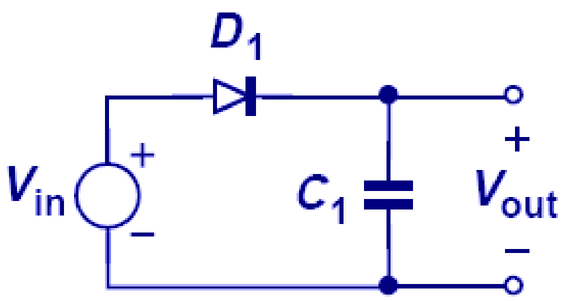
Half-Wave and Full-Wave rectifiers ⇨ Limiting Circuits ⇨ Clamping Circuits ⇨ Regulators ⇨ Voltage Doublers

Half-Wave Rectifier

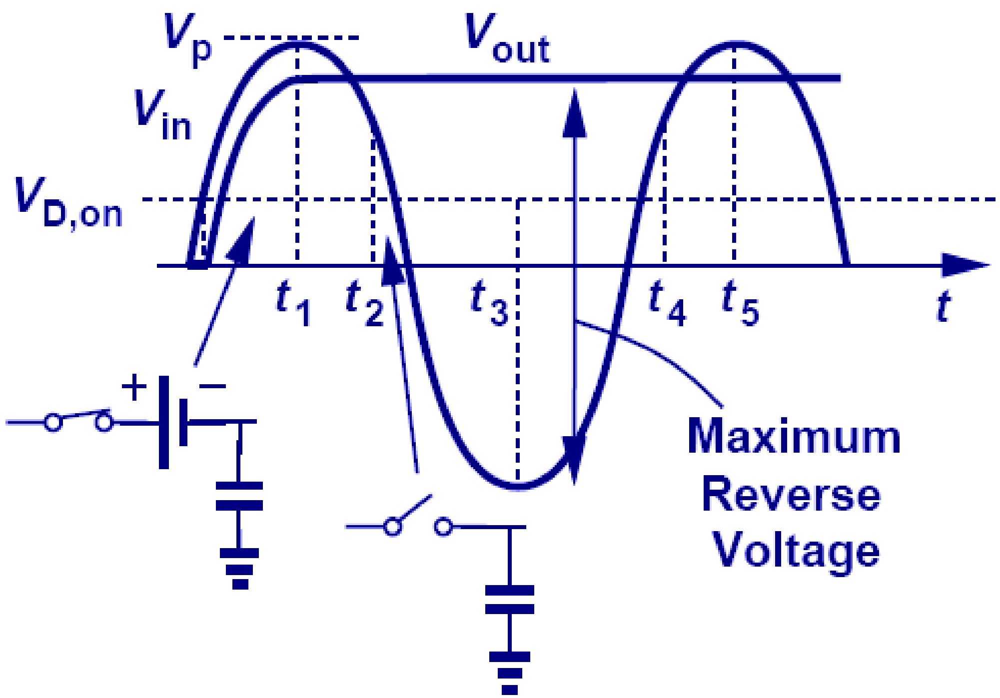


- **A very common application of diodes is half-wave rectification, where either the positive or negative half of the input is blocked.**
- **But, how do we generate a *constant* output?**

Diode-Capacitor Circuit: Constant Voltage Model



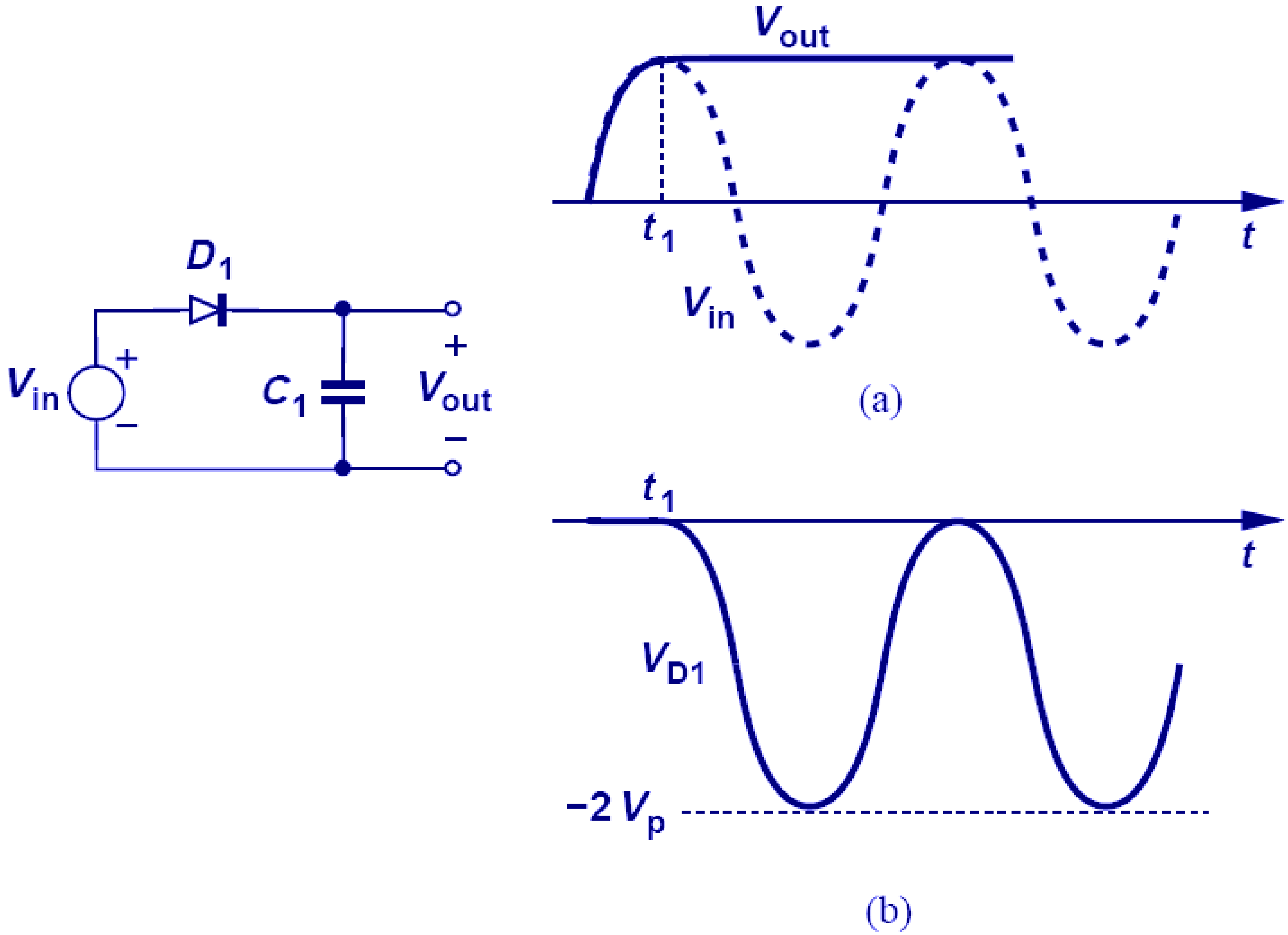
(a)



(b)

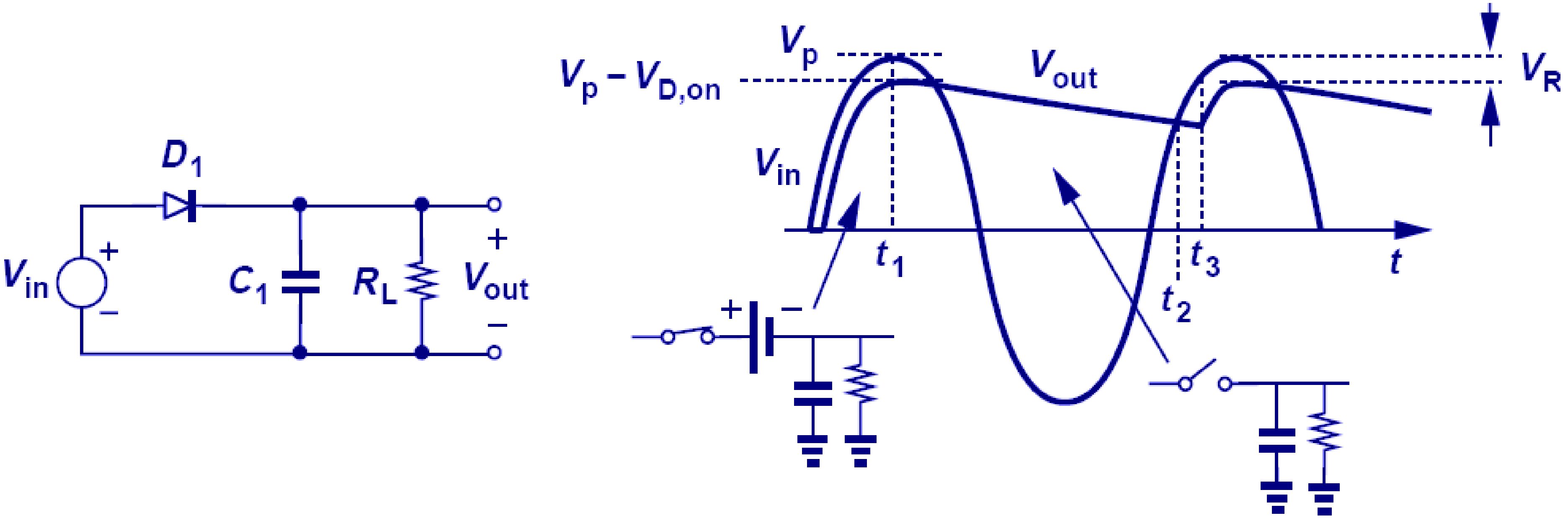
- If the resistor in half-wave rectifier is replaced by a capacitor, a fixed voltage output is obtained since the capacitor (assumed ideal) has no path to discharge.

Diode-Capacitor Circuit: Ideal Model



- Note that (b) is just like $V_{in,}$ only shifted down.

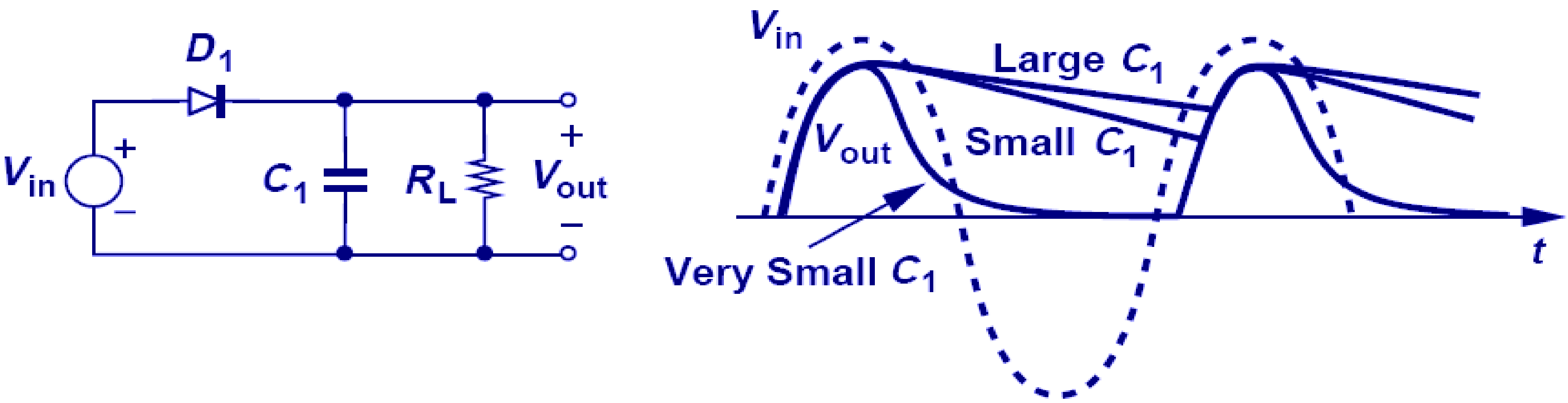
Diode-Capacitor With Load Resistor



(a) (b)

- **A path is available for capacitor to discharge. Therefore, V_{out} will not be constant and a ripple exists.**

Behavior for Different Capacitor Values



- **For large C_1, V_{out} has small ripple.**

Peak to Peak amplitude of Ripple

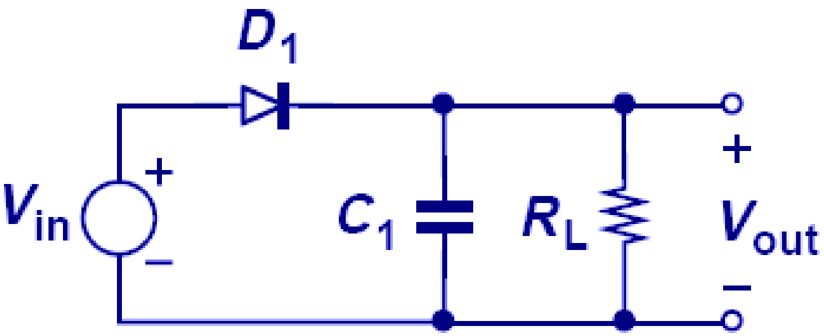
$$V_{out}(t) = (V_p - V_{D,on})\exp\frac{-t}{R_L C_1} \qquad 0 \le t \le T_{in}$$

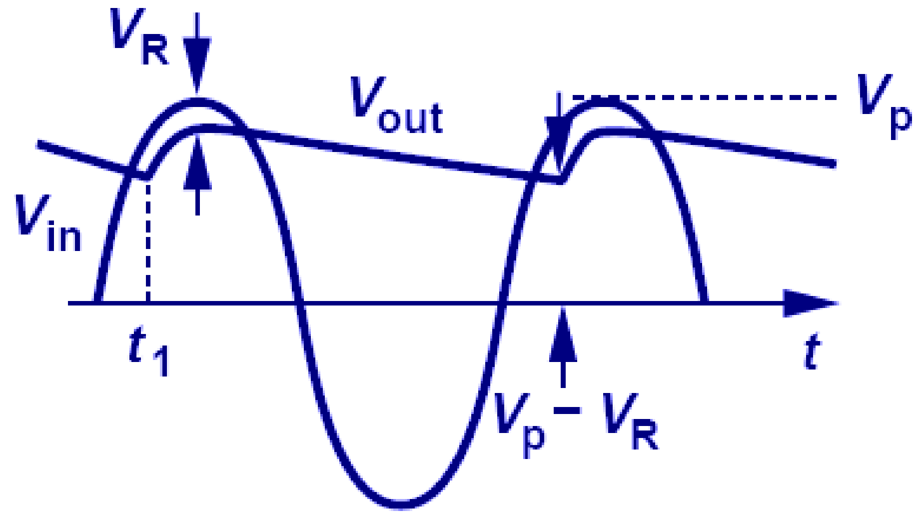
$$V_{out}(t) \approx (V_p - V_{D,on})(1 - \frac{t}{R_L C_1}) \approx (V_p - V_{D,on}) - \frac{V_p - V_{D,on}}{R_L}\frac{t}{C_1}$$

$$V_R \approx \frac{V_p - V_{D,on}}{R_L} \cdot \frac{T_{in}}{C_1} \approx \frac{V_p - V_{D,on}}{R_L C_1 f_{in}}$$

- **The ripple amplitude is the decaying part of the exponential.**
- **Ripple voltage becomes a problem if it goes above 5 to 10% of the output voltage.**

Maximum Diode Current

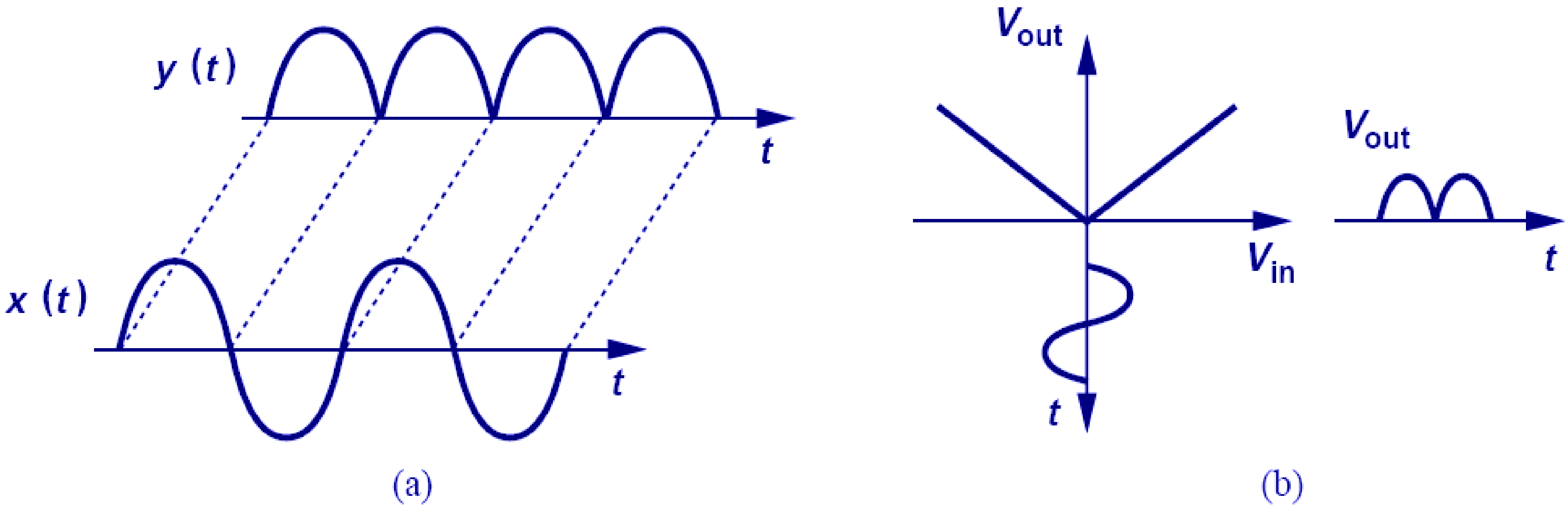




$$I_p \approx C_1 \omega_{in} V_p \sqrt{\frac{2V_R}{V_p}} + \frac{V_p}{R_L} \approx \frac{V_p}{R_L}\left(R_L C_1 \omega_{in} \sqrt{\frac{2V_R}{V_p}} + 1\right)$$

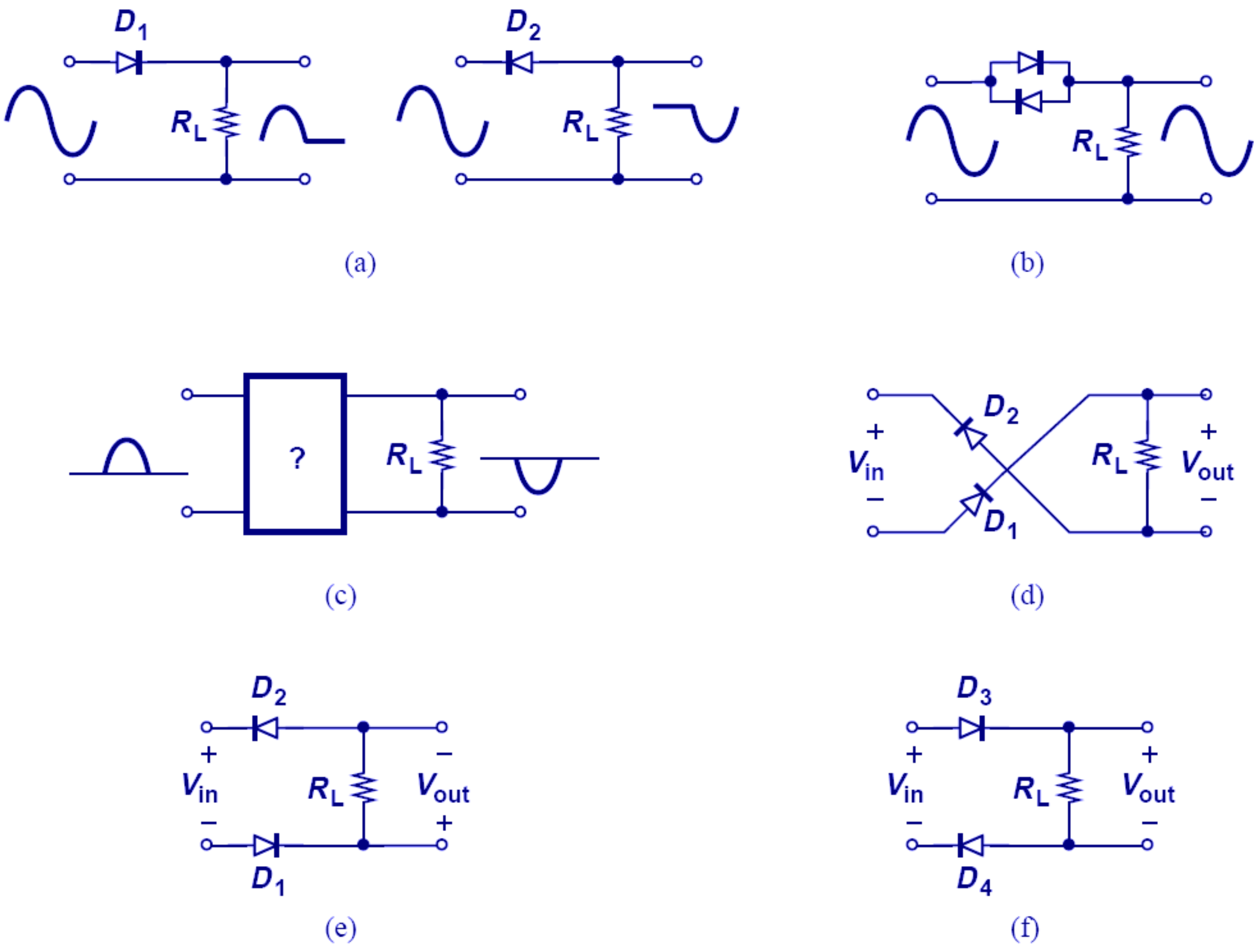
- **The diode has its maximum current at t_1, since that's when the slope of V_{out} is the greatest.**
- **This current has to be carefully controlled so it does not damage the device.**

Full-Wave Rectifier



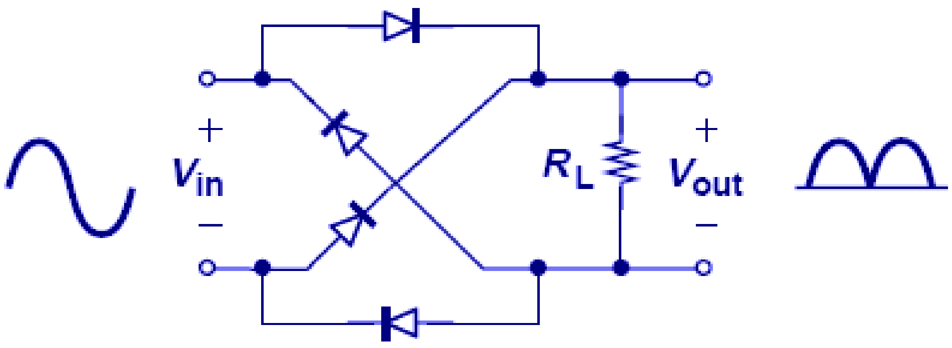
- A full-wave rectifier passes both the negative and positive half cycles of the input, while inverting the negative half of the input.
- As proved later, a full-wave rectifier reduces the ripple by a factor of two.

The Evolution of Full-Wave Rectifier

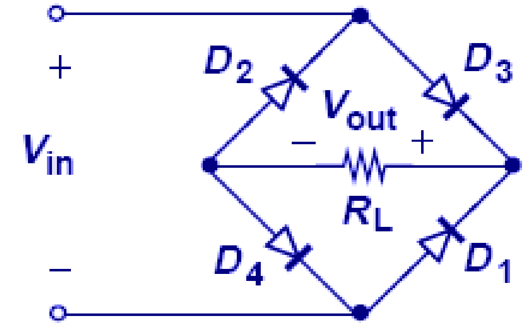


- **Figures (e) and (f) show the topology that inverts the negative half cycle of the input.**

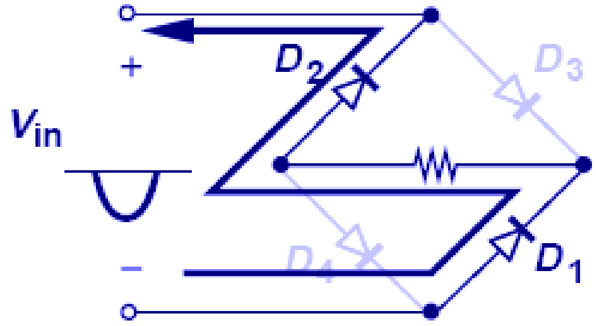
Full-Wave Rectifier: Bridge Rectifier



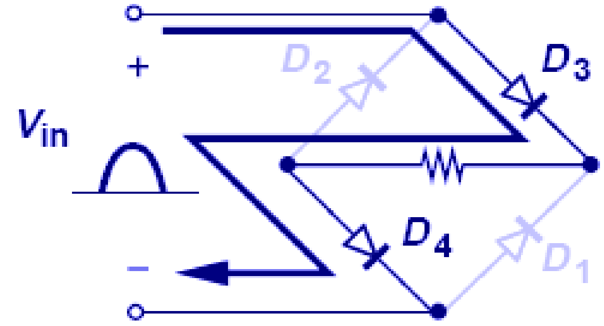
(a)



(b)



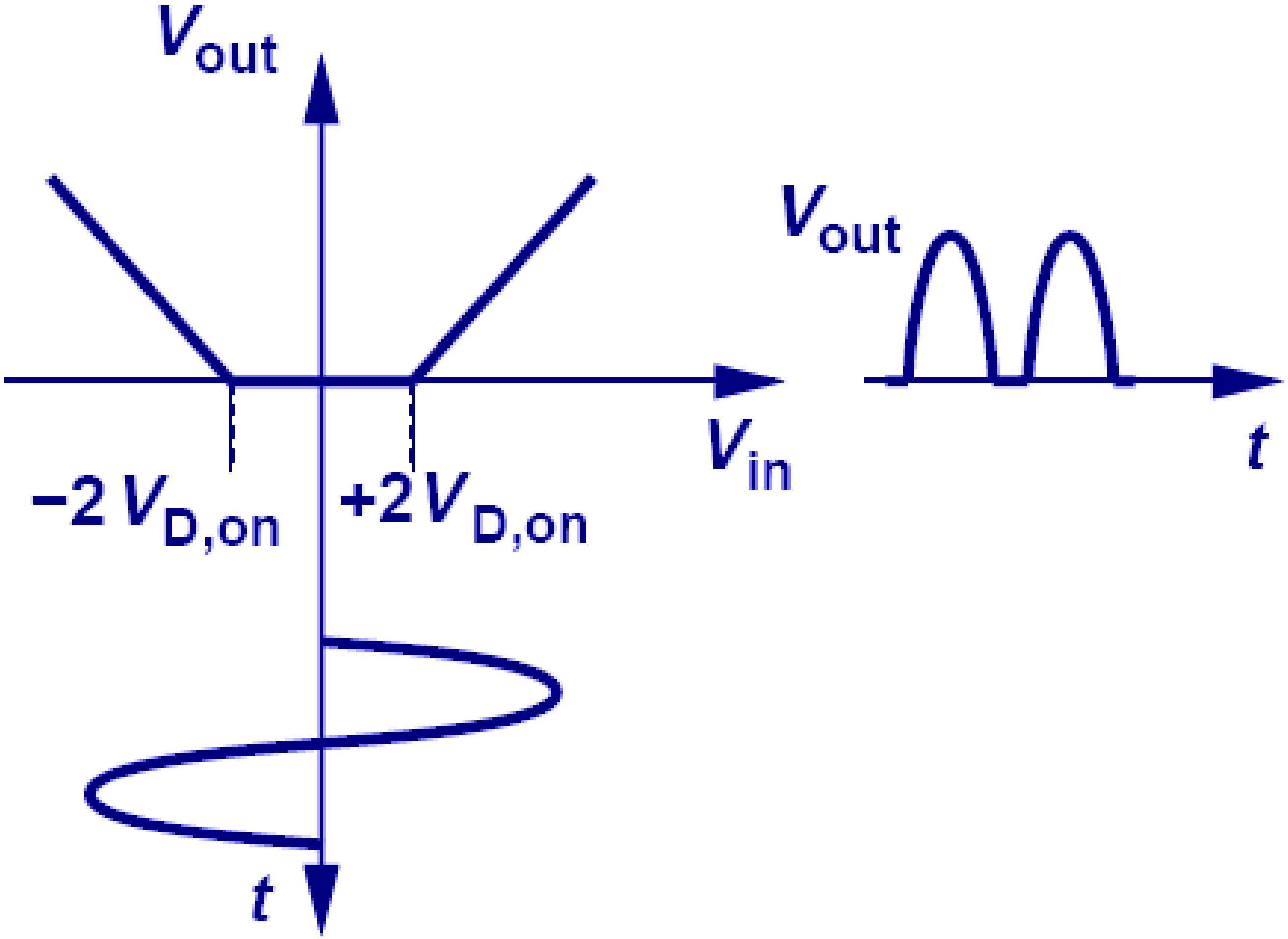
(c)



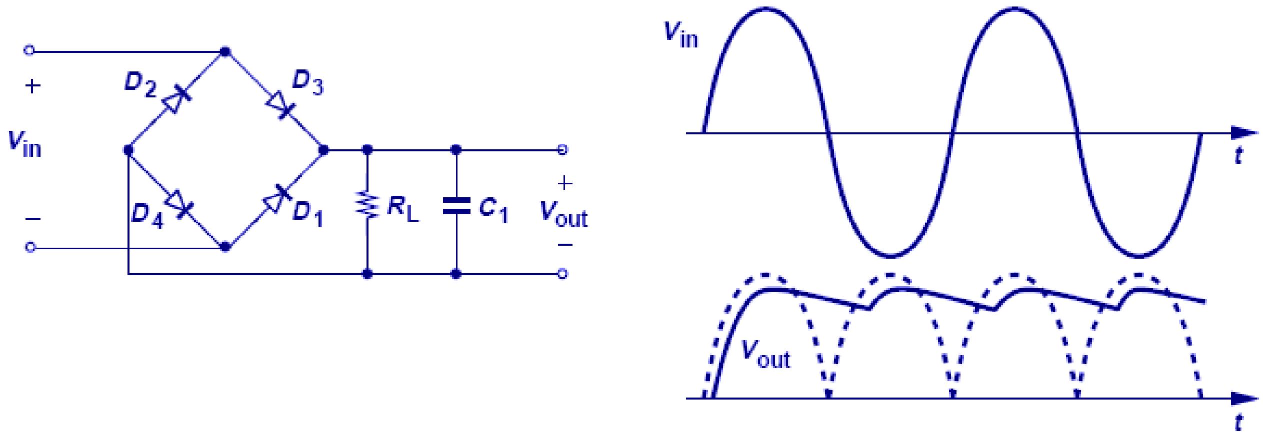
(d)

- The figure above shows a full-wave rectifier, where D_1 and D_2 pass/invert the negative half cycle of input and D_3 and D_4 pass the positive half cycle.

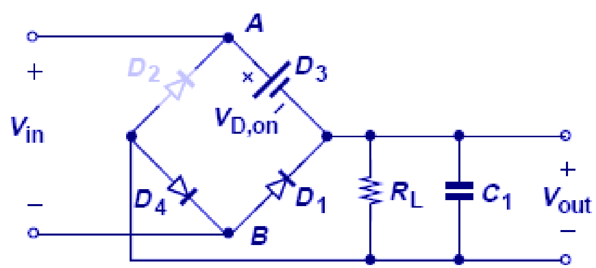
Input/Output Characteristics of a Full-Wave Rectifier (Constant-Voltage Model)



- **The dead-zone around V_{in} arises because V_{in} must exceed 2 $V_{D,ON}$ to turn on the bridge.**



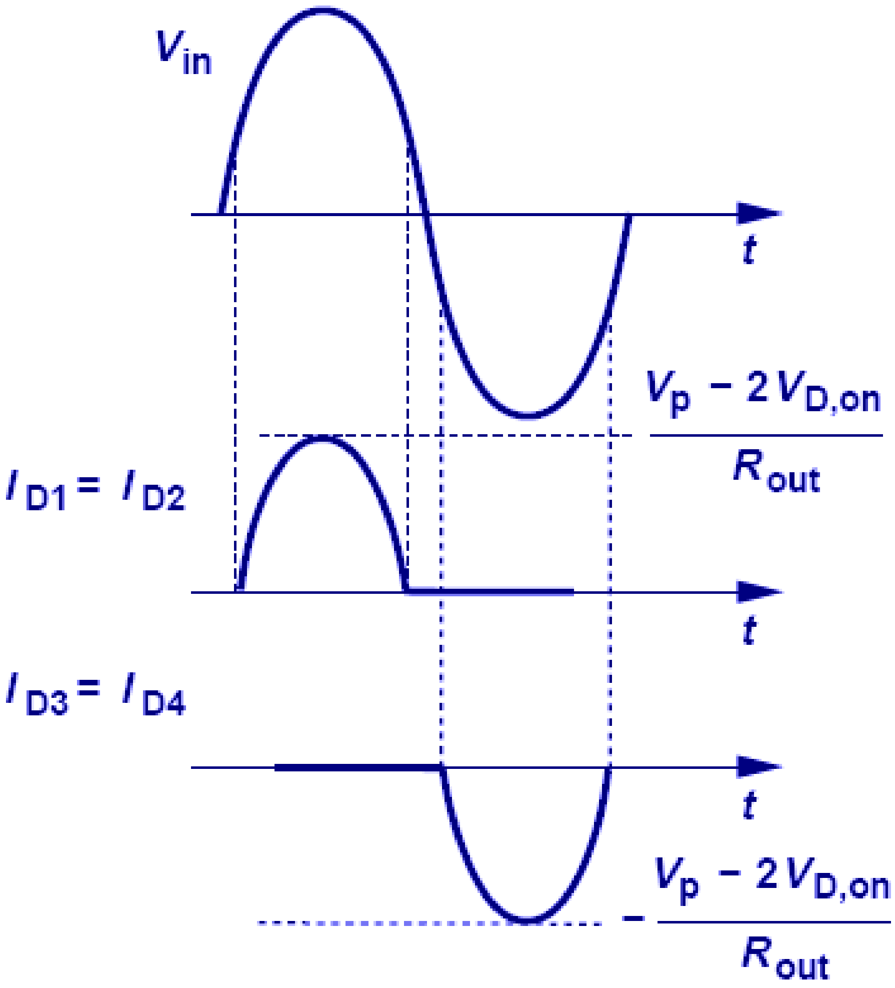
(a)



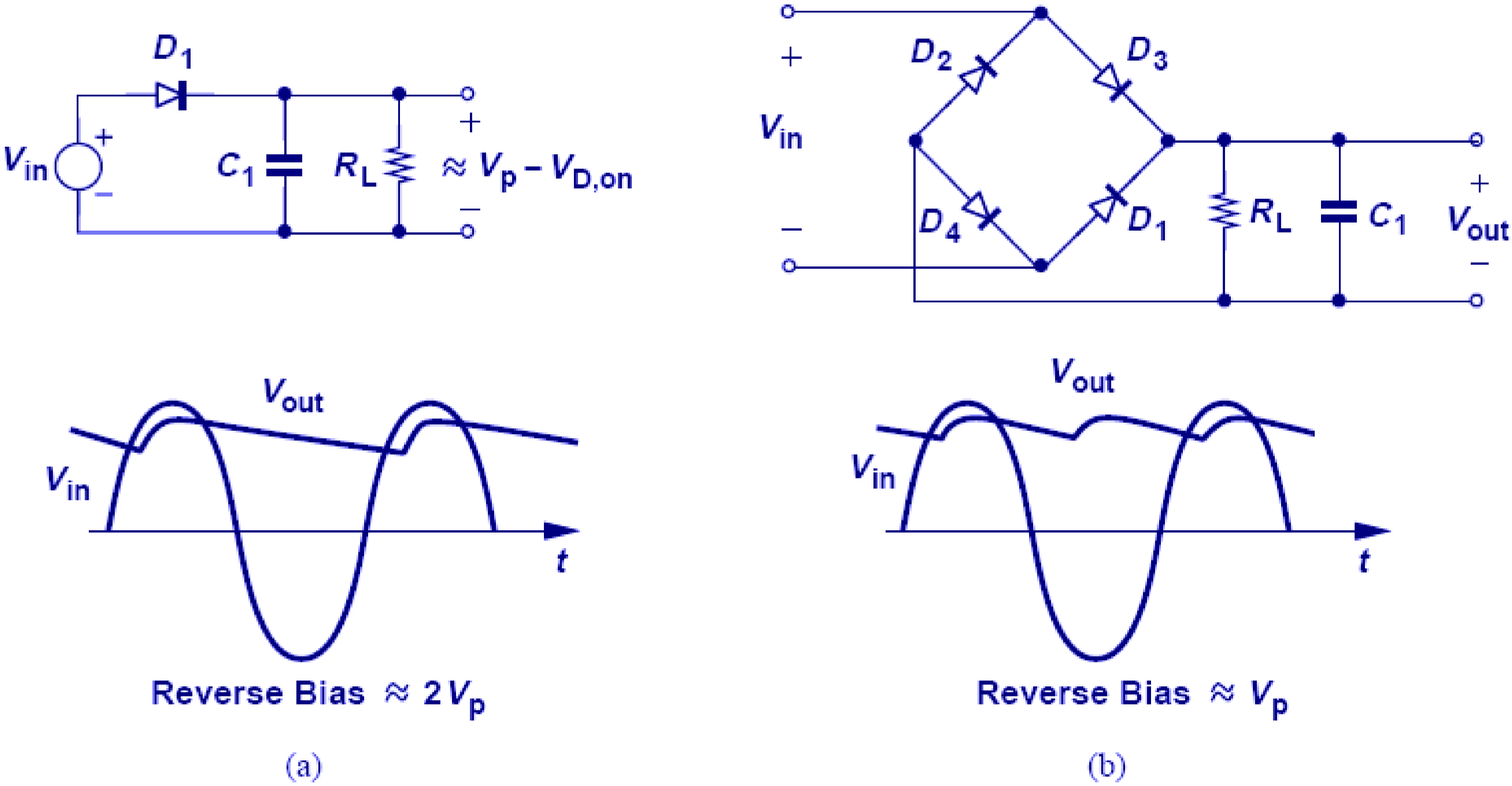
(b)

- Since C_1 only gets ½ of period to discharge, ripple voltage is decreased by a factor of 2. Also (b) shows that each diode is subjected to approximately one V_p reverse bias drop (versus $2V_p$ in half-wave rectifier).

Current Carried by Each Diode in the Full-Wave Rectifier

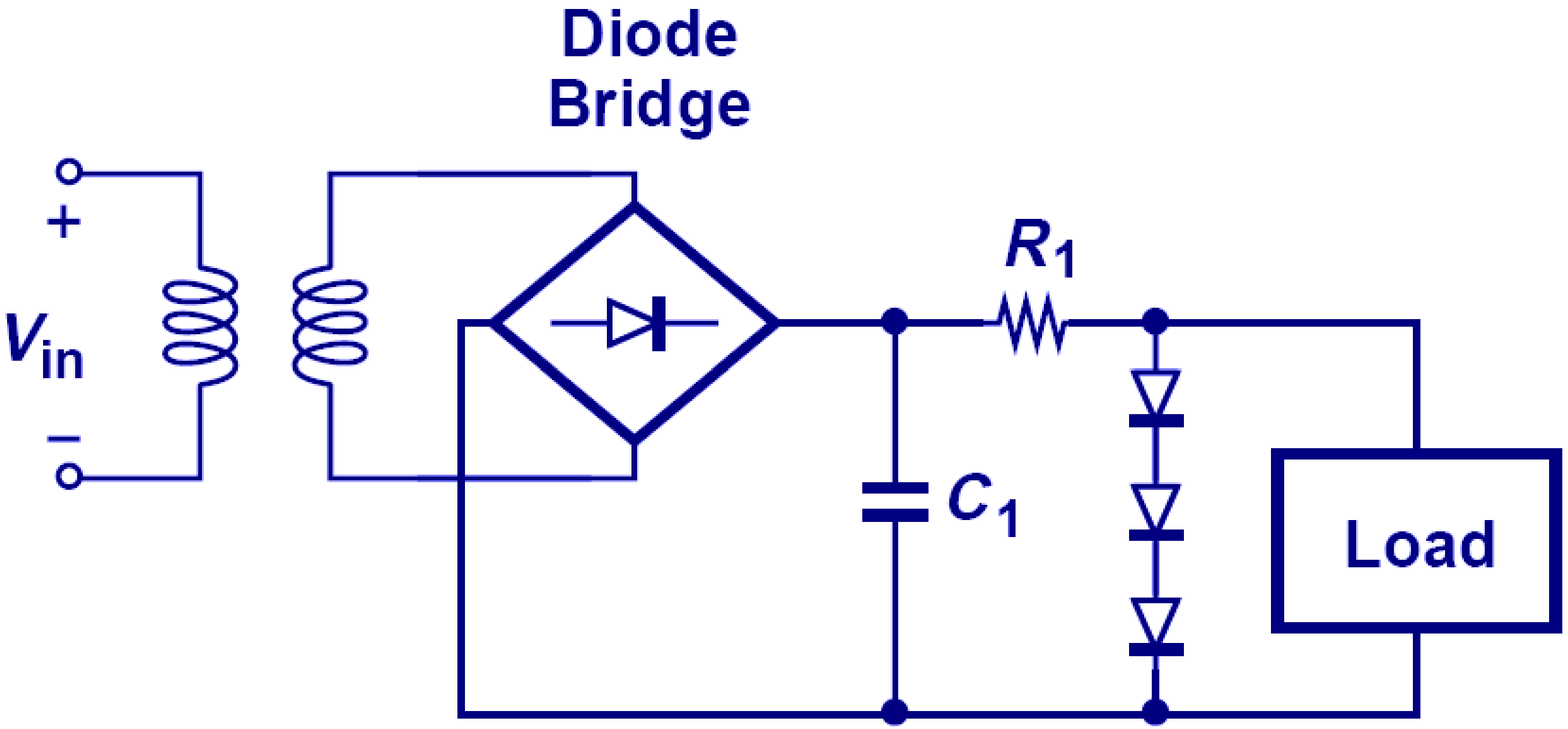


Summary of Half and Full-Wave Rectifiers



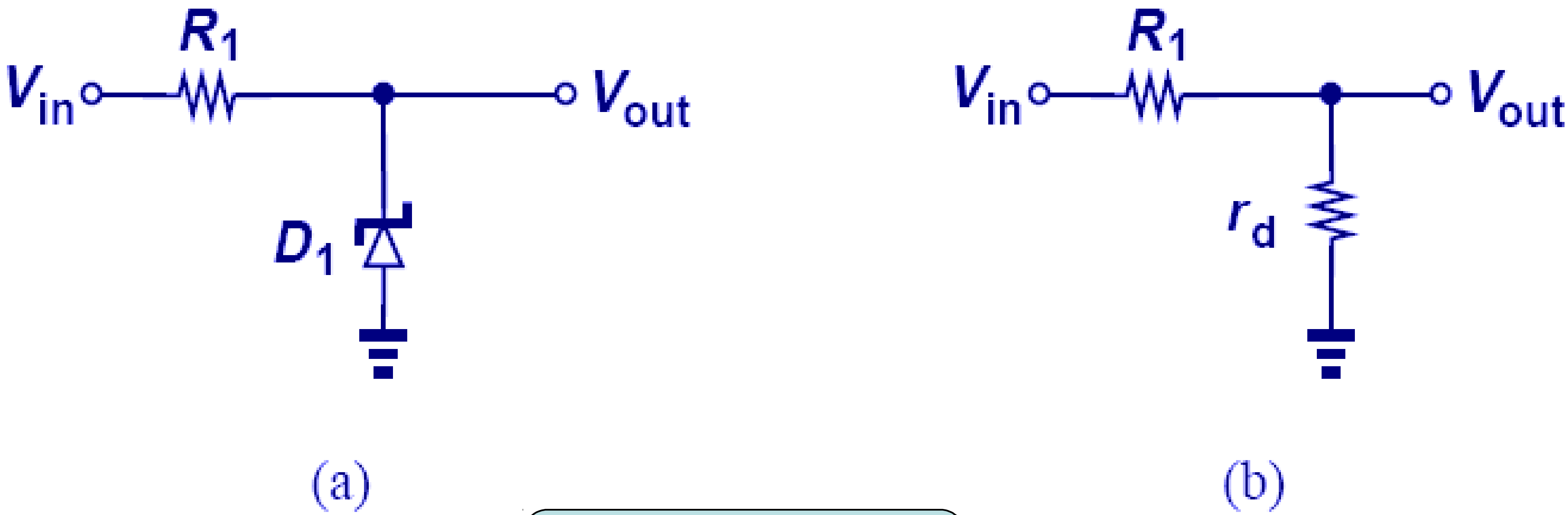
- **Full-wave rectifier is more suited to adapter and charger applications.**

Voltage Regulator



- The ripple created by the rectifier can be unacceptable to sensitive load; therefore, a regulator is required to obtain a very stable output.
- Three diodes operate as a primitive regulator.

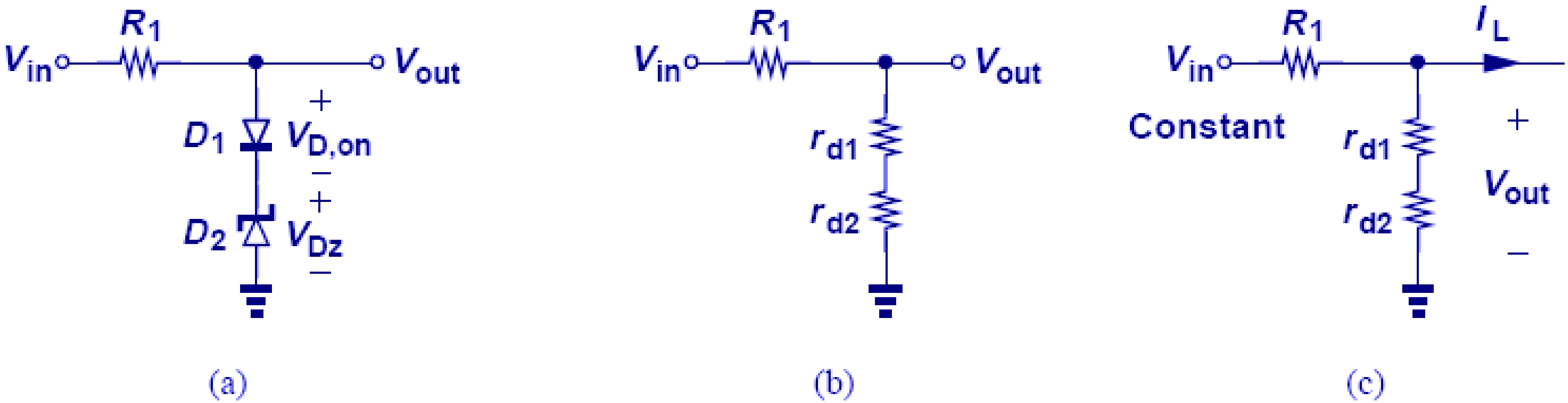
Voltage Regulation With Zener Diode



$$V_{out} = \frac{r_D}{r_D + R_1} V_{in}$$

- Voltage regulation can be accomplished with Zener diode. Since r_d is small, large change in the input will not be reflected at the output.

Line Regulation VS. Load Regulation

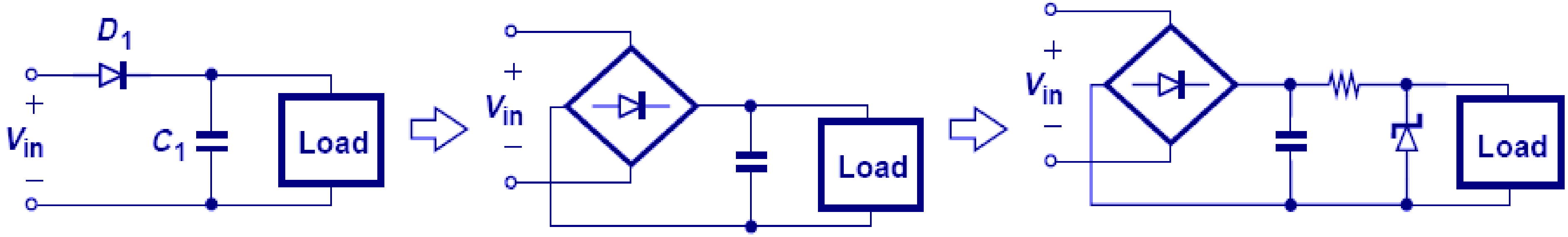


$$\frac{V_{out}}{V_{in}} = \frac{r_{D1} + r_{D2}}{r_{D1} + r_{D2} + R_1}$$

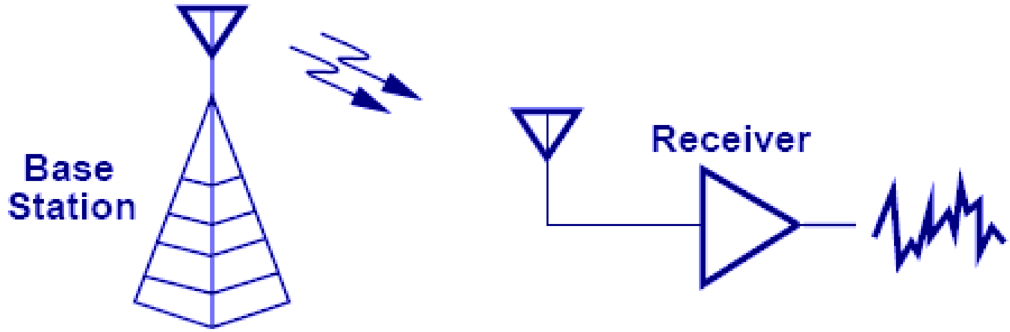
$$\left|\frac{V_{out}}{I_L}\right| = (r_{D1} + r_{D2}) \| R_1$$

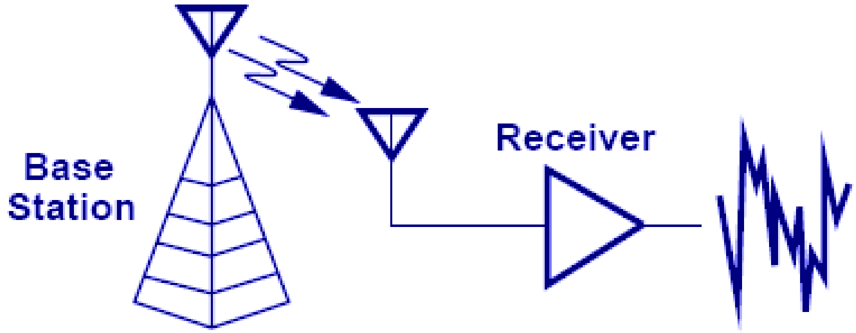
- Line regulation is the suppression of change in V_{out} due to change in V_{in} (b).
- Load regulation is the suppression of change in V_{out} due to change in load current (c).

Evolution of AC-DC Converter



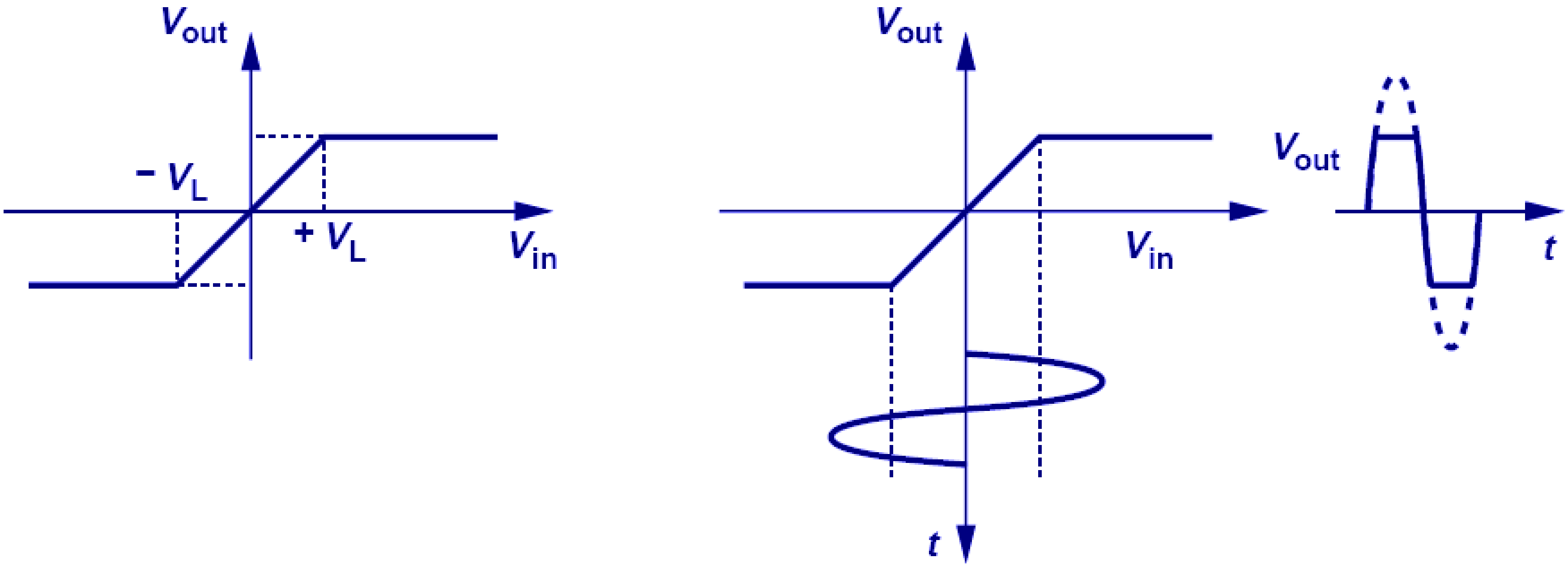
Limiting Circuits





- The motivation of having limiting circuits is to keep the signal below a threshold so it will not saturate the entire circuitry.
- When a receiver is close to a base station, signals are large and limiting circuits may be required.

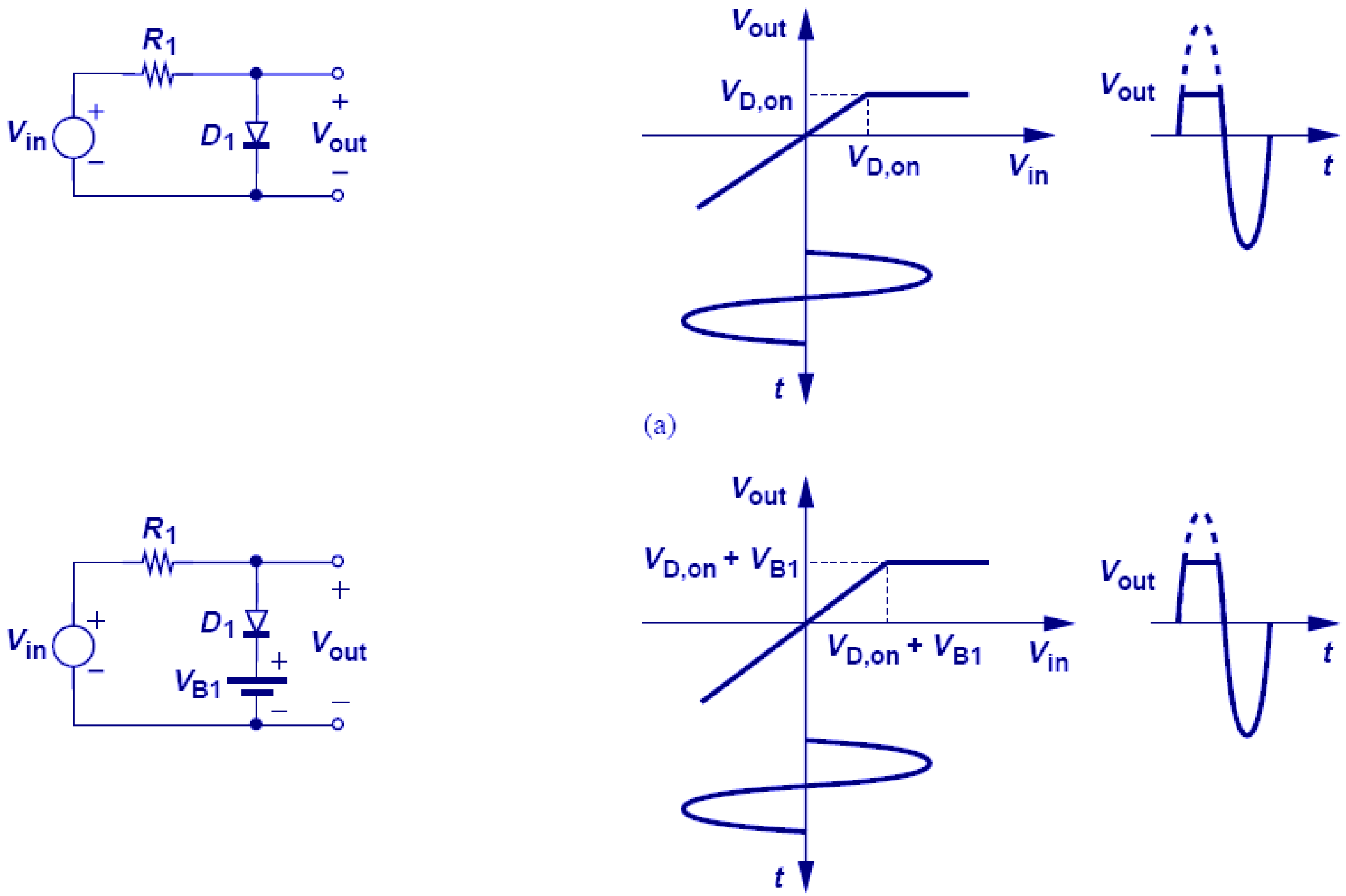
Input/Output Characteristics



(a) (b)

- **Note the clipping of the output voltage.**

Limiting Circuit Using a Diode: Positive Cycle Clipping

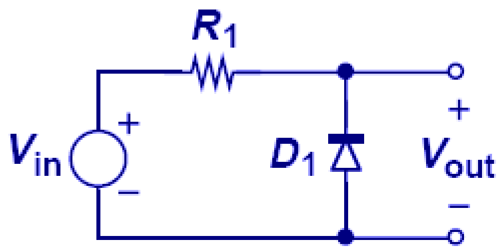


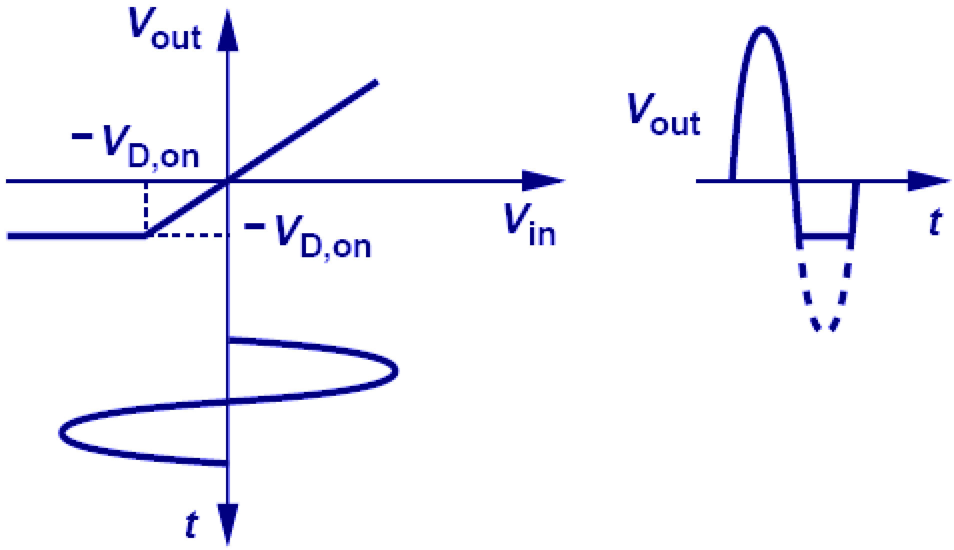
(a)

(b)

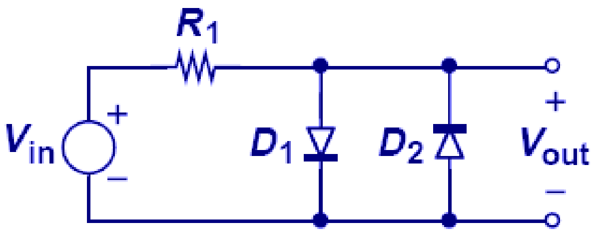
- As was studied in the past, the combination of resistor-diode creates limiting effect.

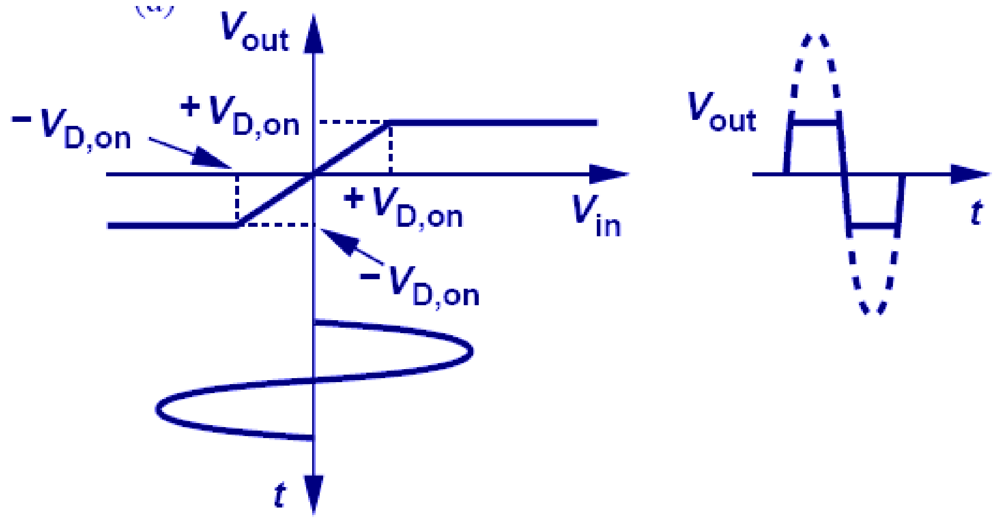
Limiting Circuit Using a Diode: Negative Cycle Clipping



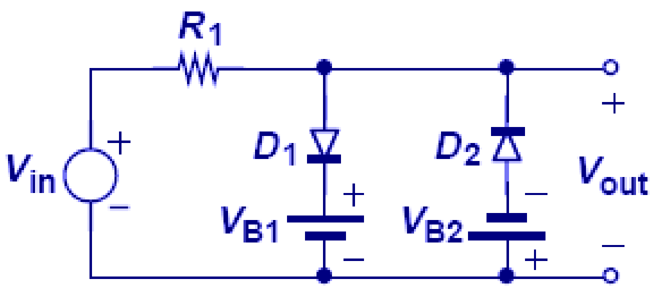


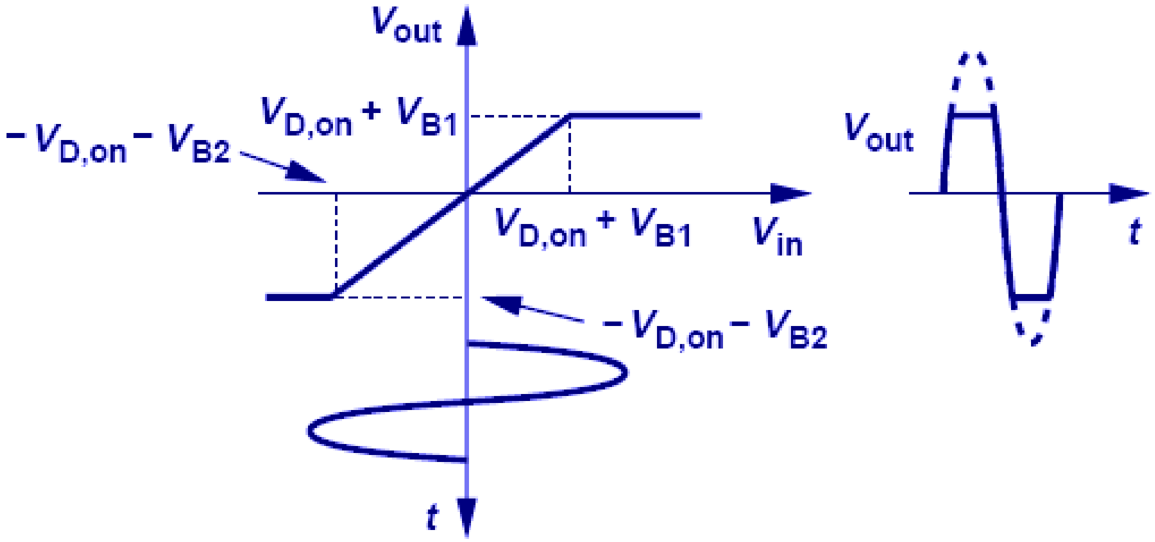
Limiting Circuit Using a Diode: Positive and Negative Cycle Clipping





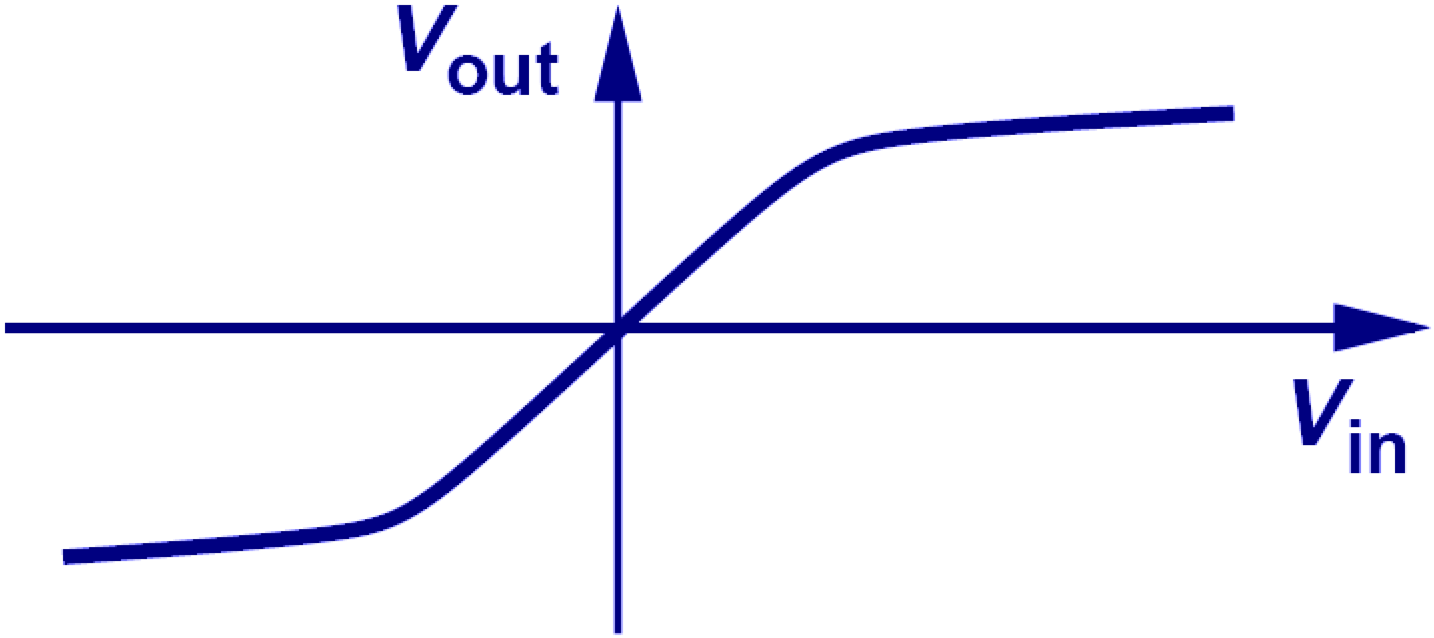
General Voltage Limiting Circuit





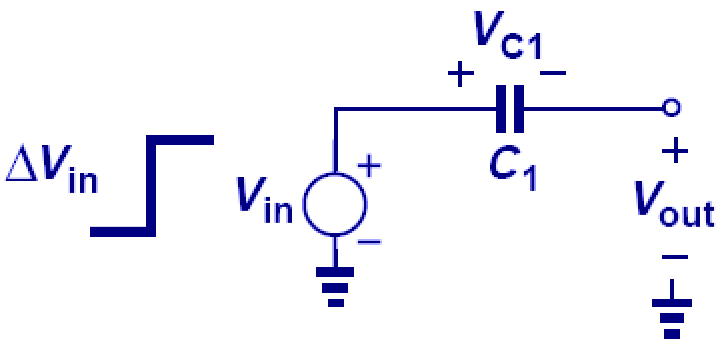
- **Two batteries in series with the antiparalle diodes control the limiting voltages.**

Non-idealities in Limiting Circuits

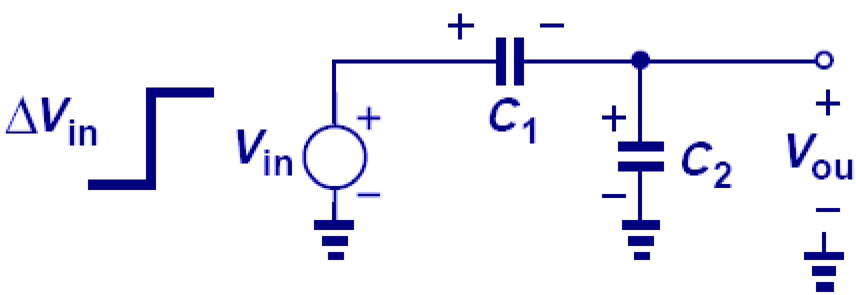


- The clipping region is not exactly flat since as Vin increases, the currents through diodes change, and so does the voltage drop.

Capacitive Divider



(a)

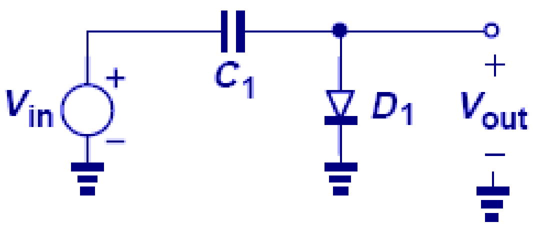


(b)

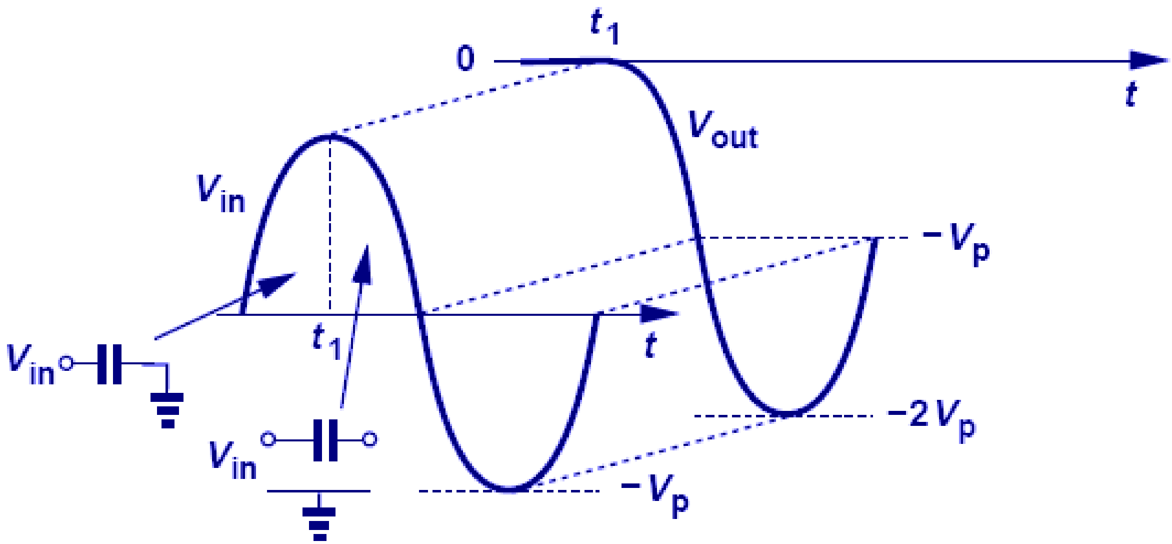
$$\Delta V_{out} = \Delta V_{in}$$

$$\Delta V_{out} = \frac{C_1}{C_1 + C_2} \Delta V_{in}$$

Waveform Shifter: Peak at -2Vp



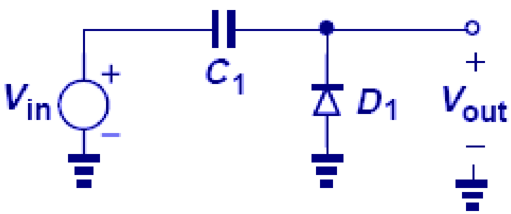
(a)



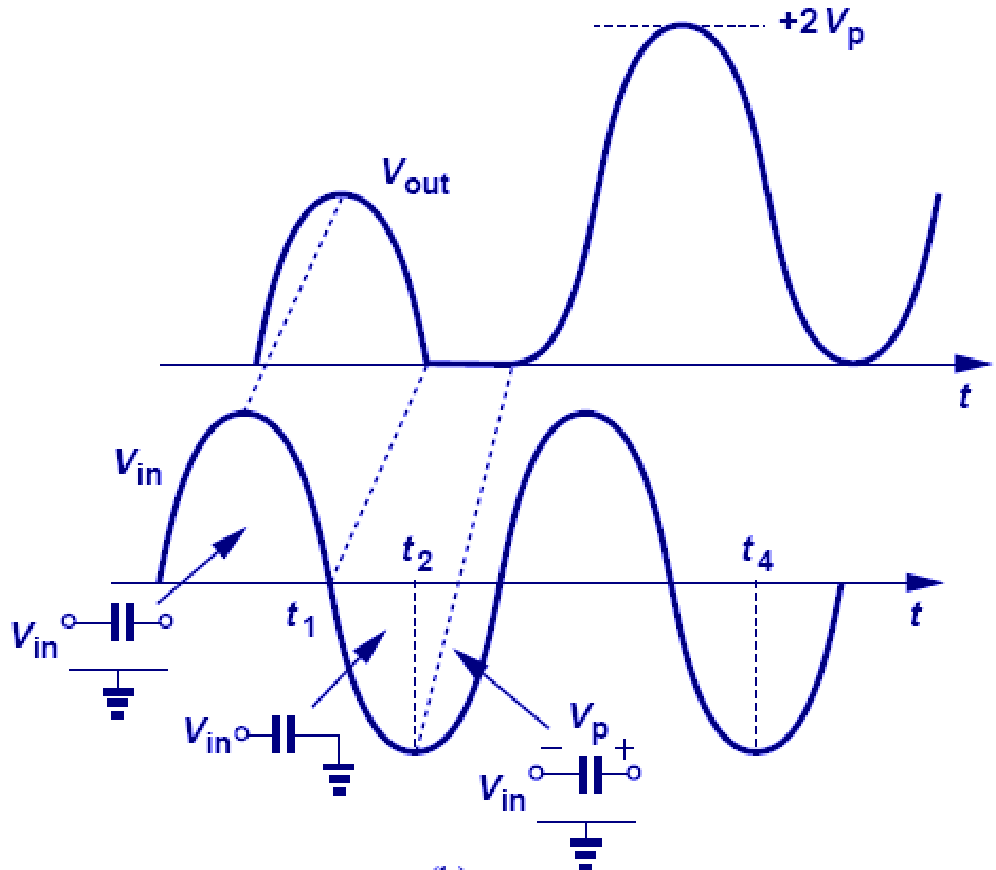
(b)

- As V_{in} increases, D_1 turns on and V_{out} is zero.
- As V_{in} decreases, D_1 turns off, and V_{out} drops with V_{in} from zero. The lowest V_{out} can go is $-2V_p$, doubling the voltage.

Waveform Shifter: Peak at 2Vp



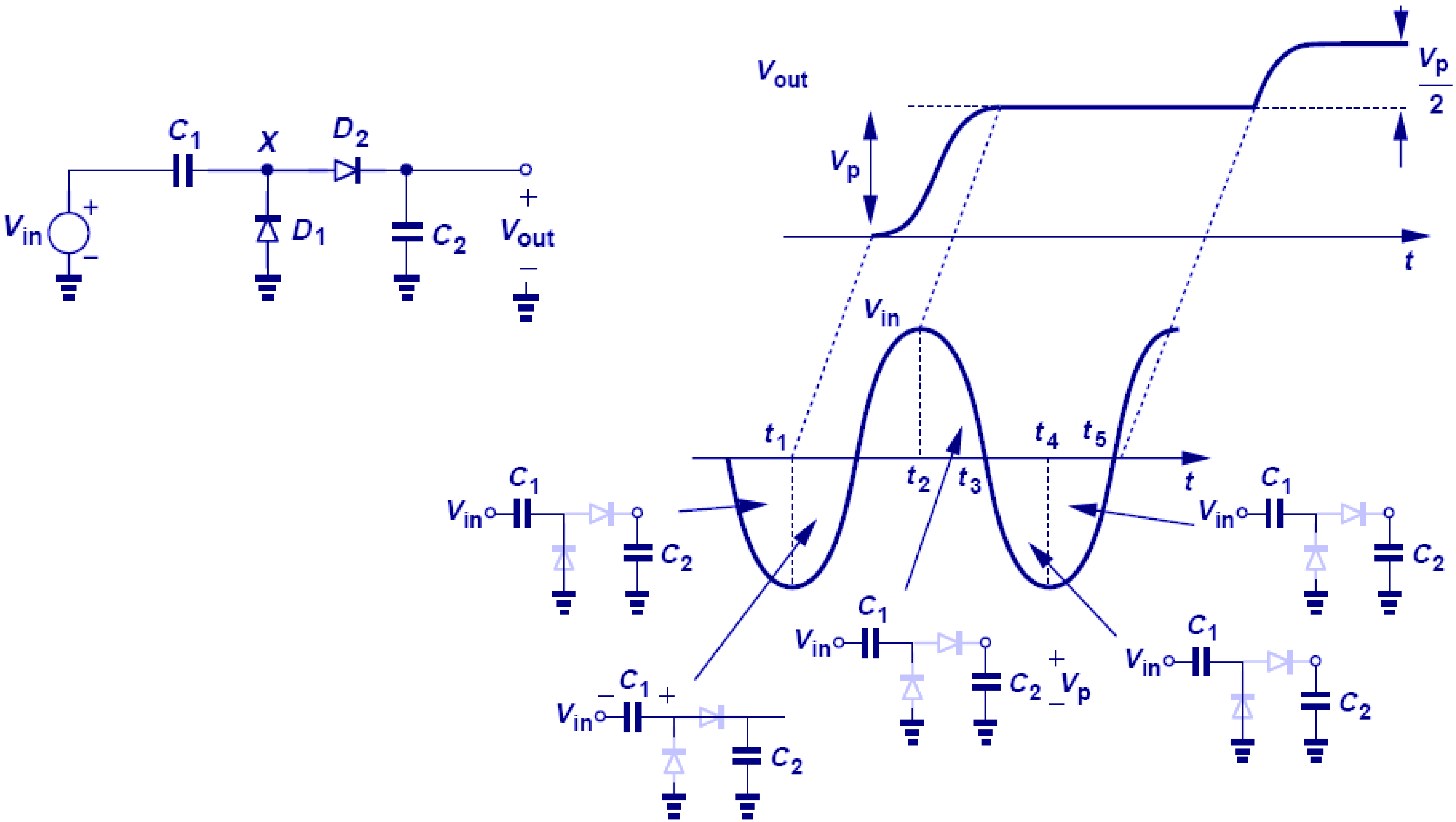
(a)



(b)

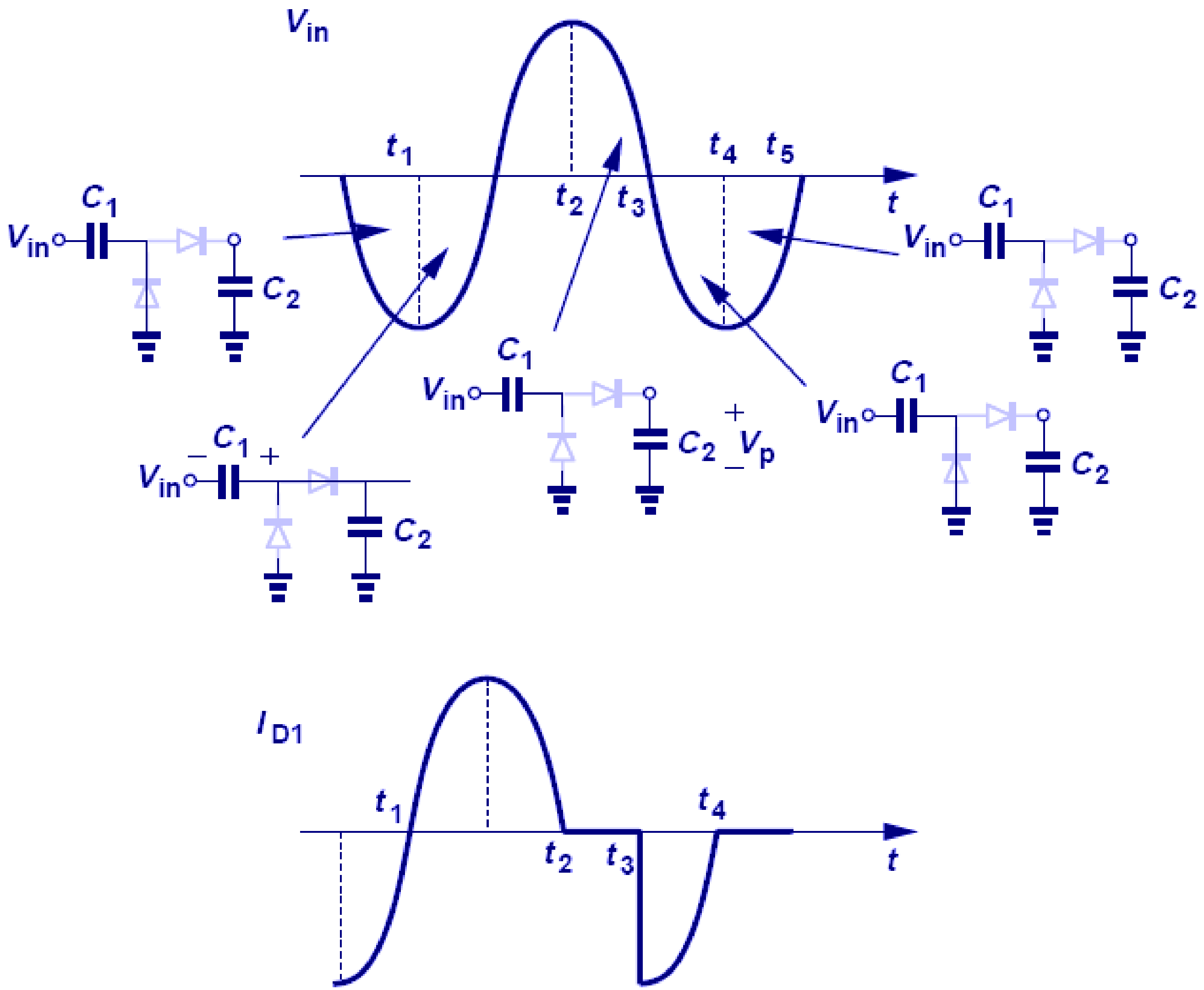
- Similarly, when the terminals of the diode are switched, a voltage doubler with peak value at $2V_p$ can be conceived.

Voltage Doubler

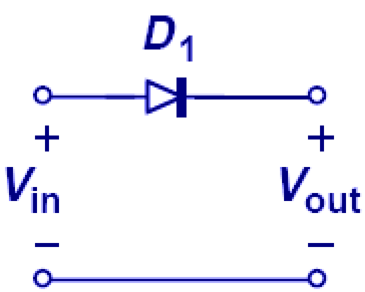


- **The output increases by V_p, $V_{p/2}$, $V_{p/4}$, etc in each input cycle, eventually settling to $2\,V_p$.**

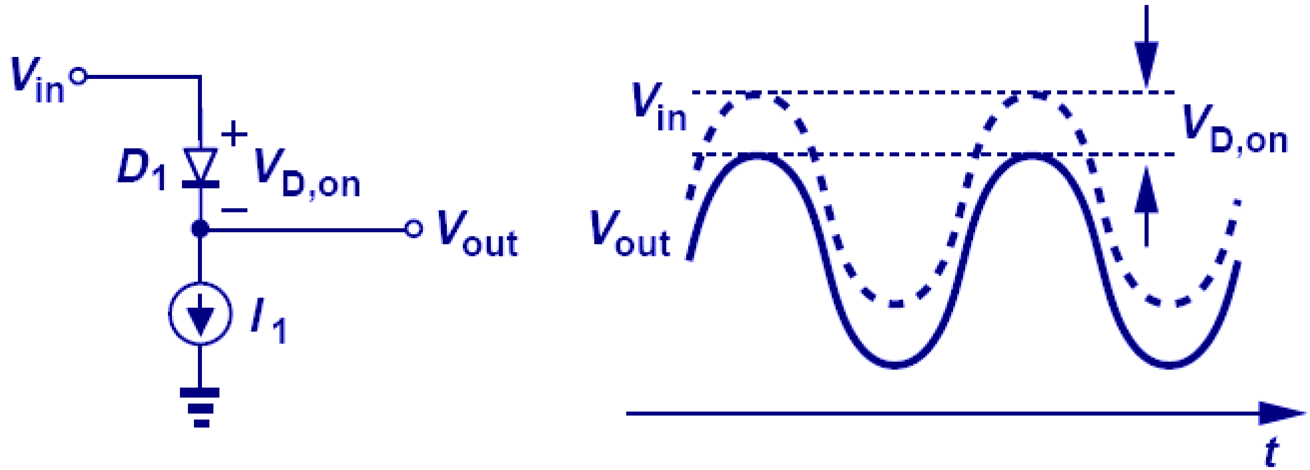
Current thru D_1 in Voltage Doubler



Another Application: Voltage Shifter

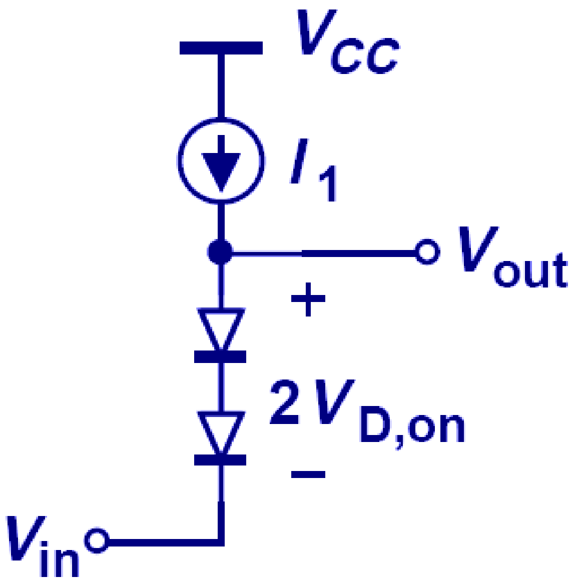


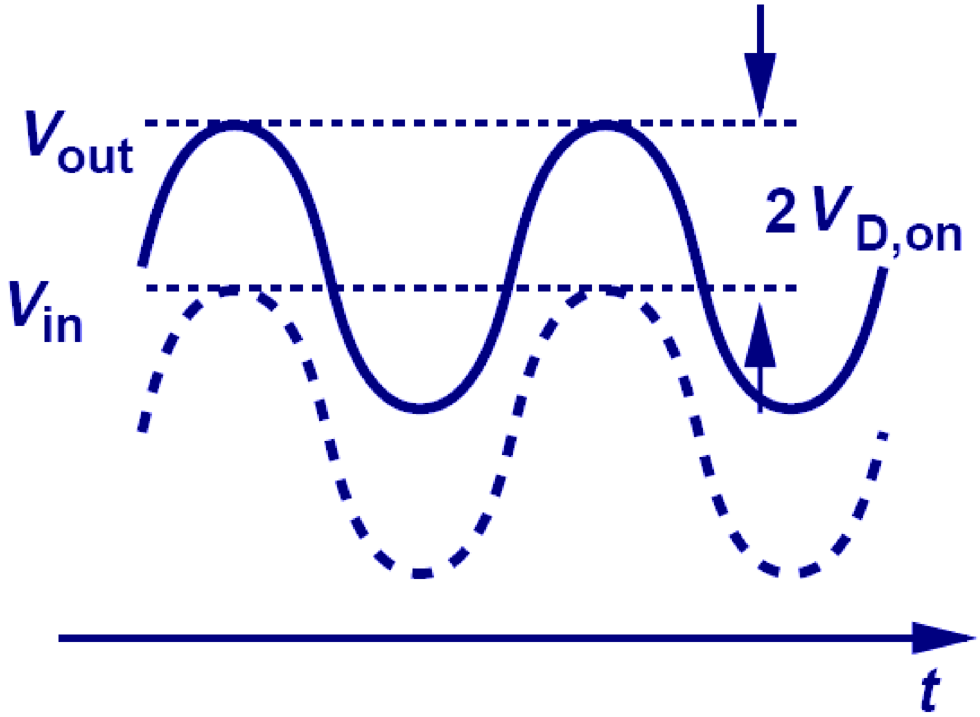
(a)



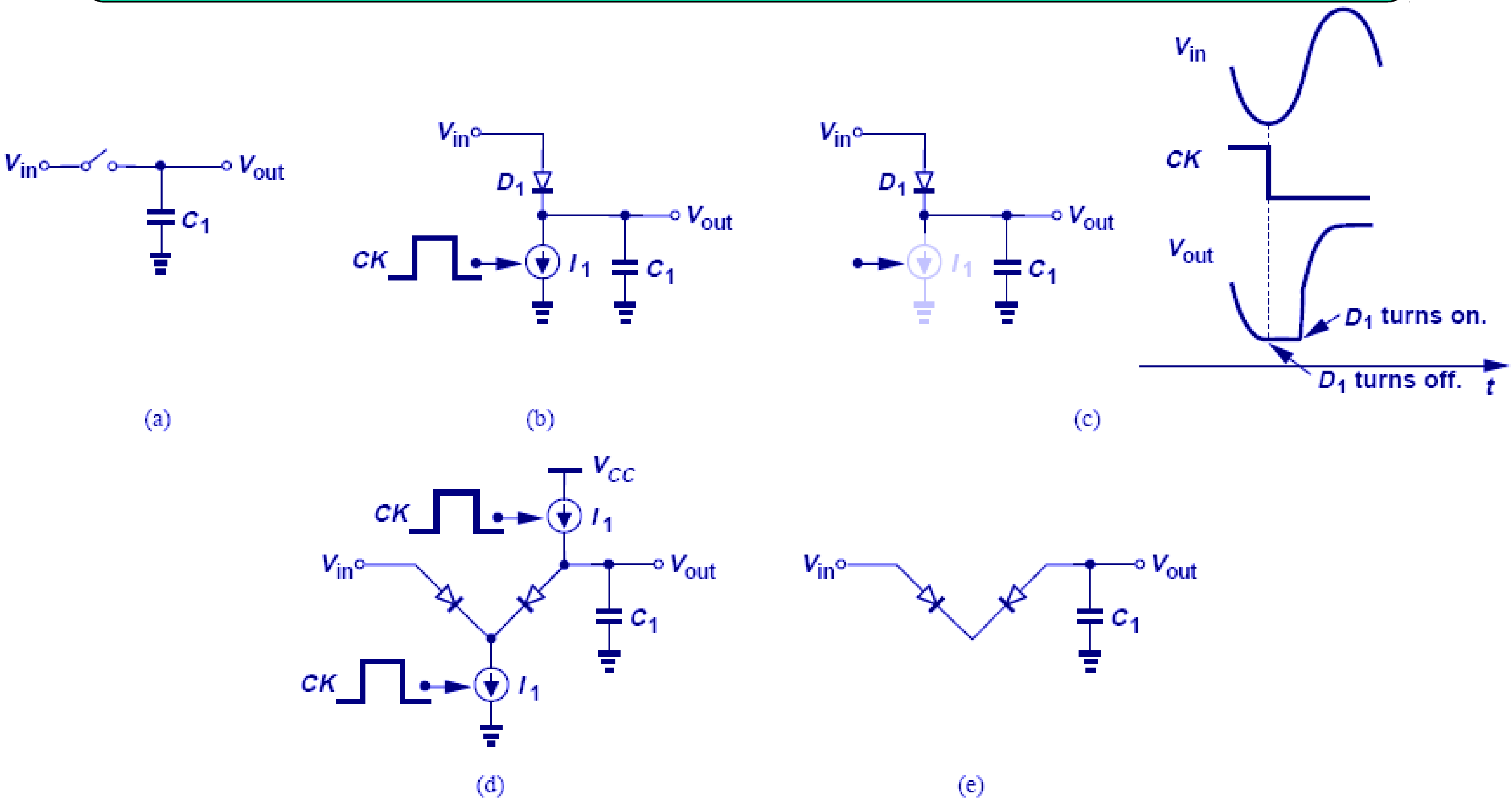
(b)

Voltage Shifter ($2V_{D,ON}$)



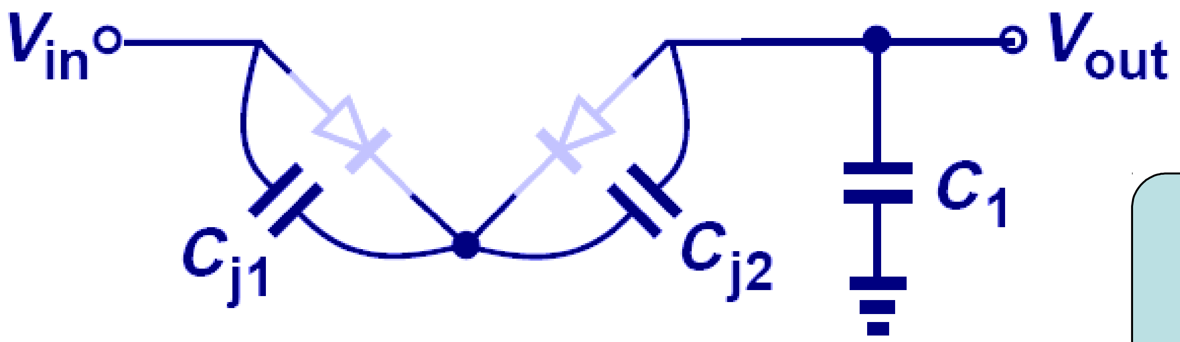


Diode as Electronic Switch



- **Diode as a switch finds application in logic circuits and data converters.**

Junction Feedthrough



$$\Delta V_{out} = \frac{C_j/2}{C_j/2 + C_1}\Delta V_{in}$$

- For the circuit shown in part e) of the previous slide, a small feedthrough from input to output via the junction capacitors exists even if the diodes are reverse biased
- Therefore, C_1 has to be large enough to minimize this feedthrough.

Chapter 4 Physics of Bipolar Transistors

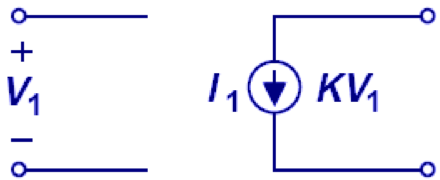
- 4.1 General Considerations
- 4.2 Structure of Bipolar Transistor
- 4.3 Operation of Bipolar Transistor in Active Mode
- 4.4 Bipolar Transistor Models
- 4.5 Operation of Bipolar Transistor in Saturation Mode
- 4.6 The PNP Transistor

Bipolar Transistor

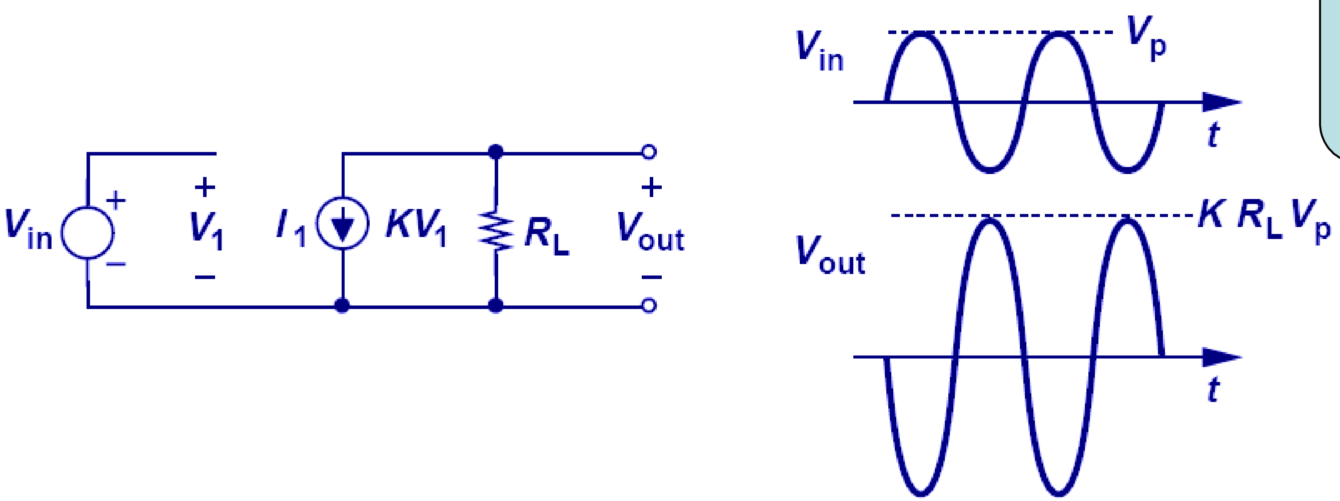
Voltage-Controlled Device as Amplifying Element ⇨ Structure of Bipolar Transistor ⇨ Operation of Bipolar Transistor ⇨ Large-Signal Model ⇨ Small-Signal Model

- **In the chapter, we will study the physics of bipolar transistor and derive large and small signal models.**

Voltage-Dependent Current Source



(a)

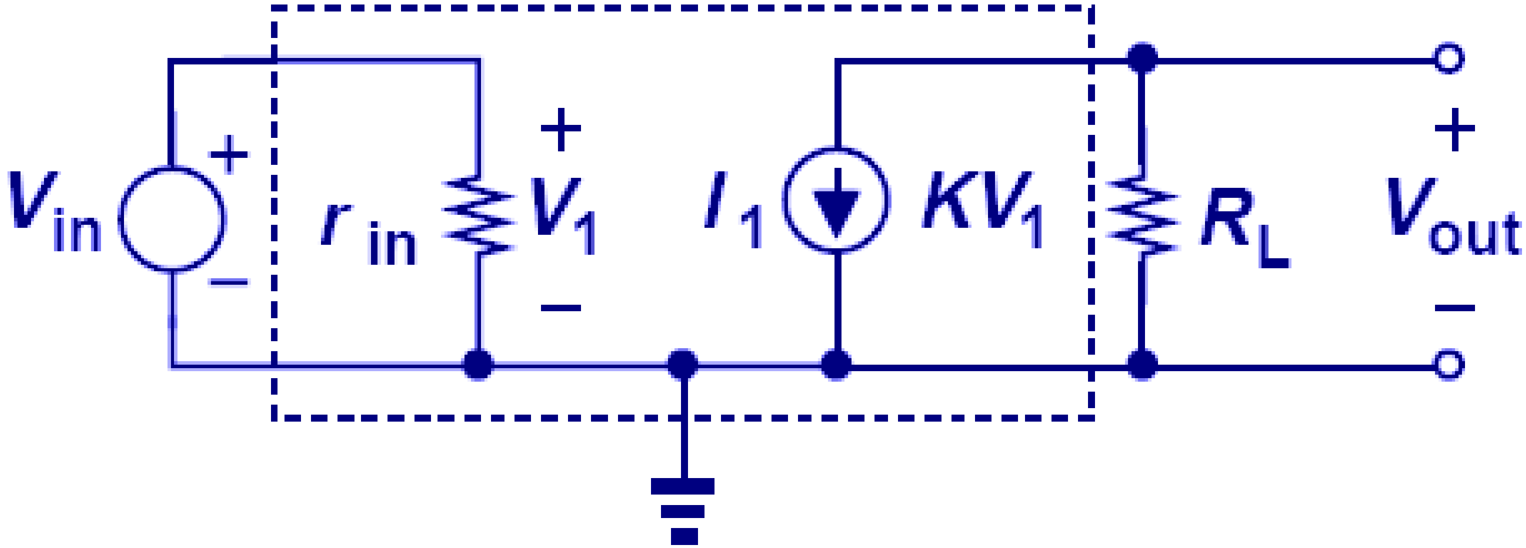


$$A_V = \frac{V_{out}}{V_{in}} = -KR_L$$

(b)

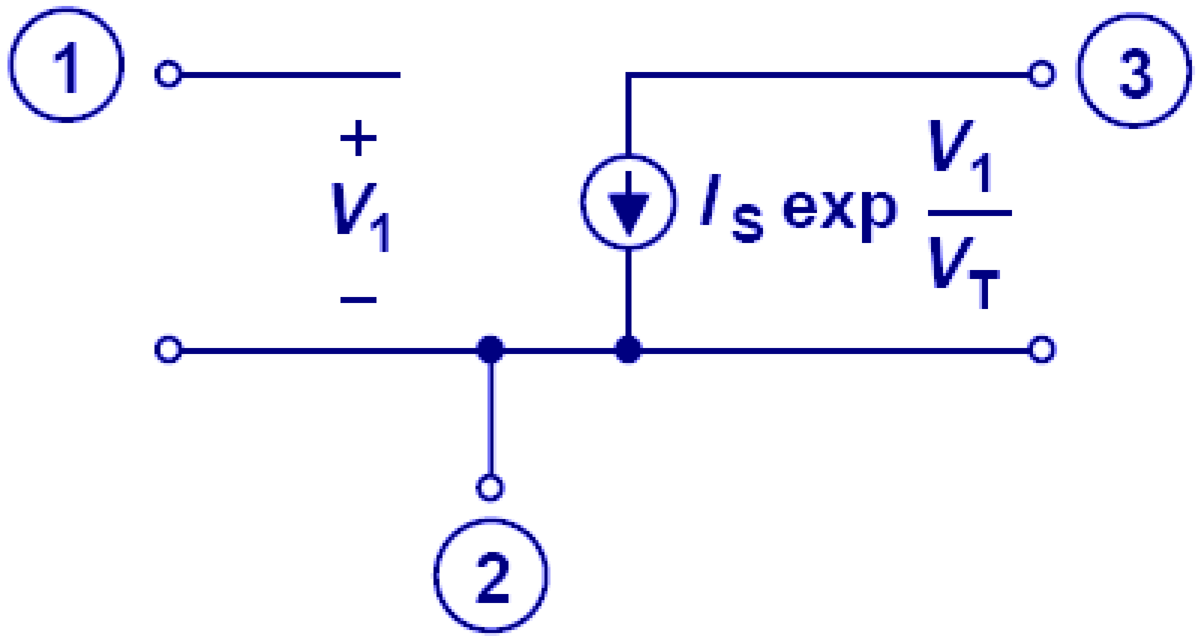
- **A voltage-dependent current source can act as an amplifier.**
- **If KR_L is greater than 1, then the signal is amplified.**

Voltage-Dependent Current Source with Input Resistance



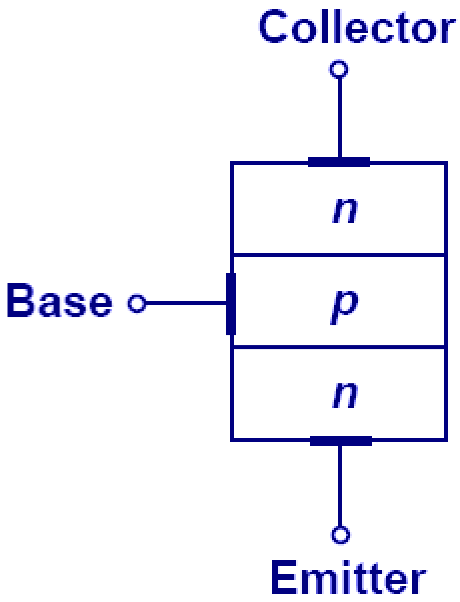
- **Regardless of the input resistance, the magnitude of amplification remains unchanged.**

Exponential Voltage-Dependent Current Source

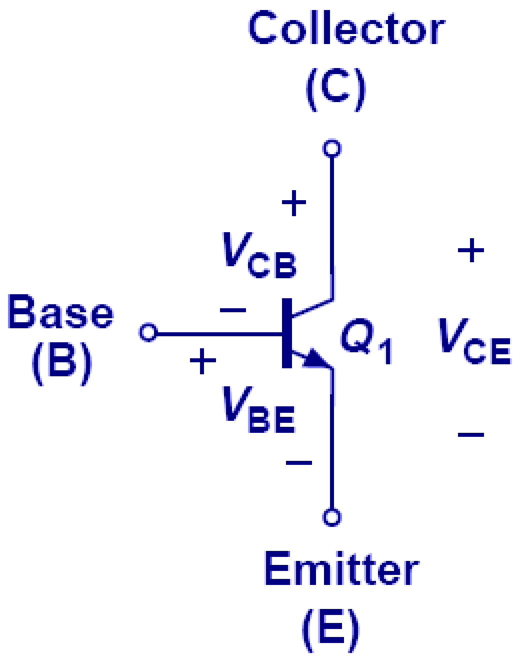


- **A three-terminal exponential voltage-dependent current source is shown above.**
- **Ideally, bipolar transistor can be modeled as such.**

Structure and Symbol of Bipolar Transistor



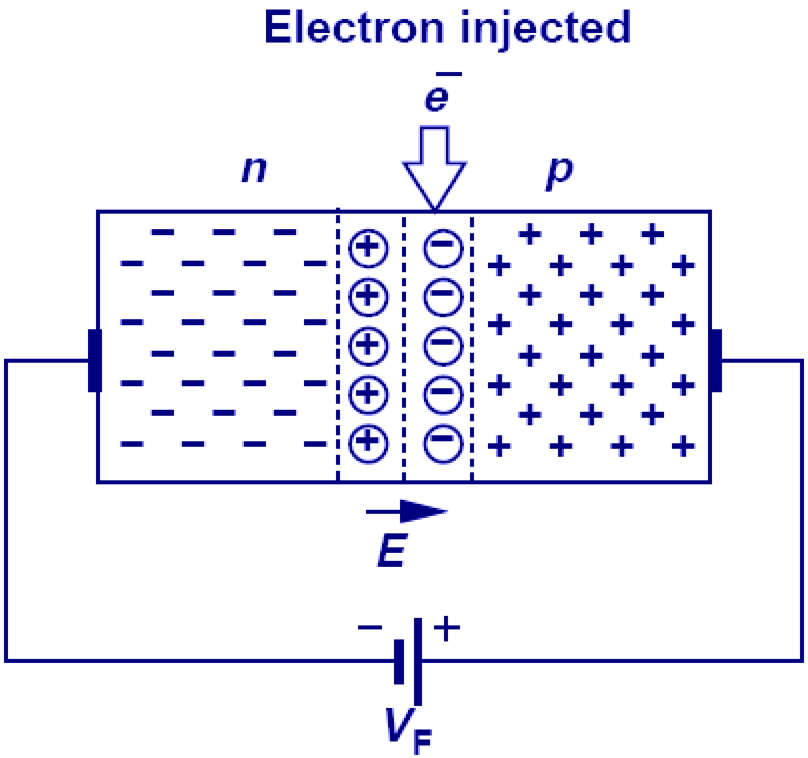
(a)



(b)

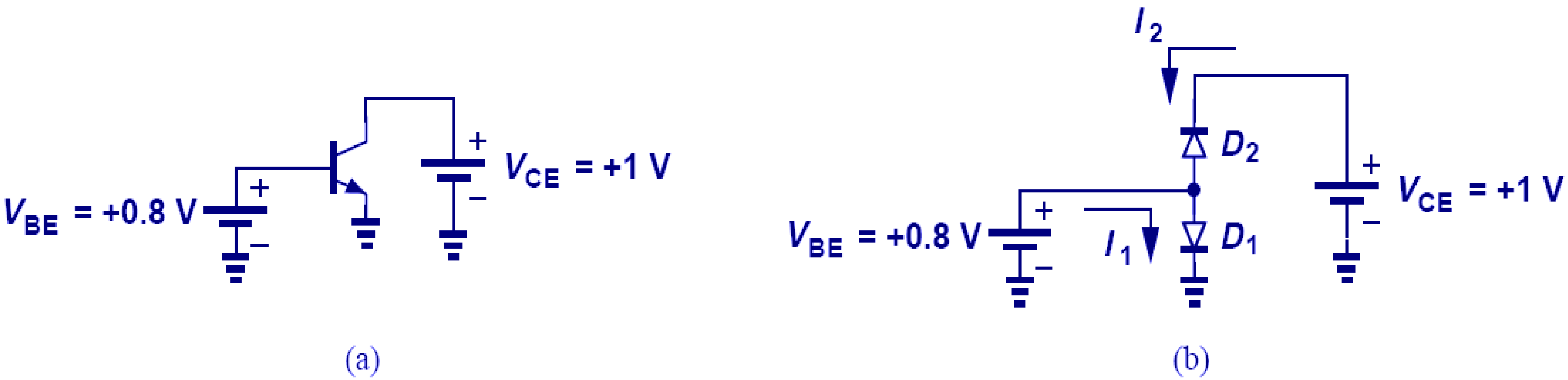
- **Bipolar transistor can be thought of as a sandwich of three doped Si regions. The outer two regions are doped with the same polarity, while the middle region is doped with opposite polarity.**

Injection of Carriers



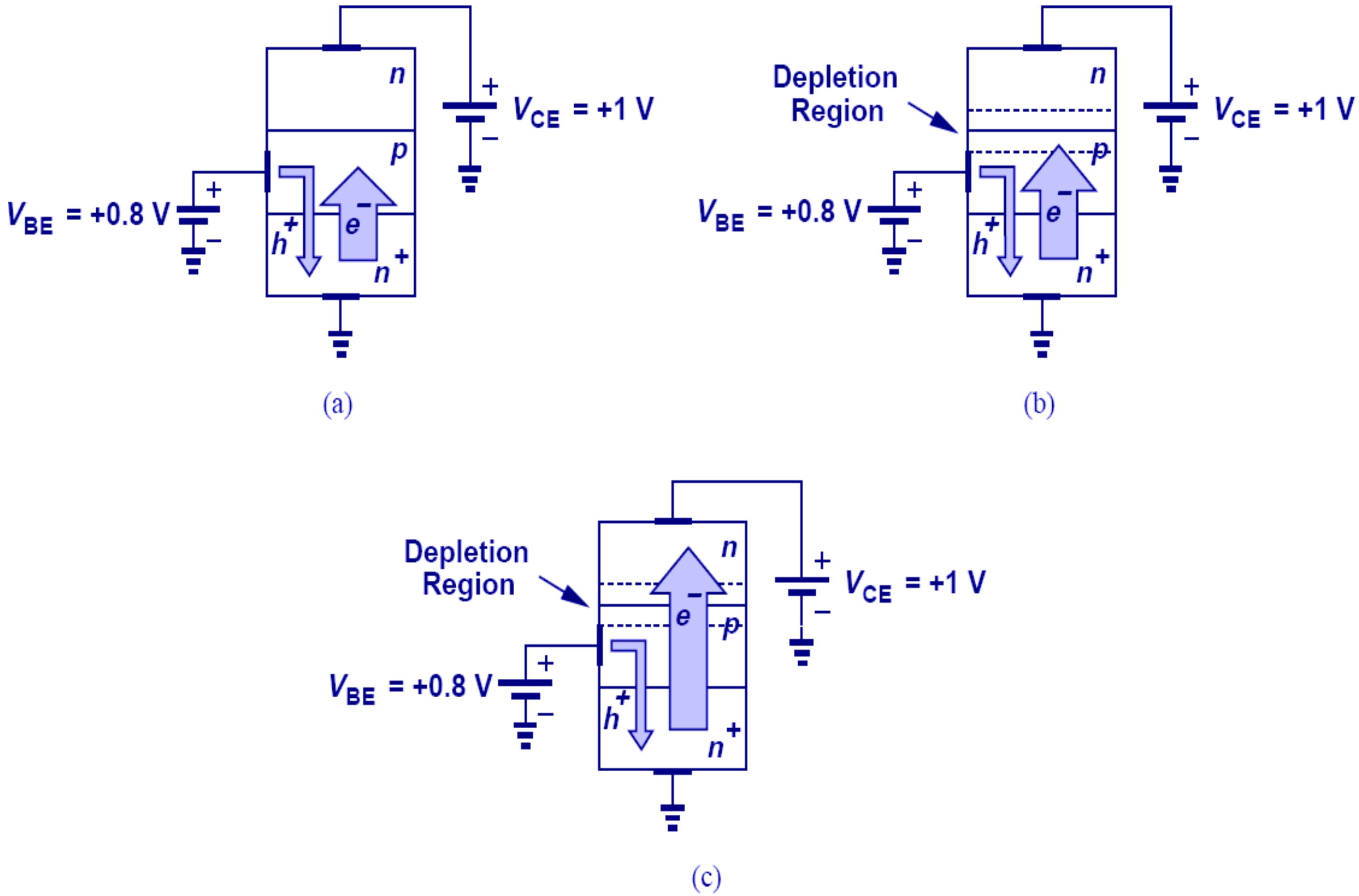
- **Reverse biased PN junction creates a large electric field that sweeps any injected minority carriers to their majority region.**
- **This ability proves essential in the proper operation of a bipolar transistor.**

Forward Active Region



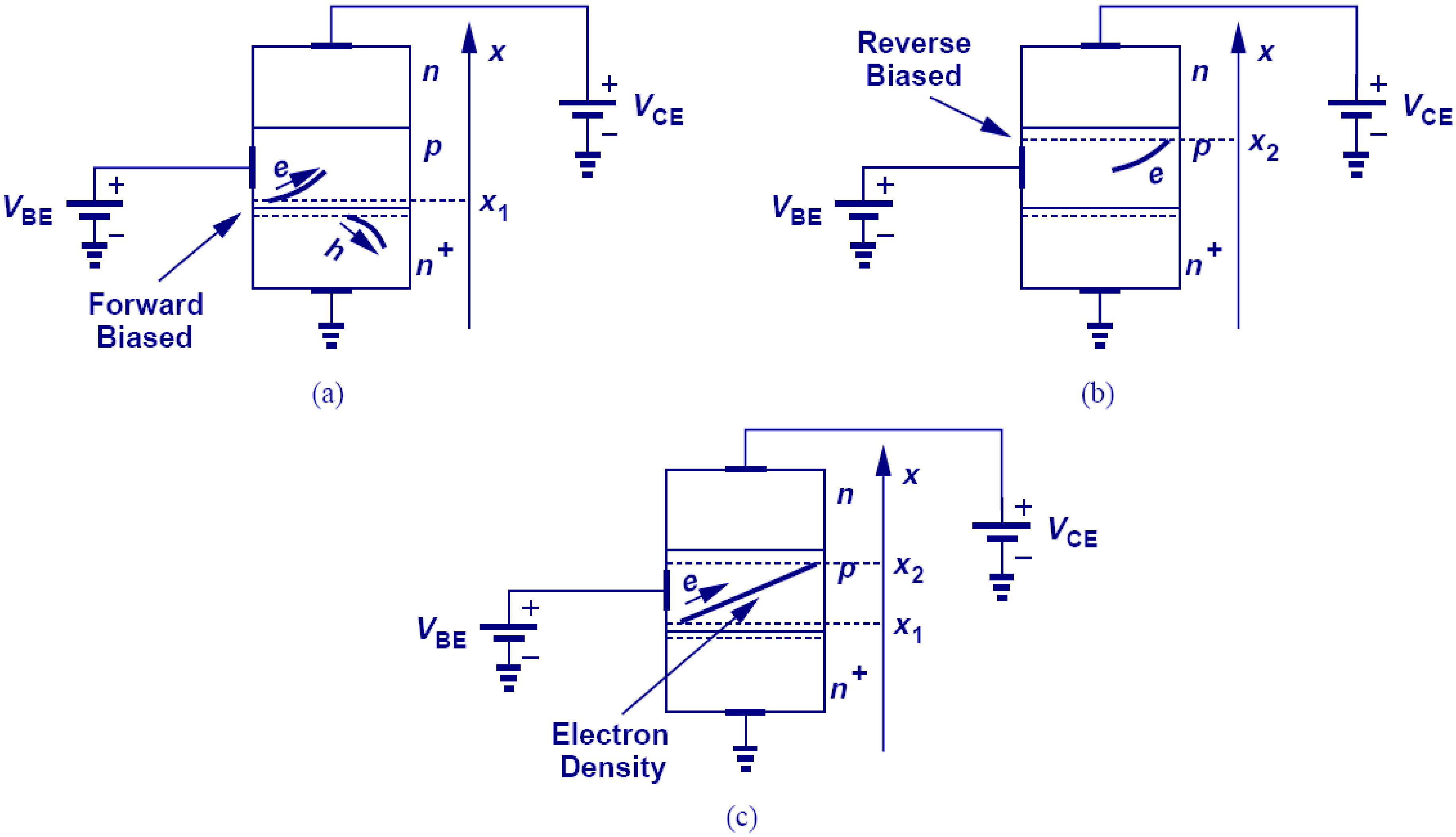
- **Forward active region: $V_{BE} > 0$, $V_{BC} < 0$.**
- **Figure b) presents a wrong way of modeling figure a).**

Accurate Bipolar Representation



- Collector also carries current due to carrier injection from base.

Carrier Transport in Base



Collector Current

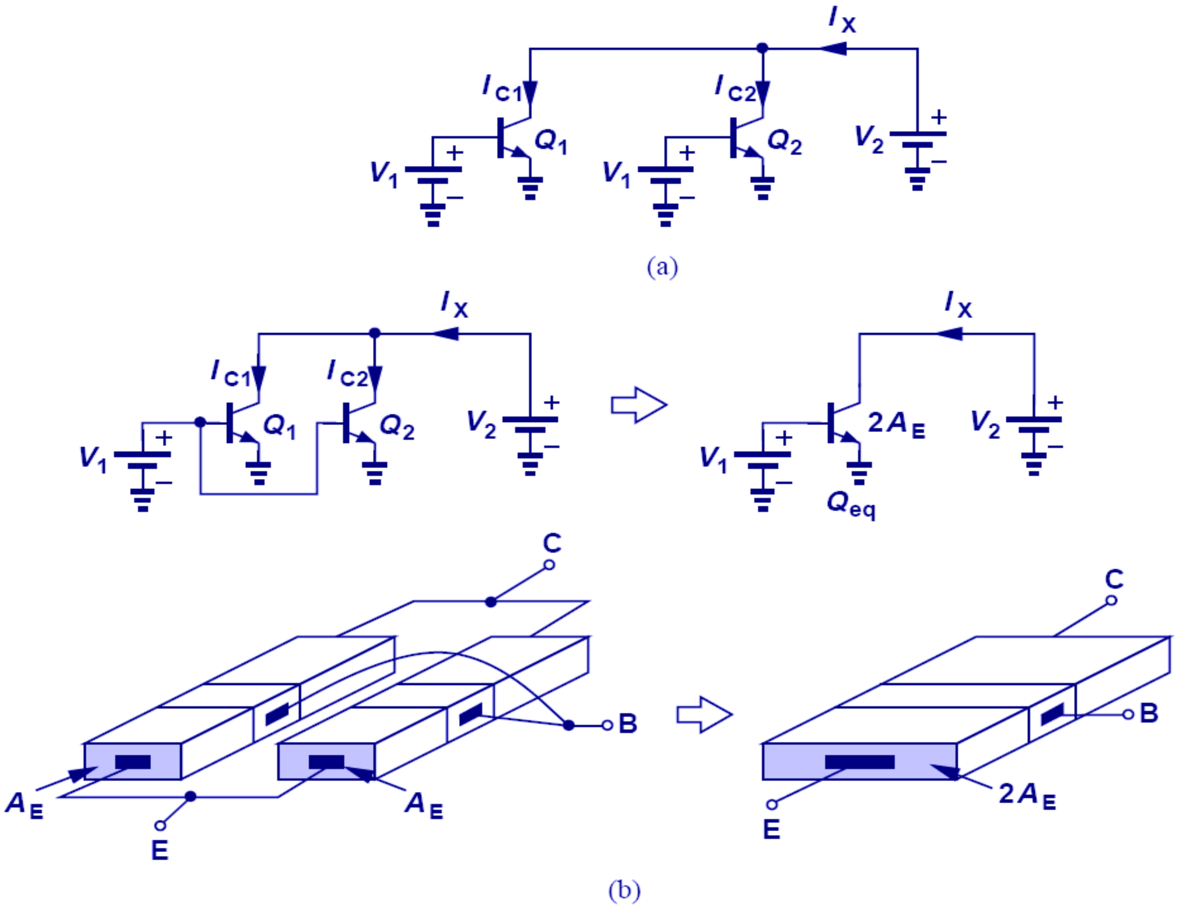
$$I_C = \frac{A_E q D_n n_i^2}{N_E W_B}\left(\exp\frac{V_{BE}}{V_T} - 1\right)$$

$$I_C = I_S \exp\frac{V_{BE}}{V_T}$$

$$I_S = \frac{A_E q D_n n_i^2}{N_E W_B}$$

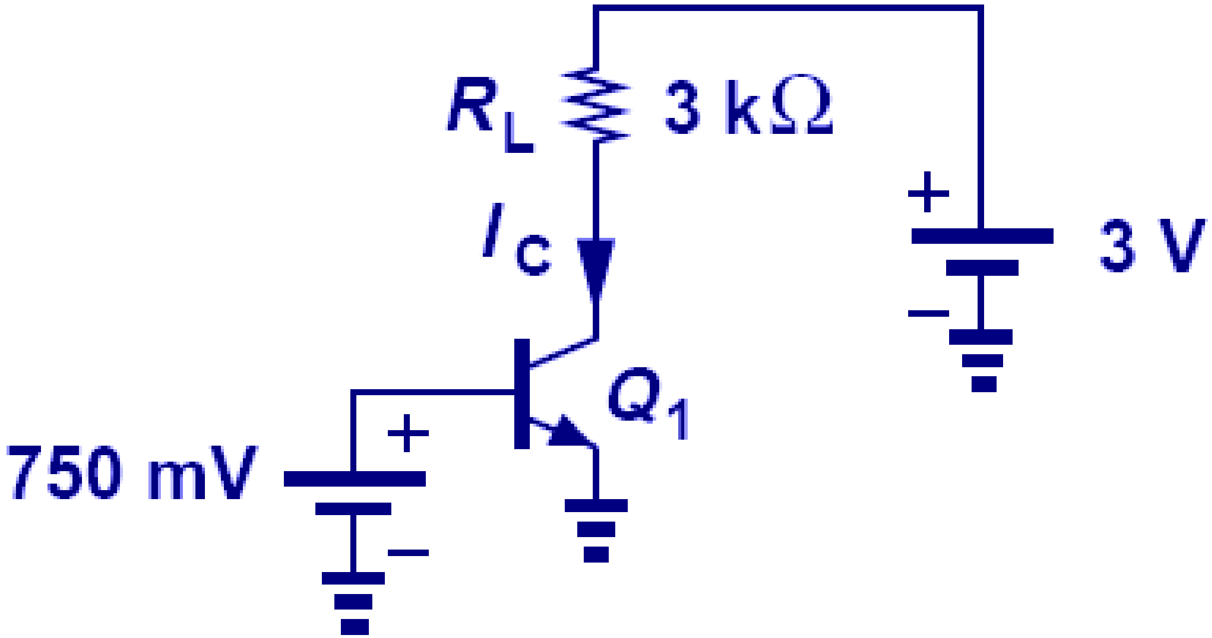
- **Applying the law of diffusion, we can determine the charge flow across the base region into the collector.**
- **The equation above shows that the transistor is indeed a voltage-controlled element, thus a good candidate as an amplifier.**

Parallel Combination of Transistors



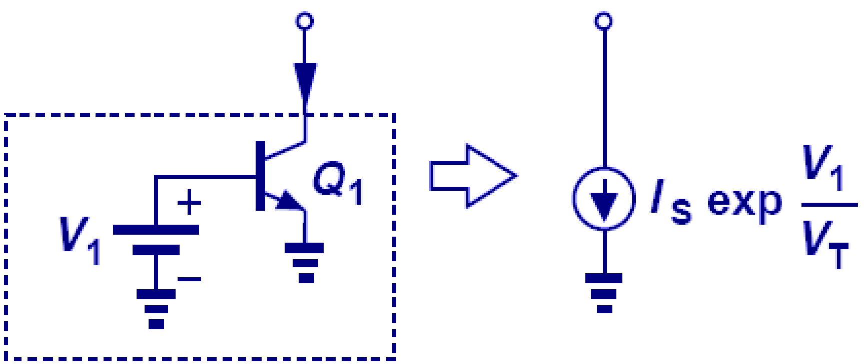
- **When two transistors are put in parallel and experience the same potential across all three terminals, they can be thought of as a single transistor with twice the emitter area.**

Simple Transistor Configuration

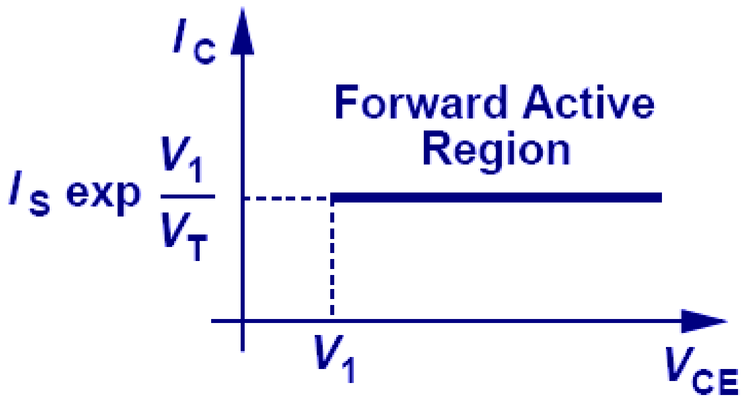


- Although a transistor is a voltage to current converter, output voltage can be obtained by inserting a load resistor at the output and allowing the controlled current to pass thru it.

Constant Current Source



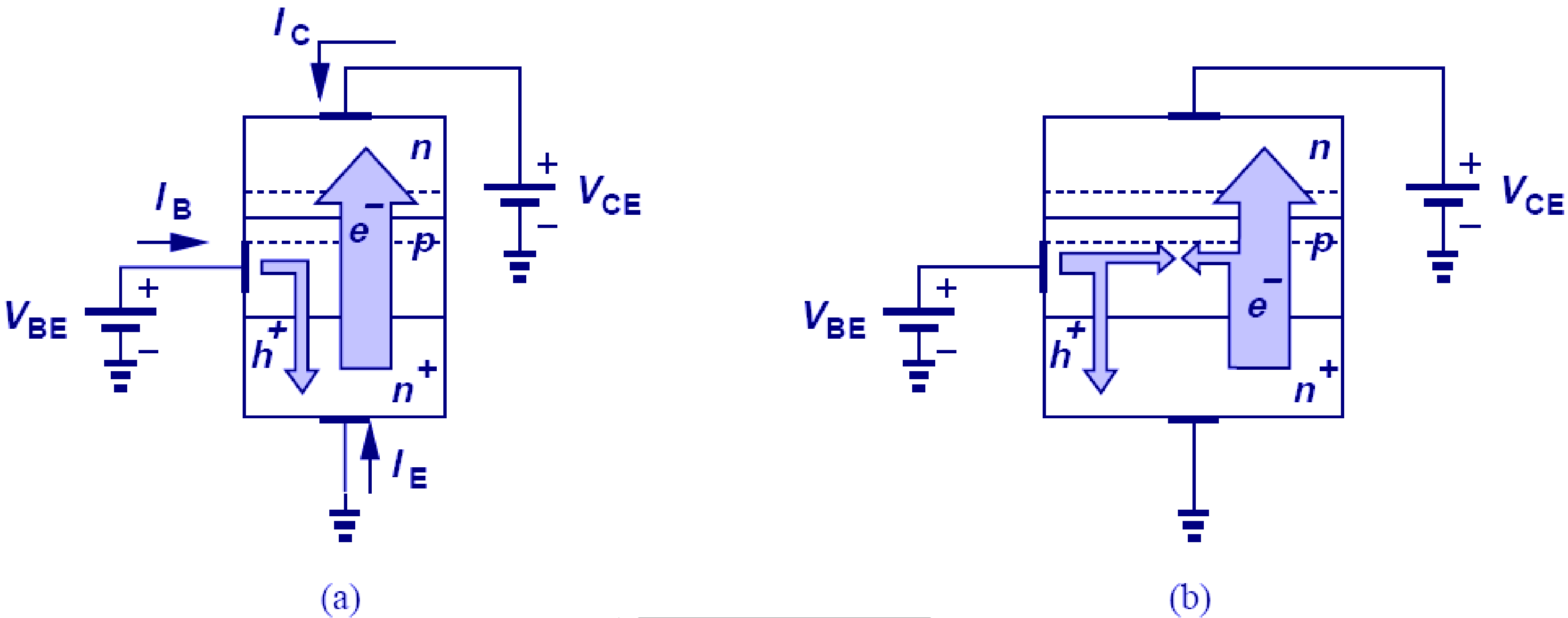
(a)



(b)

- **Ideally, the collector current does not depend on the collector to emitter voltage. This property allows the transistor to behave as a constant current source when its base-emitter voltage is fixed.**

Base Current



$$I_C = \beta I_B$$

- **Base current consists of two components: 1) Reverse injection of holes into the emitter and 2) recombination of holes with electrons coming from the emitter.**

Emitter Current

$$I_E = I_C + I_B$$

$$I_E = I_C\left(1 + \frac{1}{\beta}\right)$$

$$\beta = \frac{I_C}{I_B}$$

- **Applying Kirchoff's current law to the transistor, we can easily find the emitter current.**

Summary of Currents

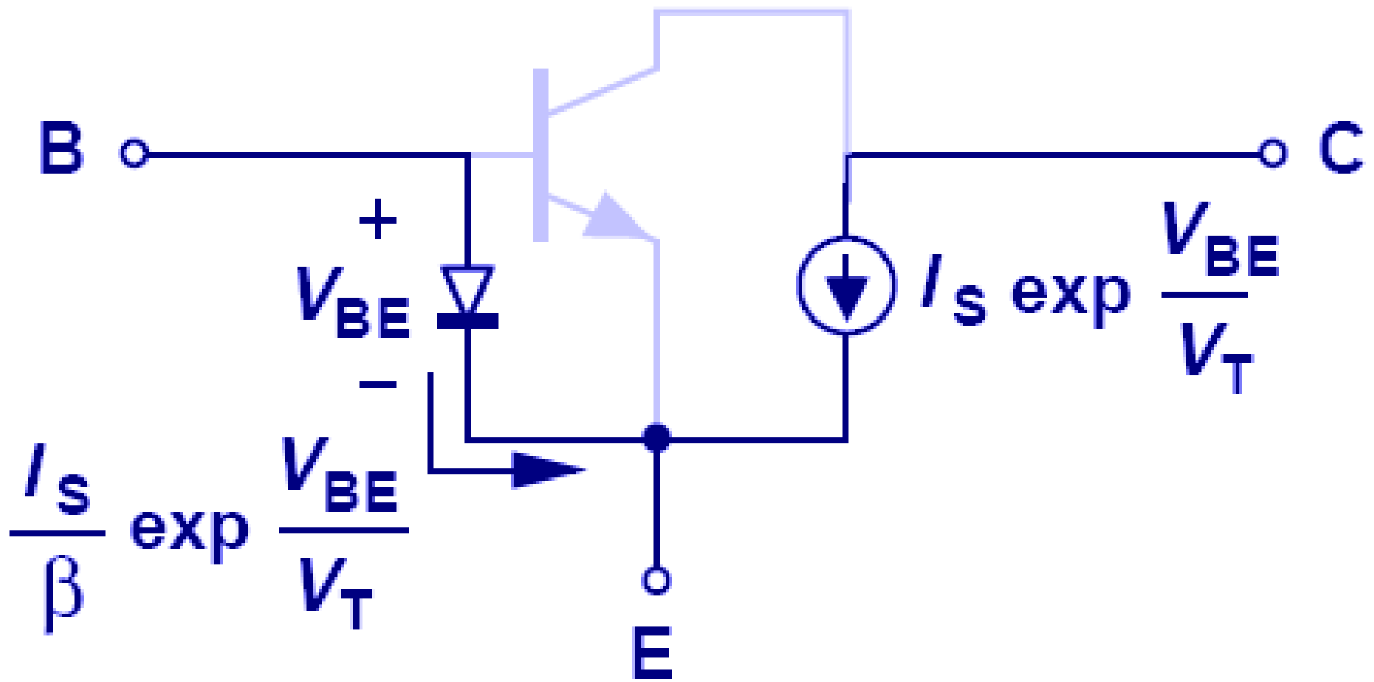
$$I_C = I_S \exp\frac{V_{BE}}{V_T}$$

$$I_B = \frac{1}{\beta} I_S \exp\frac{V_{BE}}{V_T}$$

$$I_E = \frac{\beta+1}{\beta} I_S \exp\frac{V_{BE}}{V_T}$$

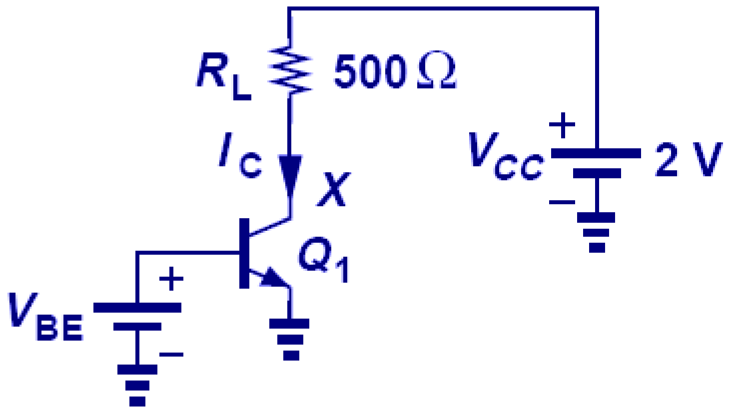
$$\frac{\beta}{\beta+1} = \alpha$$

Bipolar Transistor Large Signal Model

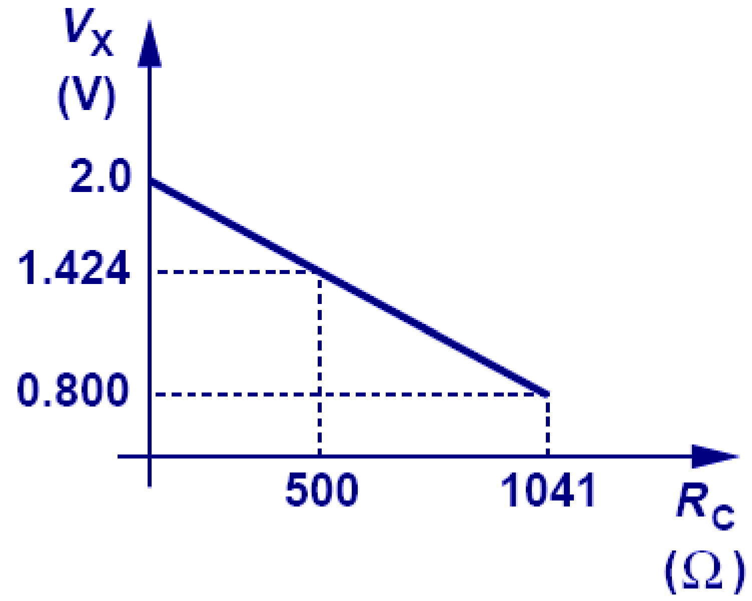


- **A diode is placed between base and emitter and a voltage controlled current source is placed between the collector and emitter.**

Example: Maximum R_L



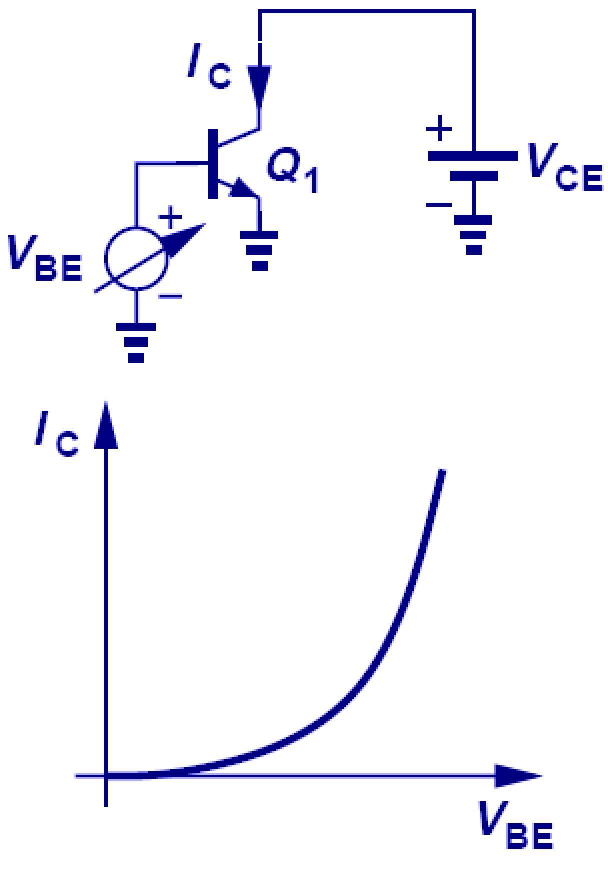
(a)



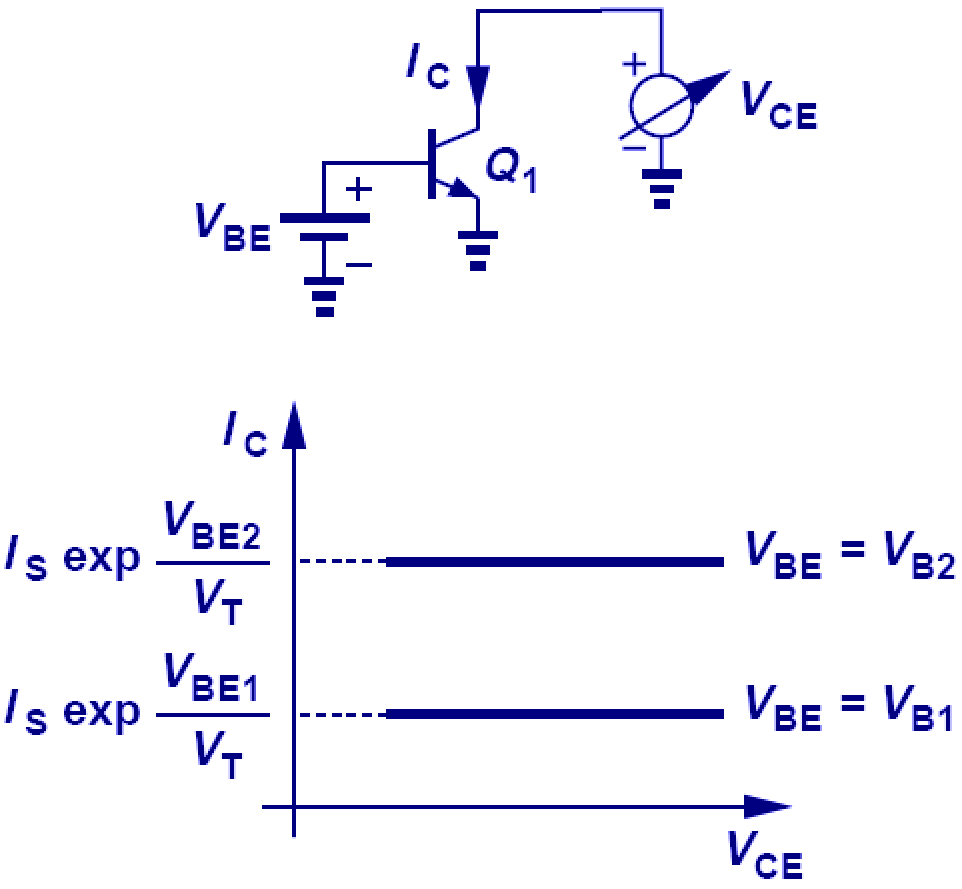
(b)

- As R_L increases, V_x drops and eventually forward biases the collector-base junction. This will force the transistor out of forward active region.
- Therefore, there exists a maximum tolerable collector resistance.

Characteristics of Bipolar Transistor

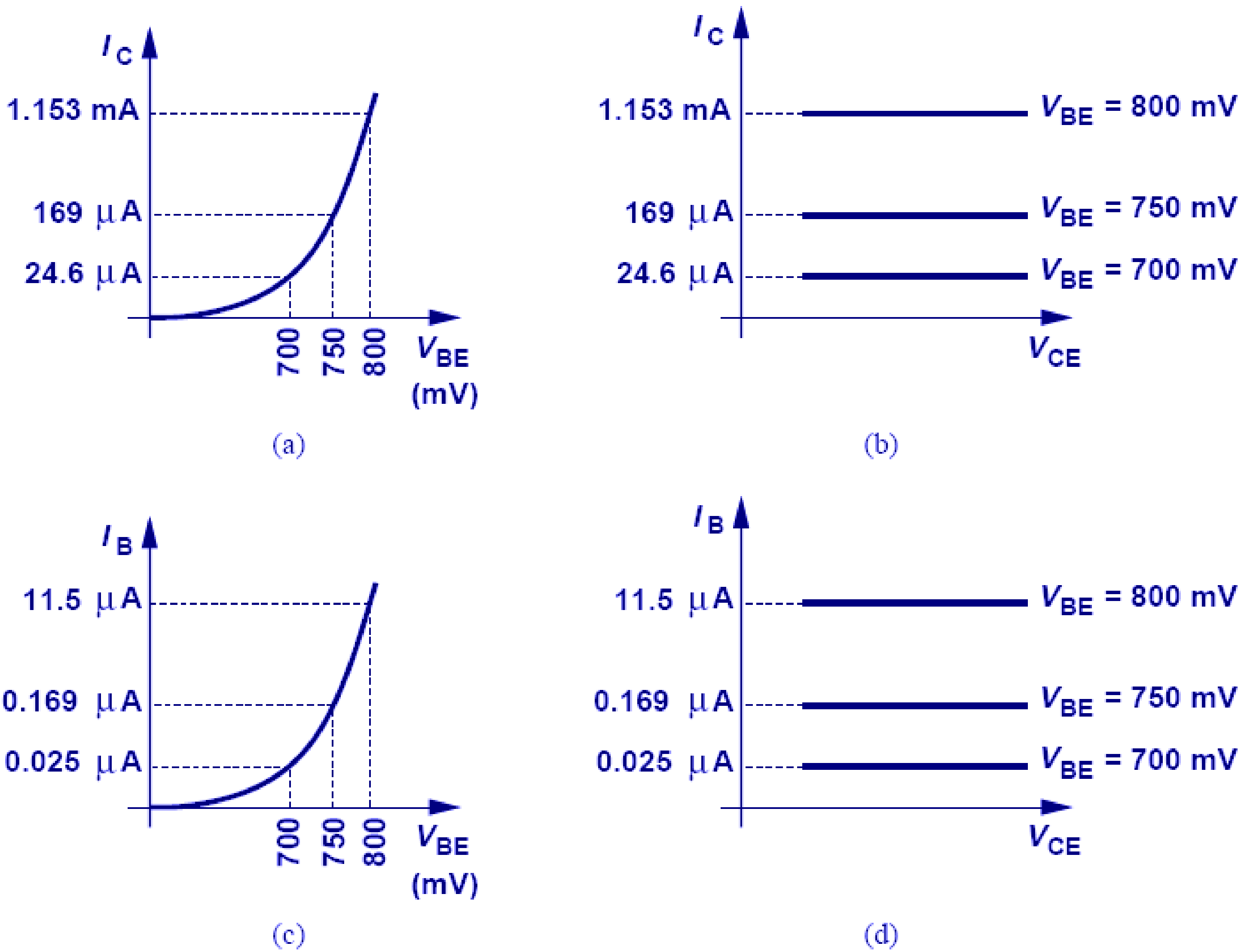


(a)

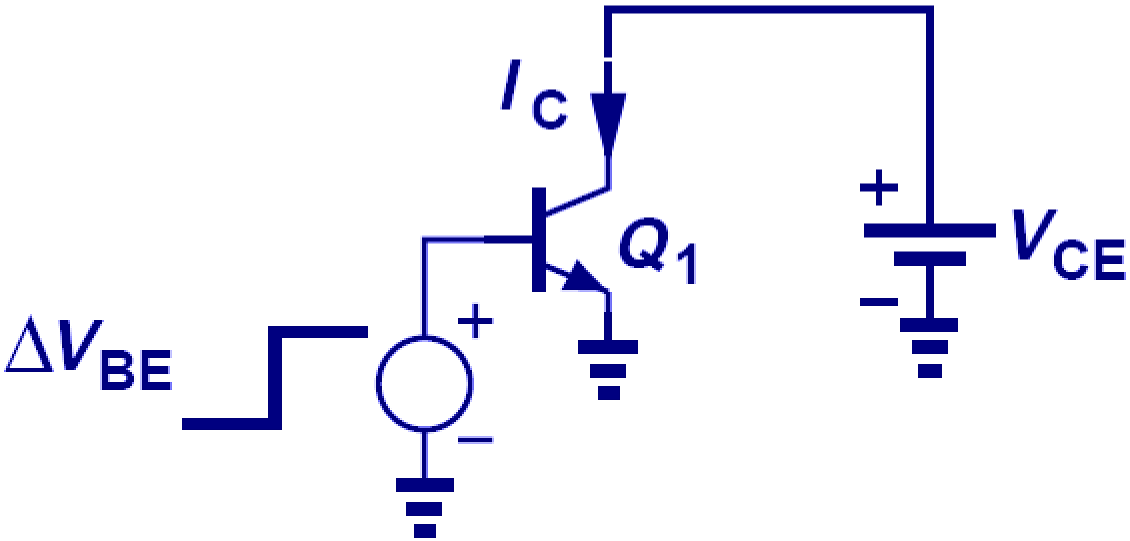


(b)

Example: IV Characteristics



Transconductance



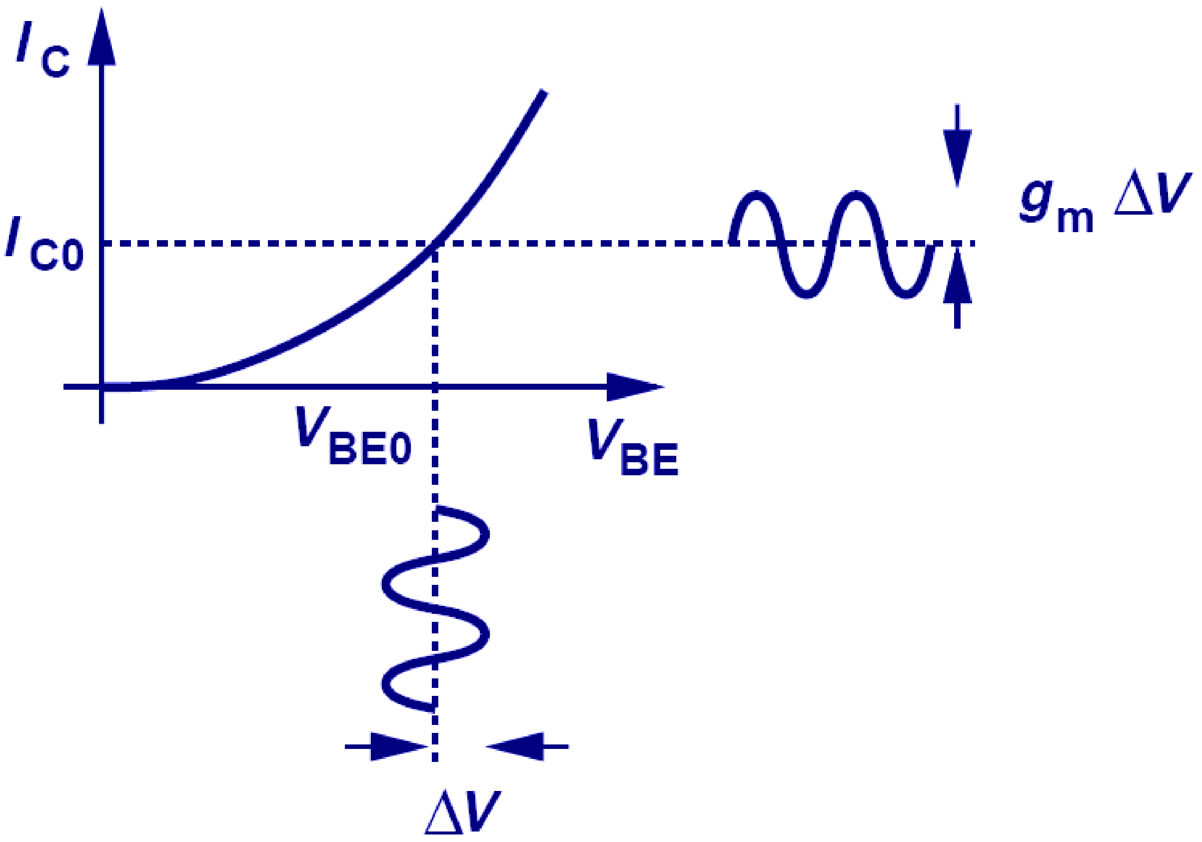
$$g_m = \frac{d}{dV_{BE}}\left(I_S \exp\frac{V_{BE}}{V_T}\right)$$

$$g_m = \frac{1}{V_T} I_S \exp\frac{V_{BE}}{V_T}$$

$$g_m = \frac{I_C}{V_T}$$

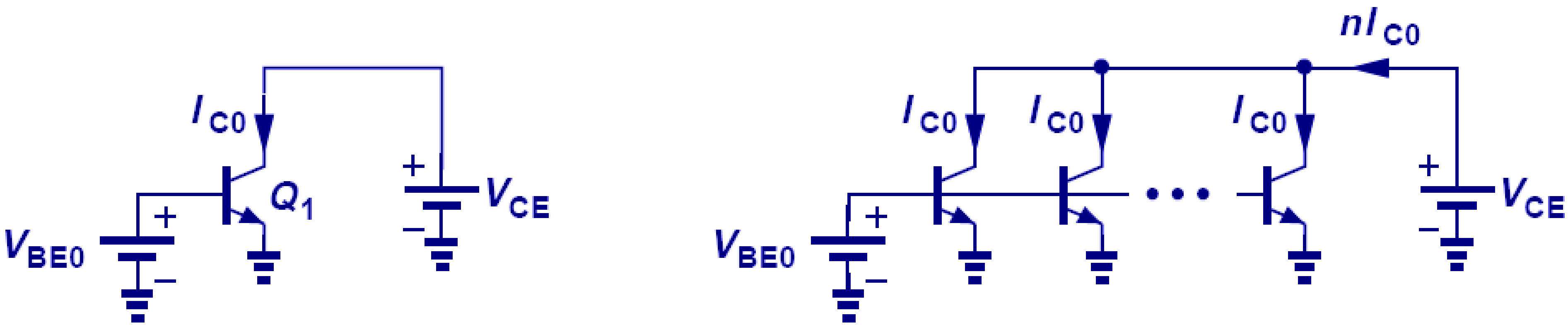
- **Transconductance, g_m shows a measure of how well the transistor converts voltage to current.**
- **It will later be shown that g_m is one of the most important parameters in circuit design.**

Visualization of Transconductance



- g_m can be visualized as the slope of I_C versus V_{BE}.
- A large I_C has a large slope and therefore a large g_m.

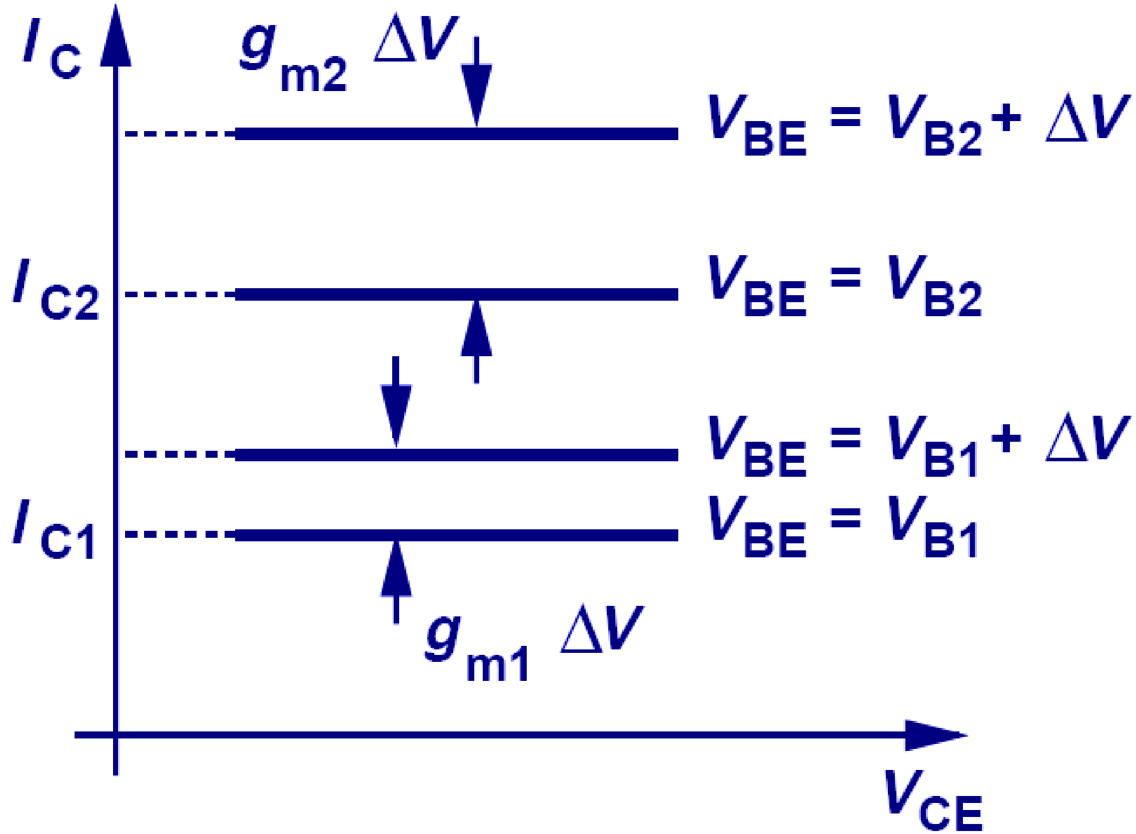
Transconductance and Area



(a) (b)

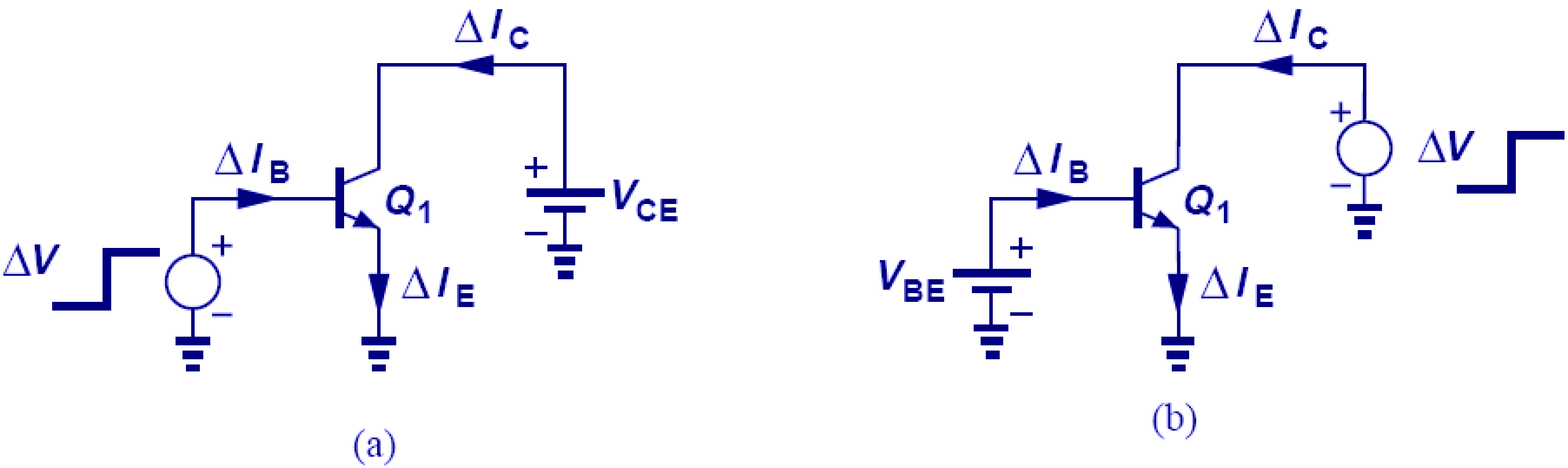
- **When the area of a transistor is increased by n, I_S increases by n. For a <u>constant</u> $V_{BE,}$ I_C and hence g_m increases by a factor of n.**

Transconductance and I_c



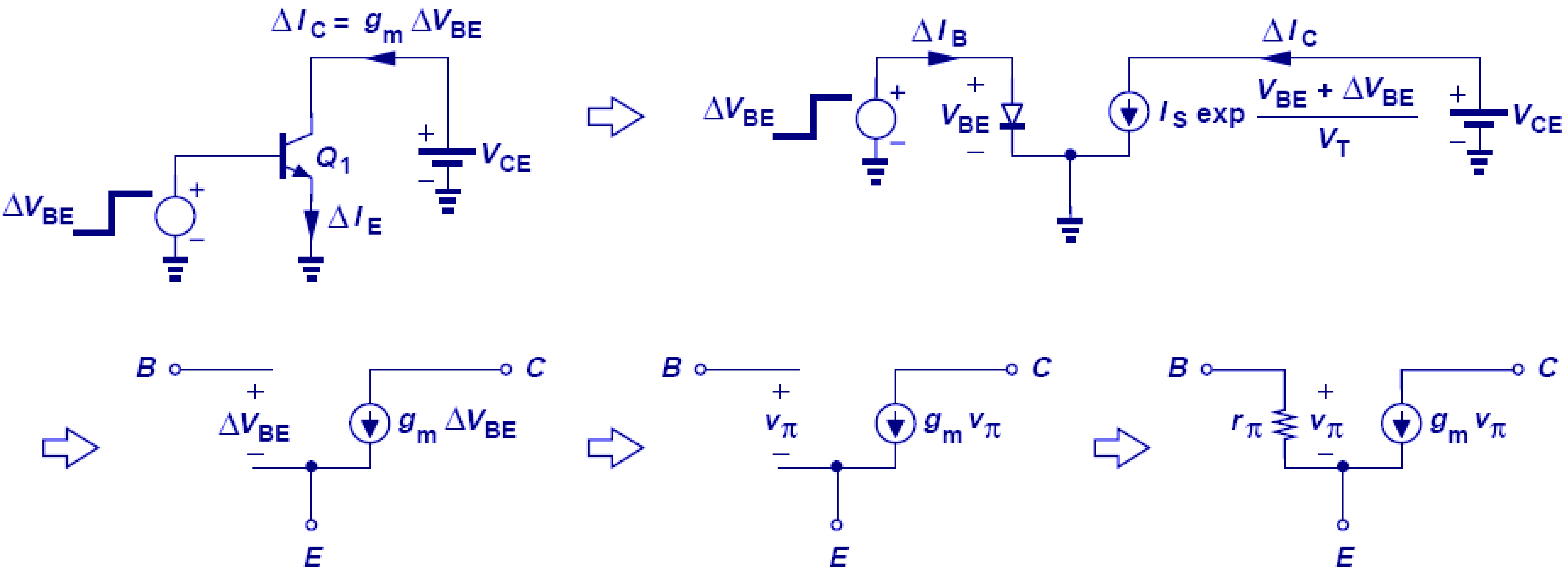
- **The figure above shows that for a given V_{BE} swing, the current excursion around I_{C2} is larger than it would be around I_{C1}. This is because g_m is larger I_{C2}.**

Small-Signal Model: Derivation

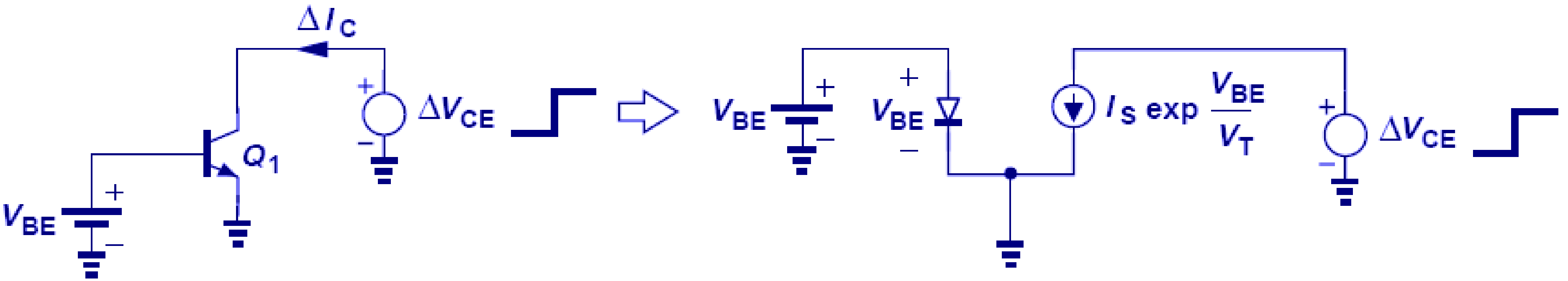


- **Small signal model is derived by perturbing voltage difference every two terminals while fixing the third terminal and analyzing the change in current of all three terminals. We then represent these changes with controlled sources or resistors.**

Small-Signal Model: V_{BE} Change

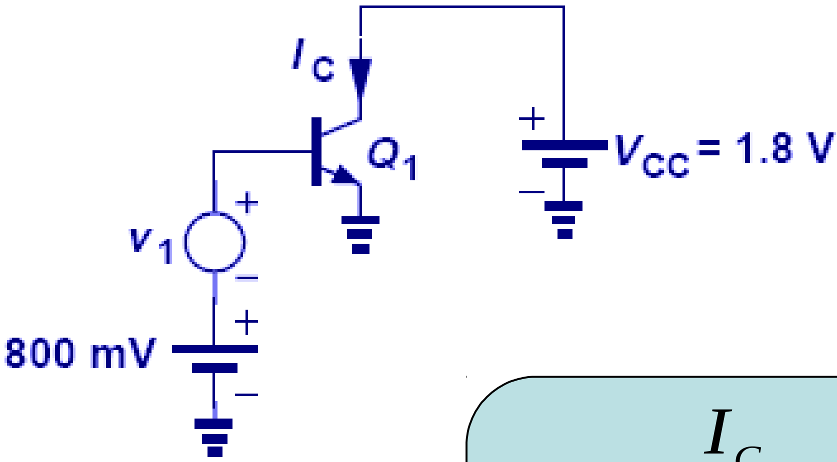


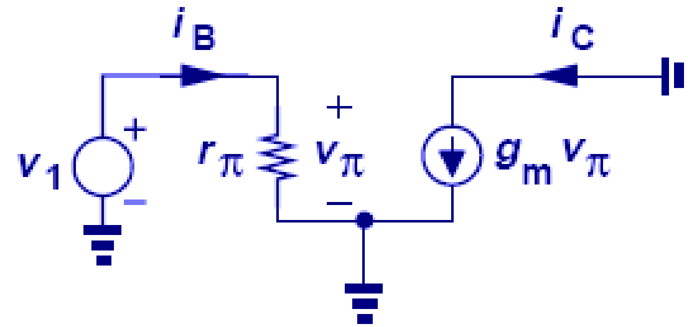
Small-Signal Model: V_{CE} Change



- Ideally, V_{CE} has no effect on the collector current. Thus, it will not contribute to the small signal model.
- It can be shown that V_{CB} has no effect on the small signal model, either.

Small Signal Example I



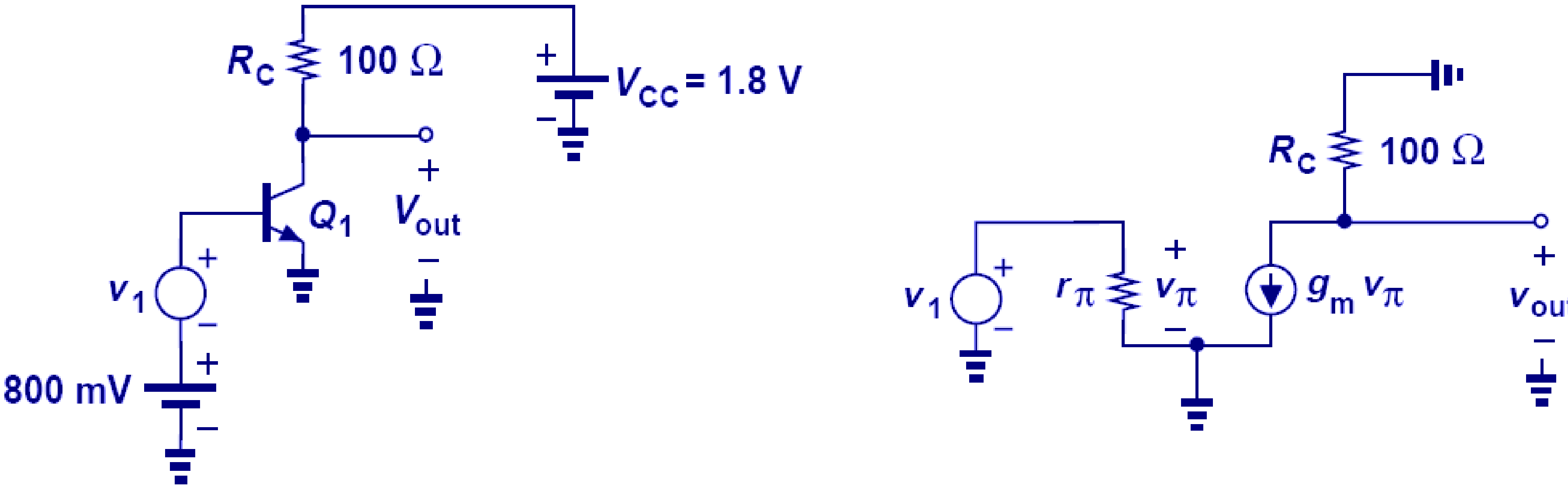


$$g_m = \frac{I_C}{V_T} = \frac{1}{3.75\Omega}$$

$$r_\pi = \frac{\beta}{g_m} = 375\Omega$$

- **Here, small signal parameters are calculated from DC operating point and are used to calculate the change in collector current due to a change in V_{BE}.**

Small Signal Example II

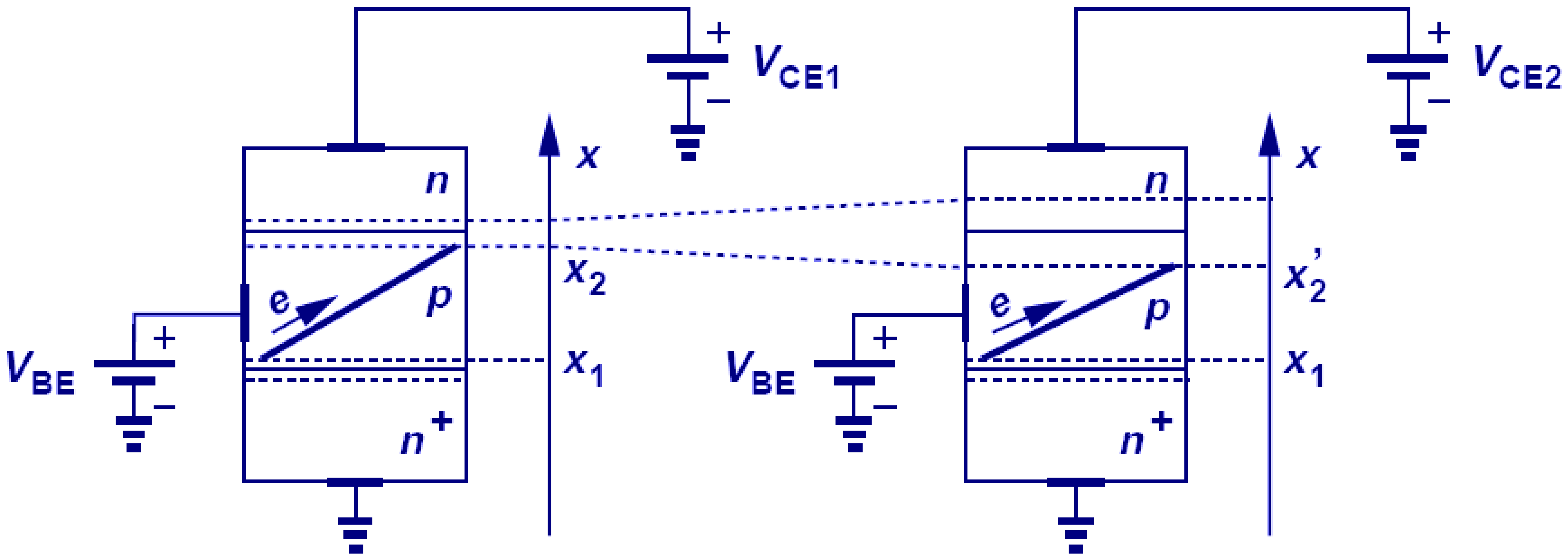


- **In this example, a resistor is placed between the power supply and collector, therefore, providing an output voltage.**

AC Ground

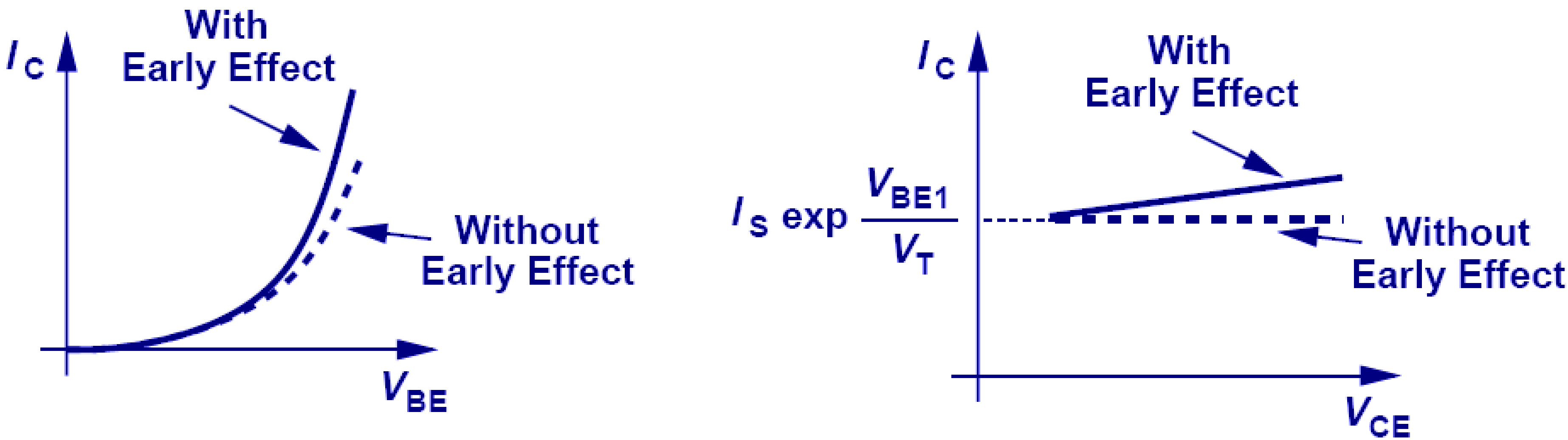
- **Since the power supply voltage does not vary with time, it is regarded as a ground in small-signal analysis.**

Early Effect



- The claim that collector current does not depend on V_{CE} is not accurate.
- As V_{CE} increases, the depletion region between base and collector increases. Therefore, the effective base width decreases, which leads to an increase in the collector current.

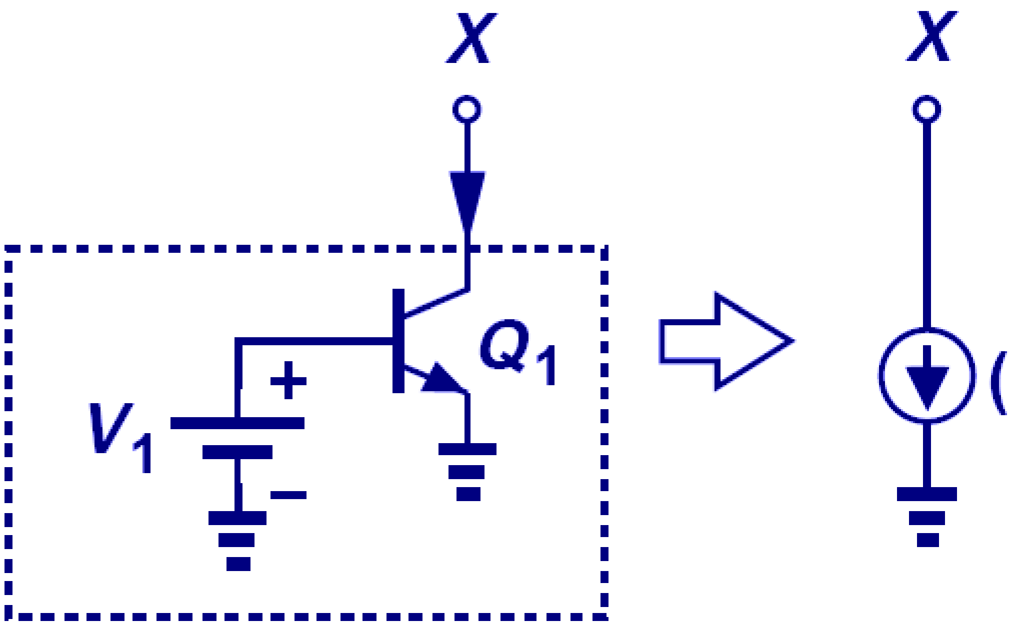
Early Effect Illustration



(a) (b)

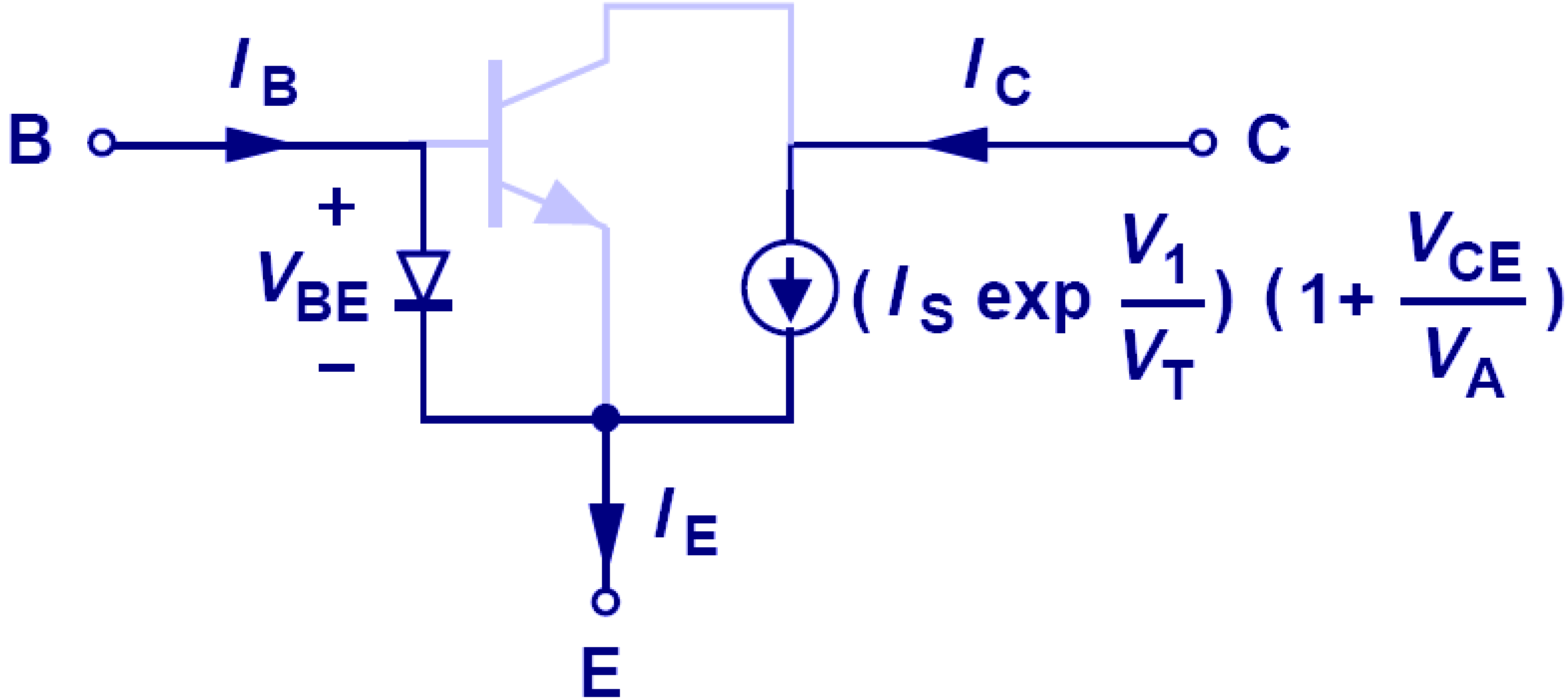
- **With Early effect, collector current becomes larger than usual and a function of V_{CE}.**

Early Effect Representation



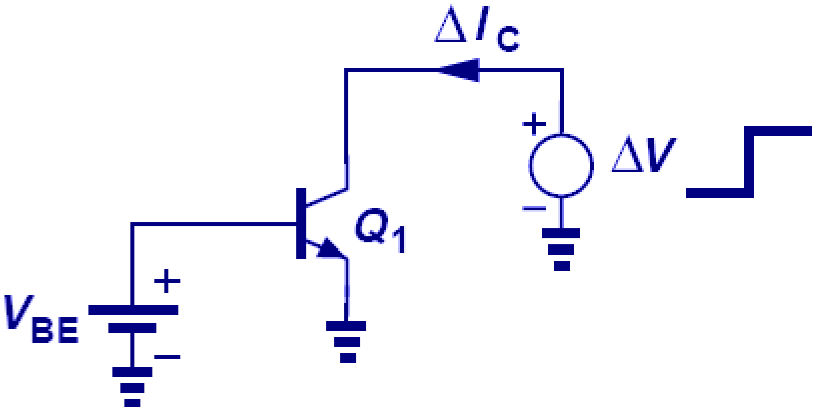
$$\left(I_S \exp \frac{V_1}{V_T}\right)\left(1+\frac{V_X}{V_A}\right)$$

Early Effect and Large-Signal Model

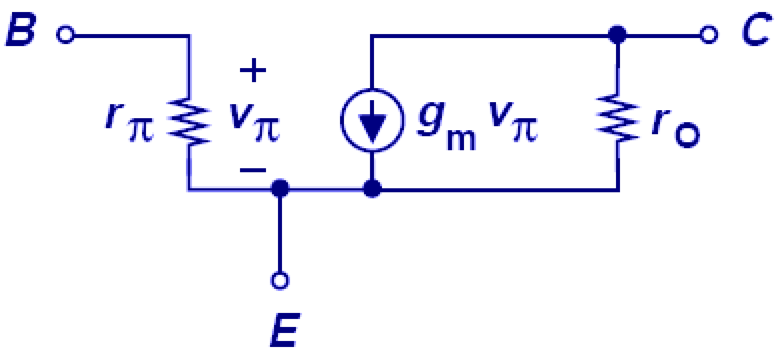


- Early effect can be accounted for in large-signal model by simply changing the collector current with a correction factor.
- In this mode, base current does not change.

Early Effect and Small-Signal Model



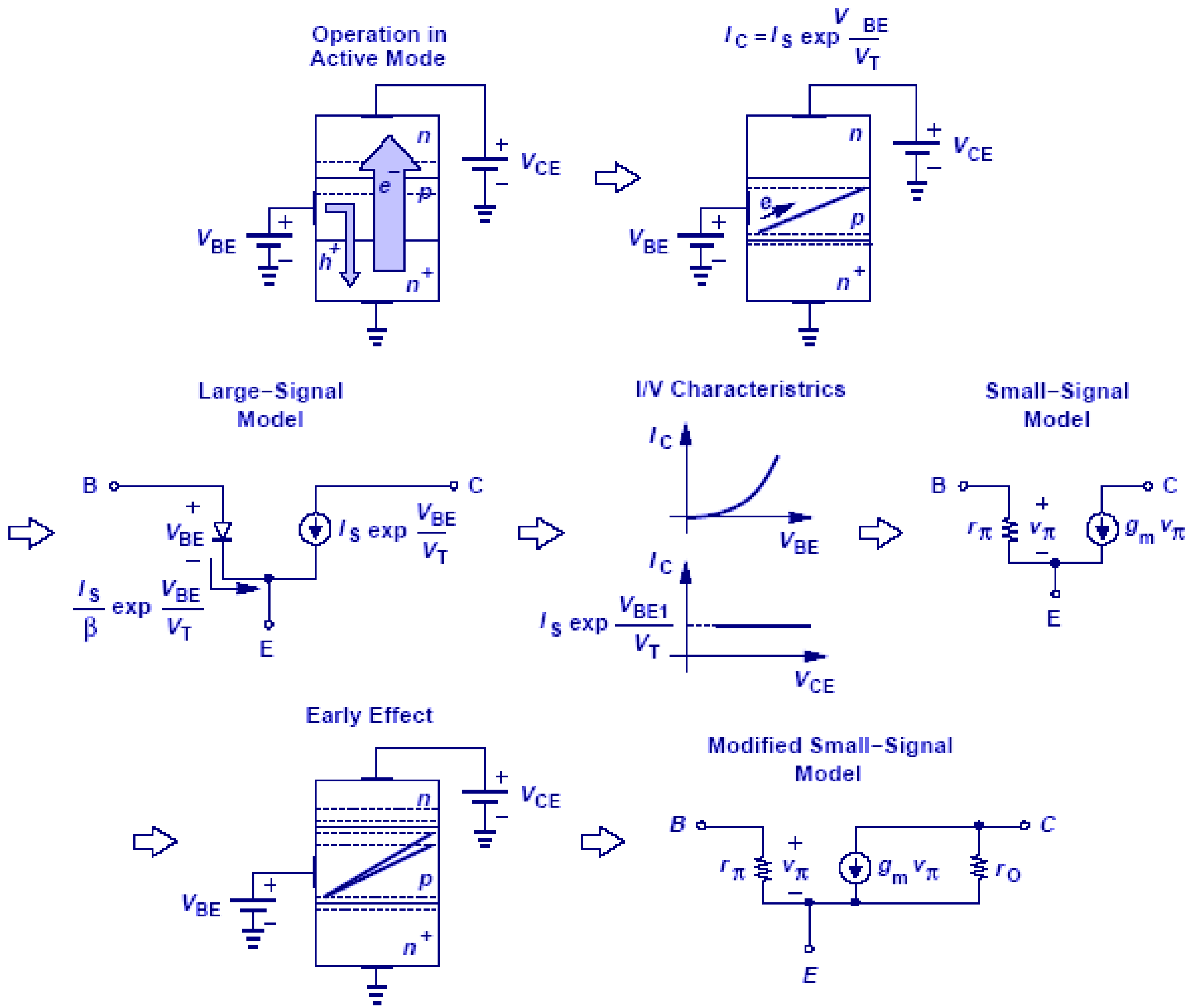
(a)



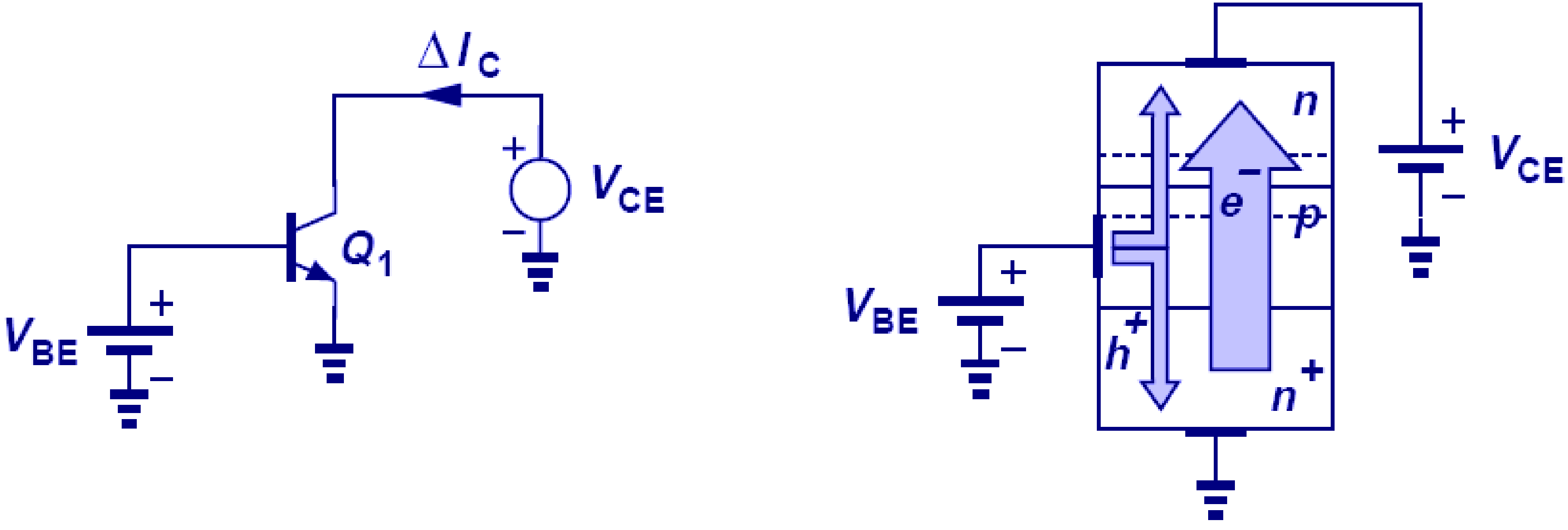
(b)

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{V_A}{I_S \exp\frac{V_{BE}}{V_T}} \approx \frac{V_A}{I_C}$$

Summary of Ideas



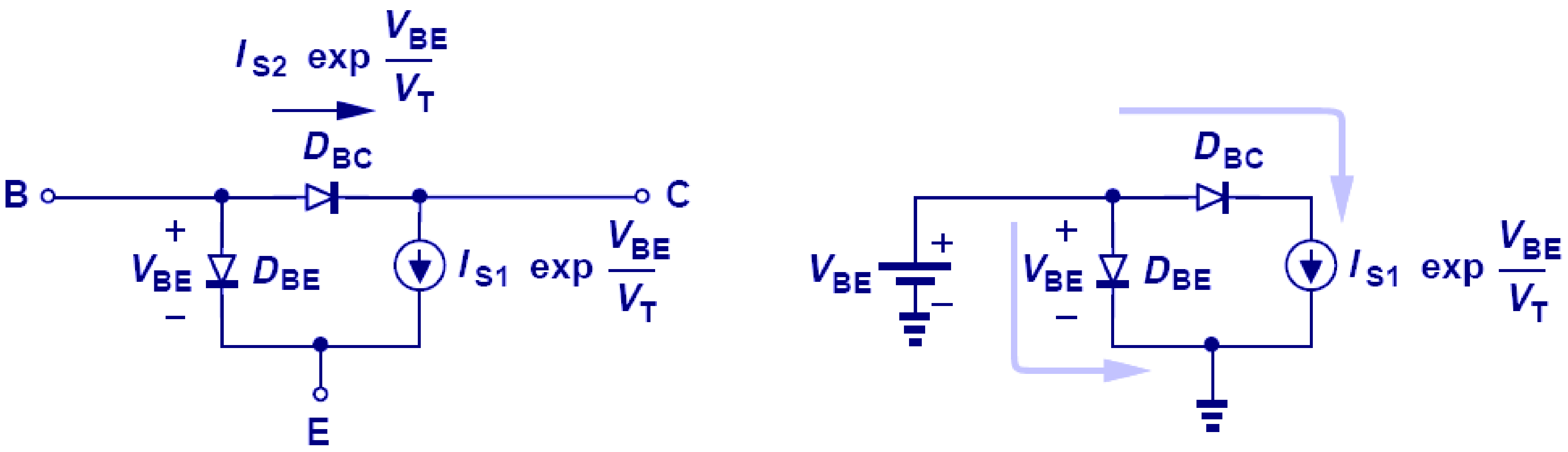
Bipolar Transistor in Saturation



(a) (b)

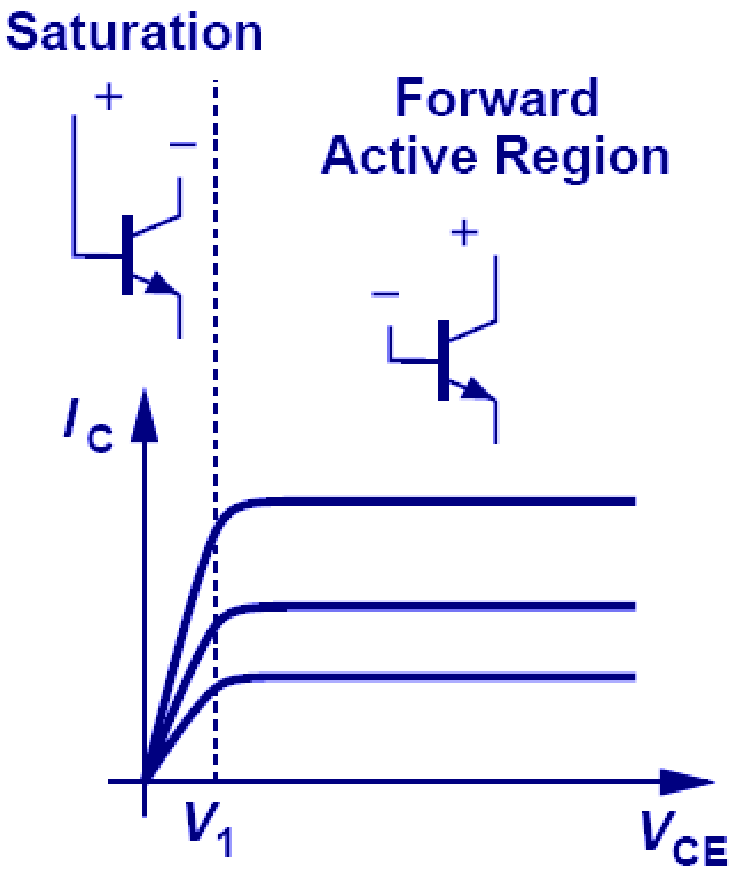
- **When collector voltage drops below base voltage and forward biases the collector-base junction, base current increases and decreases the current gain factor, β.**

Large-Signal Model for Saturation Region



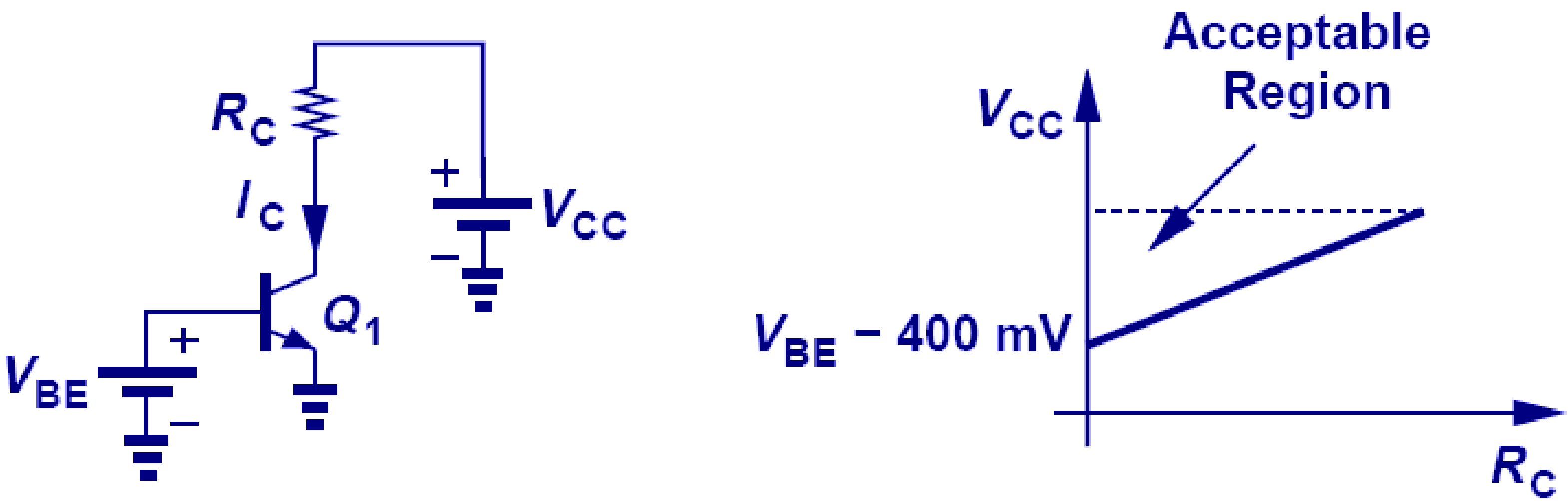
(a) (b)

Overall I/V Characteristics



- **The speed of the BJT also drops in saturation.**

Example: Acceptable V_{CC} Region

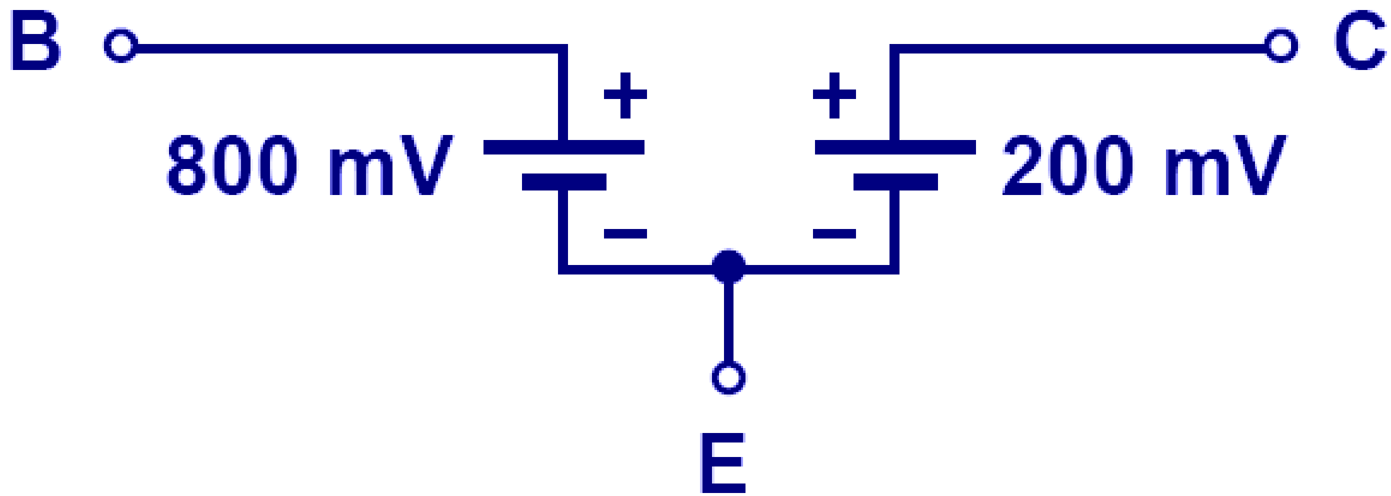


(a) (b)

$$V_{CC} \geq I_C R_C + (V_{BE} - 400mV)$$

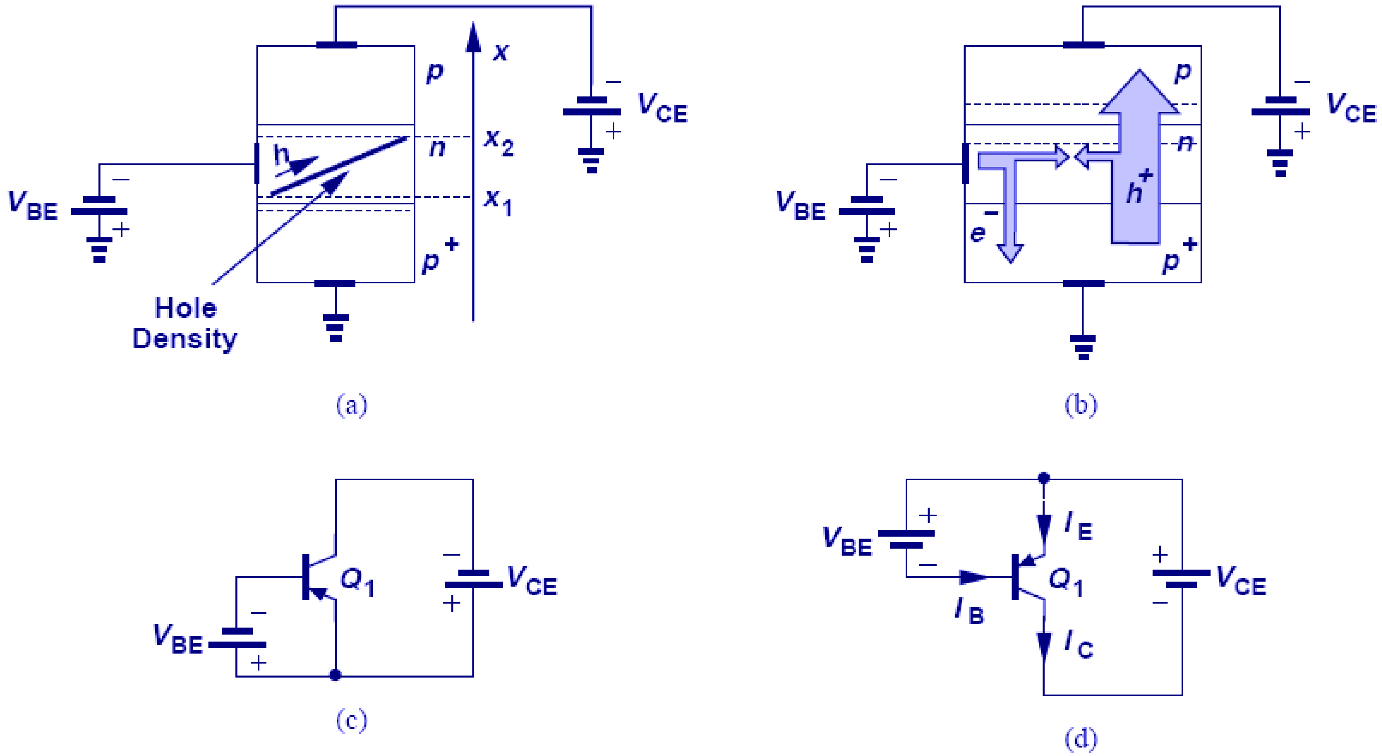
- In order to keep BJT at least in soft saturation region, the collector voltage must not fall below the base voltage by more than 400mV.
- A linear relationship can be derived for V_{CC} and R_C and an acceptable region can be chosen.

Deep Saturation



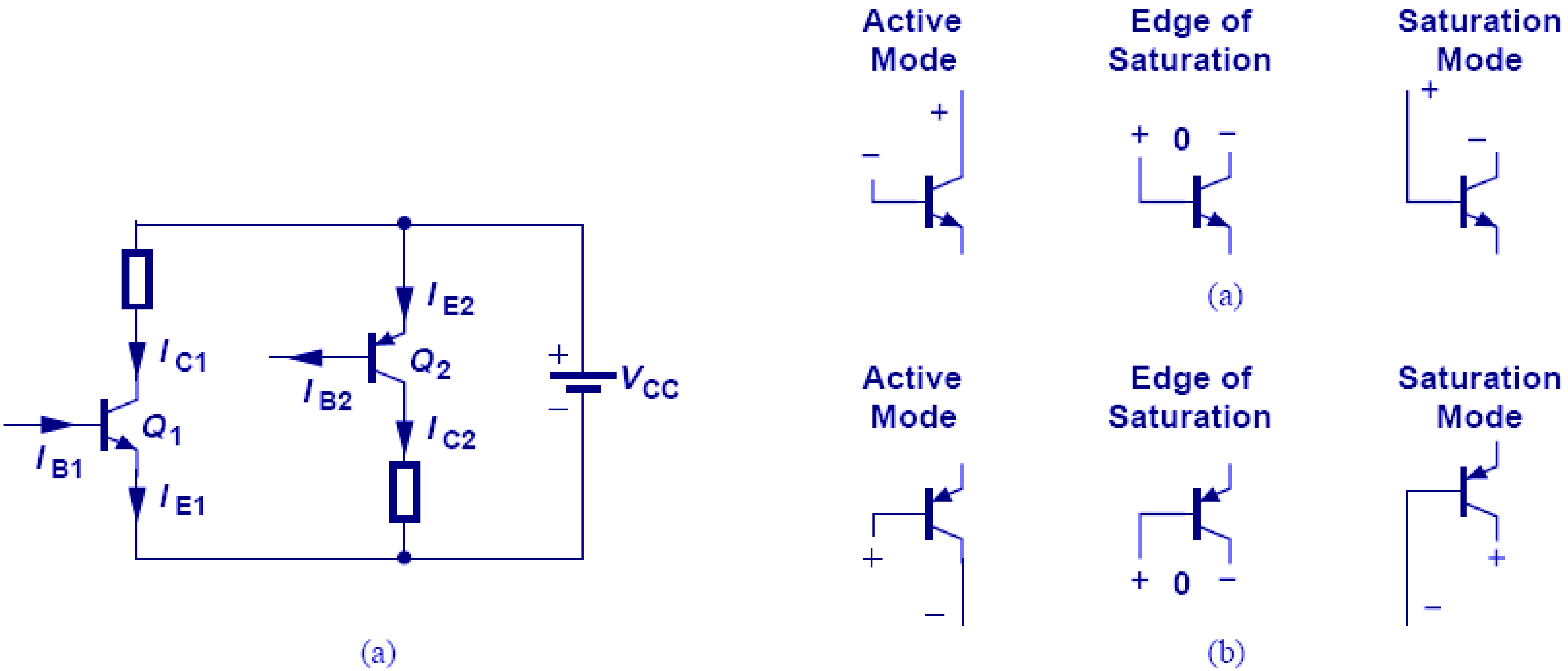
- In deep saturation region, the transistor loses its voltage-controlled current capability and V_{CE} becomes constant.

PNP Transistor



- **With the polarities of emitter, collector, and base reversed, a PNP transistor is formed.**
- **All the principles that applied to NPN's also apply to PNP's, with the exception that emitter is at a higher potential than base and base at a higher potential than collector.**

A Comparison between NPN and PNP Transistors



- The figure above summarizes the direction of current flow and operation regions for both the NPN and PNP BJT's.

PNP Equations

$$I_C = I_S \exp\frac{V_{EB}}{V_T}$$

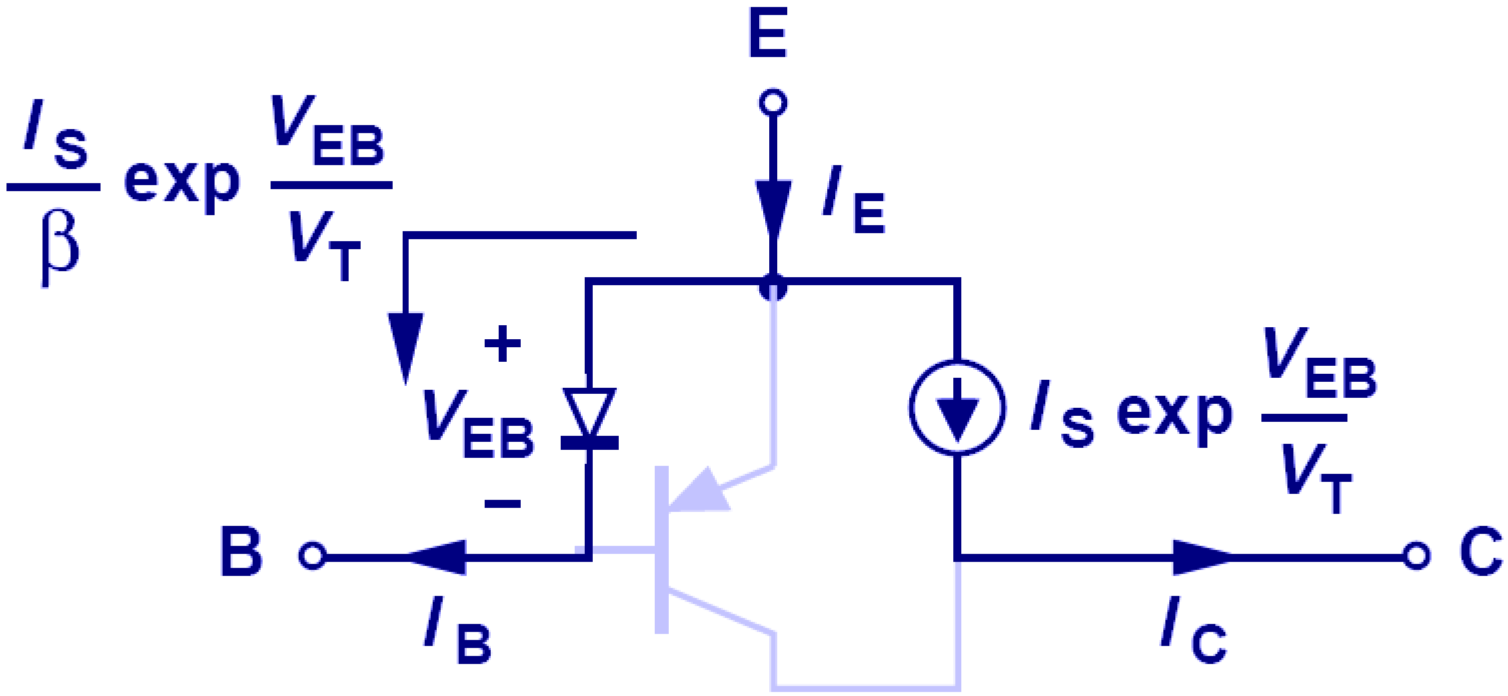
$$I_B = \frac{I_S}{\beta}\exp\frac{V_{EB}}{V_T}$$

$$I_E = \frac{\beta+1}{\beta} I_S \exp\frac{V_{EB}}{V_T}$$

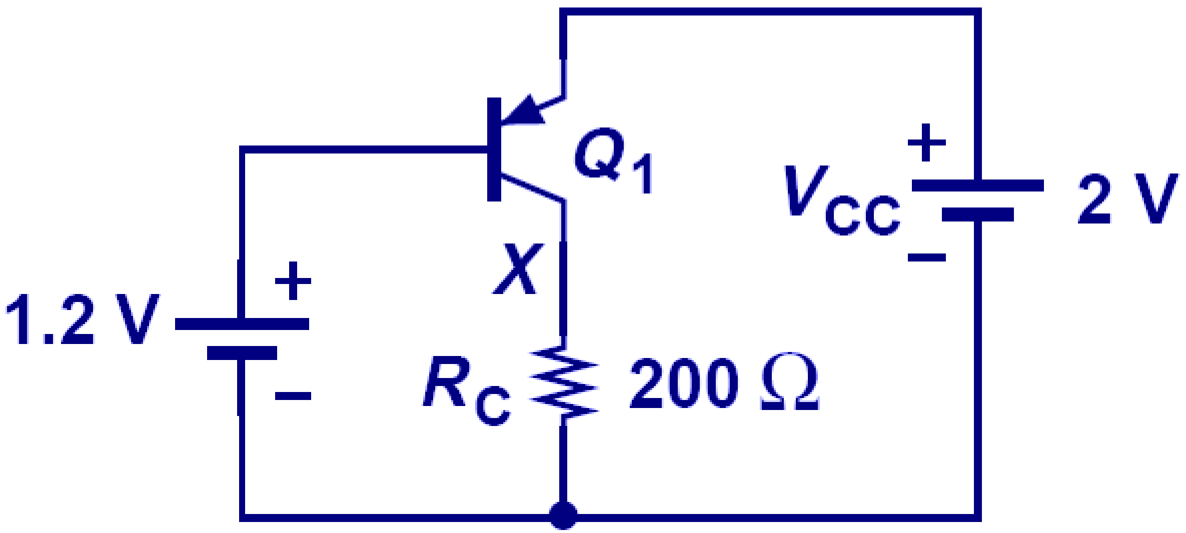
Early Effect $\Rightarrow$

$$I_C = \left(I_S \exp\frac{V_{EB}}{V_T}\right)\left(1+\frac{V_{EC}}{V_A}\right)$$

Large Signal Model for PNP

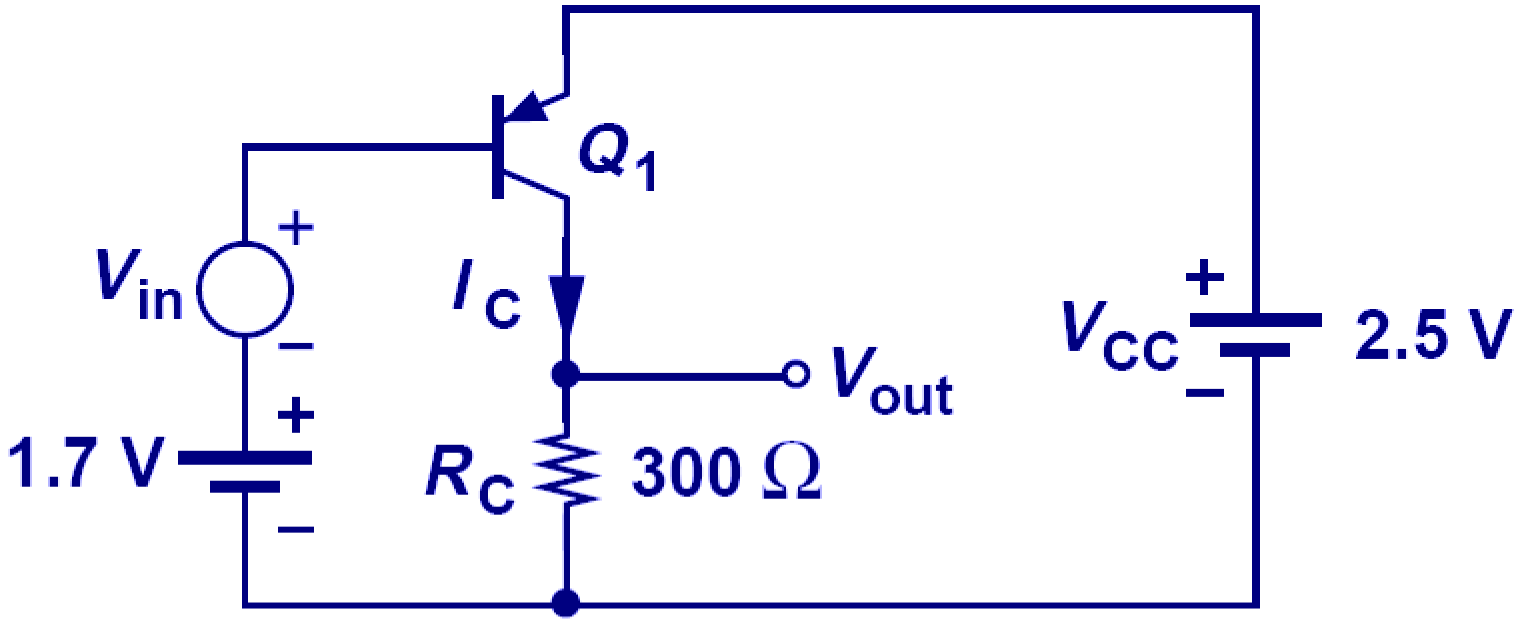


PNP Biasing

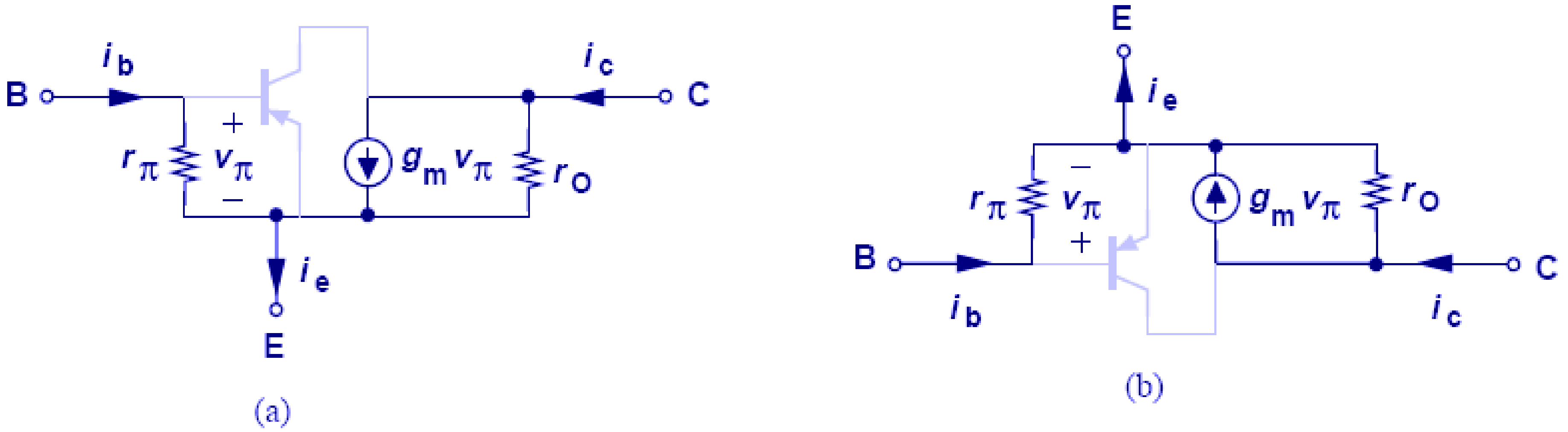


- **Note that the emitter is at a higher potential than both the base and collector.**

Small Signal Analysis

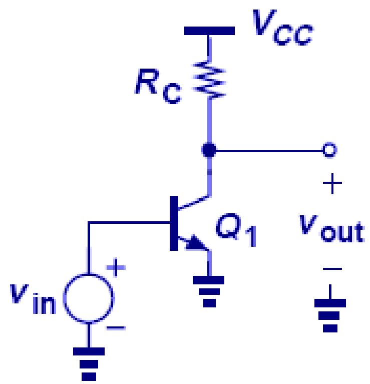


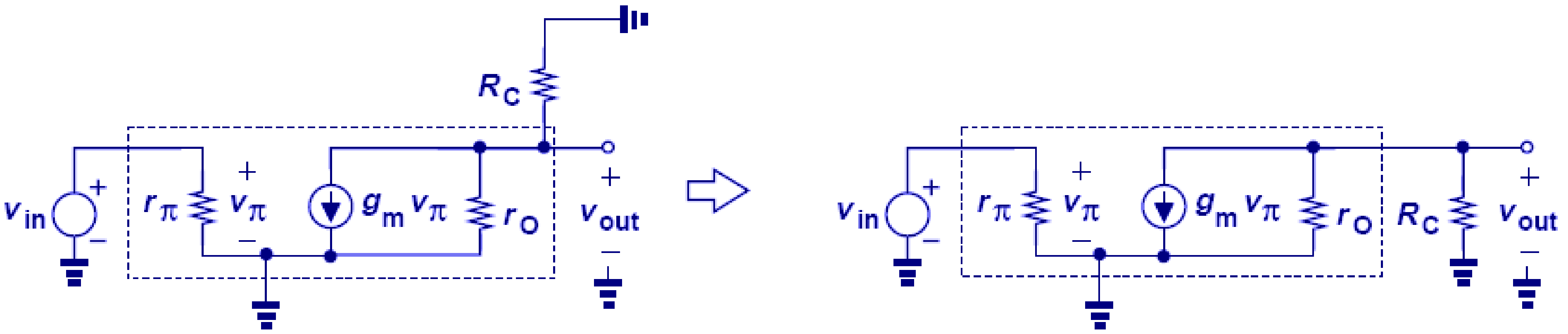
Small-Signal Model for PNP Transistor



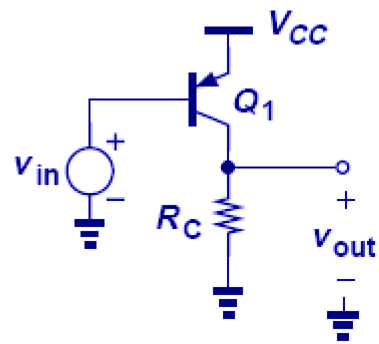
- **The small signal model for PNP transistor is exactly IDENTICAL to that of NPN. This is not a mistake because the current direction is taken care of by the polarity of V_{BE}.**

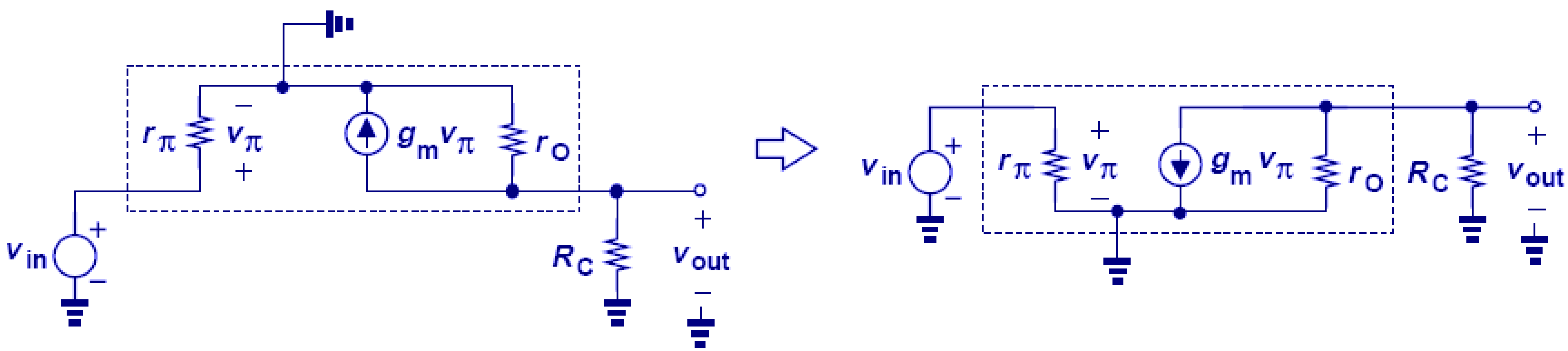
Small Signal Model Example I





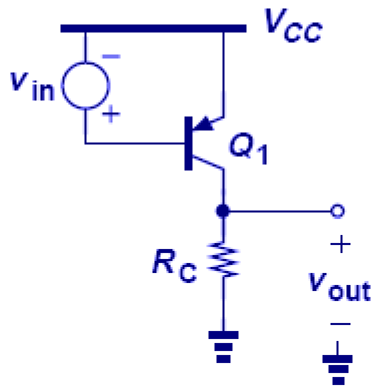
Small Signal Model Example II



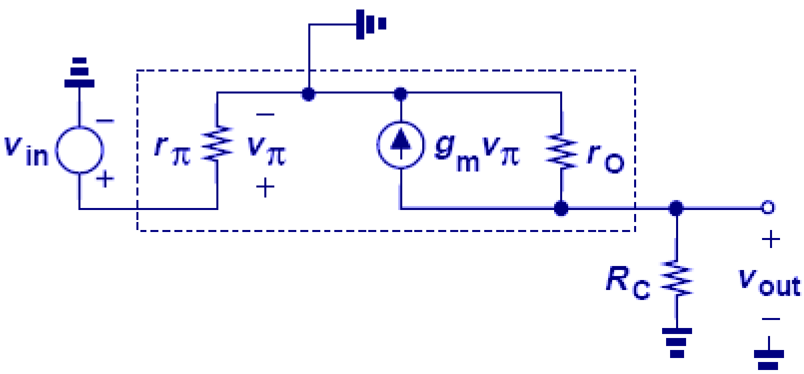


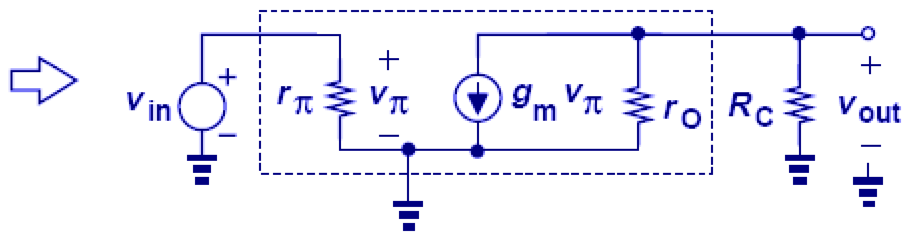
- **Small-signal model is identical to the previous ones.**

Small Signal Model Example III



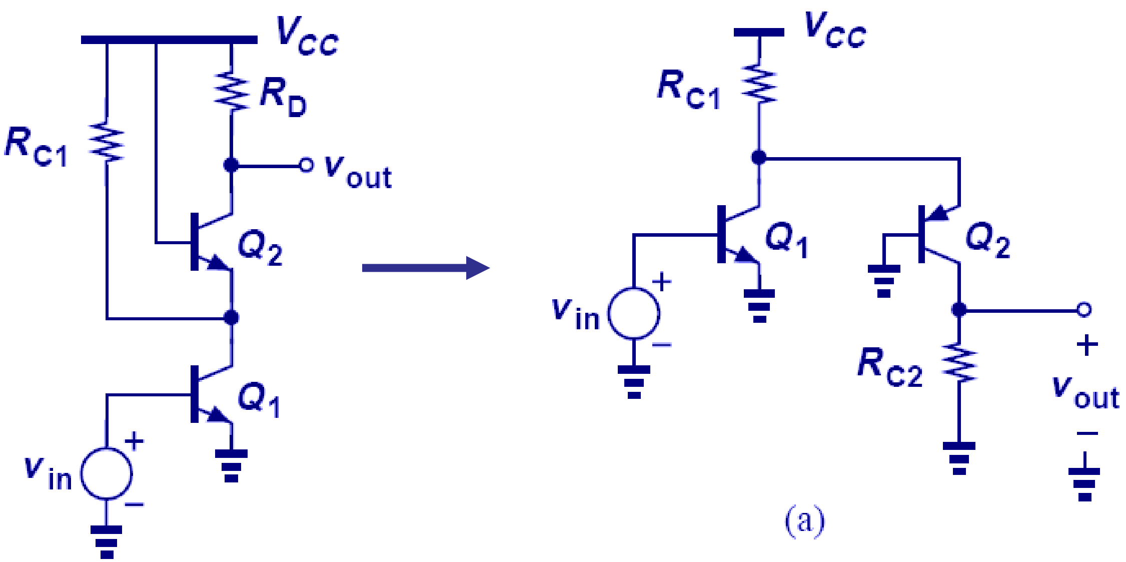
(c)



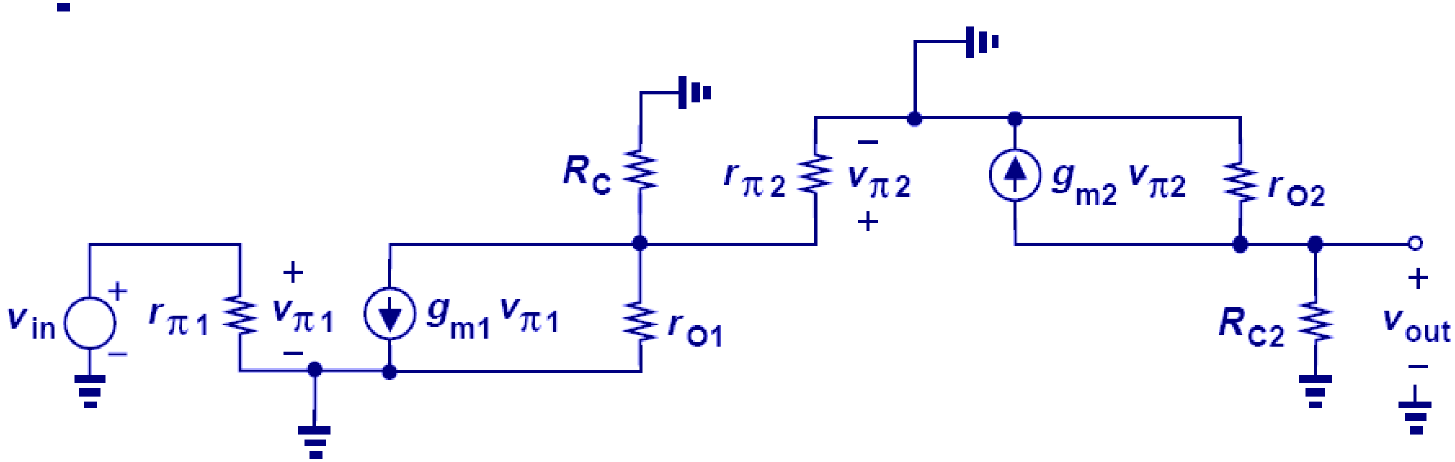


- **Since during small-signal analysis, a constant voltage supply is considered to be AC ground, the final small-signal model is identical to the previous two.**

Small Signal Model Example IV



(a)



(b)

Chapter 5 Bipolar Amplifiers

- 5.1 General Considerations
- 5.2 Operating Point Analysis and Design
- 5.3 Bipolar Amplifier Topologies
- 5.4 Summary and Additional Examples

Bipolar Amplifiers

General Concepts

- Input and Output Impedances
- Biasing
- DC and Small−Signal Analysis

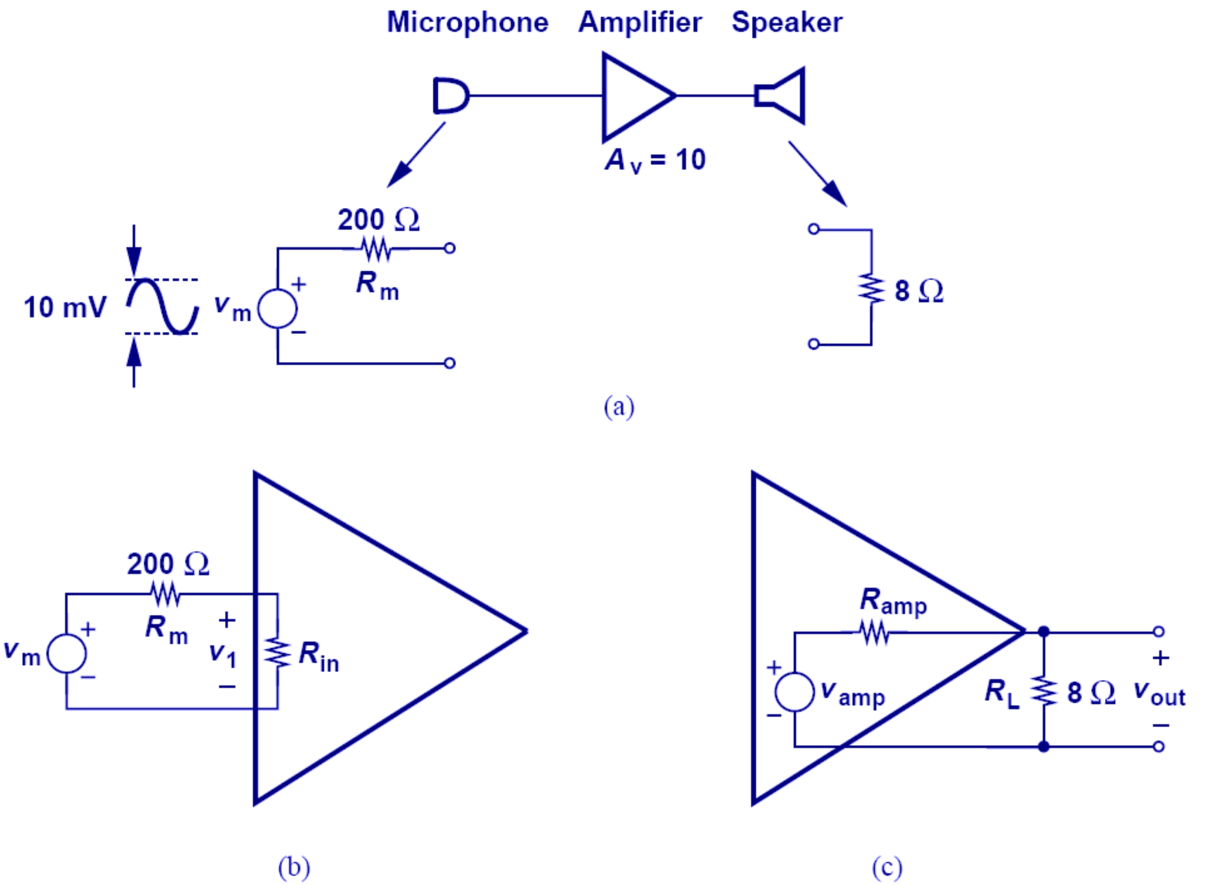
Operating Point Analysis

- Simple Biasing
- Emitter Degeneration
- Self−Biasing
- Biasing of PNP Devices

Amplifier Topologies

- Common−Emitter Stage
- Common−Base Stage
- Emtter Follower

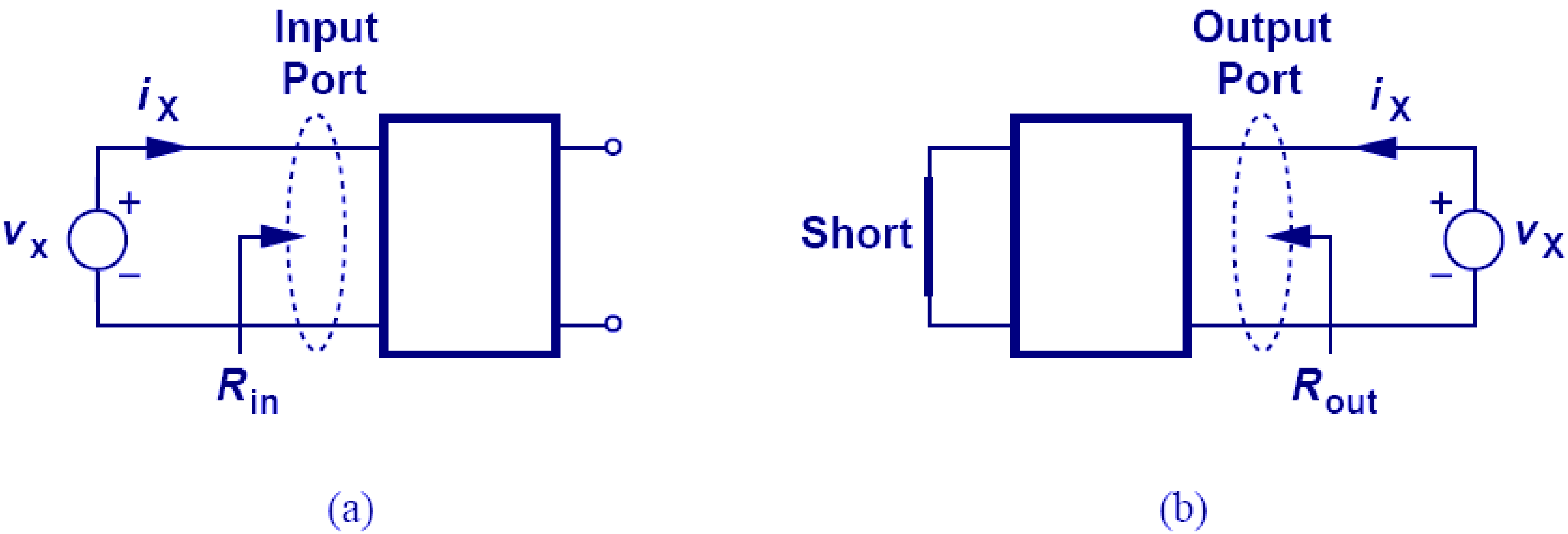
Voltage Amplifier



(a) (b) (c)

- In an ideal voltage amplifier, the input impedance is infinite and the output impedance zero.
- But in reality, input or output impedances depart from their ideal values.

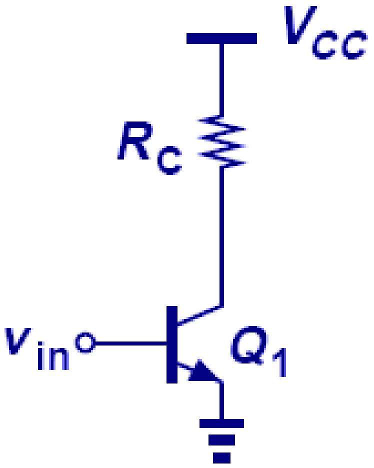
Input/Output Impedances



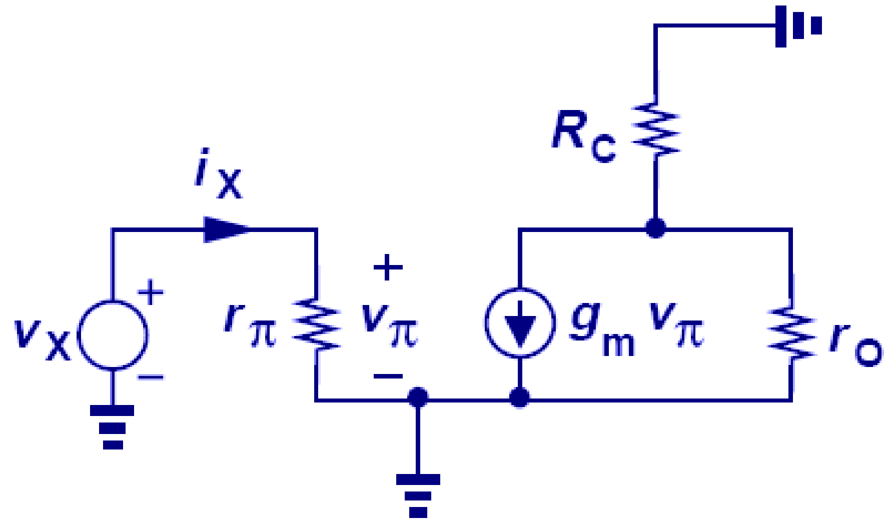
$$R_x = \frac{V_x}{i_x}$$

- **The figure above shows the techniques of measuring input and output impedances.**

Input Impedance Example I



(a)

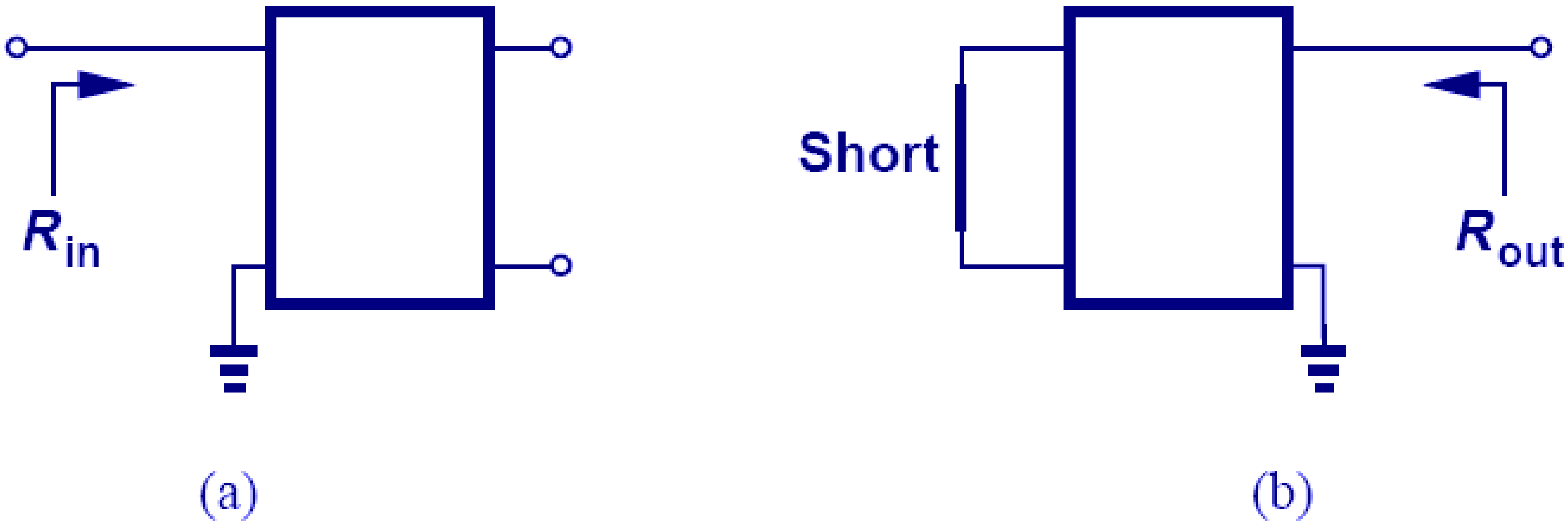


(b)

$$\frac{v_x}{i_x} = r_\pi$$

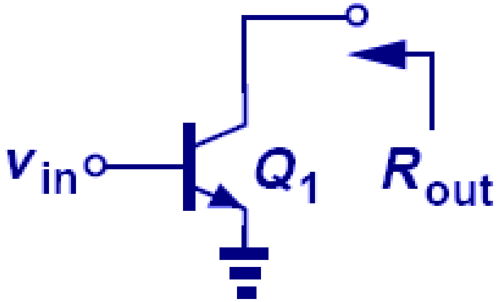
- **When calculating input/output impedance, small-signal analysis is assumed.**

Impedance at a Node

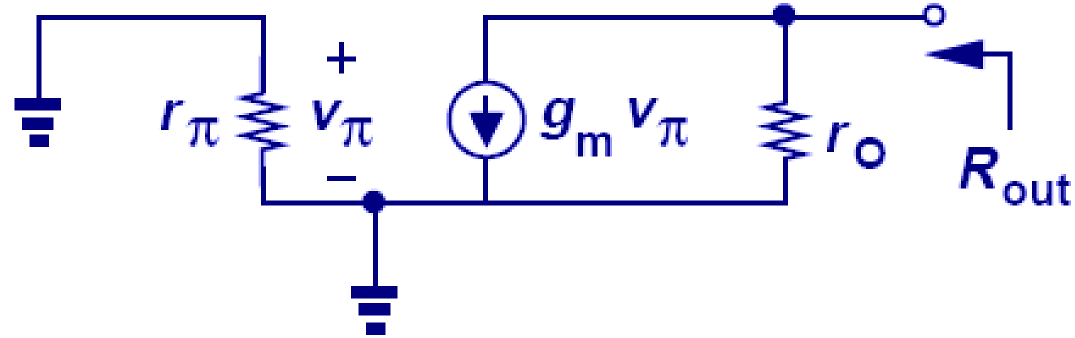


- **When calculating I/O impedances at a port, we usually ground one terminal while applying the test source to the other terminal of interest.**

Impedance at Collector



(a)

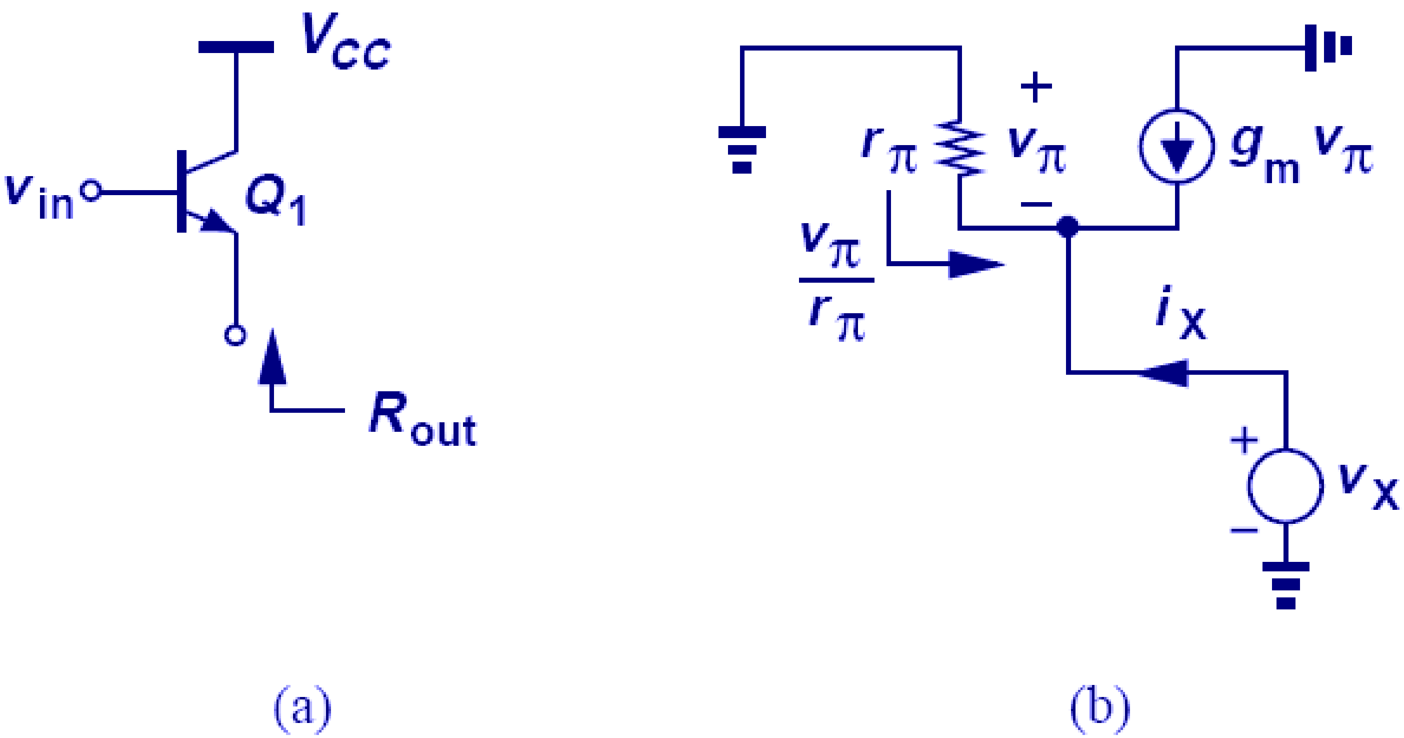


(b)

$$R_{out} = r_o$$

- **With Early effect, the impedance seen at the collector is equal to the intrinsic output impedance of the transistor (if emitter is grounded).**

Impedance at Emitter



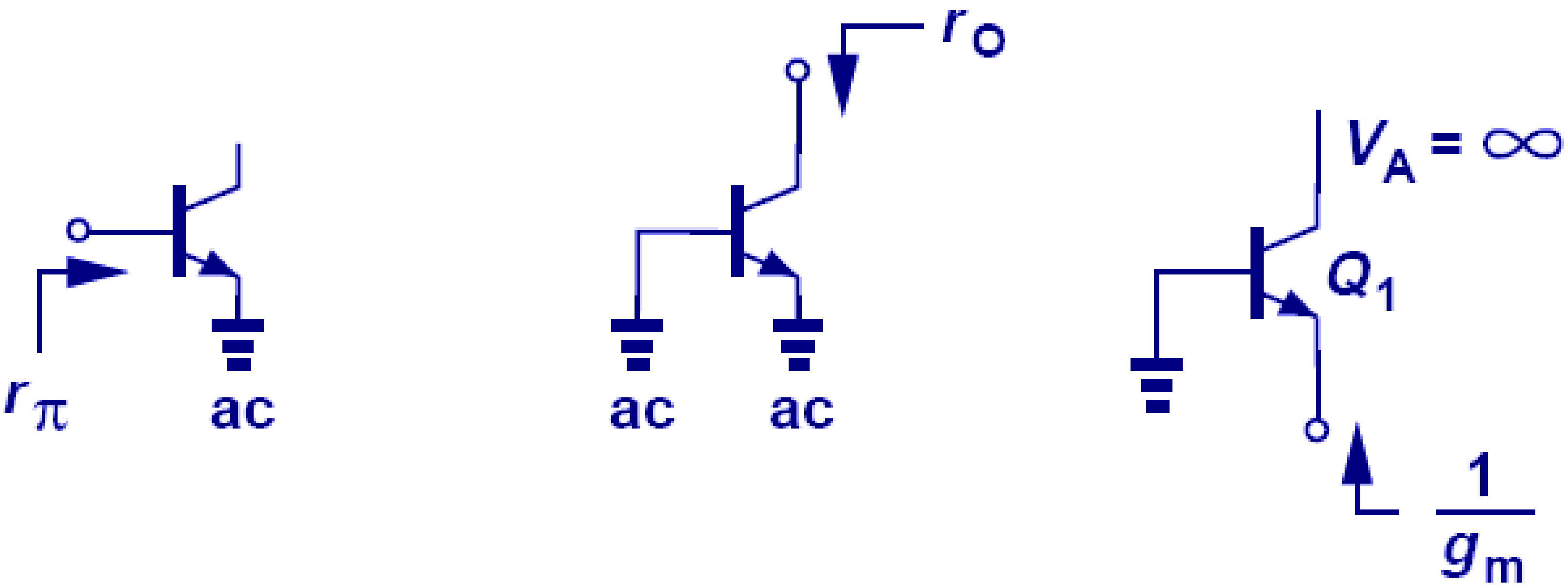
$$\frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{r_\pi}}$$

$$R_{out} \approx \frac{1}{g_m}$$

$$(V_A = \infty)$$

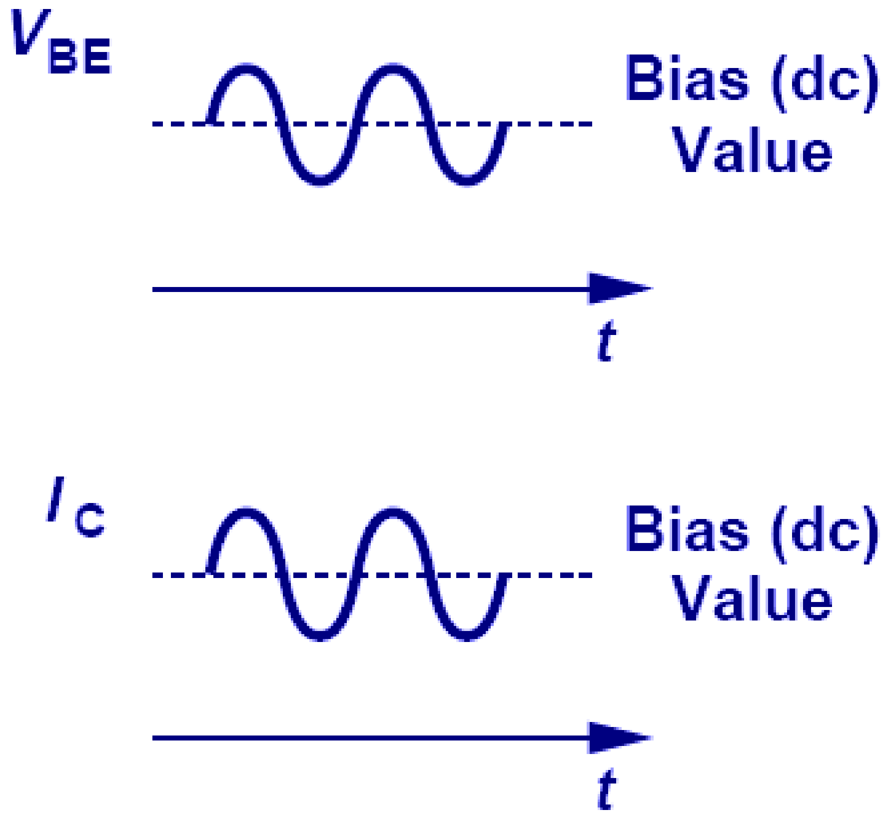
- **The impedance seen at the emitter of a transistor is approximately equal to one over its transconductance (if the base is grounded).**

Three Master Rules of Transistor Impedances



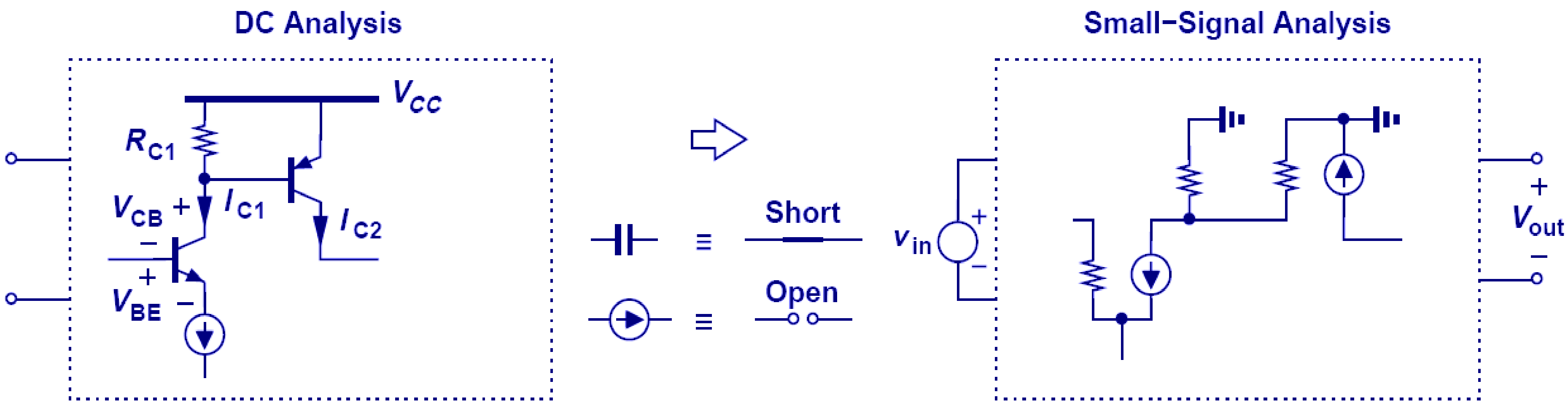
- **Rule # 1: looking into the base, the impedance is r_π if emitter is (ac) grounded.**
- **Rule # 2: looking into the collector, the impedance is r_o if emitter is (ac) grounded.**
- **Rule # 3: looking into the emitter, the impedance is $1/g_m$ if base is (ac) grounded and Early effect is neglected.**

Biasing of BJT



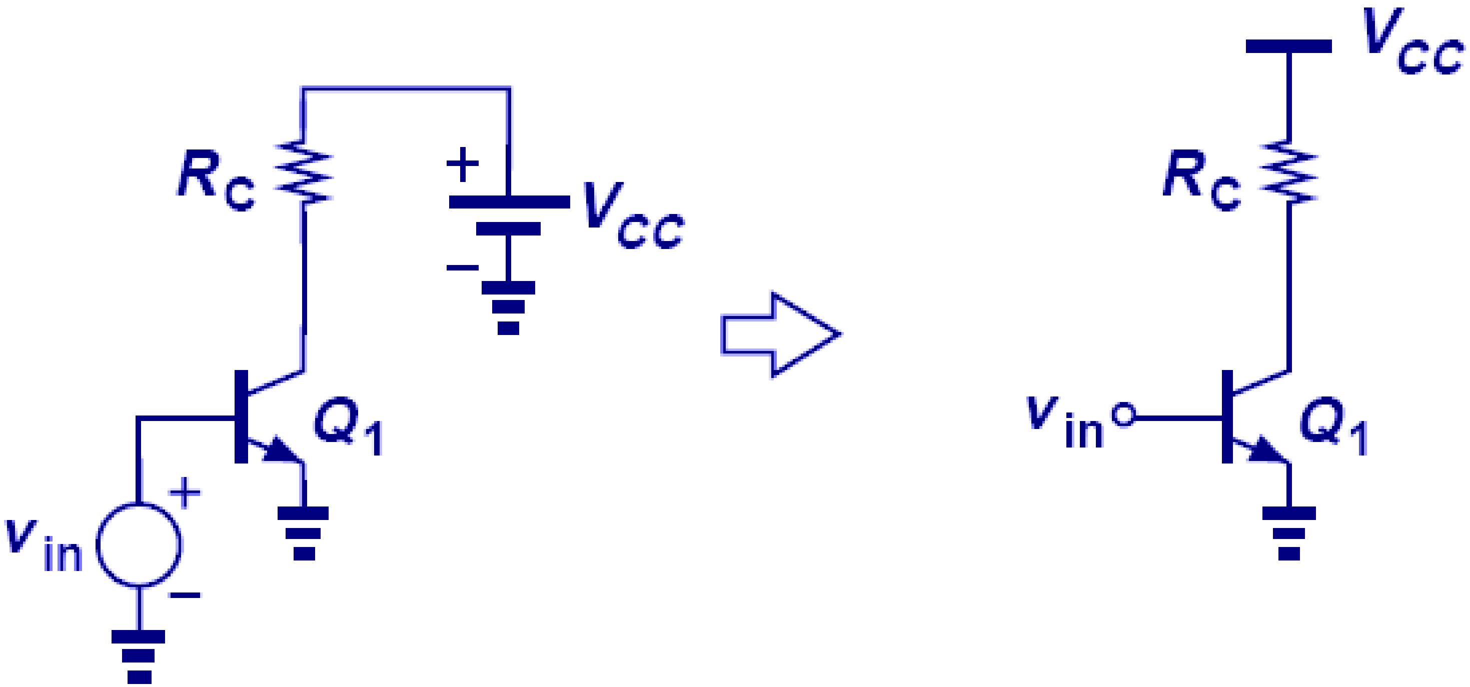
- **Transistors and circuits must be biased because (1) transistors must operate in the active region, (2) their small-signal parameters depend on the bias conditions.**

DC Analysis vs. Small-Signal Analysis



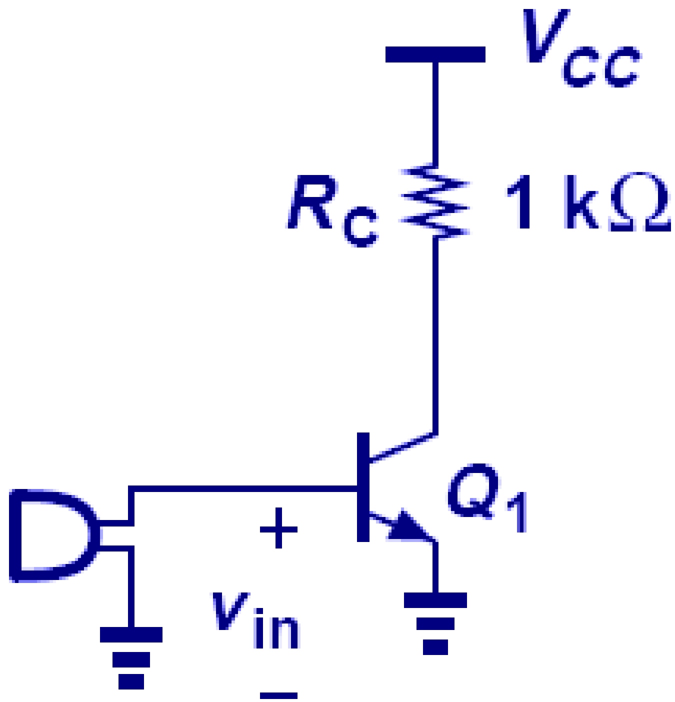
- **First, DC analysis is performed to determine operating point and obtain small-signal parameters.**
- **Second, sources are set to zero and small-signal model is used.**

Notation Simplification



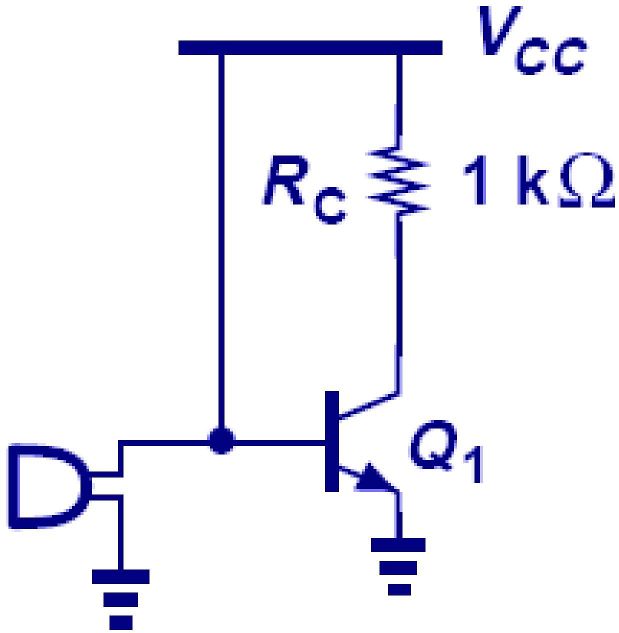
- Hereafter, the battery that supplies power to the circuit is replaced by a horizontal bar labeled Vcc, and input signal is simplified as one node called $V_{in.}$

Example of Bad Biasing



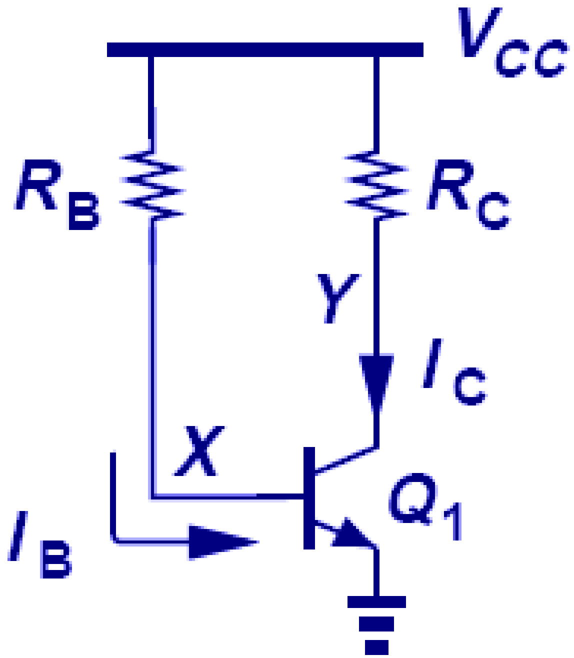
- **The microphone is connected to the amplifier in an attempt to amplify the small output signal of the microphone.**
- **Unfortunately, there's no DC bias current running thru the transistor to set the transconductance.**

Another Example of Bad Biasing



- **The base of the amplifier is connected to V_{cc}, trying to establish a DC bias.**
- **Unfortunately, the output signal produced by the microphone is shorted to the power supply.**

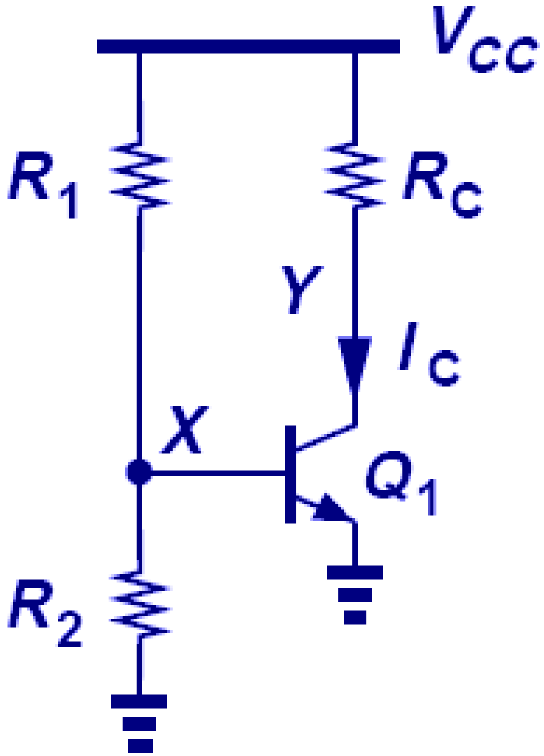
Biasing with Base Resistor



$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, I_C = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

- **Assuming a constant value for V_{BE}, one can solve for both I_B and I_C and determine the terminal voltages of the transistor.**
- **However, bias point is sensitive to β variations.**

Improved Biasing: Resistive Divider

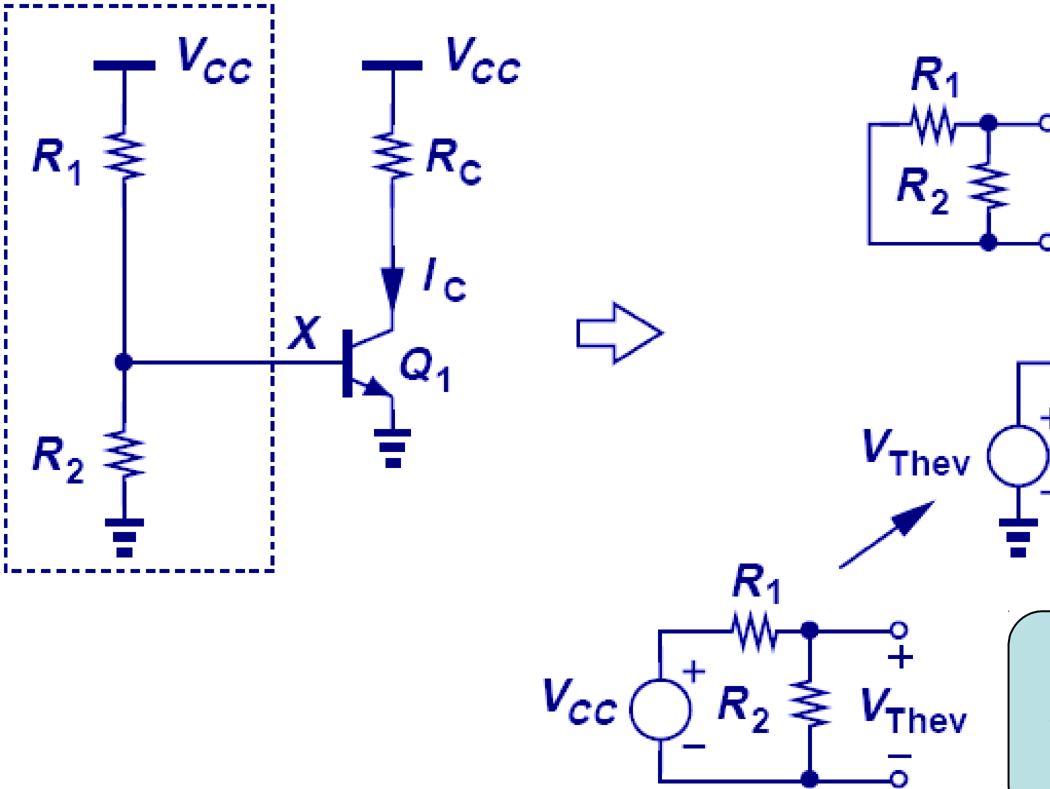


$$V_X = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \frac{V_{CC}}{V_T}\right)$$

- **Using resistor divider to set V_{BE}, it is possible to produce an I_C that is relatively independent of β if base current is small.**

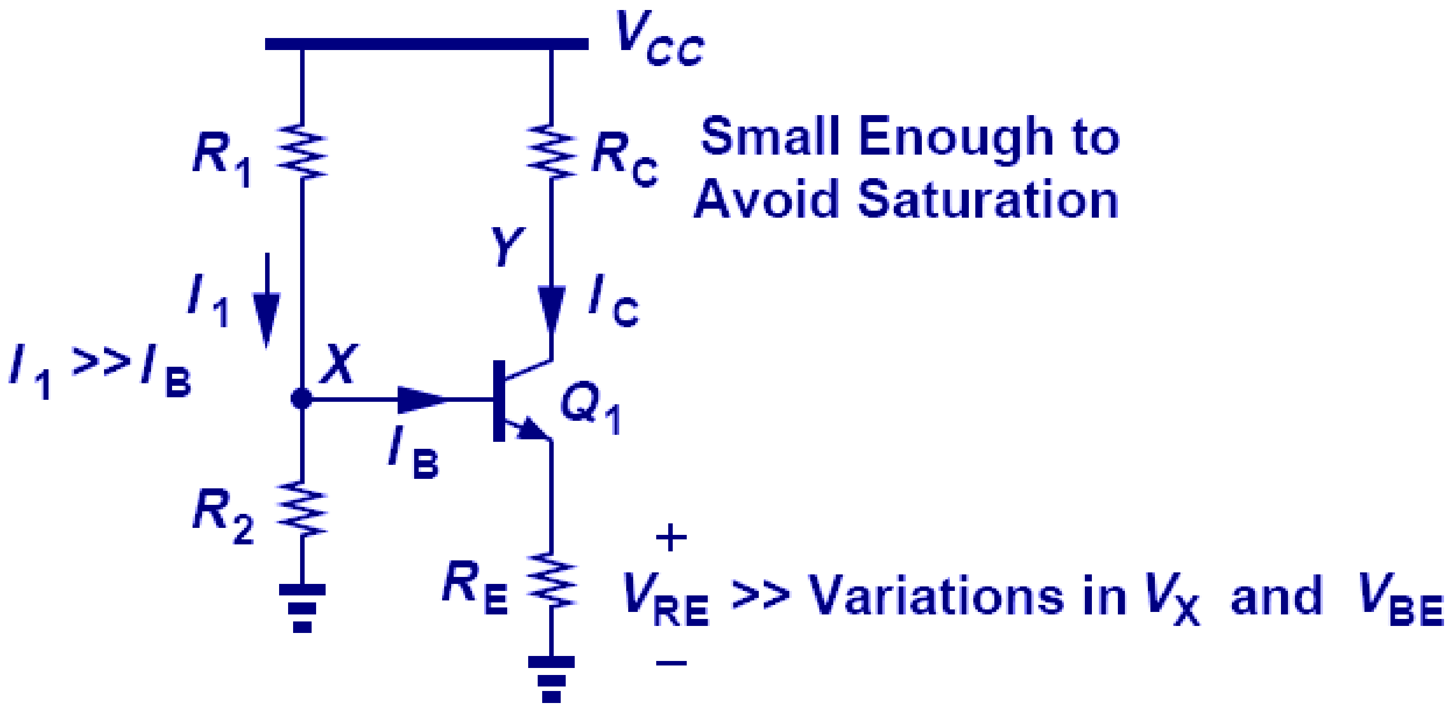
Accounting for Base Current



$$I_C = I_S \exp\left(\frac{V_{Thev} - I_B R_{Thev}}{V_T}\right)$$

- **With proper ratio of R_1 and R_2, I_C can be insensitive to β; however, its exponential dependence on resistor deviations makes it less useful.**

Emitter Degeneration Biasing

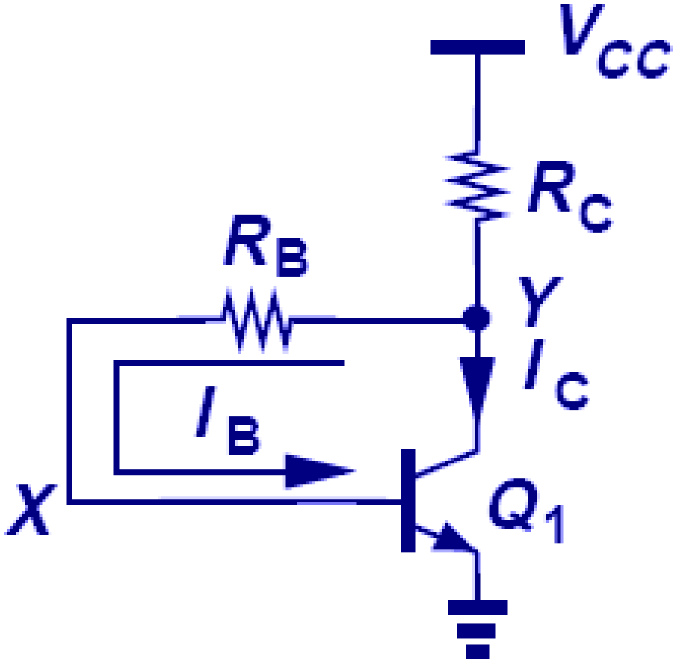


- **The presence of R_E helps to absorb the error in V_X so V_{BE} stays relatively constant.**
- **This bias technique is less sensitive to β ($I_1 >> I_B$) and V_{BE} variations.**

Design Procedure

- Choose an I_C to provide the necessary small signal parameters, g_m, r_π, etc.
- Considering the variations of R_1, R_2, and V_{BE}, choose a value for V_{RE}.
- With V_{RE} chosen, and V_{BE} calculated, V_x can be determined.
- Select R_1 and R_2 to provide V_x.

Self-Biasing Technique



- This bias technique utilizes the collector voltage to provide the necessary V_x and I_B.
- One important characteristic of this technique is that collector has a higher potential than the base, thus guaranteeing active operation of the transistor.

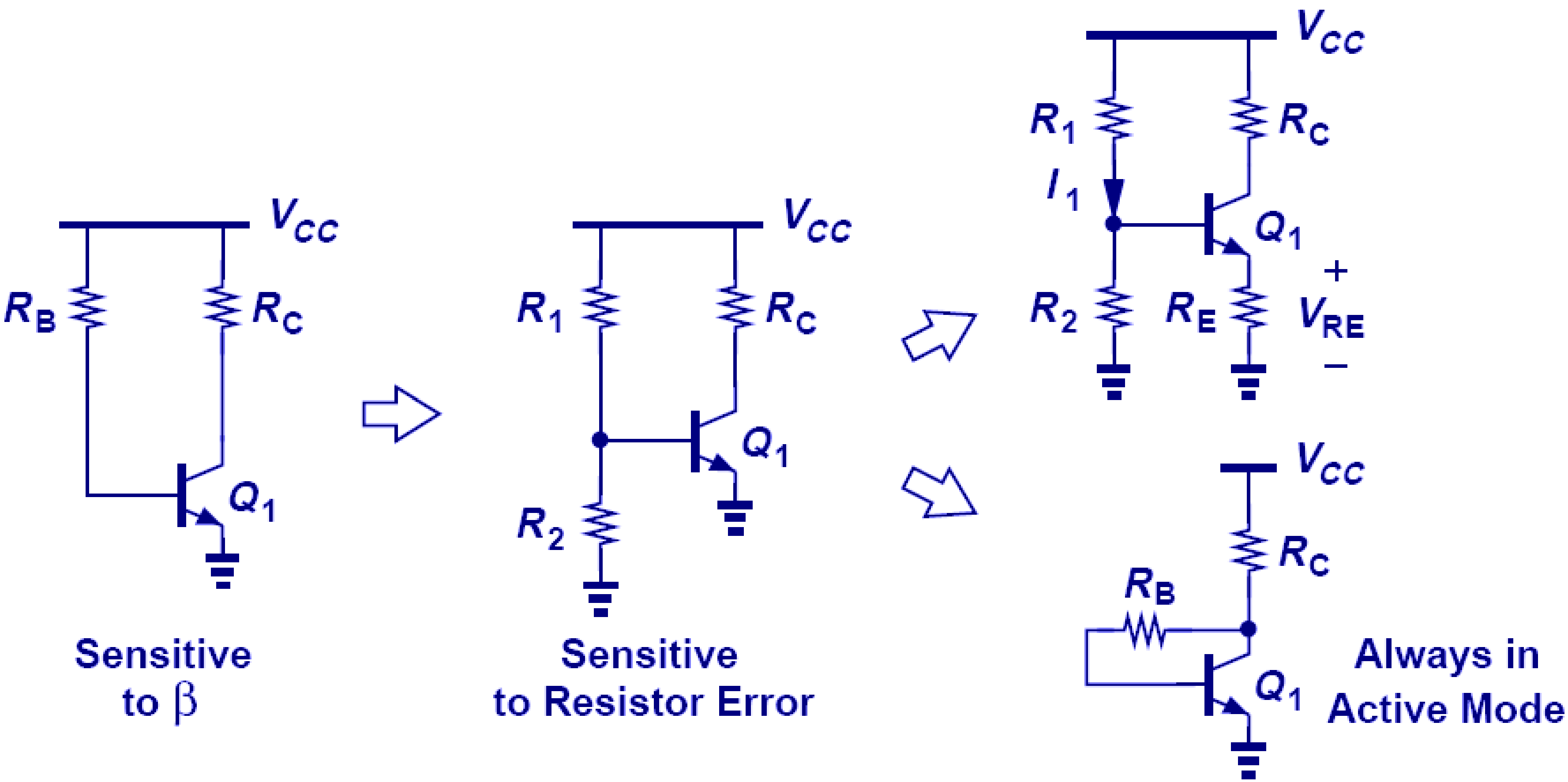
Self-Biasing Design Guidelines

$$(1) \quad R_C \gg \frac{R_B}{\beta}$$

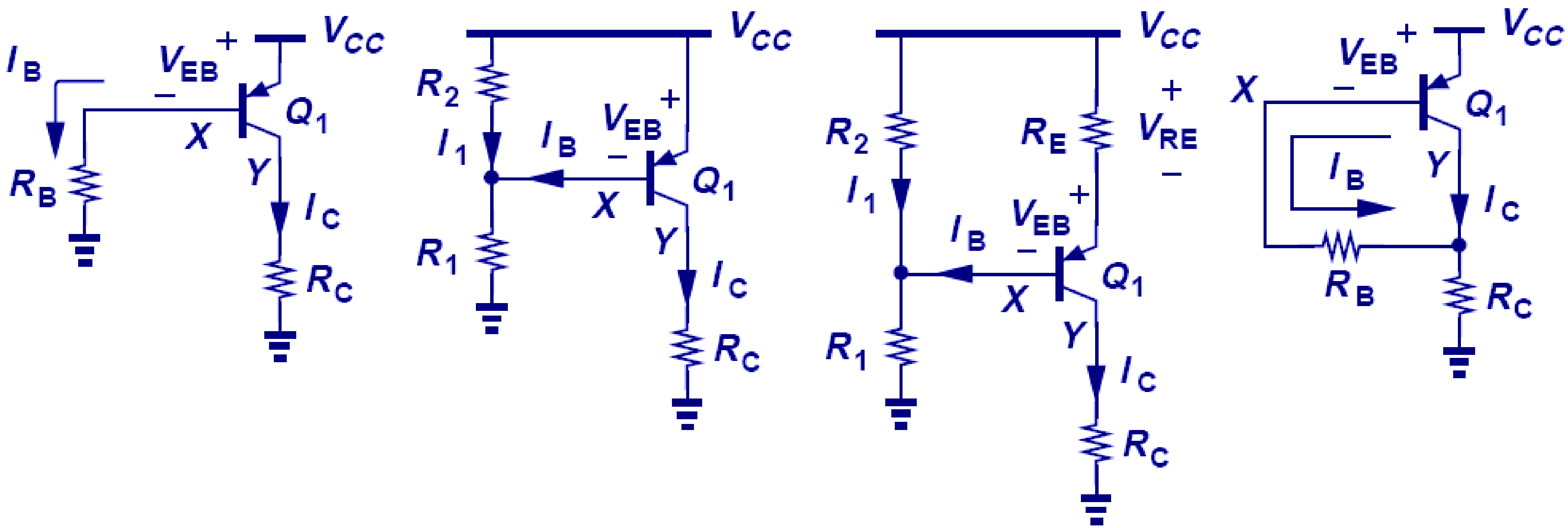
$$(2) \quad \Delta V_{BE} \ll V_{CC} - V_{BE}$$

- **(1) provides insensitivity to β .**
- **(2) provides insensitivity to variation in V_{BE} .**

Summary of Biasing Techniques

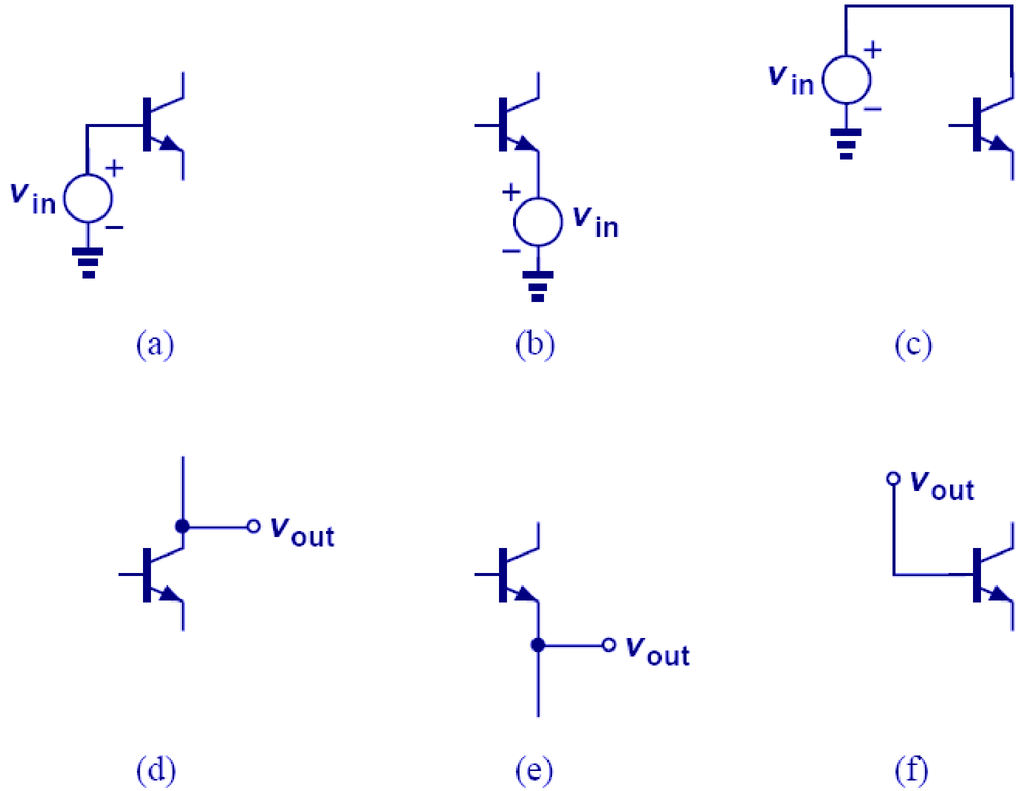


PNP Biasing Techniques



- **Same principles that apply to NPN biasing also apply to PNP biasing with only polarity modifications.**

Possible Bipolar Amplifier Topologies

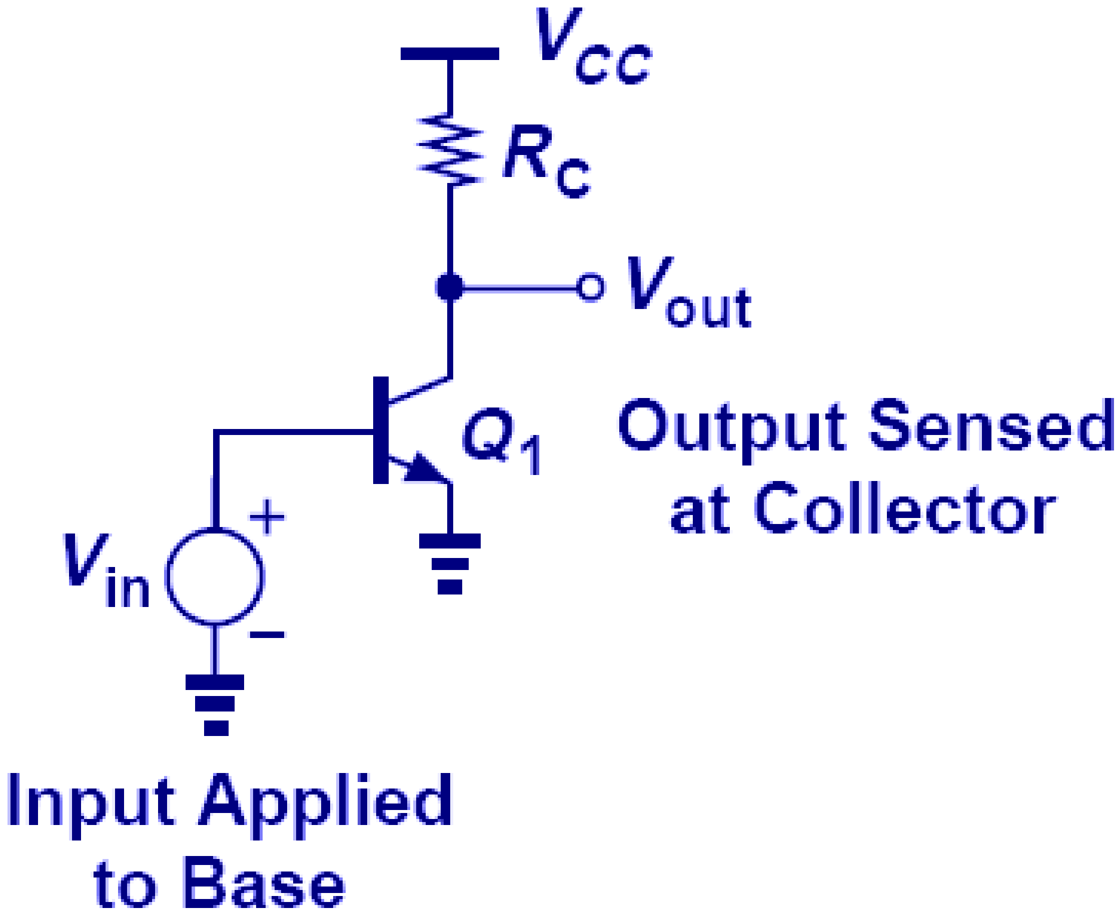


- Three possible ways to apply an input to an amplifier and three possible ways to sense its output.
- However, in reality only three of six input/output combinations are useful.

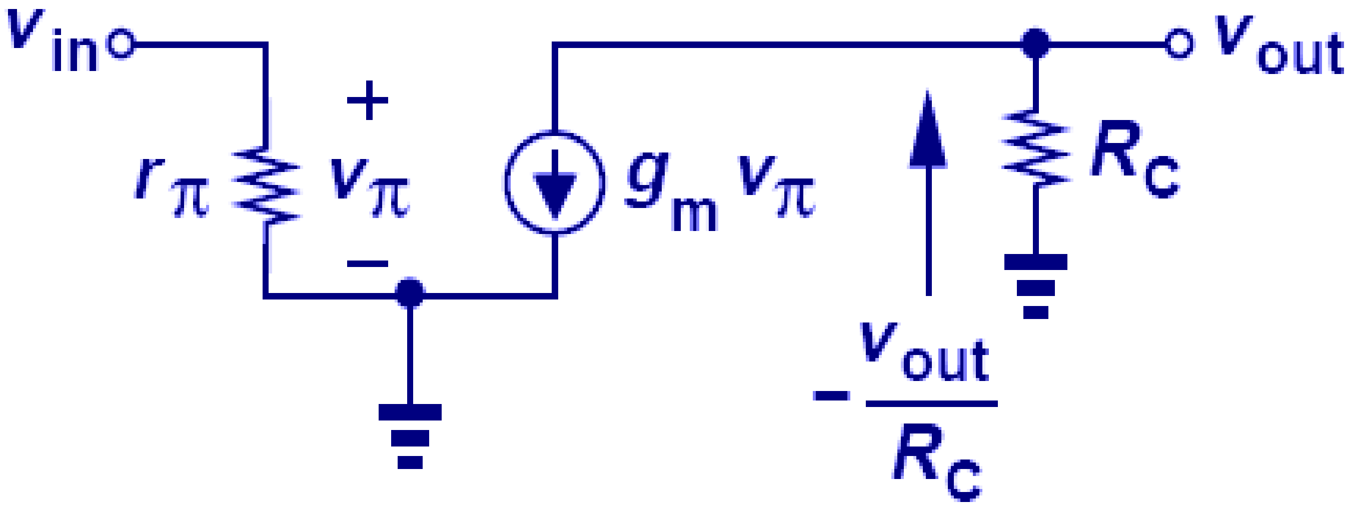
Study of Common-Emitter Topology

- ***Analysis of CE Core***
  - ***Inclusion of Early Effect***
- ***Emitter Degeneration***
  - ***Inclusion of Early Effect***
- ***CE Stage with Biasing***

Common-Emitter Topology



Small Signal of CE Amplifier

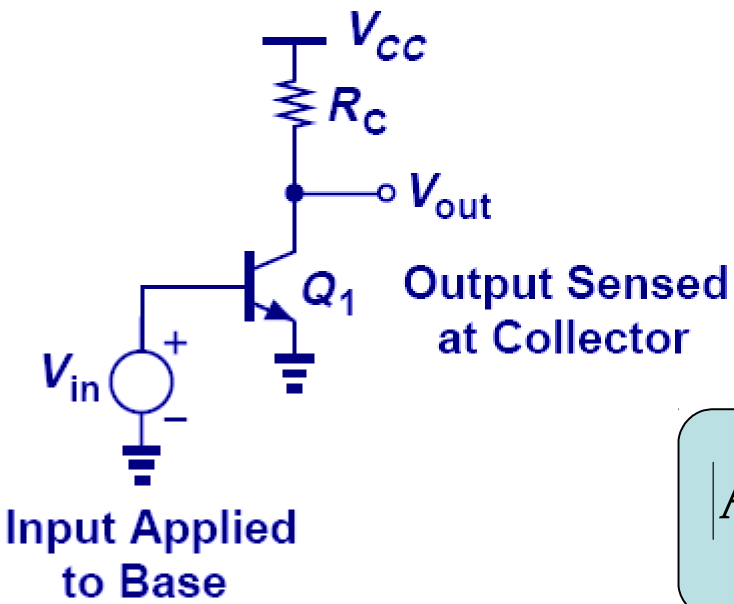


$$A_v = \frac{v_{out}}{v_{in}}$$

$$-\frac{v_{out}}{R_C} = g_m v_\pi = g_m v_{in}$$

$$A_v = -g_m R_C$$

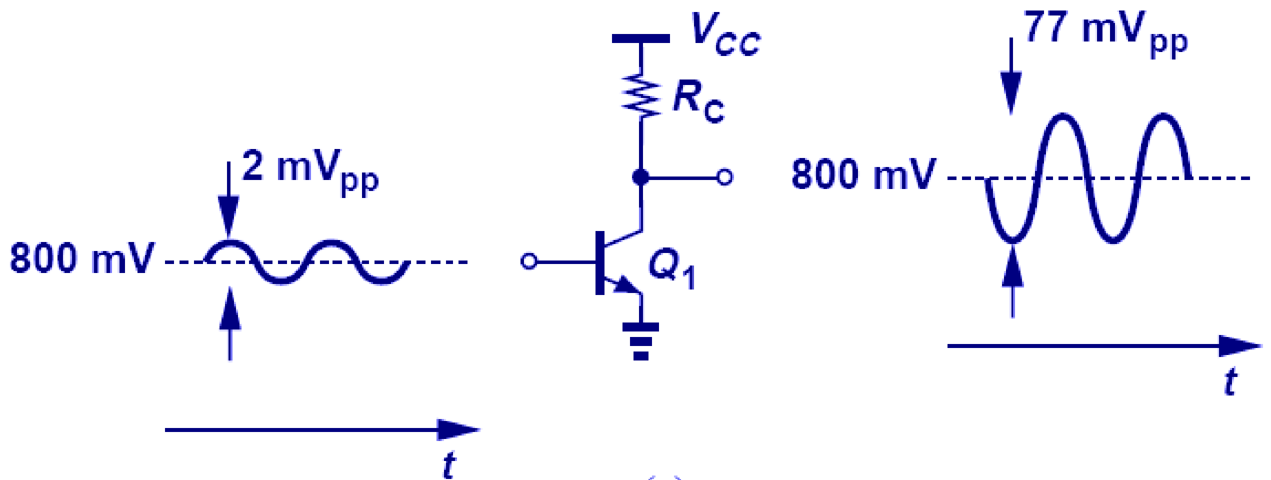
Limitation on CE Voltage Gain



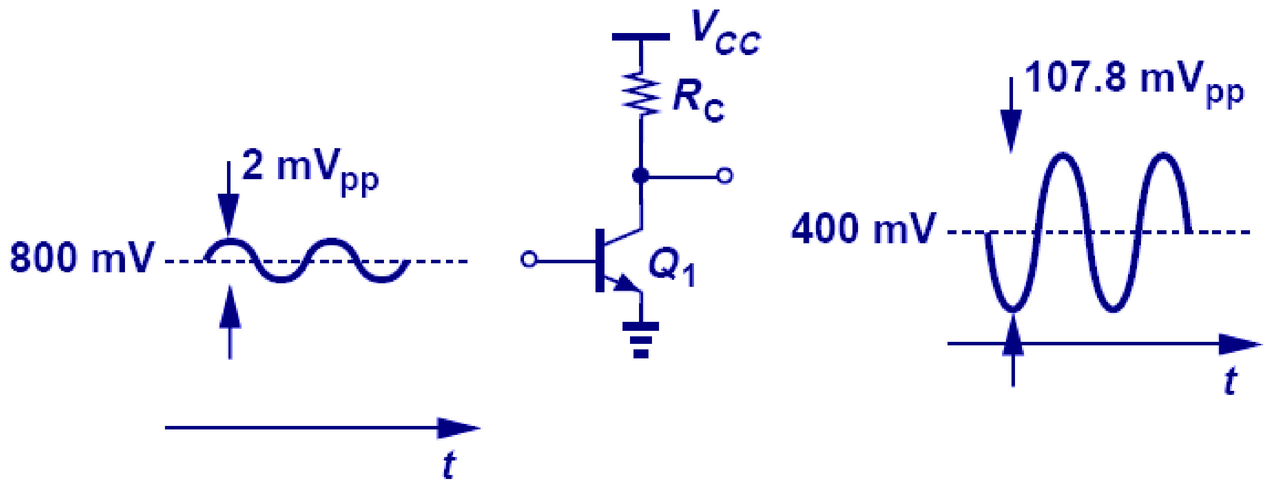
$$|A_v| = \frac{I_C R_C}{V_T} \qquad |A_v| = \frac{V_{RC}}{V_T} \qquad |A_v| < \frac{V_{CC} - V_{BE}}{V_T}$$

- **Since g_m can be written as I_C/V_T, the CE voltage gain can be written as the ratio of V_{RC} and V_T.**
- **V_{RC} is the potential difference between V_{CC} and V_{CE}, and V_{CE} cannot go below V_{BE} in order for the transistor to be in active region.**

Tradeoff between Voltage Gain and Headroom

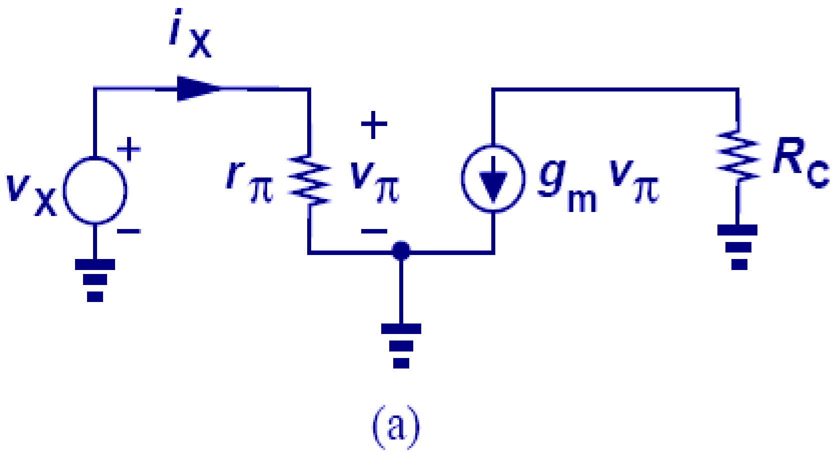


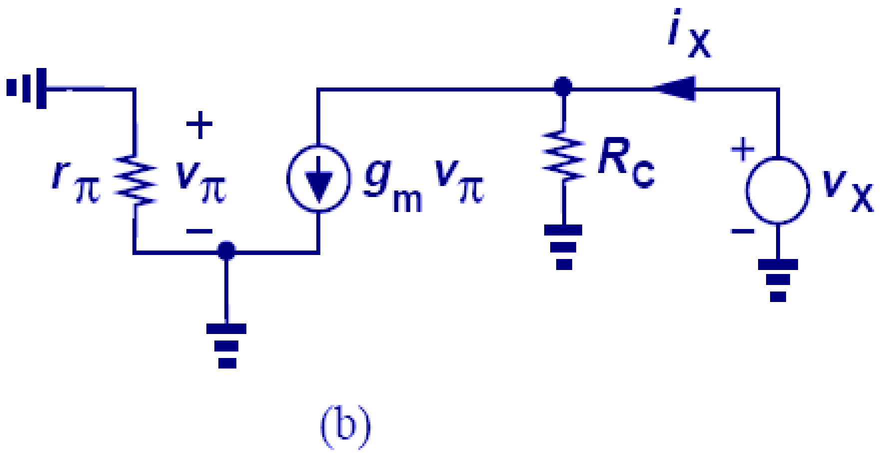
(a)



(b)

I/O Impedances of CE Stage



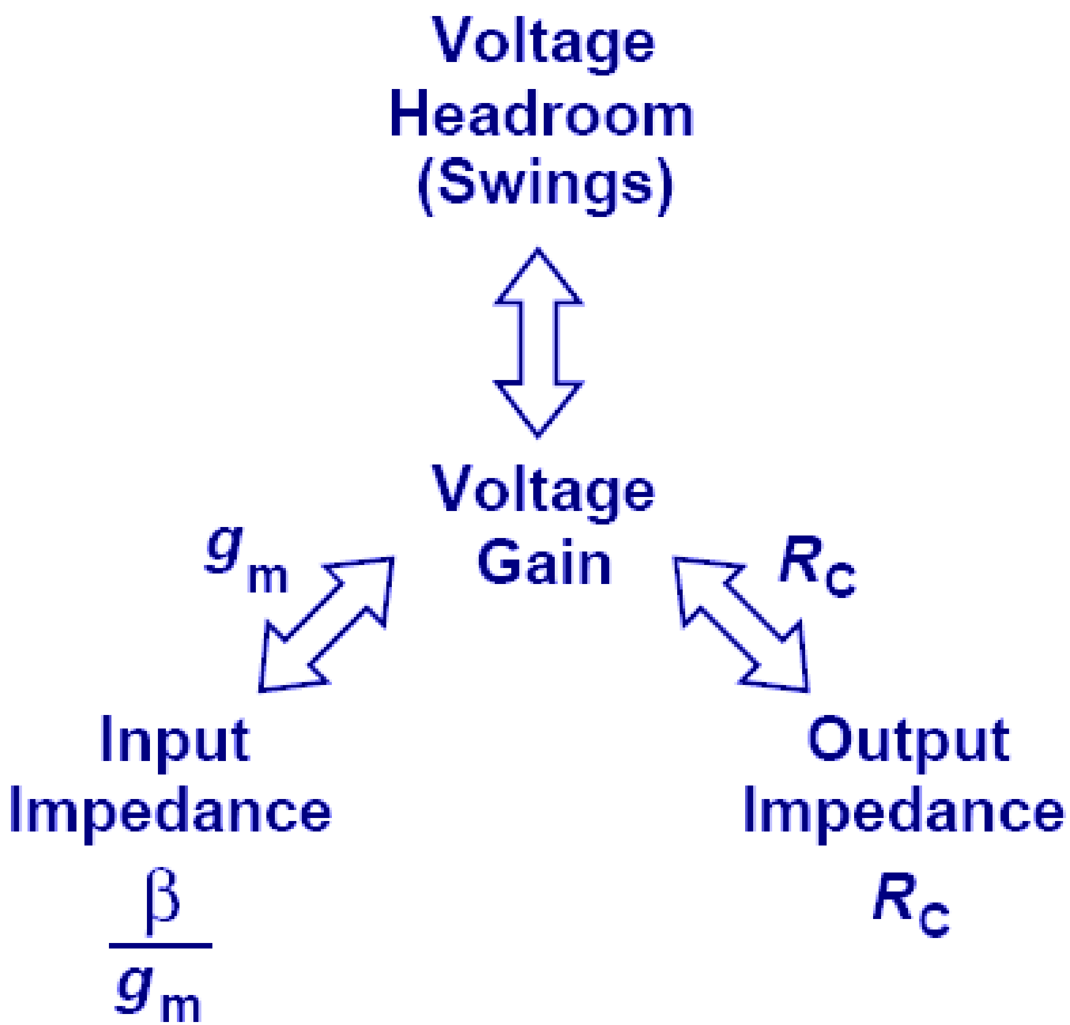


$$R_{in} = \frac{v_X}{i_X} = r_\pi$$

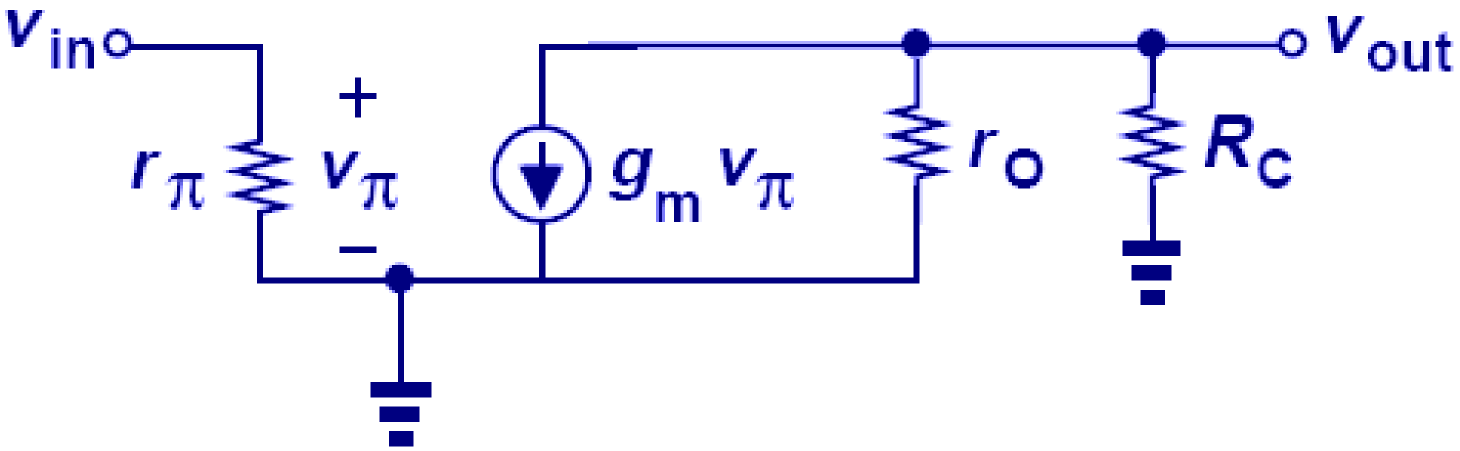
$$R_{out} = \frac{v_X}{i_X} = R_C$$

- When measuring output impedance, the input port has to be grounded so that $V_{in} = 0$.

CE Stage Trade-offs



Inclusion of Early Effect



$$A_v = -g_m (R_C \| r_O)$$

$$R_{out} = R_C \| r_O$$

- **Early effect will lower the gain of the CE amplifier, as it appears in parallel with R_C.**

Intrinsic Gain

$$A_v = -g_m r_O$$

$$|A_v| = \frac{V_A}{V_T}$$

- As R_C goes to infinity, the voltage gain reaches the product of g_m and r_O, which represents the maximum voltage gain the amplifier can have.
- The intrinsic gain is independent of the bias current.

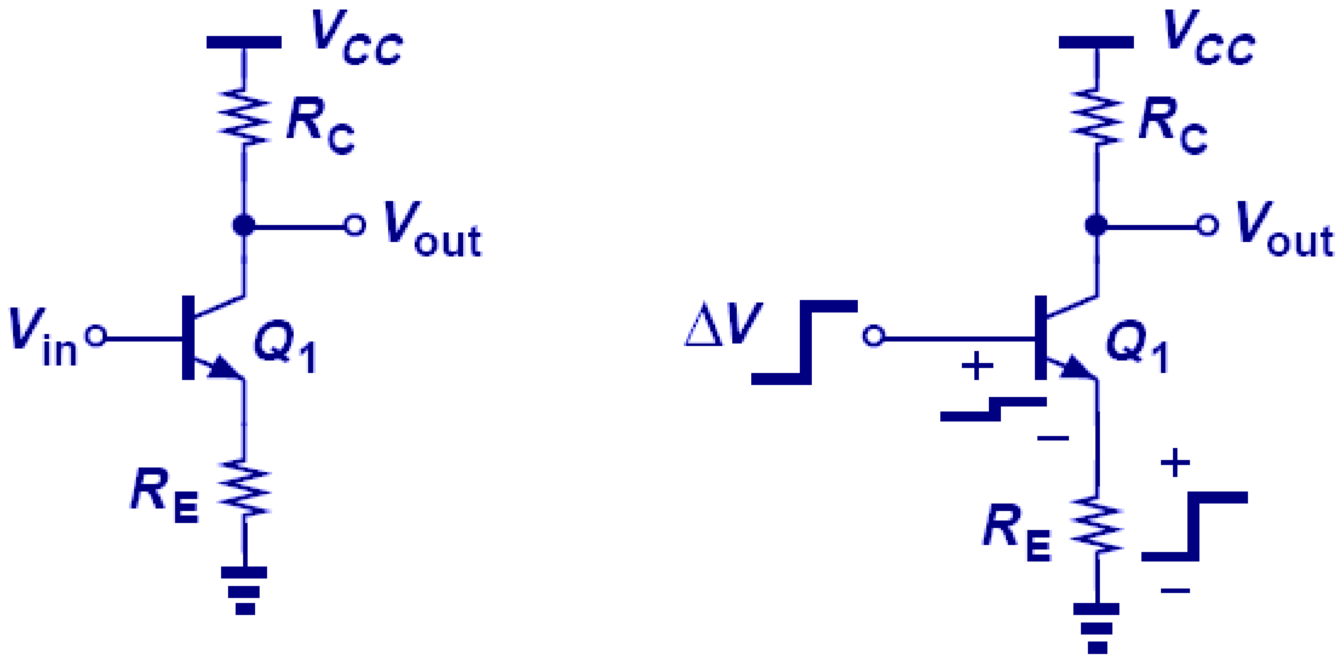
Current Gain

$$A_I = \frac{i_{out}}{i_{in}}$$

$$A_I \Big|_{CE} = \beta$$

- Another parameter of the amplifier is the current gain, which is defined as the ratio of current delivered to the load to the current flowing into the input.
- For a CE stage, it is equal to β.

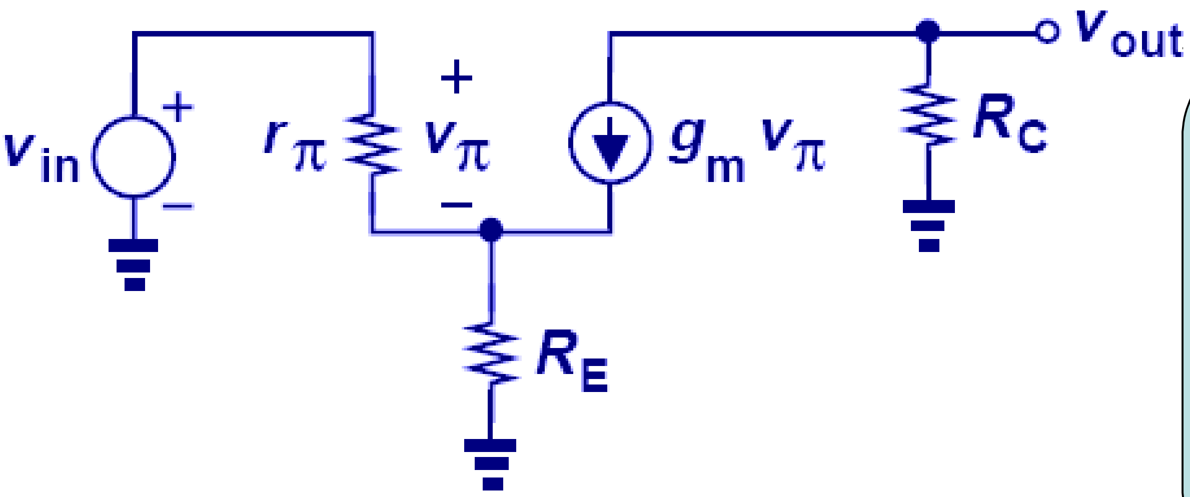
Emitter Degeneration



(a) (b)

- By inserting a resistor in series with the emitter, we "degenerate" the CE stage.
- This topology will decrease the gain of the amplifier but improve other aspects, such as linearity, and input impedance.

Small-Signal Model

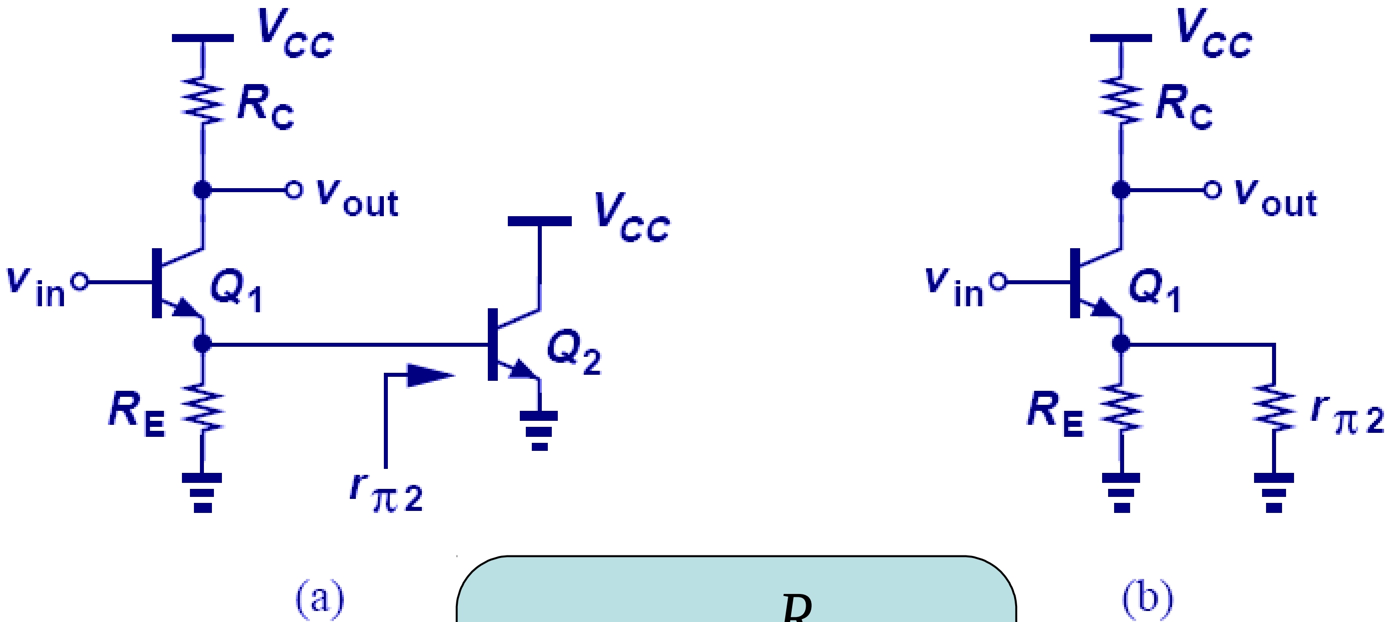


$$A_v = -\frac{g_m R_C}{1 + g_m R_E}$$

$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

- Interestingly, this gain is equal to the total load resistance to ground divided by $1/g_m$ plus the total resistance placed in series with the emitter.

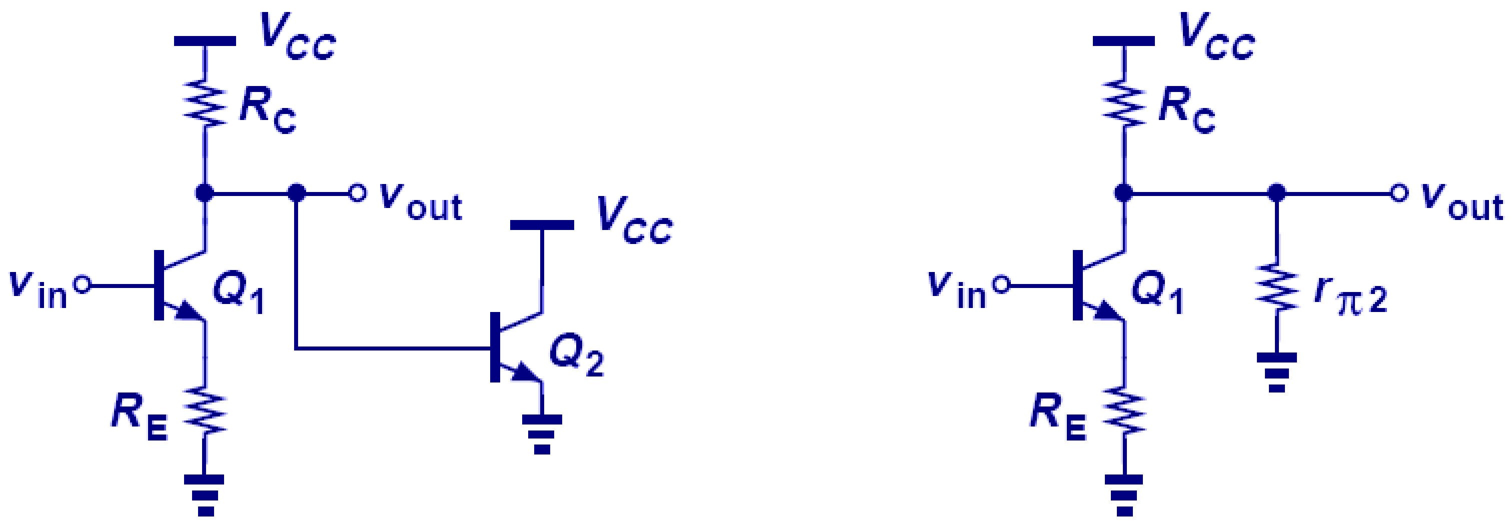
Emitter Degeneration Example I



$$A_v = -\frac{R_C}{\frac{1}{g_{m1}} + R_E \| r_{\pi 2}}$$

- **The input impedance of Q_2 can be combined in parallel with R_E to yield an equivalent impedance that degenerates Q_1.**

Emitter Degeneration Example II

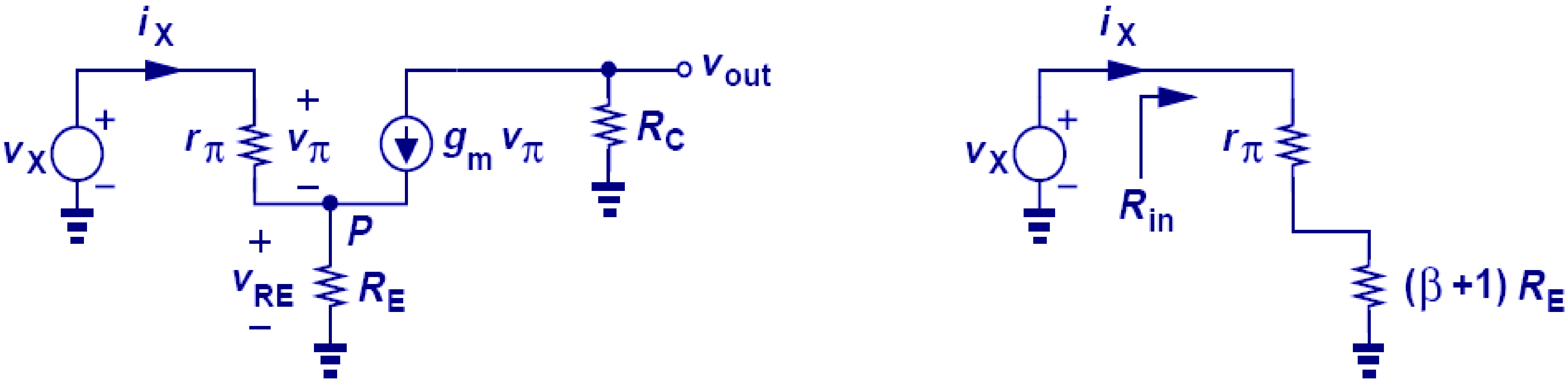


(a) (b)

$$A_v = -\frac{R_C \| r_{\pi 2}}{\frac{1}{g_{m1}} + R_E}$$

- **In this example, the input impedance of Q_2 can be combined in parallel with R_C to yield an equivalent collector impedance to ground.**

Input Impedance of Degenerated CE Stage



(a) (b)

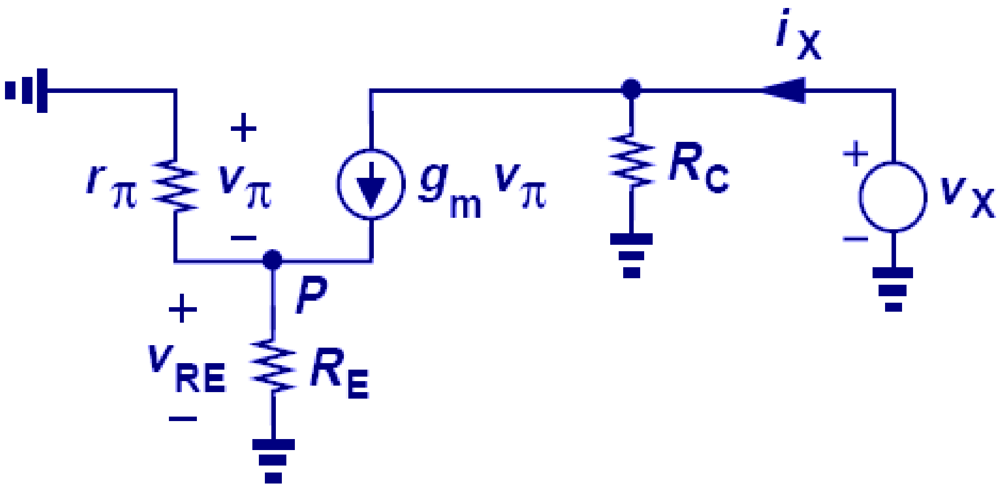
$$V_A = \infty$$

$$v_X = r_\pi i_X + R_E(1+\beta) i_X$$

$$R_{in} = \frac{v_X}{i_X} = r_\pi + (\beta+1)R_E$$

- **With emitter degeneration, the input impedance is increased from r_π to $r_\pi + (\beta+1)R_E$; a desirable effect.**

Output Impedance of Degenerated CE Stage



(a)

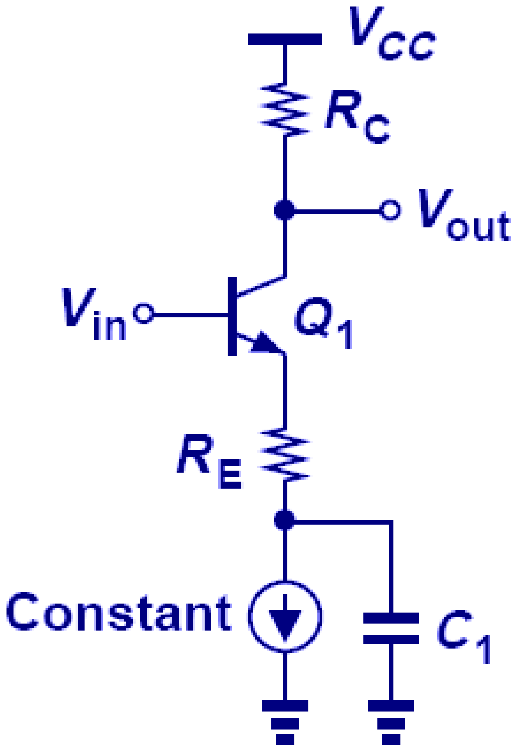
$$V_A = \infty$$

$$v_{in} = 0 = v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E \Rightarrow v_\pi = 0$$

$$R_{out} = \frac{v_X}{i_X} = R_C$$

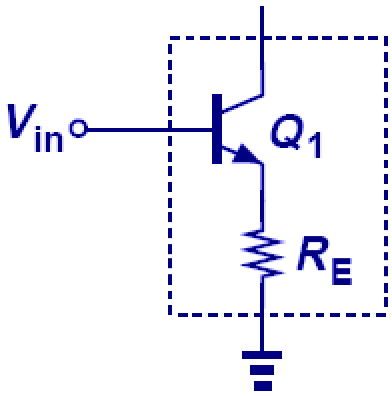
- **Emitter degeneration does not alter the output impedance in this case. (More on this later.)**

Capacitor at Emitter

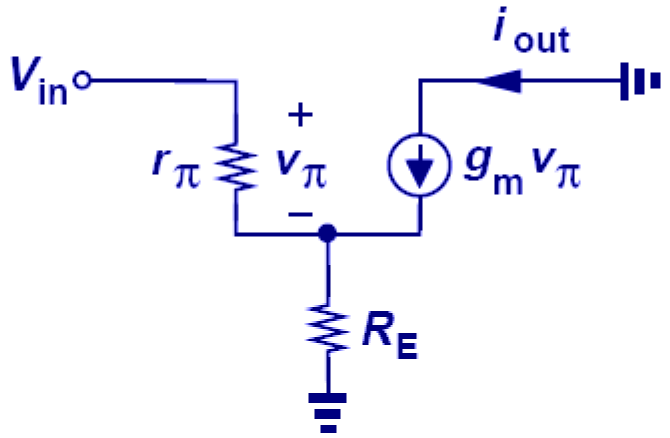


- At DC the capacitor is open and the current source biases the amplifier.
- For ac signals, the capacitor is short and the amplifier is degenerated by R_E.

Example: Design CE Stage with Degeneration as a Black Box



(a)



(b)

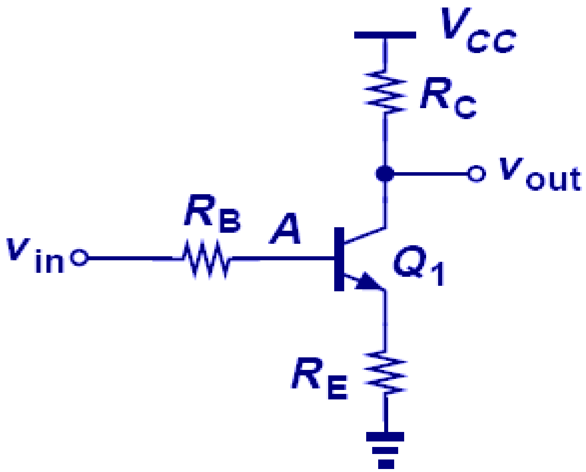
$$V_A = \infty$$

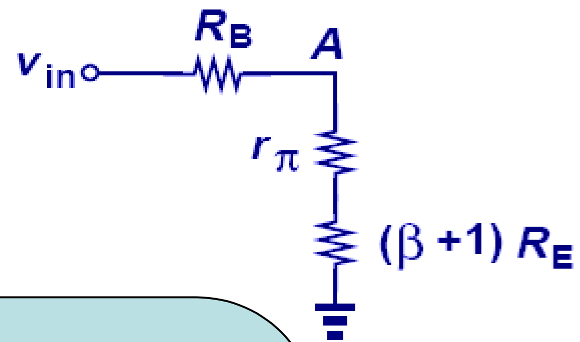
$$i_{out} = g_m \frac{v_{in}}{1 + (r_\pi^{-1} + g_m) R_E}$$

$$G_m = \frac{i_{out}}{v_{in}} \approx \frac{g_m}{1 + g_m R_E}$$

- **If $g_m R_E$ is much greater than unity, G_m is more linear.**

Degenerated CE Stage with Base Resistance





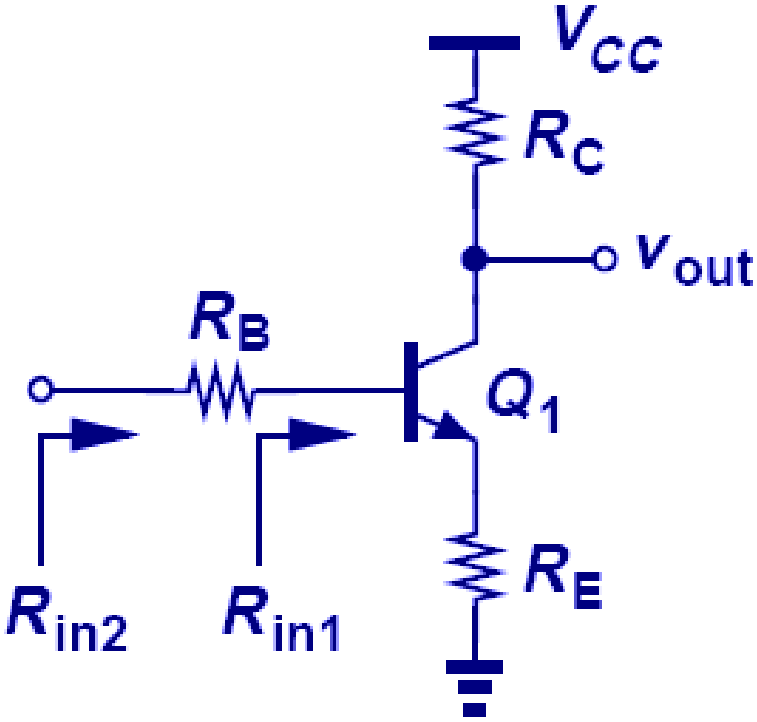
$$V_A = \infty$$

$$\frac{v_{out}}{v_{in}} = \frac{v_A}{v_{in}} \cdot \frac{v_{out}}{v_A}$$

$$\frac{v_{out}}{v_{in}} = \frac{-\beta R_C}{r_\pi + (\beta + 1) R_E + R_B}$$

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta + 1}}$$

Input/Output Impedances



$$V_A = \infty$$

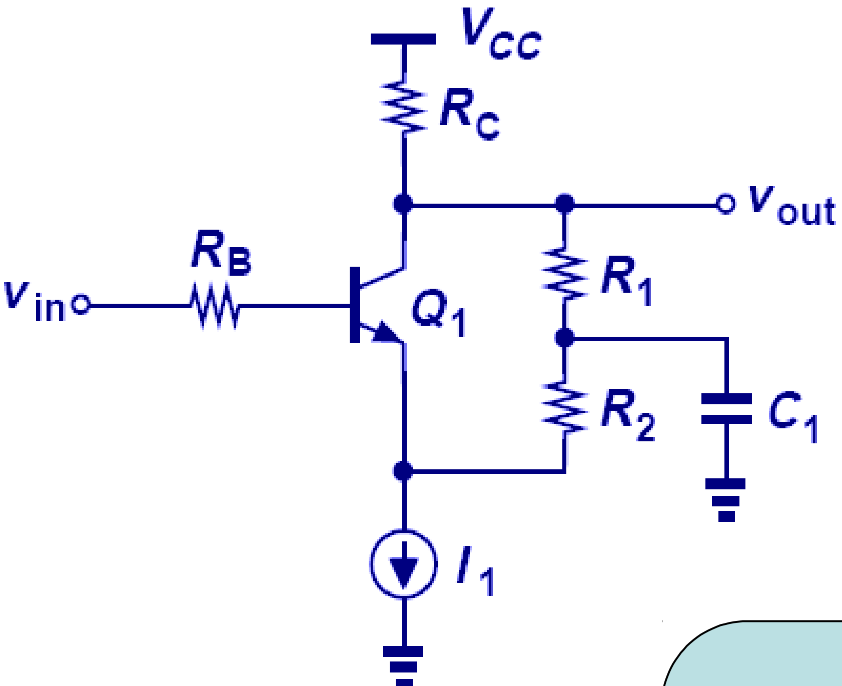
$$R_{in1} = r_\pi + (\beta + 1)R_E$$

$$R_{in2} = R_B + r_{\pi 2} + (\beta + 1)R_E$$

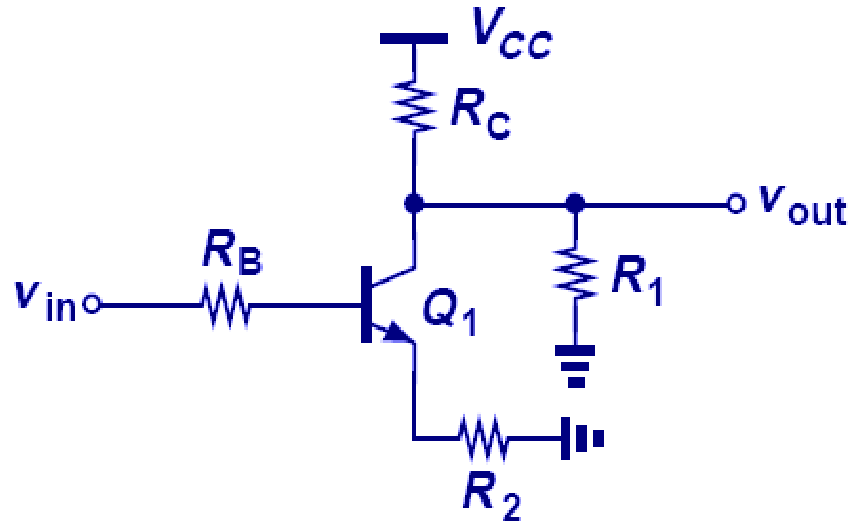
$$R_{out} = R_C$$

- **R_{in1} is more important in practice as R_B is often the output impedance of the previous stage.**

Emitter Degeneration Example III



(a)



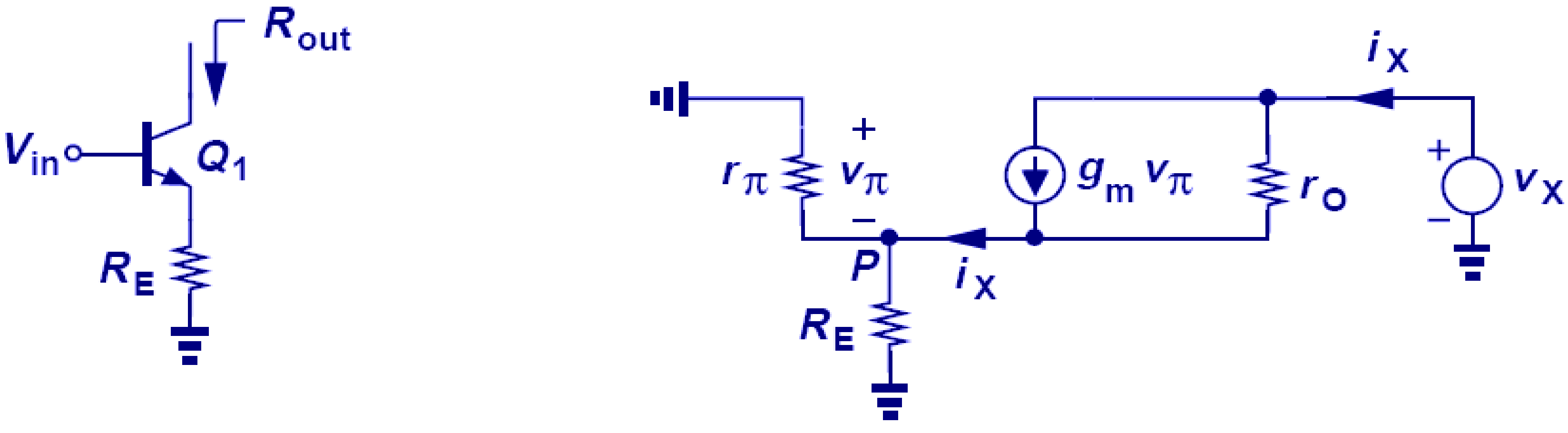
(b)

$$A_v = \frac{-(R_C \,\|\, R_1)}{\dfrac{1}{g_m} + R_2 + \dfrac{R_B}{\beta+1}}$$

$$R_{in} = r_\pi + (\beta+1)R_2$$

$$R_{out} = R_C \,\|\, R_1$$

Output Impedance of Degenerated Stage with $V_A < \infty$



(a) (b)

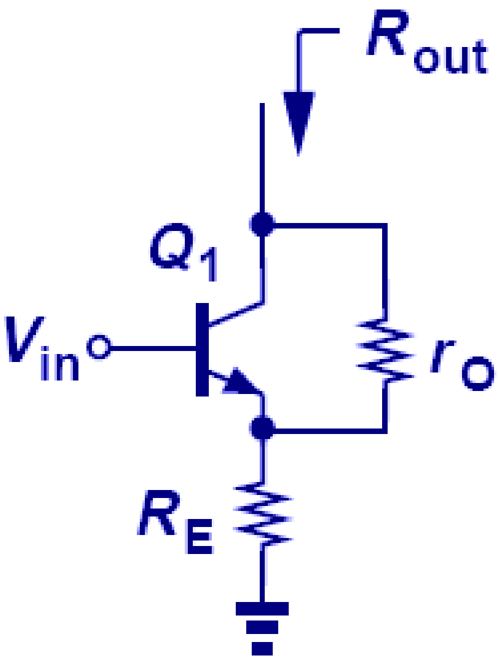
$$R_{out} = \left[1 + g_m (R_E \| r_\pi)\right] r_O + R_E \| r_\pi$$

$$R_{out} = r_O + (g_m r_O + 1)(R_E \| r_\pi)$$

$$R_{out} \approx r_O \left[1 + g_m (R_E \| r_\pi)\right]$$

- **Emitter degeneration boosts the output impedance by a factor of $1+g_m(R_E||r_\pi)$.**
- **This improves the gain of the amplifier and makes the circuit a better current source.**

Two Special Cases



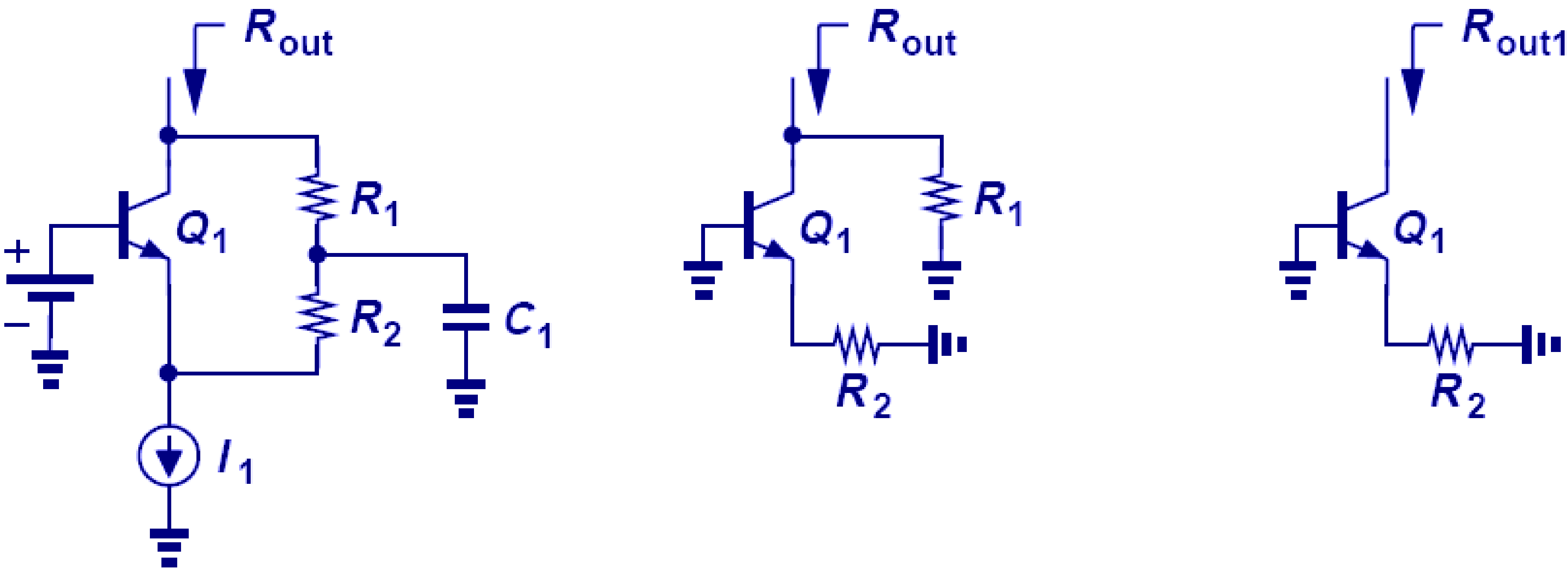
1) $R_E >> r_\pi$

$$R_{out} \approx r_O(1+g_m r_\pi) \approx \beta r_O$$

2) $R_E << r_\pi$

$$R_{out} \approx (1+g_m R_E) r_O$$

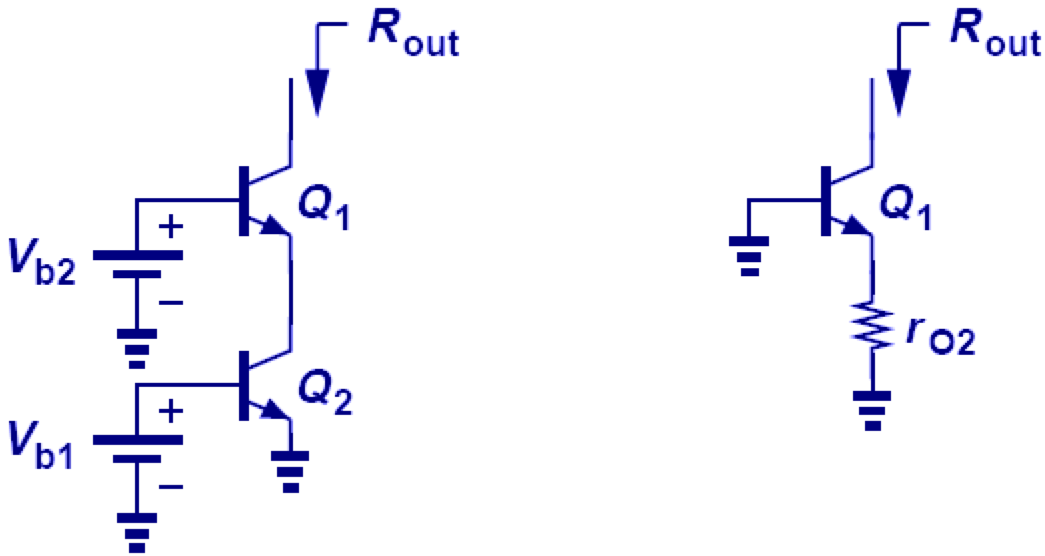
Analysis by Inspection



$$R_{out} = R_1 \,||\, R_{out1} \Longrightarrow R_{out1} = \left[1 + g_m (R_2 \,||\, r_\pi)\right] r_O \Longrightarrow R_{out} = \left[1 + g_m (R_2 \,||\, r_\pi)\right] r_O \,||\, R_1$$

- **This seemingly complicated circuit can be greatly simplified by first recognizing that the capacitor creates an AC short to ground, and gradually transforming the circuit to a known topology.**

Example: Degeneration by Another Transistor



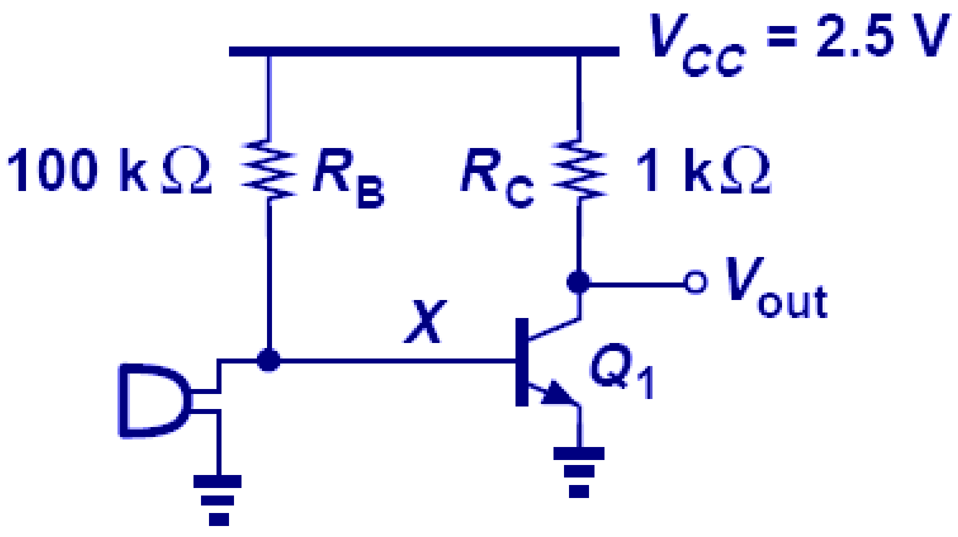
$$R_{out} = \left[1 + g_{m1}(r_{O2} \parallel r_{\pi 1})\right] r_{O1}$$

- **Called a "cascode", the circuit offers many advantages that are described later in the book.**

Study of Common-Emitter Topology

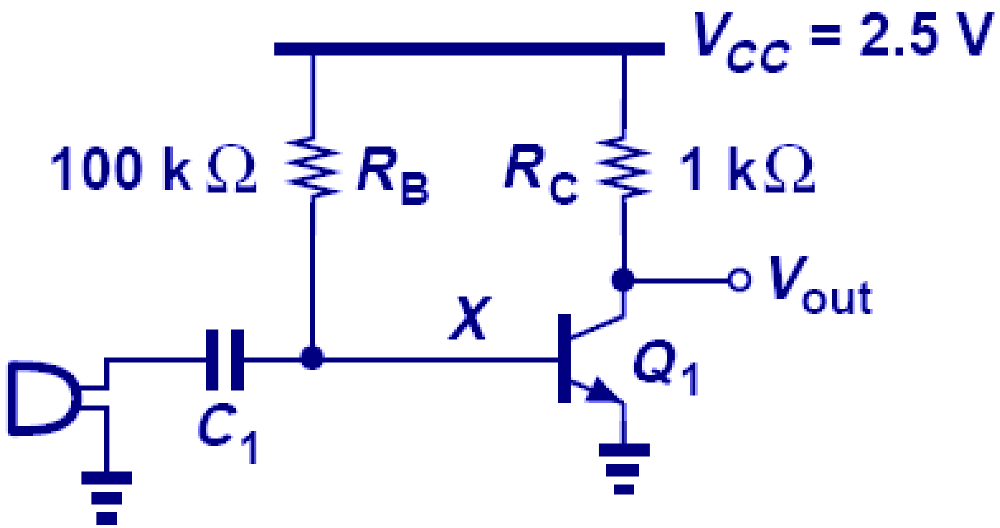
- **Analysis of CE Core**
  - **Inclusion of Early Effect**
- **Emitter Degeneration**
  - **Inclusion of Early Effect**
- ***CE Stage with Biasing***

Bad Input Connection



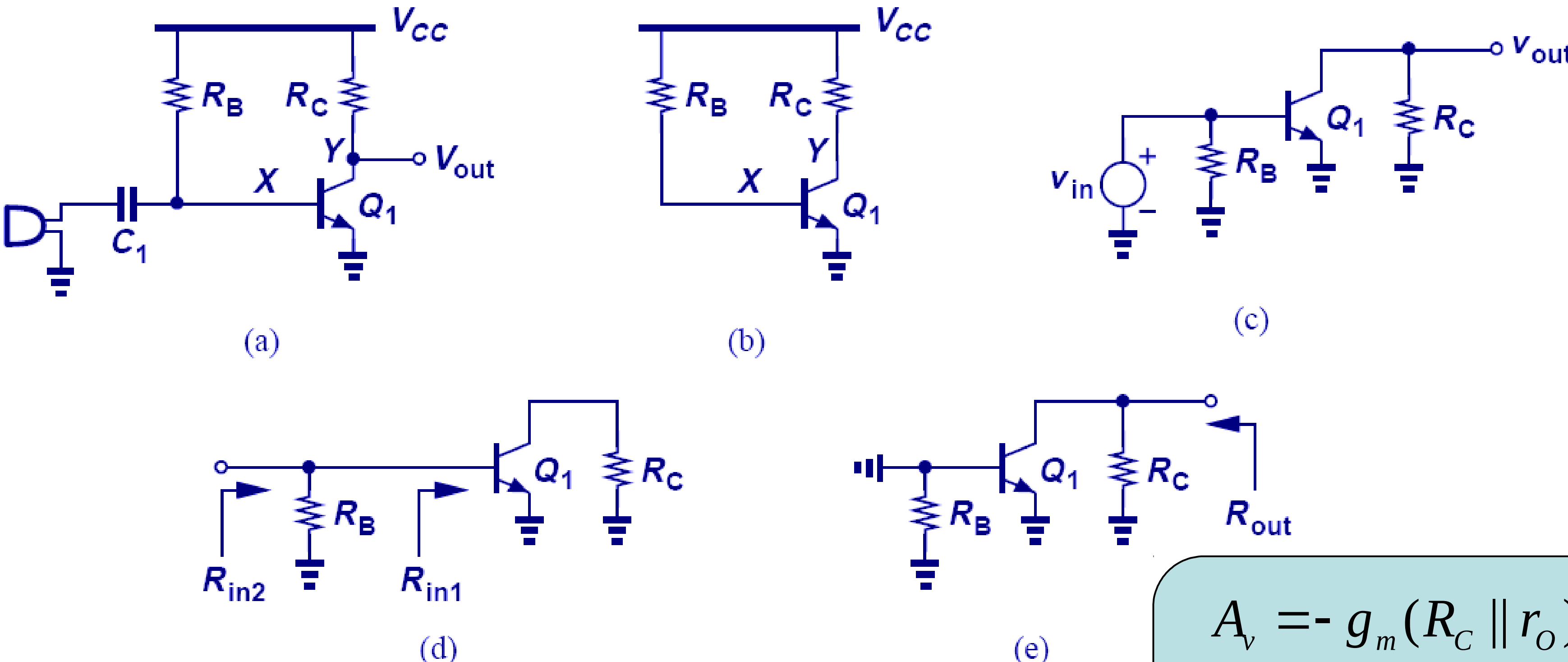
- Since the microphone has a very low resistance that connects from the base of Q_1 to ground, it attenuates the base voltage and renders Q_1 without a bias current.

Use of Coupling Capacitor



- **Capacitor isolates the bias network from the microphone at DC but shorts the microphone to the amplifier at higher frequencies.**

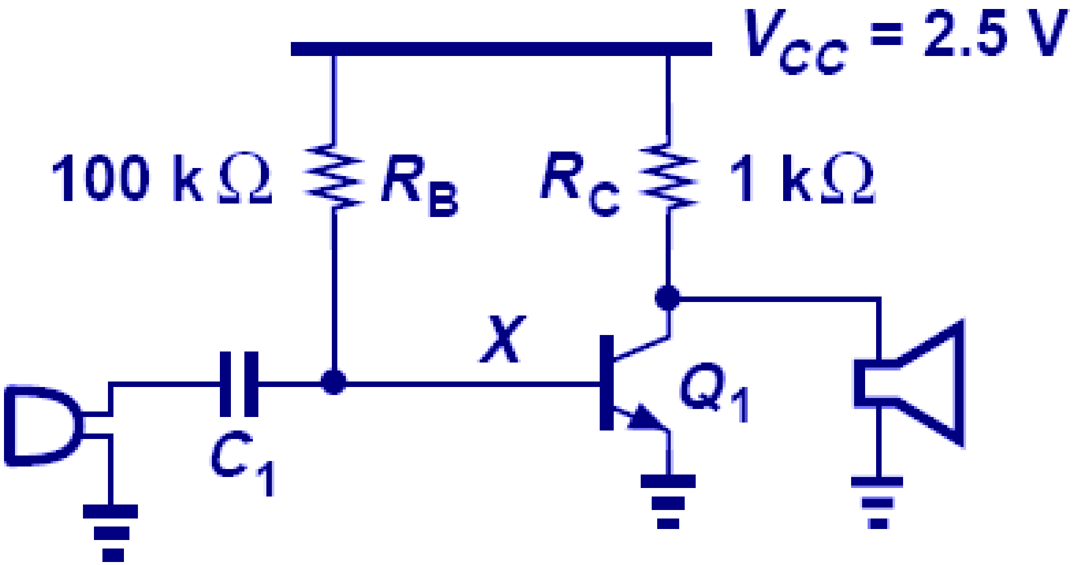
DC and AC Analysis



$$A_v = -g_m(R_C \| r_O)$$
$$R_{in} = r_\pi \| R_B$$
$$R_{out} = R_C \| r_O$$

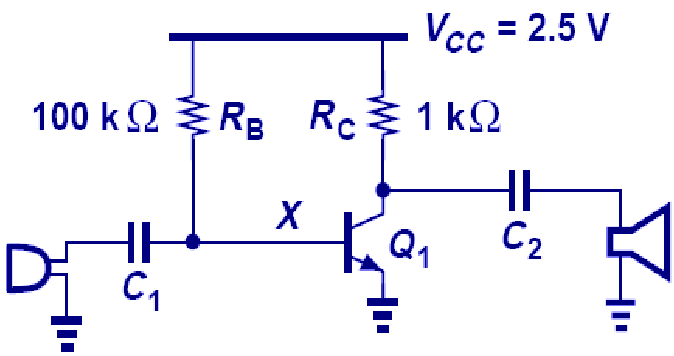
- **Coupling capacitor is open for DC calculations and shorted for AC calculations.**

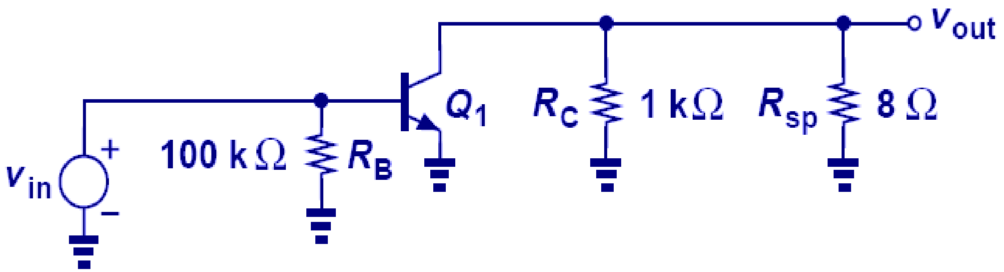
Bad Output Connection



- Since the speaker has an inductor, connecting it directly to the amplifier would short the collector at DC and therefore push the transistor into deep saturation.

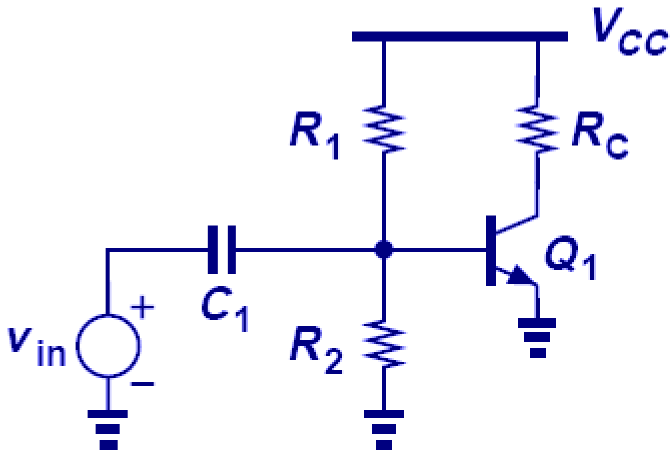
Still No Gain!!!

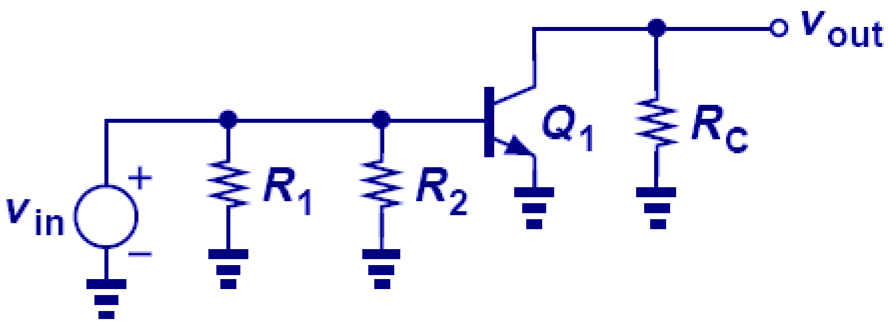




- In this example, the AC coupling indeed allows correct biasing. However, due to the speaker's small input impedance, the overall gain drops considerably.

CE Stage with Biasing



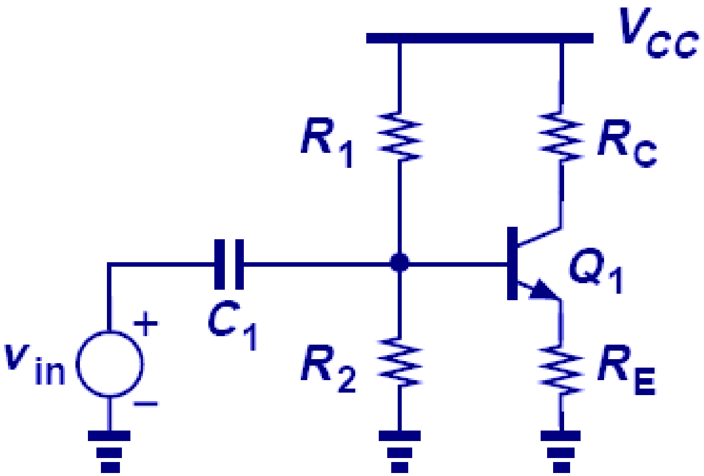


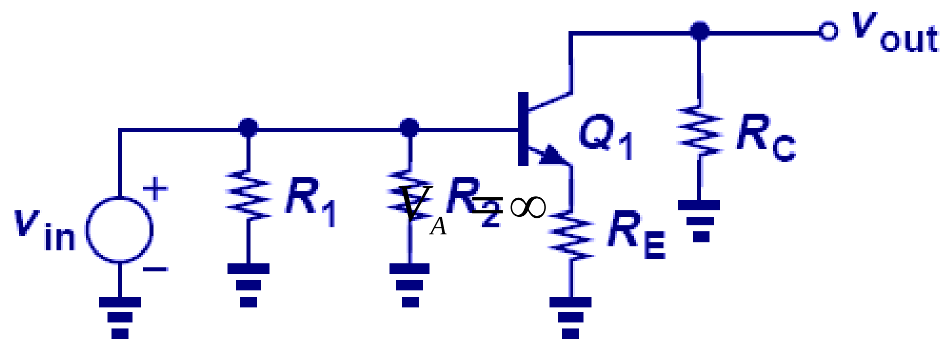
$$A_v = -g_m(R_C \,\|\, r_O)$$

$$R_{in} = r_\pi \,\|\, R_1 \,\|\, R_2$$

$$R_{out} = R_C \,\|\, r_O$$

CE Stage with Robust Biasing





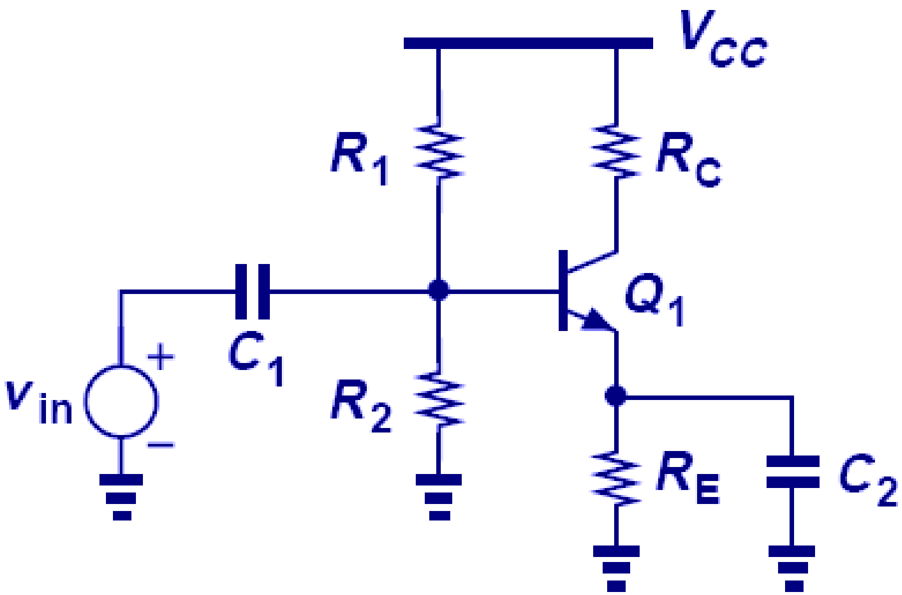
$V_A = \infty$

$$A_v = \frac{-R_C}{\frac{1}{g_m} + R_E}$$

$$R_{in} = \left[r_\pi + (\beta + 1)R_E\right] \parallel R_1 \parallel R_2$$

$$R_{out} = R_C$$

Removal of Degeneration for Signals at AC



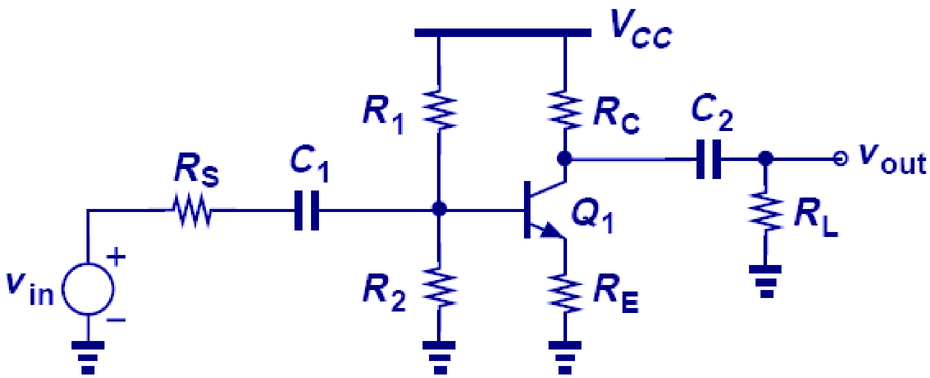
$$A_v = -g_m R_C$$

$$R_{in} = r_\pi \,||\, R_1 \,||\, R_2$$

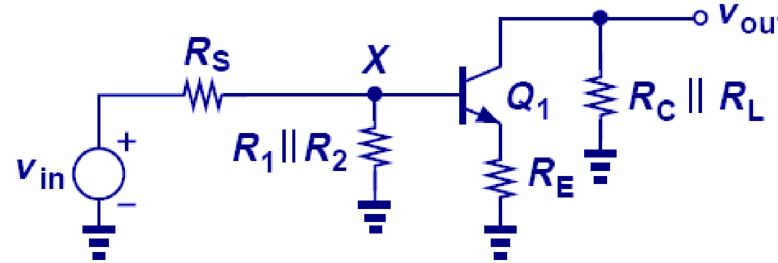
$$R_{out} = R_C$$

- **Capacitor shorts out R_E at higher frequencies and removes degeneration.**

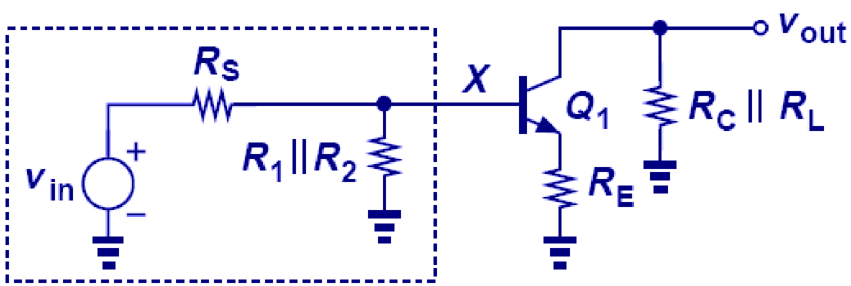
Complete CE Stage



(a)



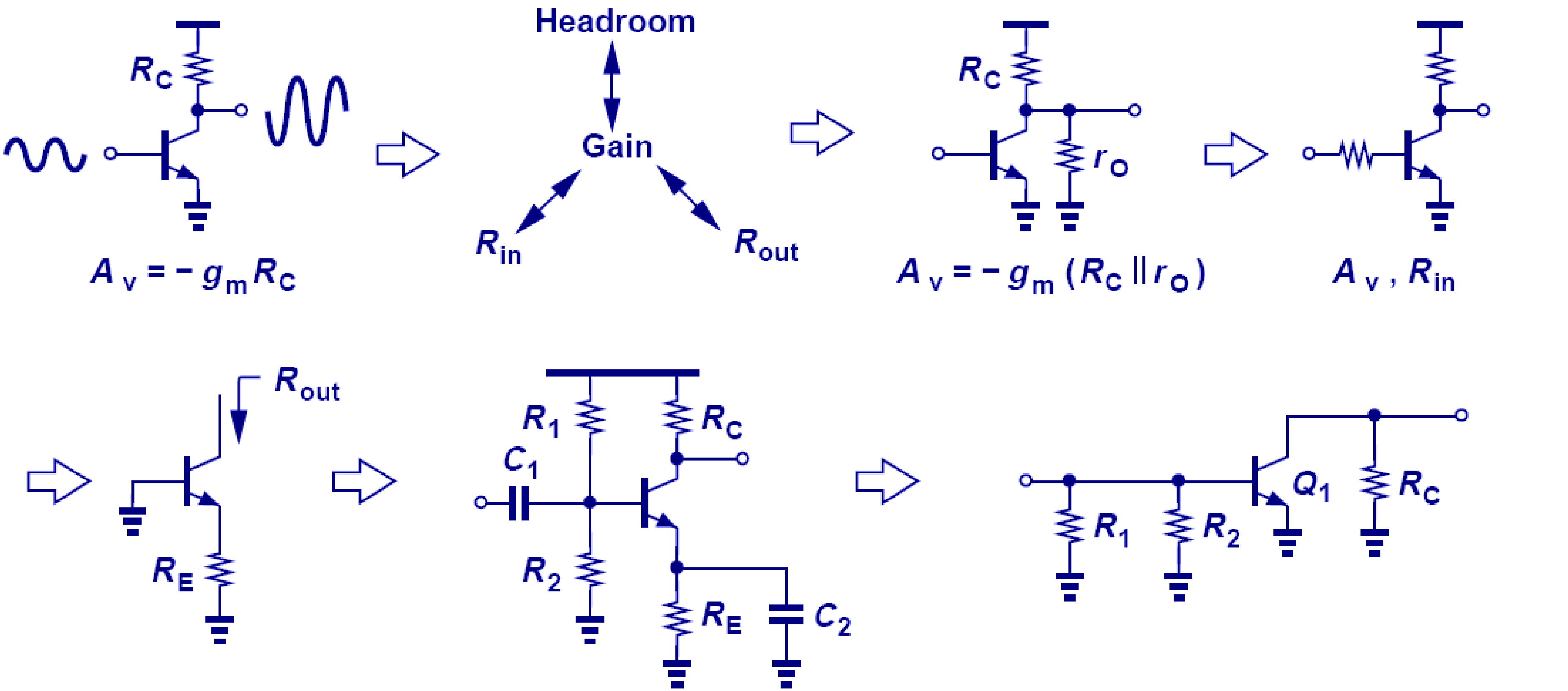
(b)



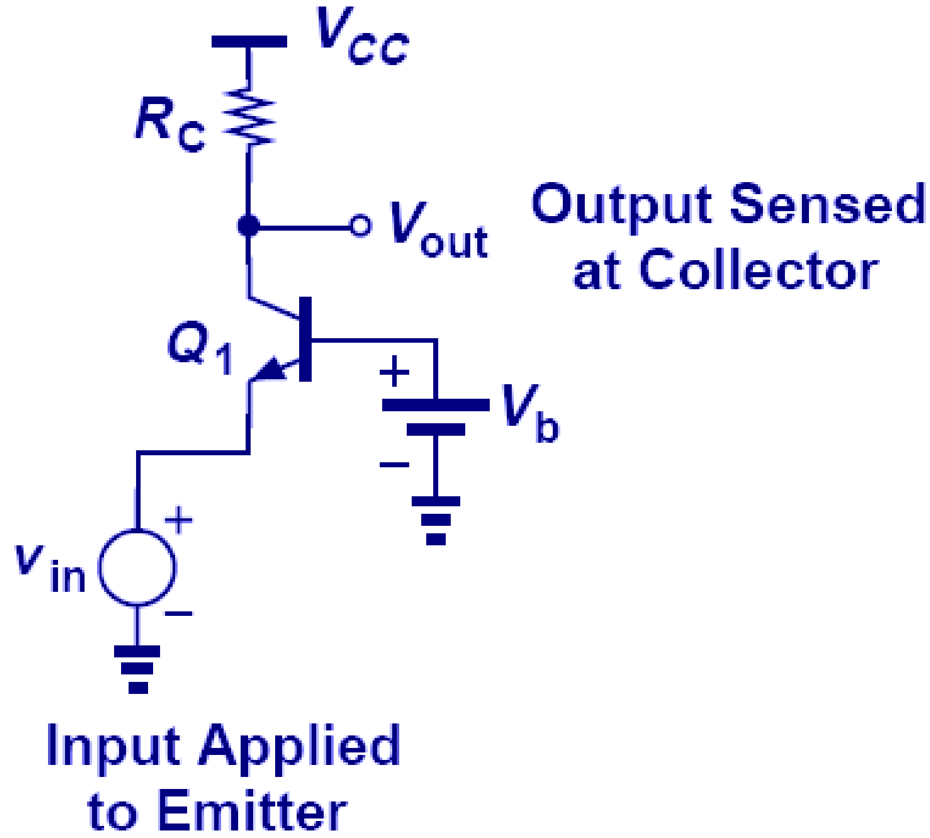
(b)

$$A_v = \frac{-R_C \parallel R_L}{\dfrac{1}{g_m} + R_E + \dfrac{R_s \parallel R_1 \parallel R_2}{\beta + 1}}$$

Summary of CE Concepts

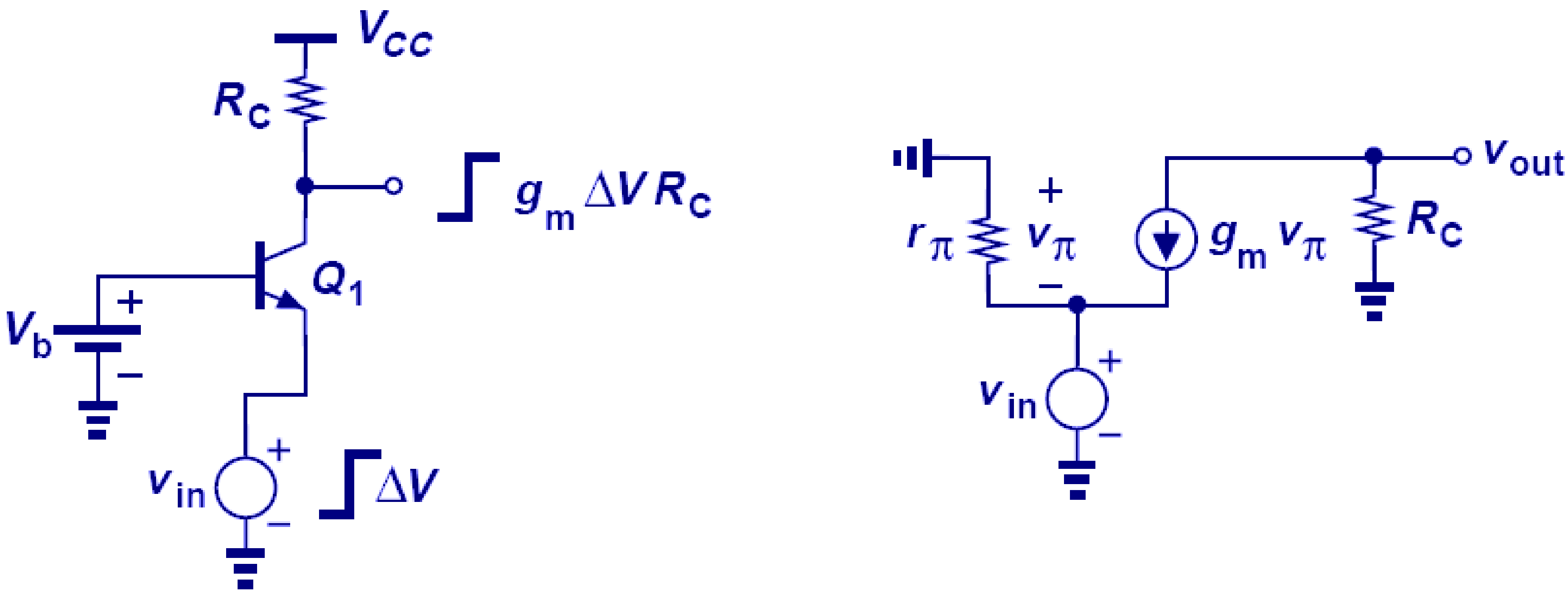


Common Base (CB) Amplifier



- **In common base topology, where the base terminal is biased with a fixed voltage, emitter is fed with a signal, and collector is the output.**

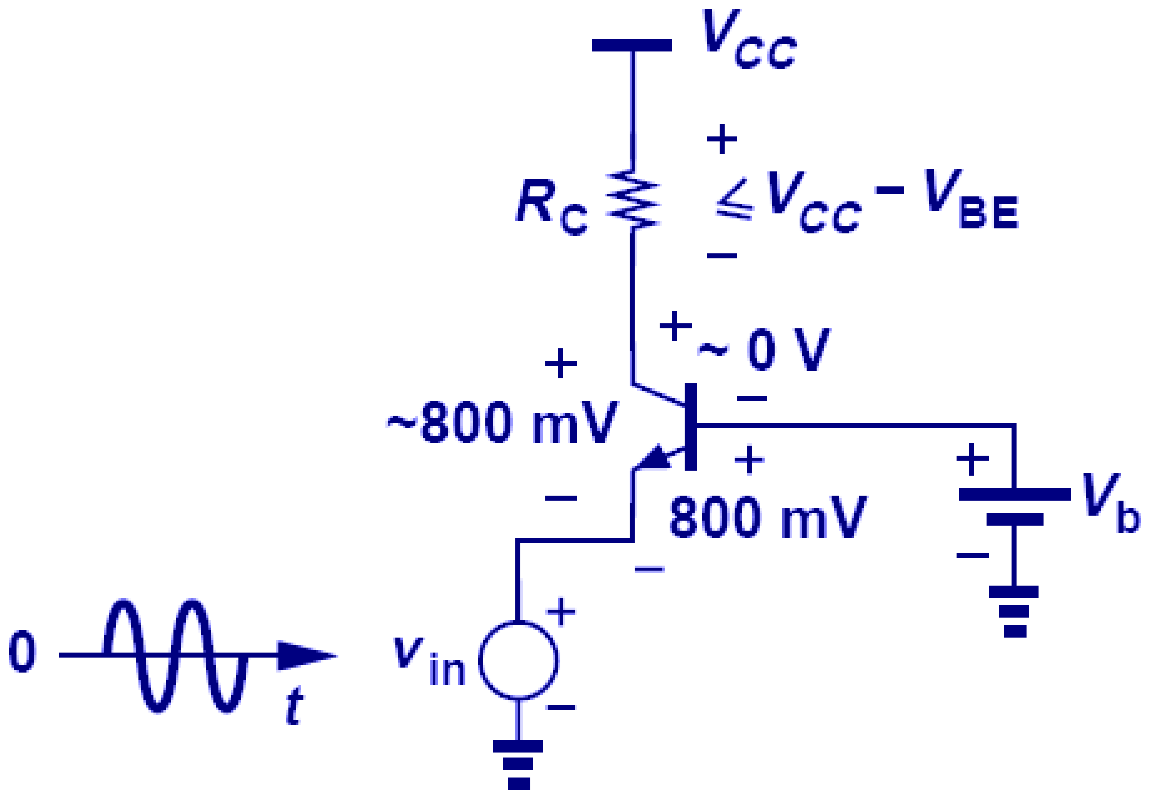
CB Core



$$A_v = g_m R_C$$

- **The voltage gain of CB stage is $g_m R_C$, which is identical to that of CE stage in magnitude and opposite in phase.**

Tradeoff between Gain and Headroom

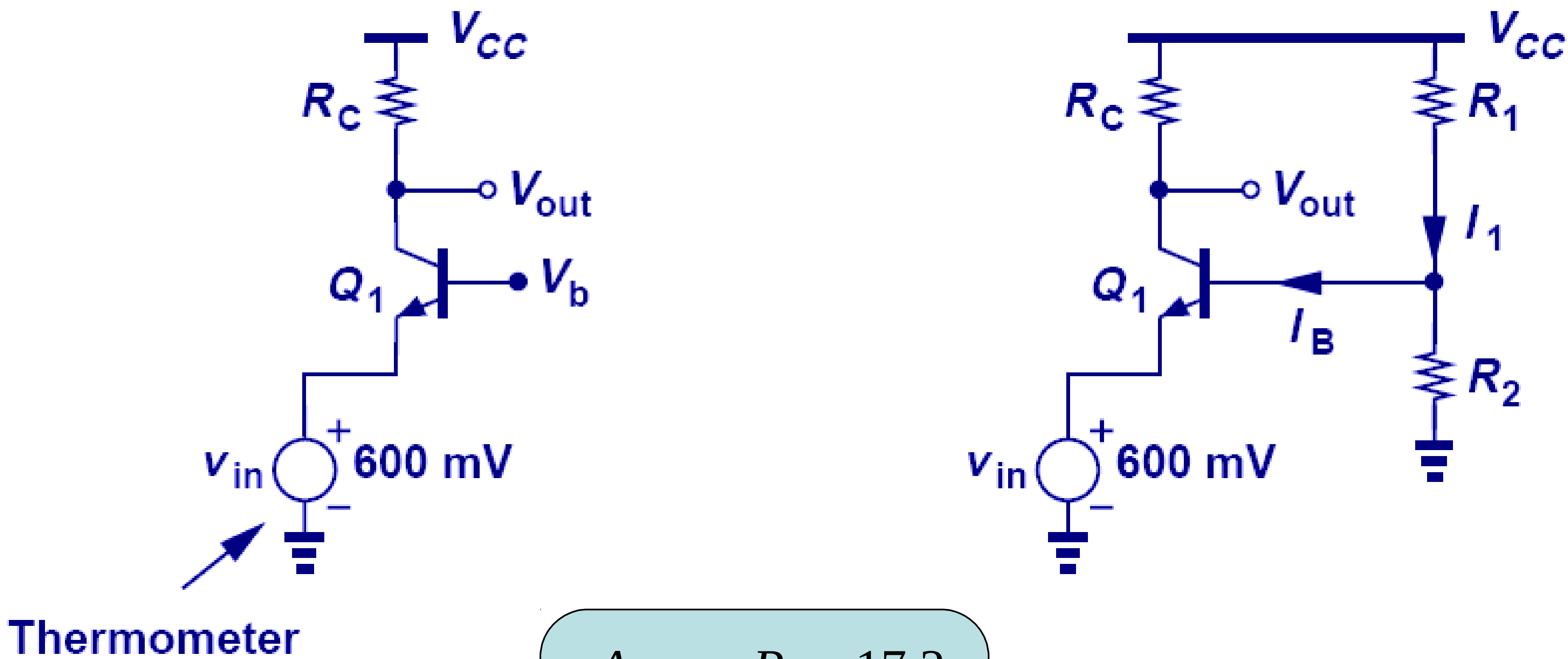


$$A_v = \frac{I_C}{V_T} . R_C$$

$$= \frac{V_{CC} - V_{BE}}{V_T}$$

- To maintain the transistor out of saturation, the maximum voltage drop across R_C cannot exceed V_{CC}-$V_{BE.}$

Simple CB Example

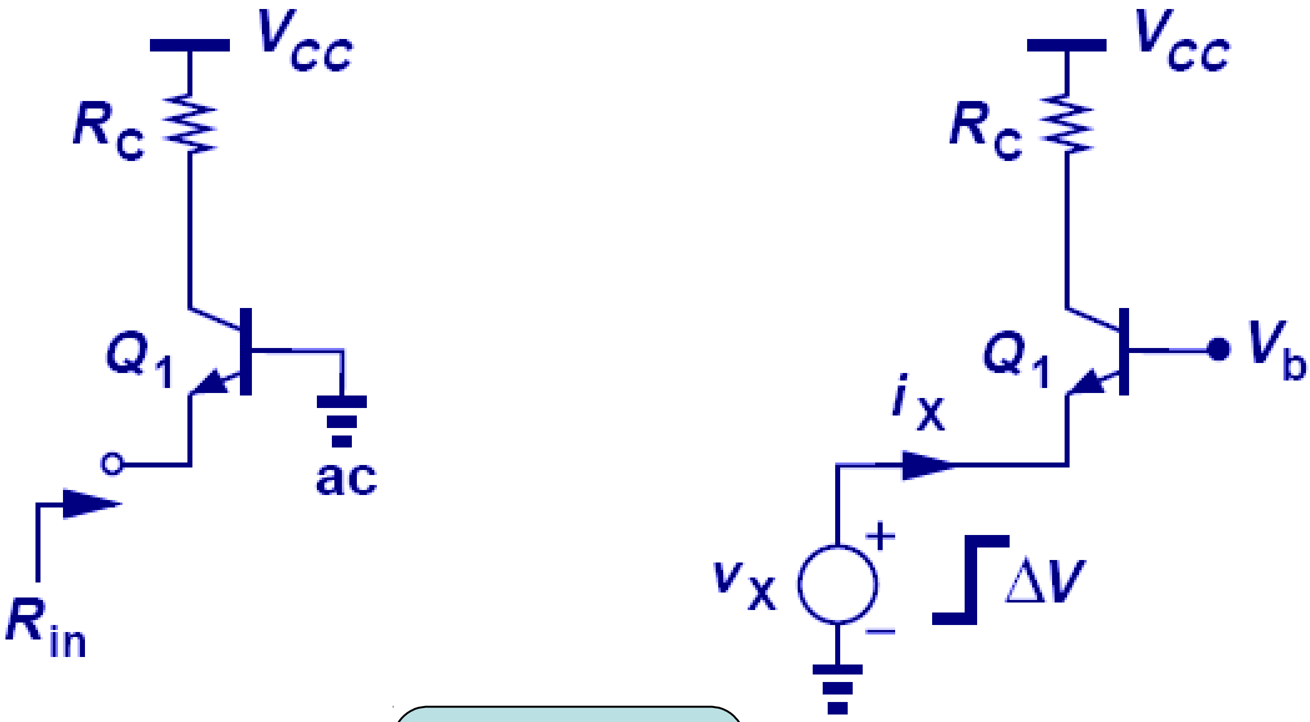


$$A_v = g_m R_C = 17.2$$

$$R_1 = 22.3K\Omega$$

$$R_2 = 67.7K\Omega$$

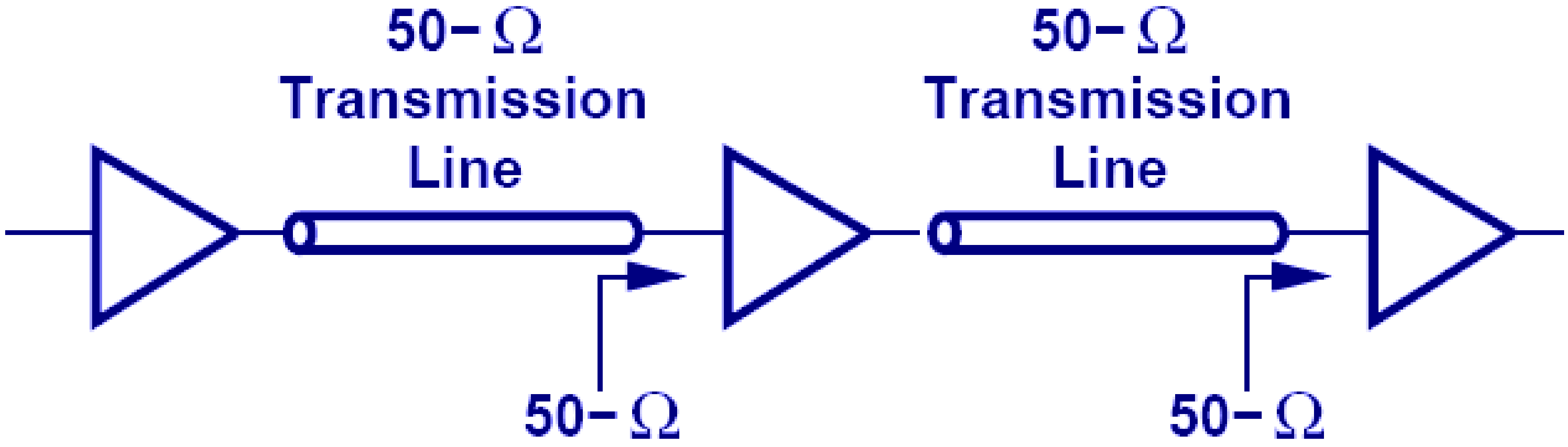
Input Impedance of CB



$$R_{in} = \frac{1}{g_m}$$

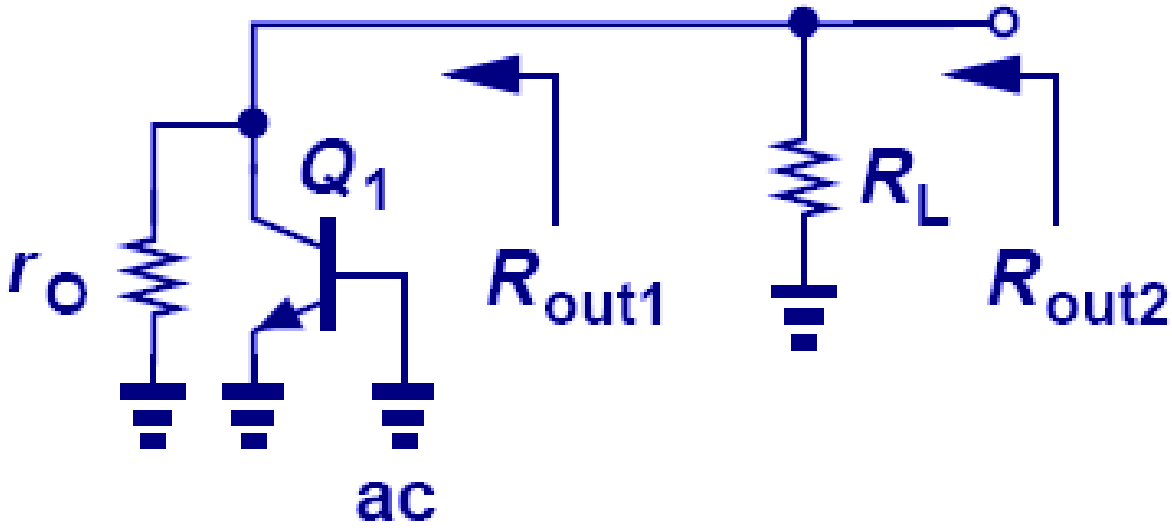
- **The input impedance of CB stage is much smaller than that of the CE stage.**

Practical Application of CB Stage



- To avoid "reflections", need impedance matching.
- CB stage's low input impedance can be used to create a match with 50 Ω.

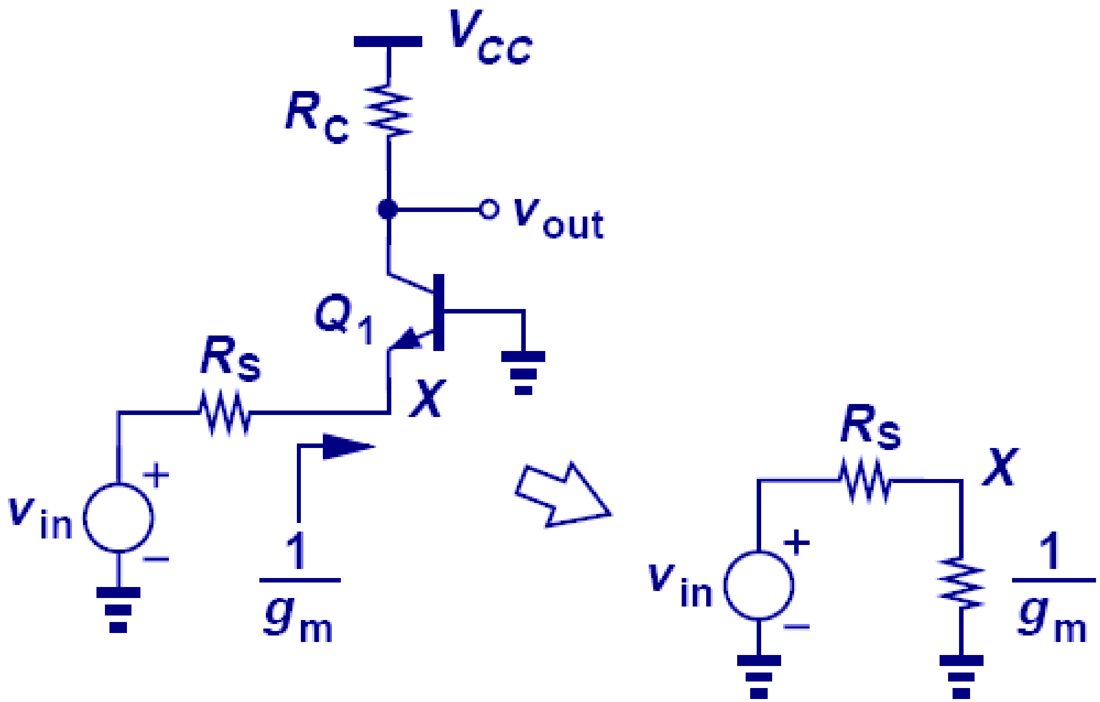
Output Impedance of CB Stage



$$R_{out} = r_O \,||\, R_C$$

- **The output impedance of CB stage is similar to that of CE stage.**

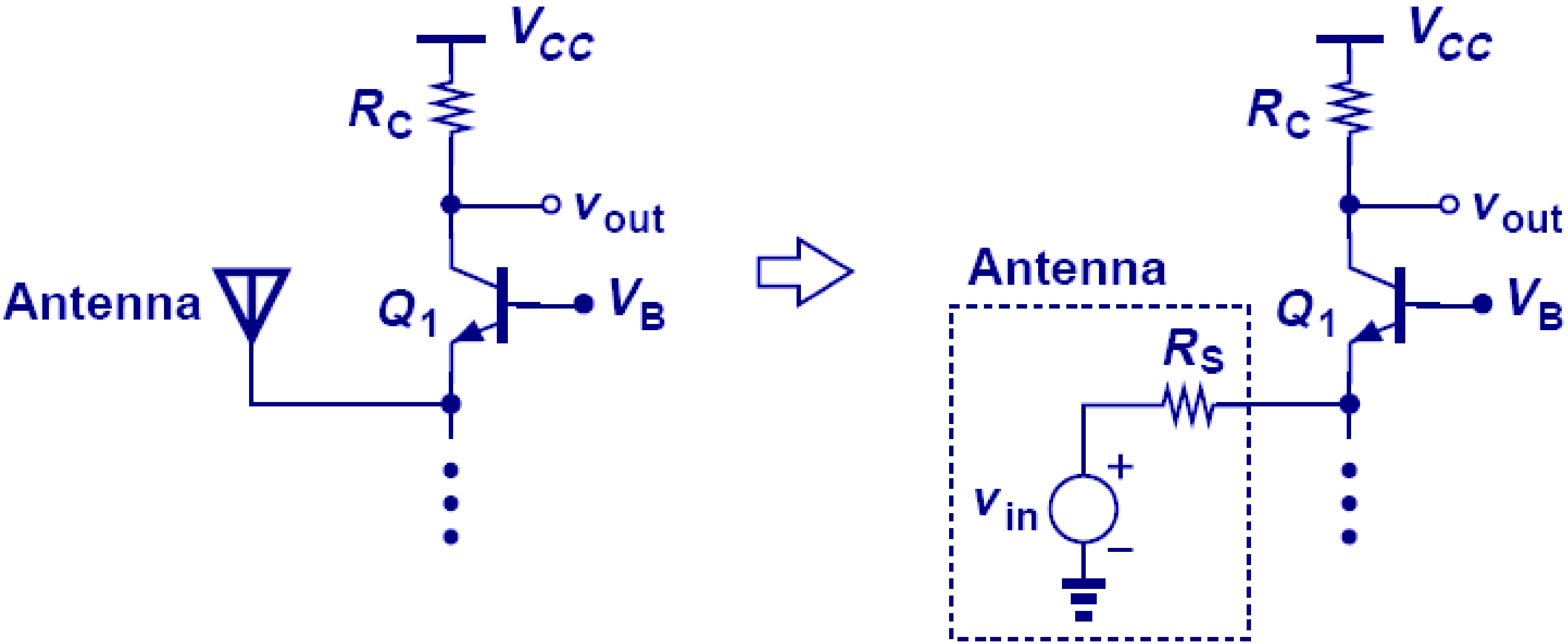
CB Stage with Source Resistance



$$A_v = \frac{R_C}{\frac{1}{g_m} + R_S}$$

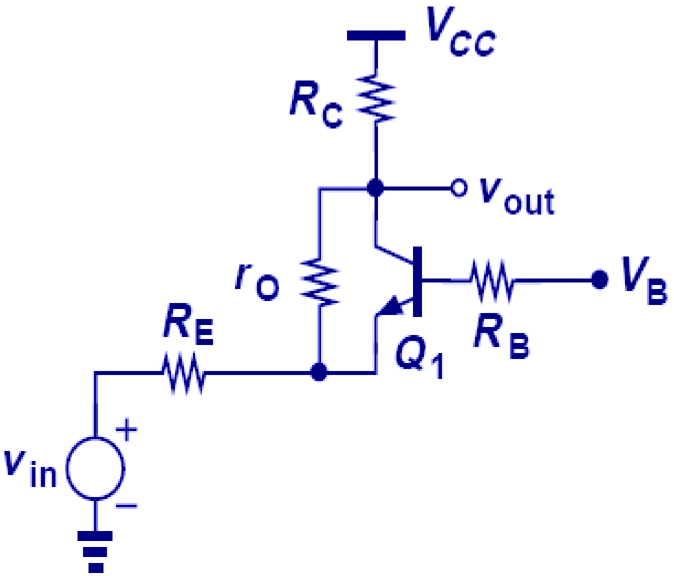
- **With an inclusion of a source resistor, the input signal is attenuated before it reaches the emitter of the amplifier; therefore, we see a lower voltage gain.**
- **This is similar to CE stage emitter degeneration; only the phase is reversed.**

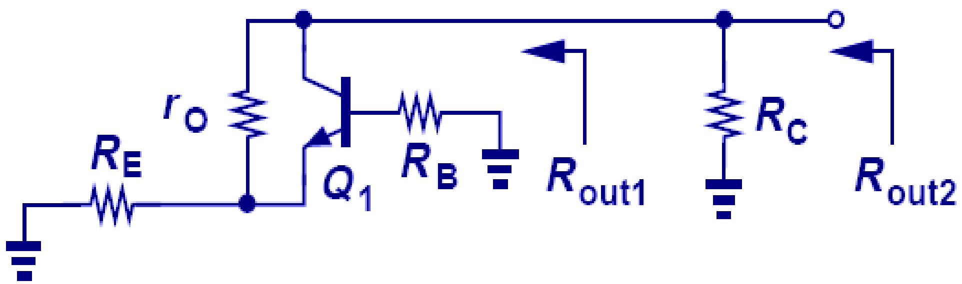
Practical Example of CB Stage



- An antenna usually has low output impedance; therefore, a correspondingly low input impedance is required for the following stage.

Realistic Output Impedance of CB Stage



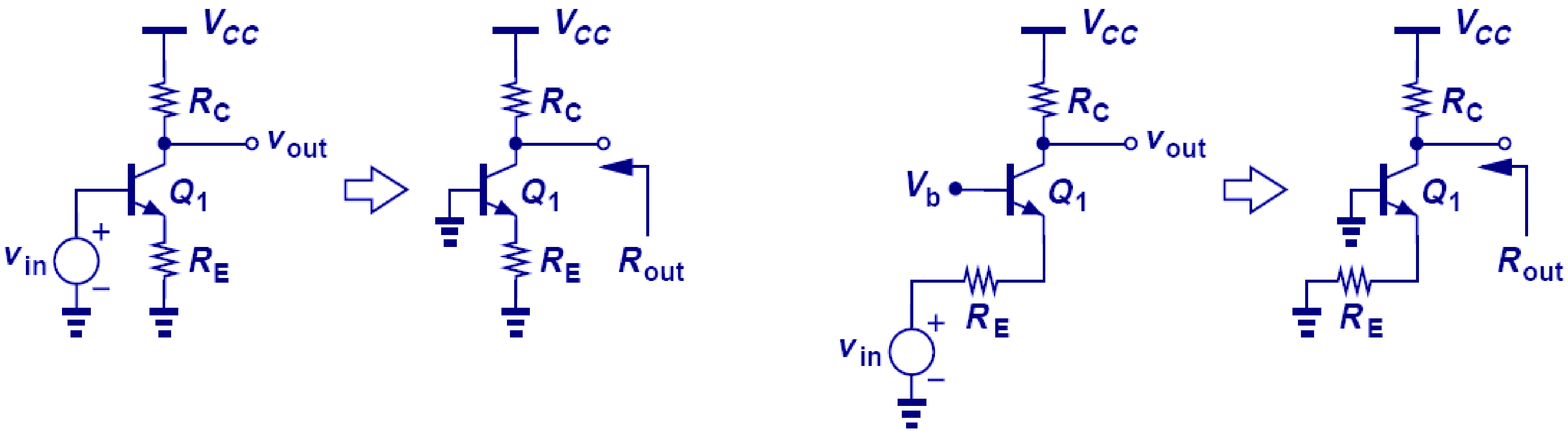


$$R_{out1} = \left[1 + g_m (R_E \,||\, r_\pi)\right] r_O + (R_E \,||\, r_\pi)$$

$$R_{out} = R_C \,||\, R_{out1}$$

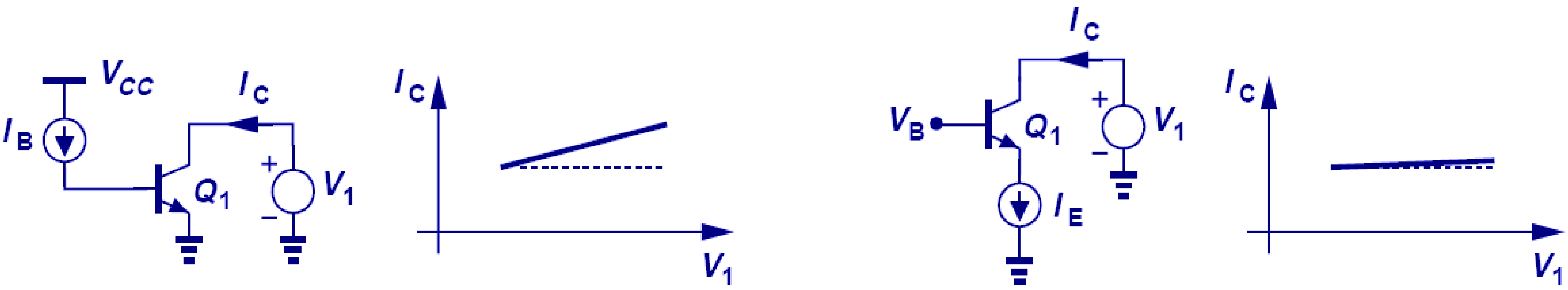
- The output impedance of CB stage is equal to R_C in parallel with the impedance looking down into the collector.

Output Impedance of CE and CB Stages



- **The output impedances of CE, CB stages are the same if both circuits are under the same condition. This is because when calculating output impedance, the input port is grounded, which renders the same circuit for both CE and CB stages.**

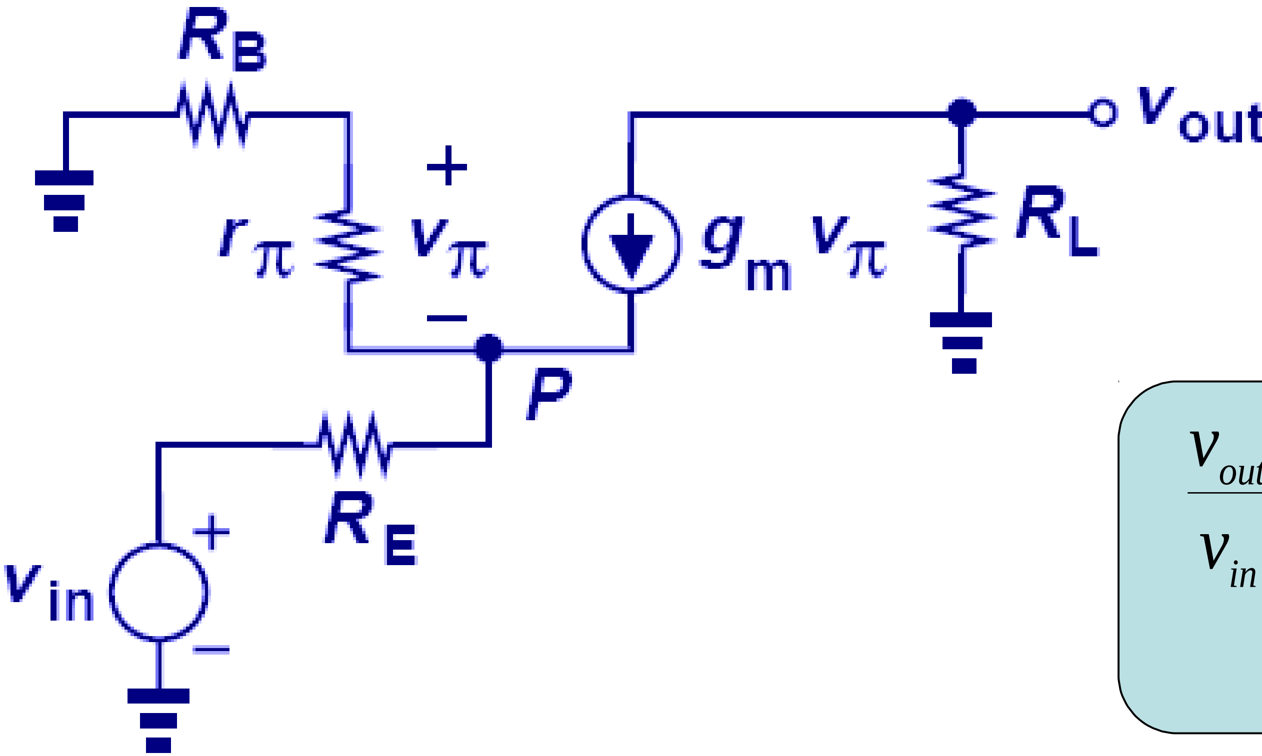
Fallacy of the “Old Wisdom”



(a) (b)

- **The statement “CB output impedance is higher than CE output impedance” is flawed.**

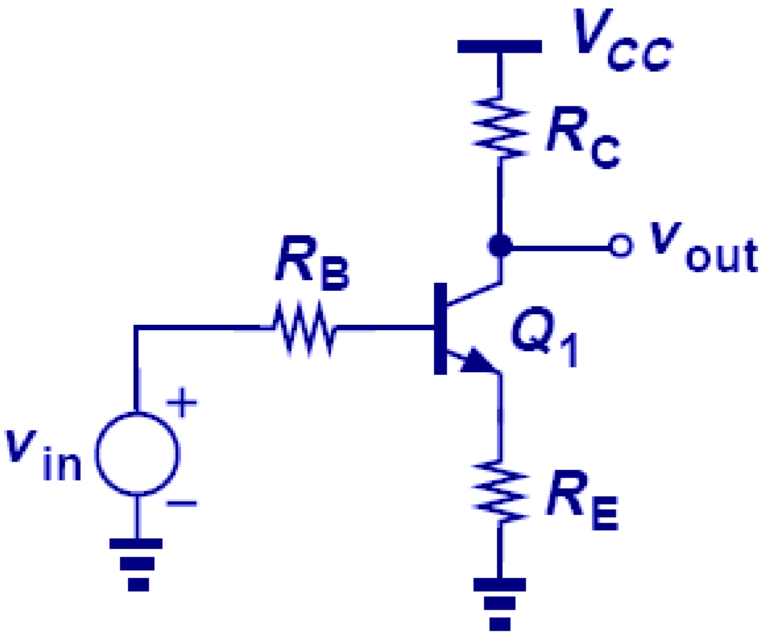
CB with Base Resistance

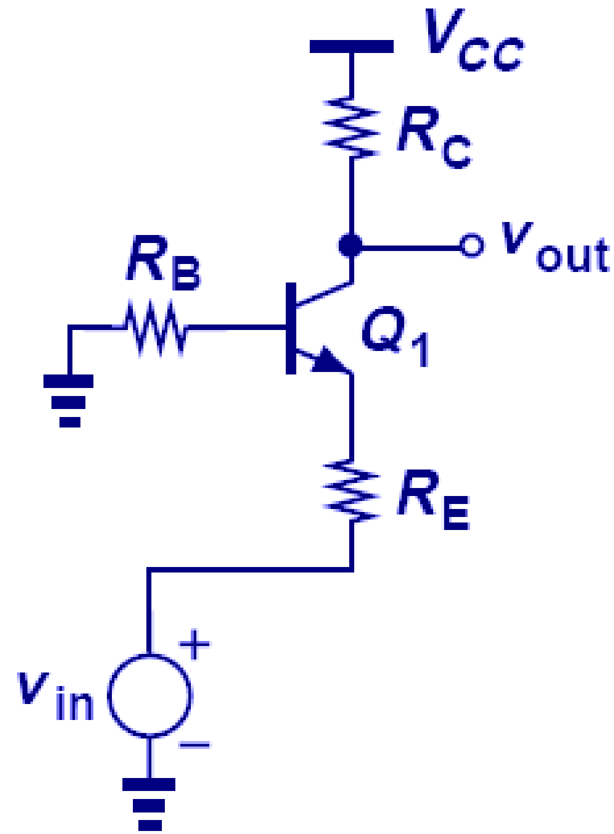


$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \frac{R_B}{\beta + 1} + \frac{1}{g_m}}$$

- With an addition of base resistance, the voltage gain degrades.

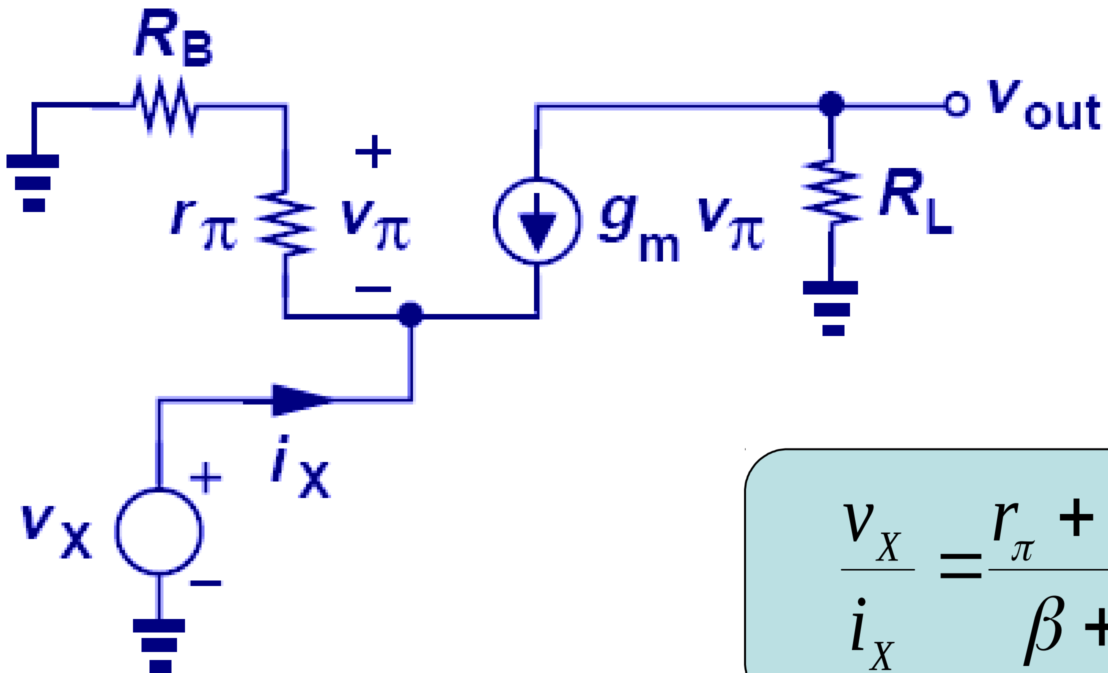
Comparison of CE and CB Stages with Base Resistance





- **The voltage gain of CB amplifier with base resistance is exactly the same as that of CE stage with base resistance and emitter degeneration, except for a negative sign.**

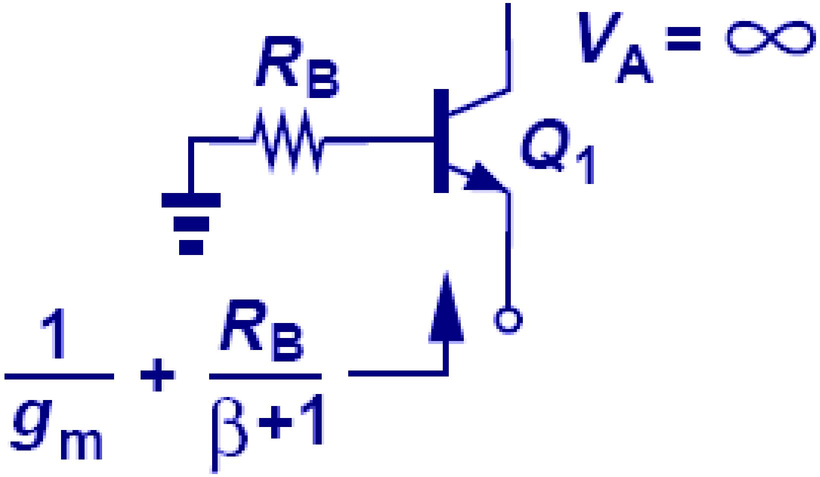
Input Impedance of CB Stage with Base Resistance

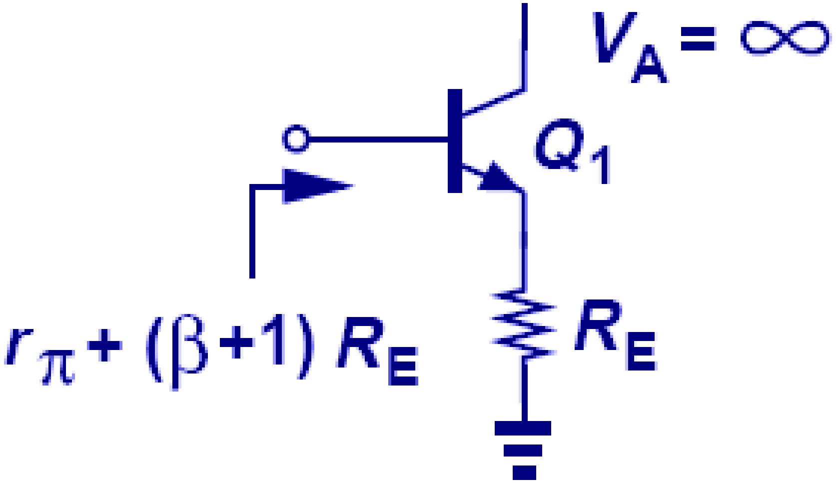


$$\frac{v_X}{i_X} = \frac{r_\pi + R_B}{\beta + 1} \approx \frac{1}{g_m} + \frac{R_B}{\beta + 1}$$

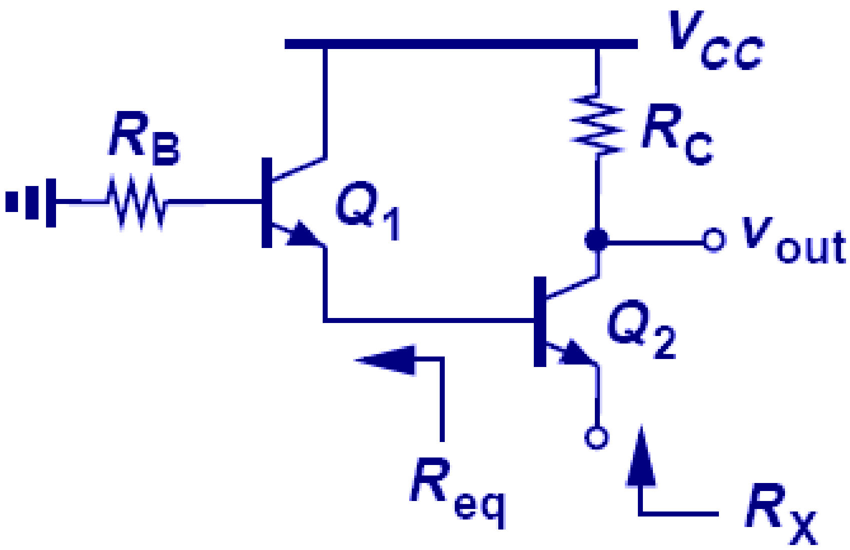
- **The input impedance of CB with base resistance is equal to $1/g_m$ plus R_B divided by (β+1). This is in contrast to degenerated CE stage, in which the resistance in series with the emitter is *multiplied* by (β+1) when seen from the base.**

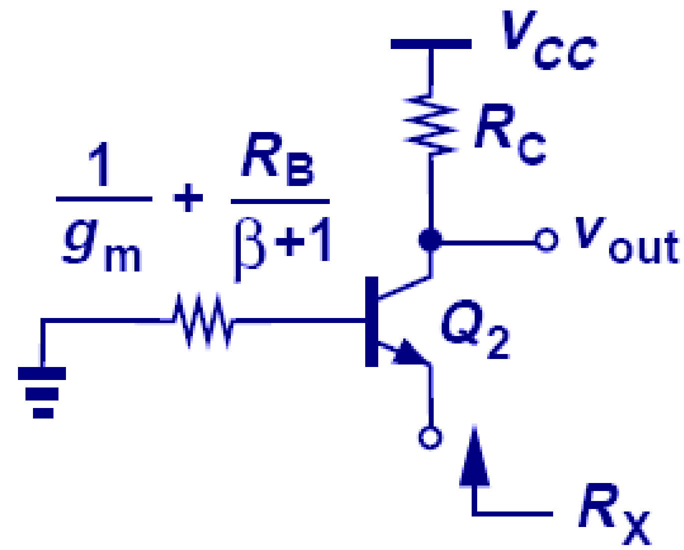
Input Impedance Seen at Emitter and Base





Input Impedance Example

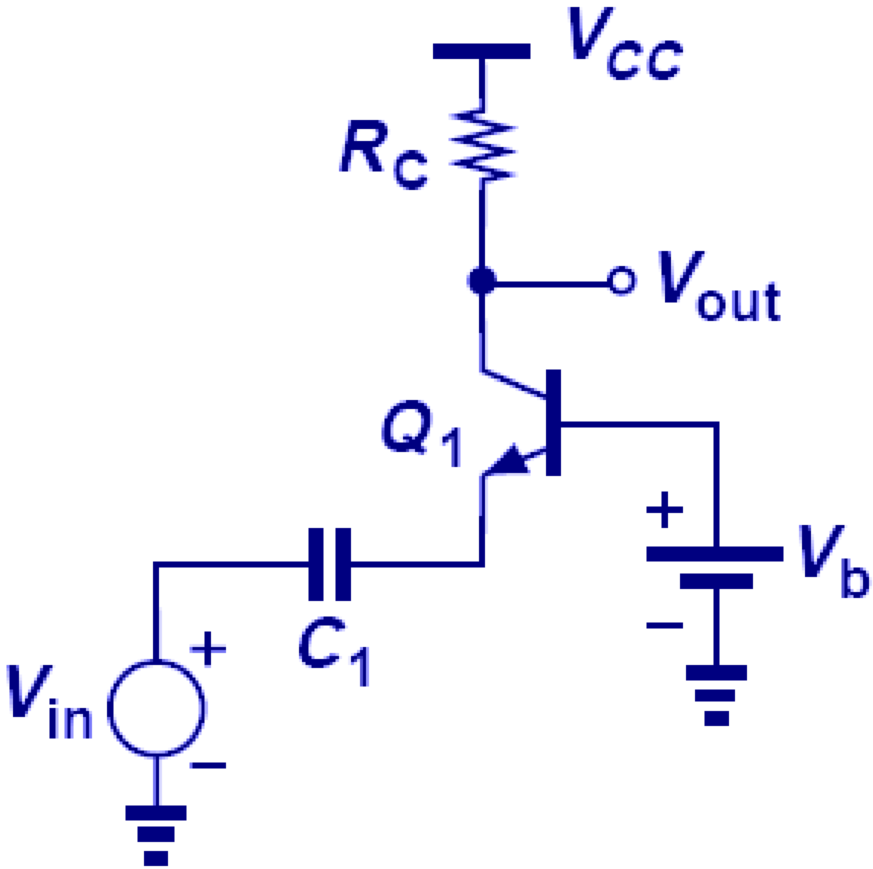




$$R_X = \frac{1}{g_{m2}} + \frac{1}{\beta+1}\left(\frac{1}{g_{m1}} + \frac{R_B}{\beta+1}\right)$$

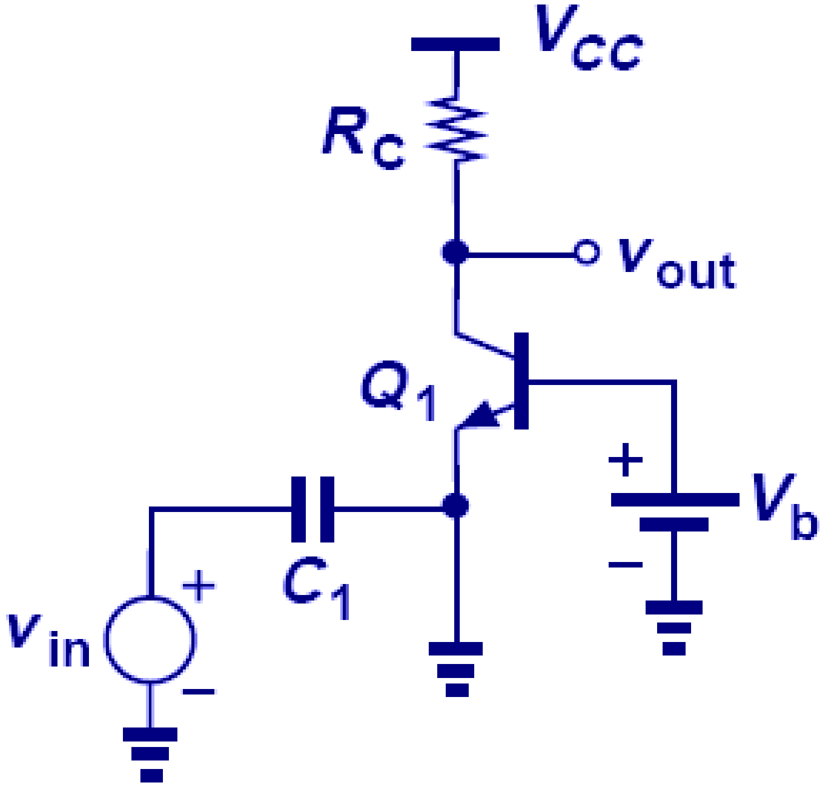
- **To find the R_X, we have to first find $R_{eq,}$ treat it as the base resistance of Q_2 and divide it by (β+1).**

Bad Bias Technique for CB Stage



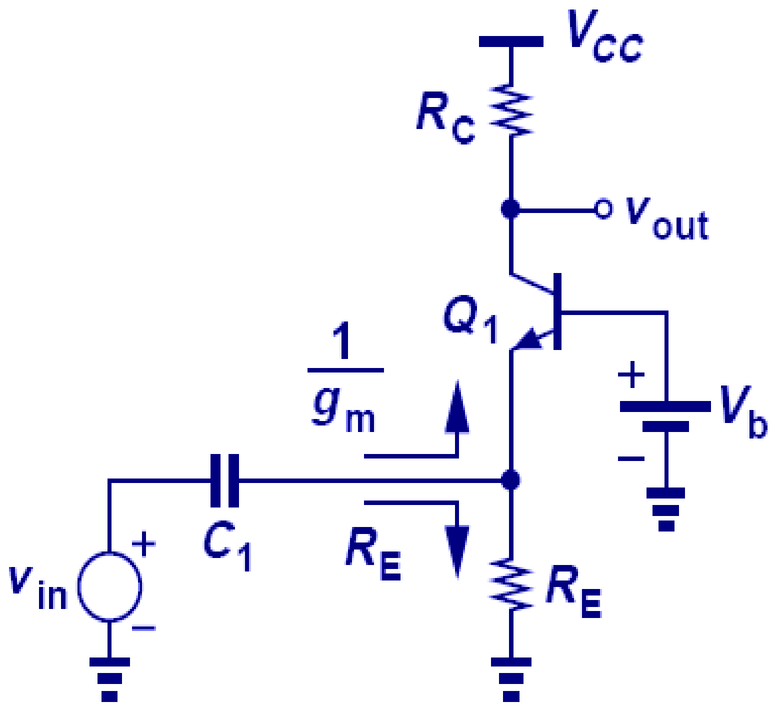
- Unfortunately, no emitter current can flow.

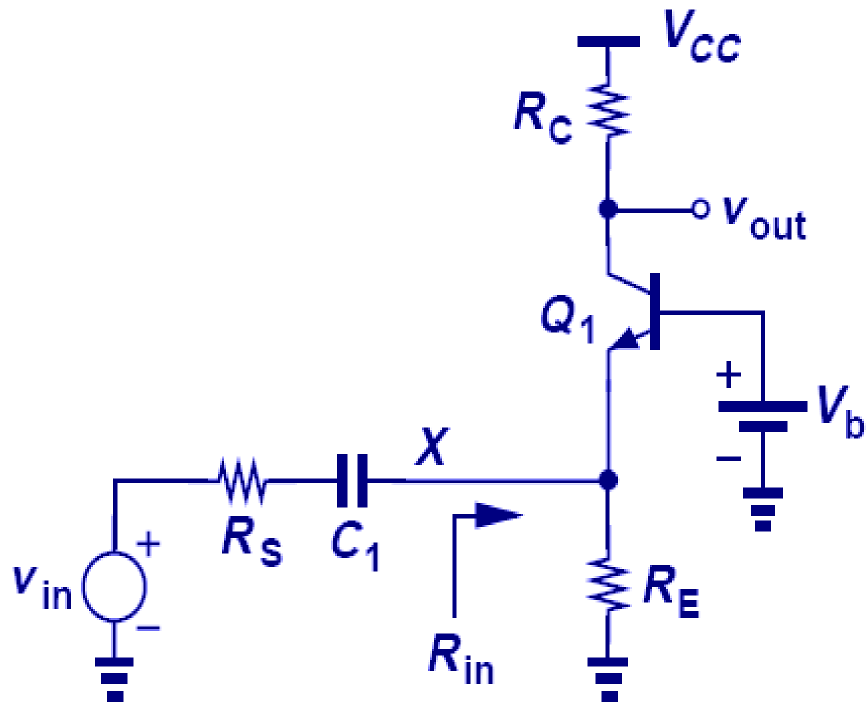
Still No Good



- In haste, the student connects the emitter to ground, thinking it will provide a DC current path to bias the amplifier. Little did he/she know that the input signal has been shorted to ground as well. The circuit still does not amplify.

Proper Biasing for CB Stage

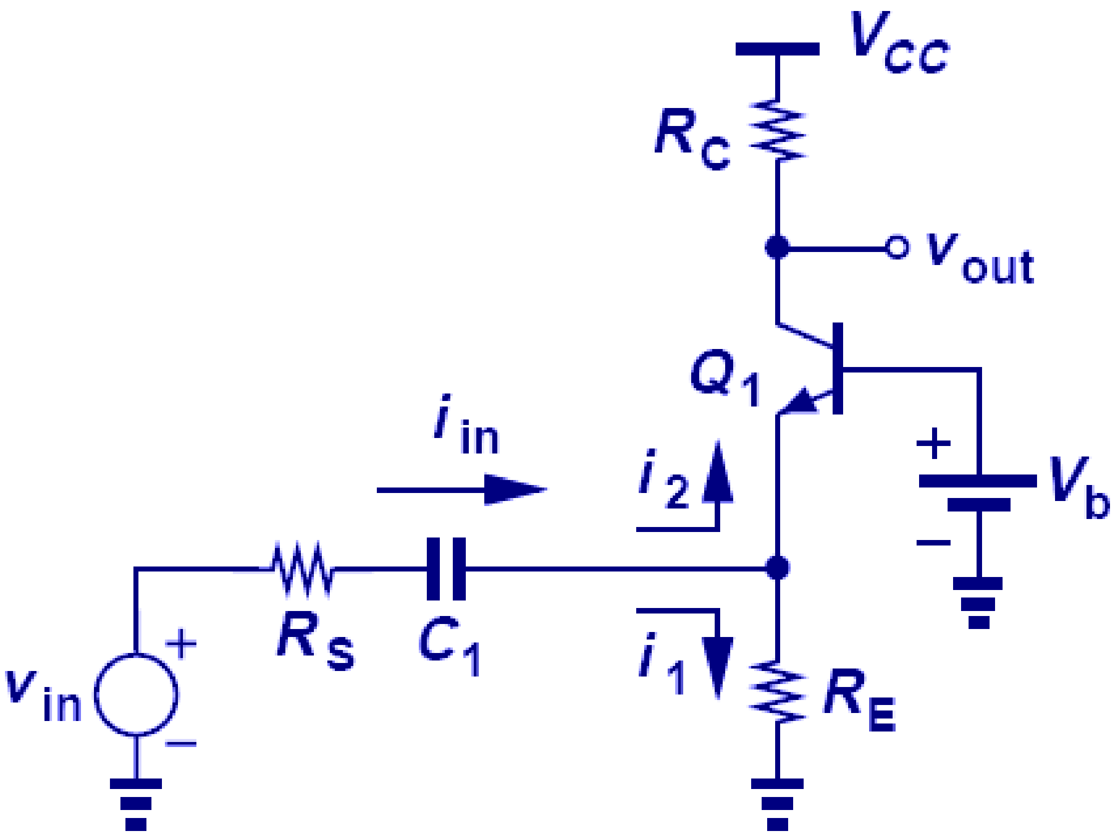




$$R_{in} = \frac{1}{g_m} \parallel R_E$$

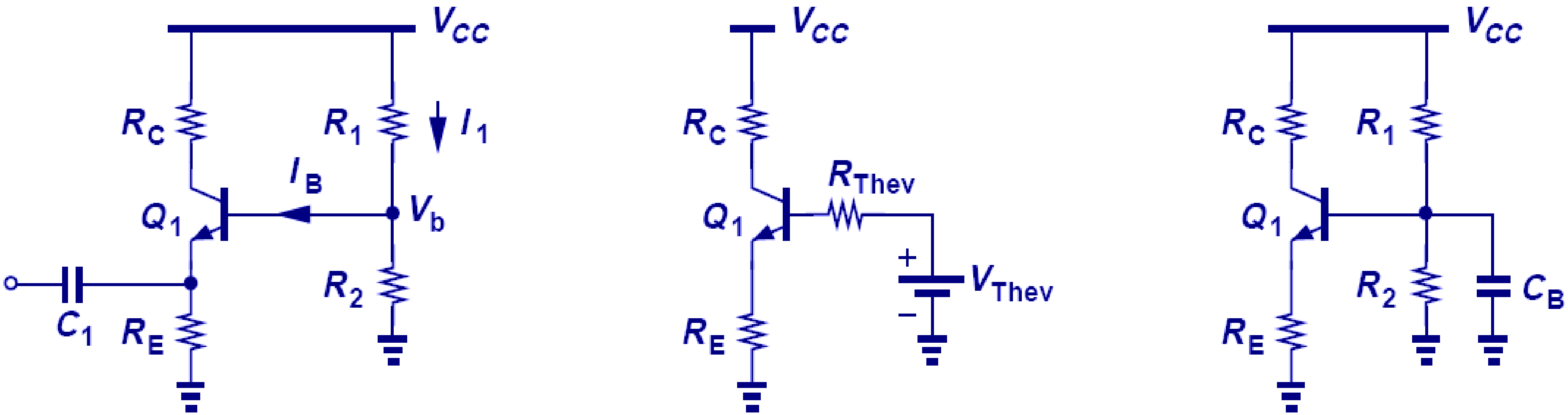
$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + (1 + g_m R_E) R_S} g_m R_C$$

Reduction of Input Impedance Due to R_E



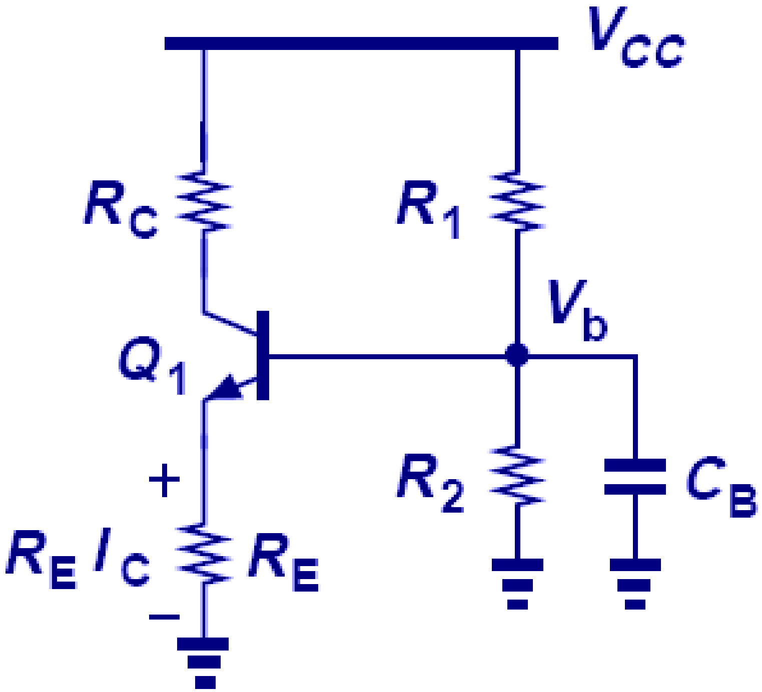
- The reduction of input impedance due to R_E is bad because it shunts part of the input current to ground instead of to Q_1 (and R_c) .

Creation of V_b



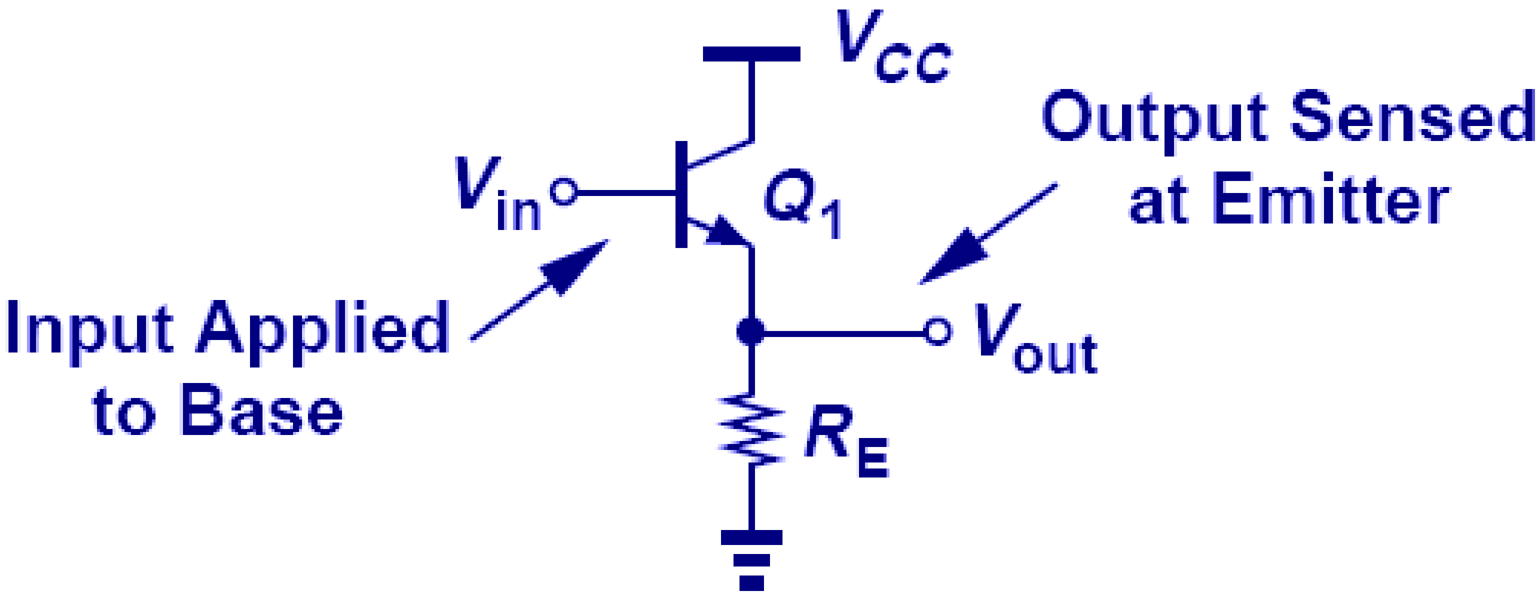
- **Resistive divider lowers the gain.**
- **To remedy this problem, a capacitor is inserted from base to ground to short out the resistor divider at the frequency of interest.**

Example of CB Stage with Bias

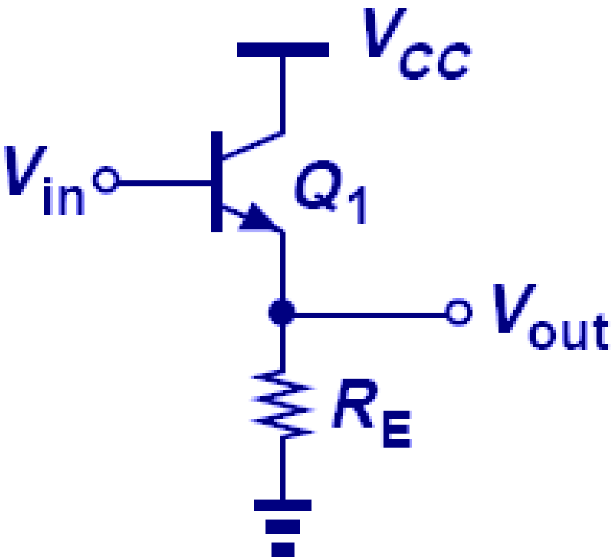


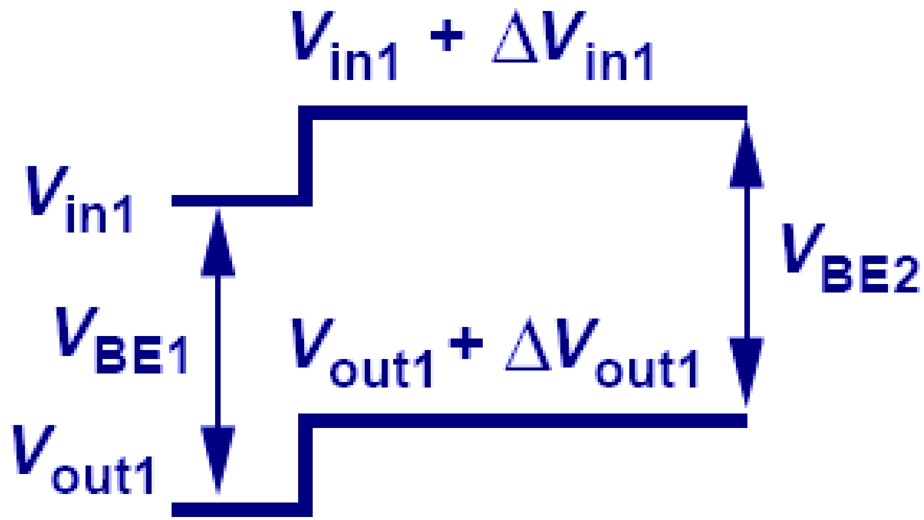
- For the circuit shown above, $R_E \gg 1/g_m$.
- R_1 and R_2 are chosen so that V_b is at the appropriate value and the current that flows thru the divider is much larger than the base current.
- Capacitors are chosen to be small compared to $1/g_m$ at the required frequency.

Emitter Follower (Common Collector Amplifier)



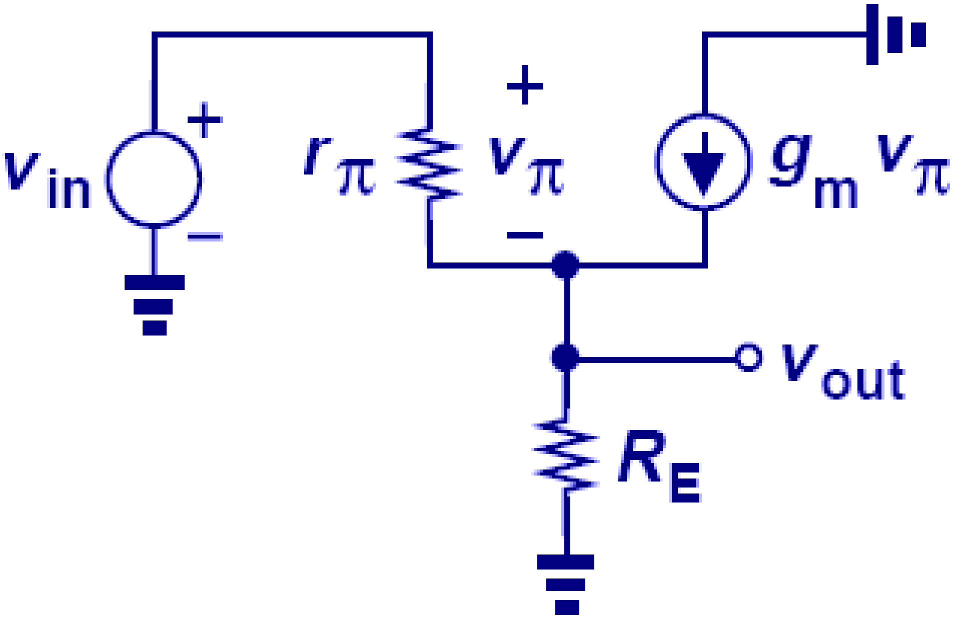
Emitter Follower Core





- When the input is increased by ΔV, output is also increased by an amount that is less than ΔV due to the increase in collector current and hence the increase in potential drop across R_E.
- However the absolute values of input and output differ by a V_{BE}.

Small-Signal Model of Emitter Follower

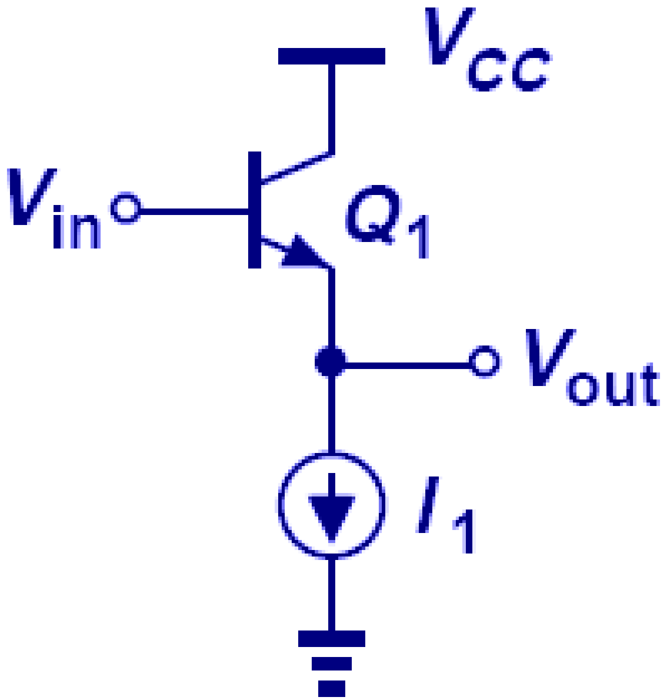


$$V_A = \infty$$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + \frac{r_\pi}{\beta + 1} \cdot \frac{1}{R_E}} \approx \frac{R_E}{R_E + \frac{1}{g_m}}$$

- **As shown above, the voltage gain is less than unity and positive.**

Unity-Gain Emitter Follower

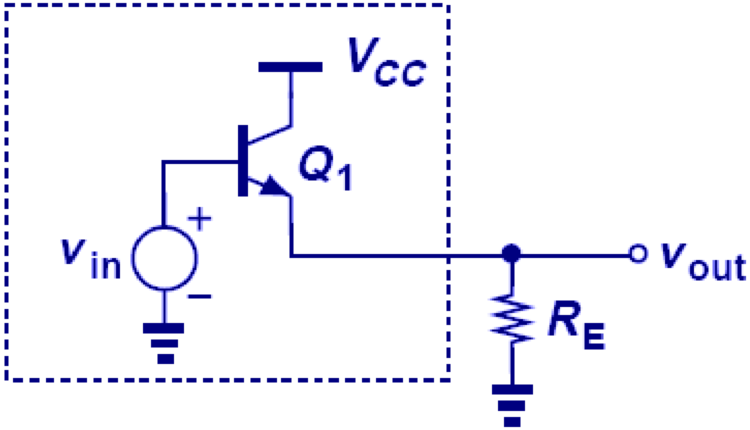


$$V_A = \infty$$

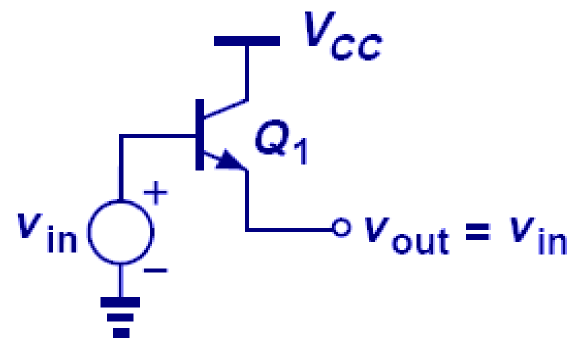
$$A_v = 1$$

- The voltage gain is unity because a constant collector current (= I_1) results in a constant V_{BE}, and hence V_{out} follows V_{in} exactly.

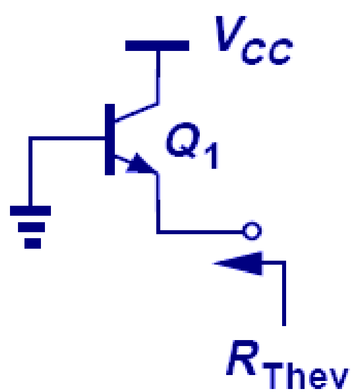
Analysis of Emitter Follower as a Voltage Divider



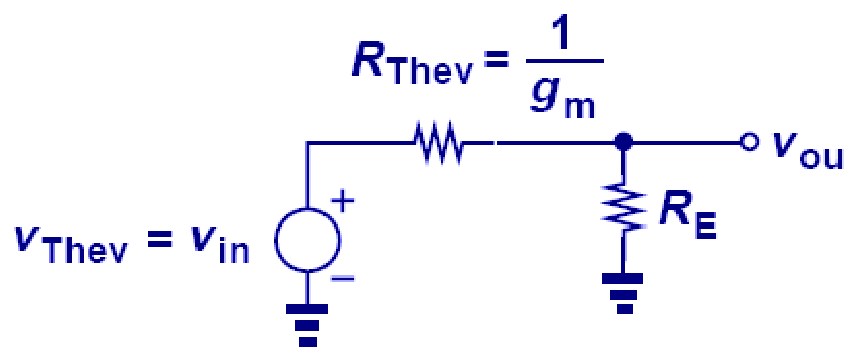
(a)



(b)



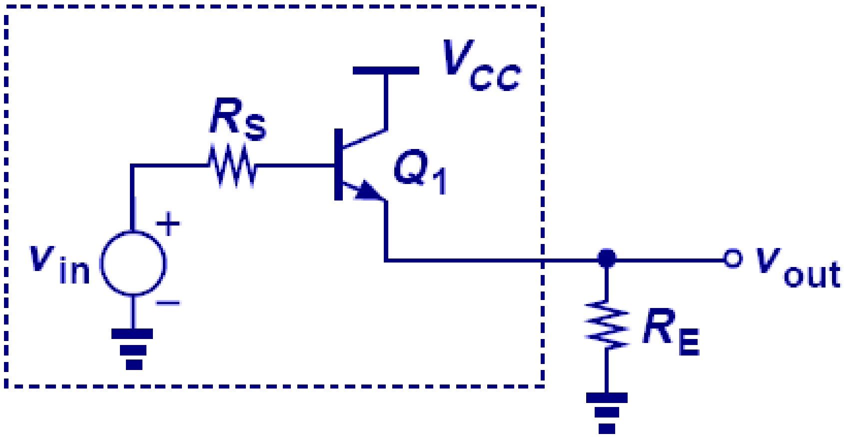
(c)



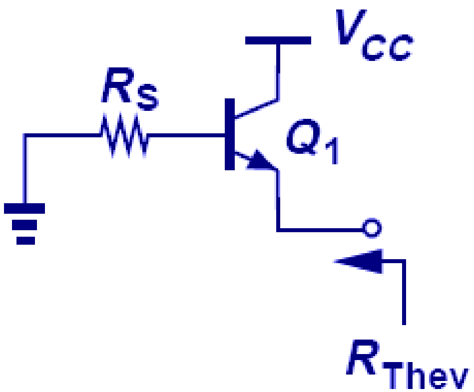
(d)

$$V_A = \infty$$

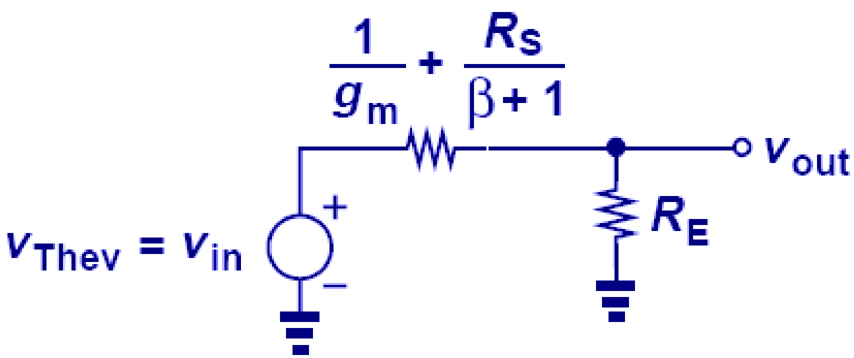
Emitter Follower with Source Resistance



(a)



(b)

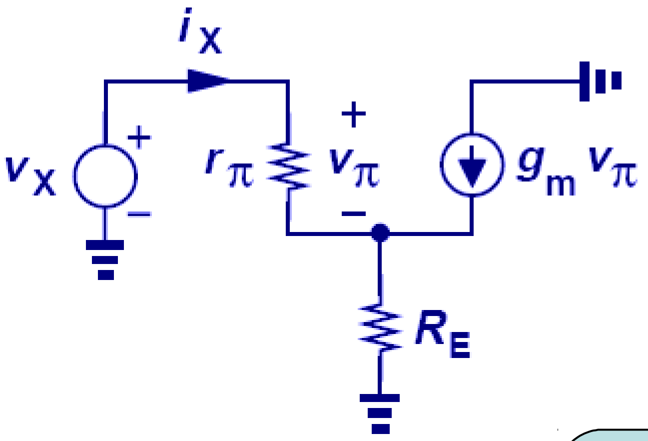


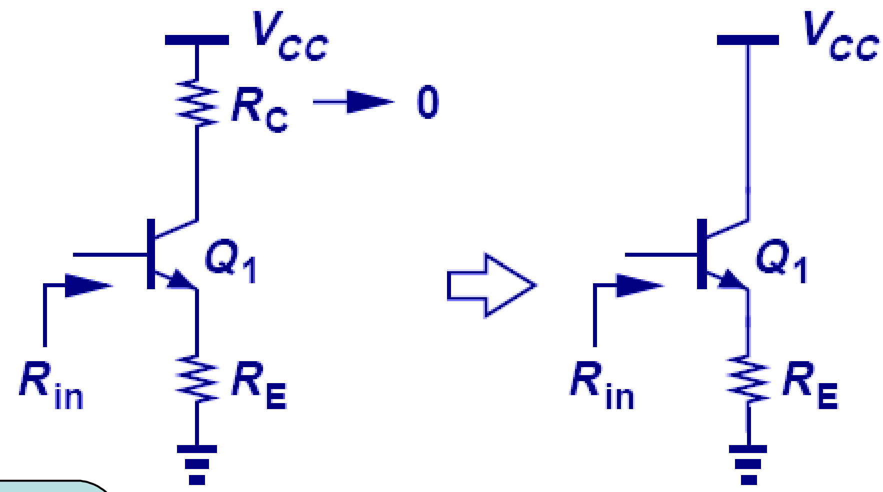
(c)

$$V_A = \infty$$

$$\frac{v_{out}}{v_{in}} = \frac{R_E}{R_E + \frac{R_S}{\beta + 1} + \frac{1}{g_m}}$$

Input Impedance of Emitter Follower



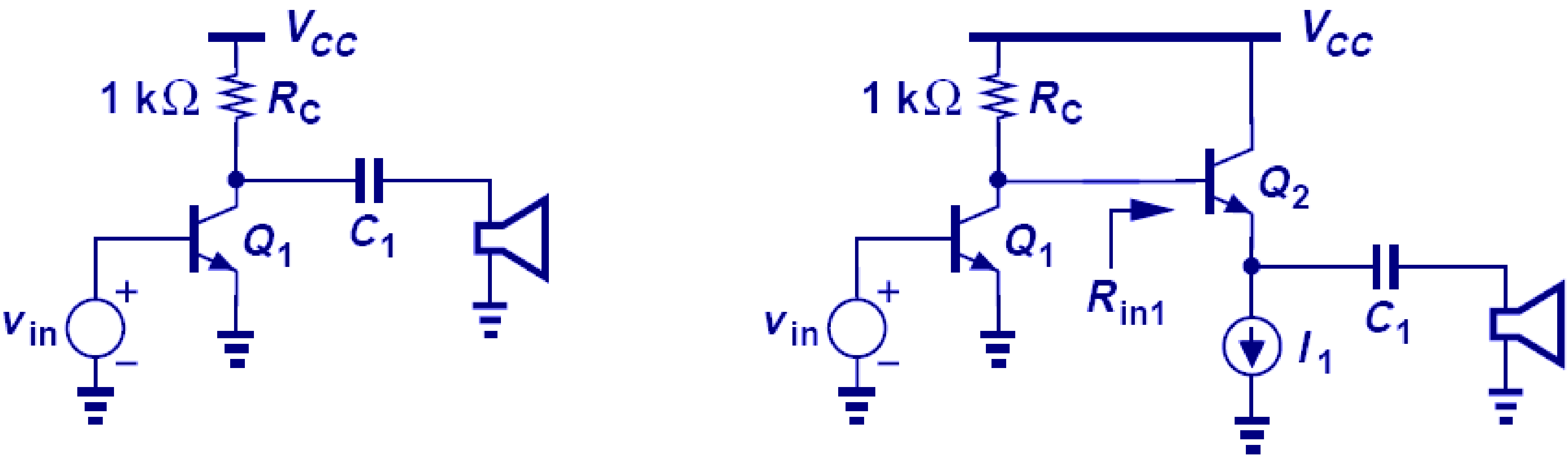


$$V_A = \infty$$

$$\frac{v_X}{i_X} = r_\pi + (1+\beta)R_E$$

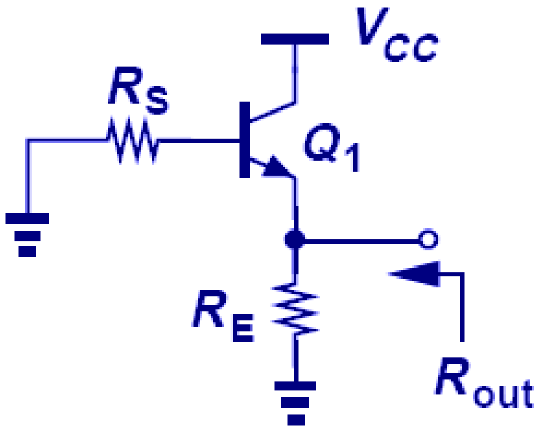
- **The input impedance of emitter follower is exactly the same as that of CE stage with emitter degeneration. This is not surprising because the input impedance of CE with emitter degeneration does not depend on the collector resistance.**

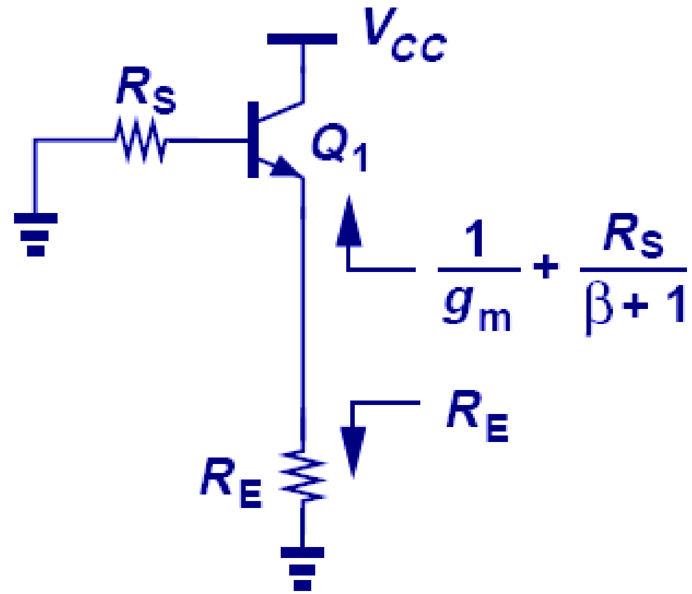
Emitter Follower as Buffer



- Since the emitter follower increases the load resistance to a much higher value, it is suited as a buffer between a CE stage and a heavy load resistance to alleviate the problem of gain degradation.

Output Impedance of Emitter Follower

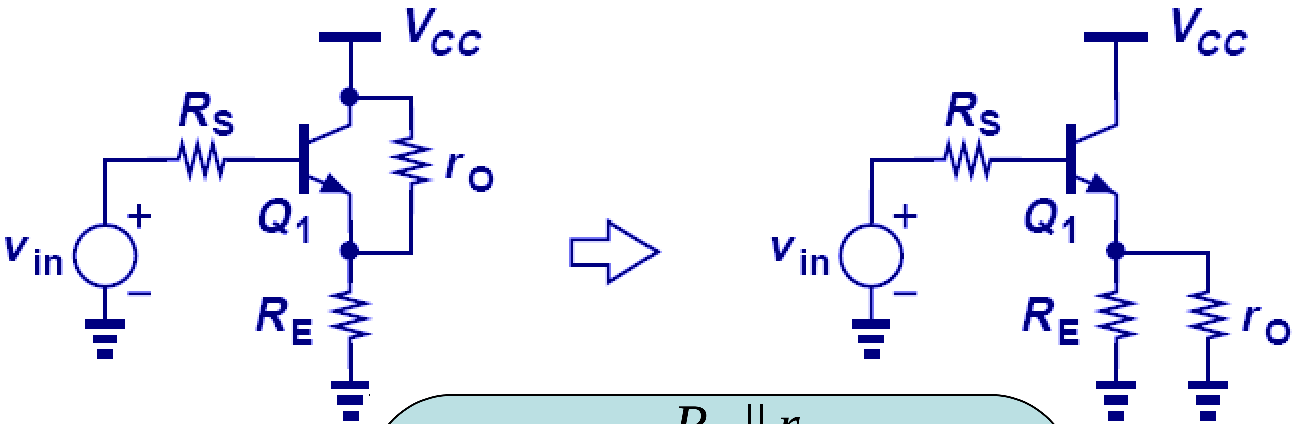




$$R_{out} = \left(\frac{R_s}{\beta + 1} + \frac{1}{g_m} \right) \| R_E$$

- Emitter follower <u>lowers</u> the source impedance by a factor of β+1 → improved driving capability.

Emitter Follower with Early Effect



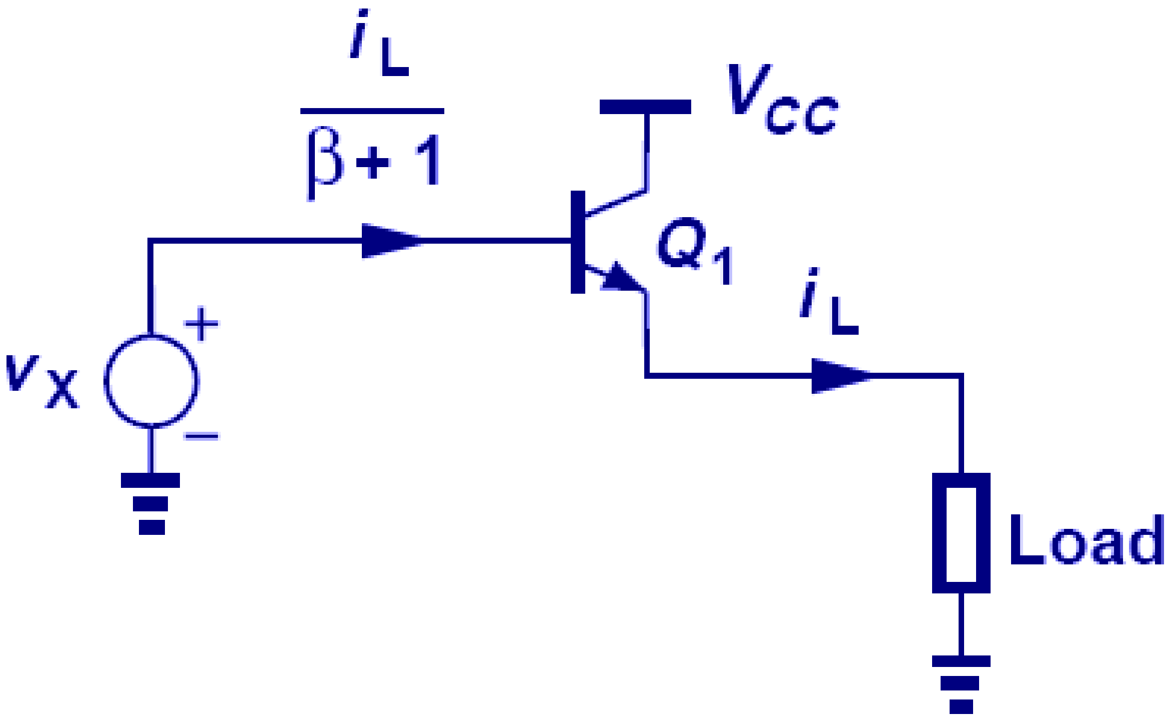
$$A_v = \frac{R_E \parallel r_O}{R_E \parallel r_O + \frac{R_S}{\beta + 1} + \frac{1}{g_m}}$$

$$R_{in} = r_\pi + (\beta + 1)(R_E \parallel r_O)$$

$$R_{out} = \left(\frac{R_s}{\beta + 1} + \frac{1}{g_m}\right) \parallel R_E \parallel r_O$$

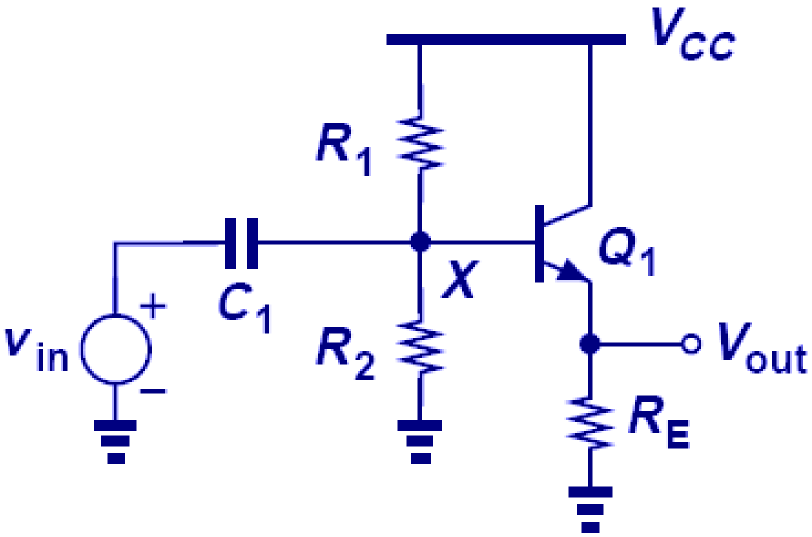
- Since r_O is in parallel with R_E, its effect can be easily incorporated into voltage gain and input and output impedance equations.

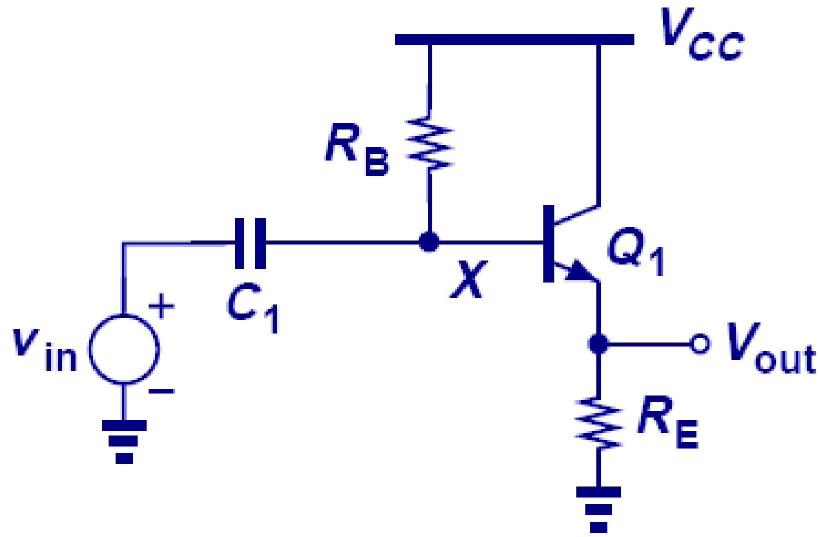
Current Gain



- There is a current gain of (β+1) from base to emitter.
- Effectively speaking, the load resistance is multiplied by (β+1) as seen from the base.

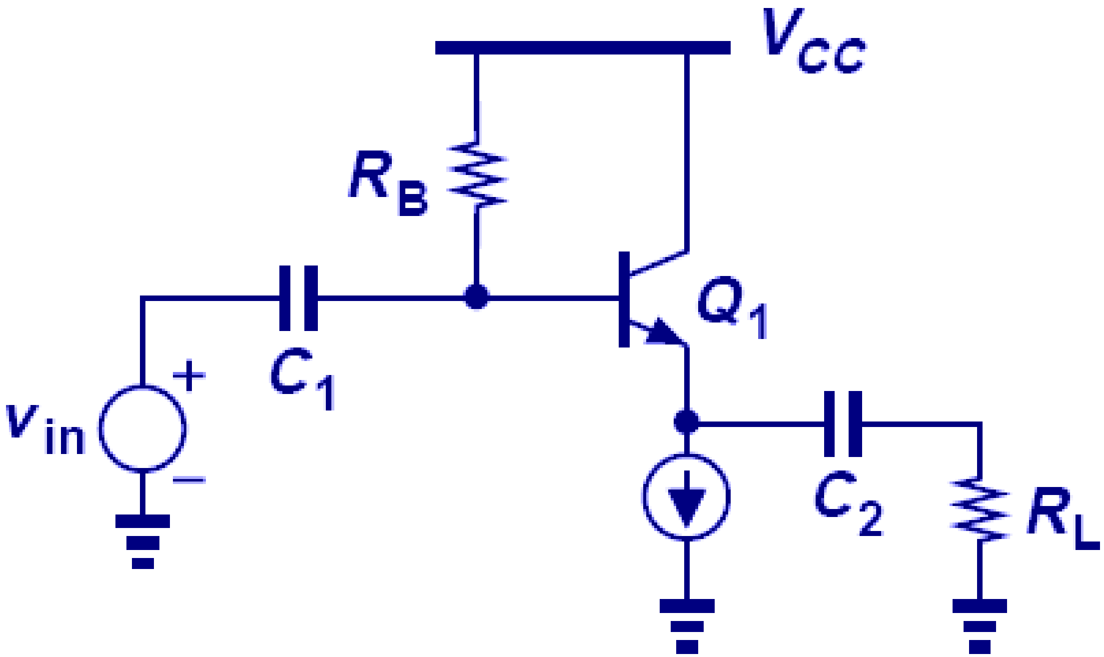
Emitter Follower with Biasing





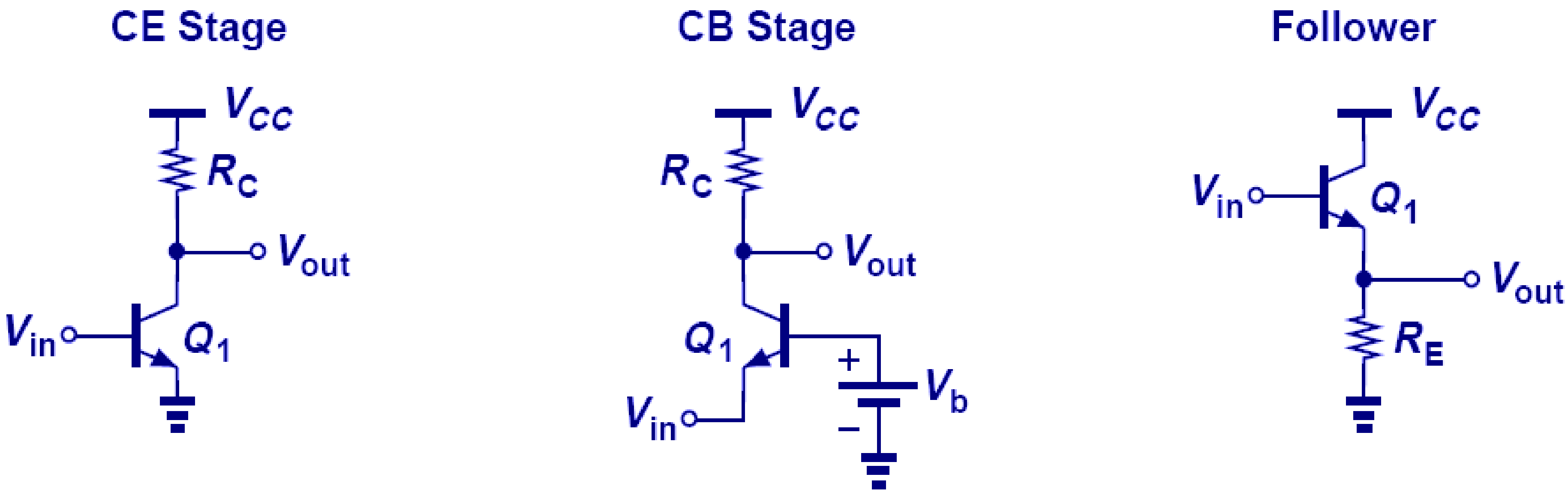
- A biasing technique similar to that of CE stage can be used for the emitter follower.
- Also, V_b can be close to V_{cc} because the collector is also at V_{cc}.

Supply-Independent Biasing



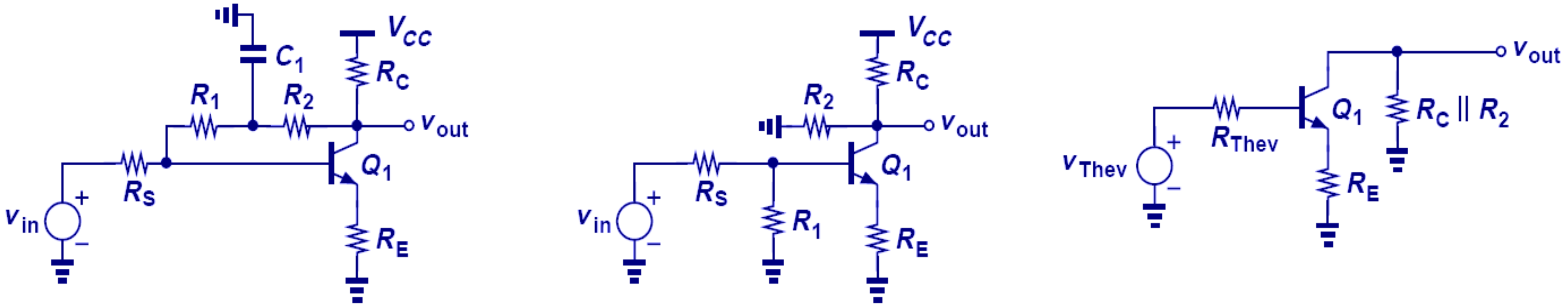
- By putting a constant current source at the emitter, the bias current, V_{BE}, and $I_B R_B$ are fixed regardless of the supply value.

Summary of Amplifier Topologies



- **The three amplifier topologies studied so far have different properties and are used on different occasions.**
- **CE and CB have voltage gain with magnitude greater than one, while follower's voltage gain is at most one.**

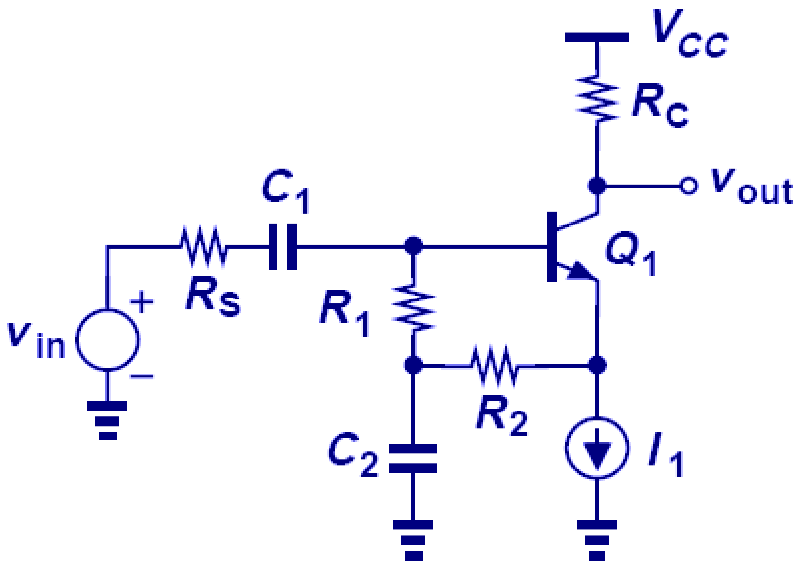
Amplifier Example I

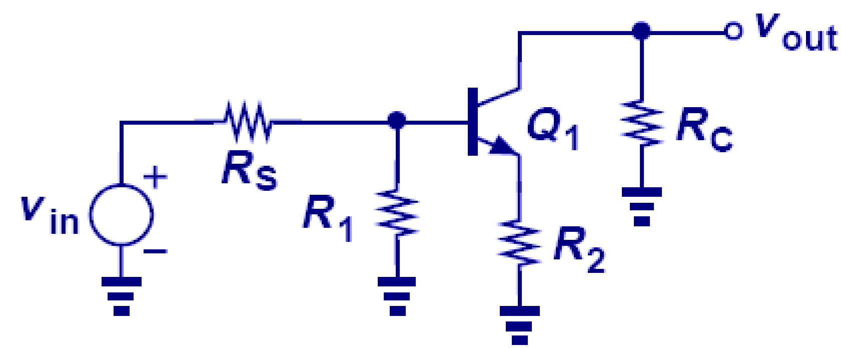


$$\frac{v_{out}}{v_{in}} = -\frac{R_2 \| R_C}{\frac{R_1 \| R_S}{\beta+1} + \frac{1}{g_m} + R_E} \cdot \frac{R_1}{R_1 + R_S}$$

- **The keys in solving this problem are recognizing the AC ground between R_1 and R_2, and Thevenin transformation of the input network.**

Amplifier Example II

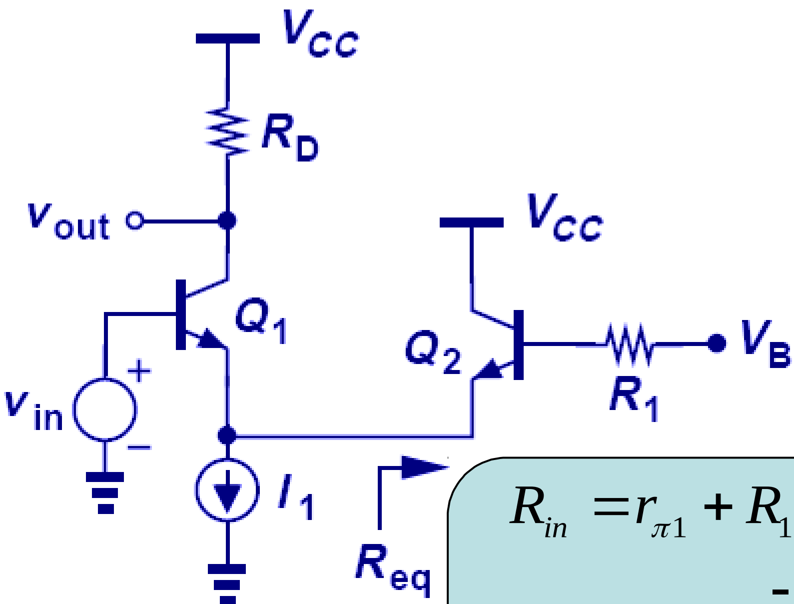




$$\frac{v_{out}}{v_{in}} = -\frac{R_C}{\frac{R_S \parallel R_1}{\beta+1} + \frac{1}{g_m} + R_2} \cdot \frac{R_1}{R_1 + R_S}$$

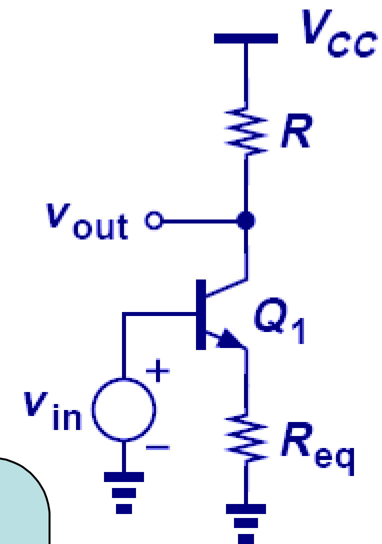
- **Again, AC ground/short and Thevenin transformation are needed to transform the complex circuit into a simple stage with emitter degeneration.**

Amplifier Example III



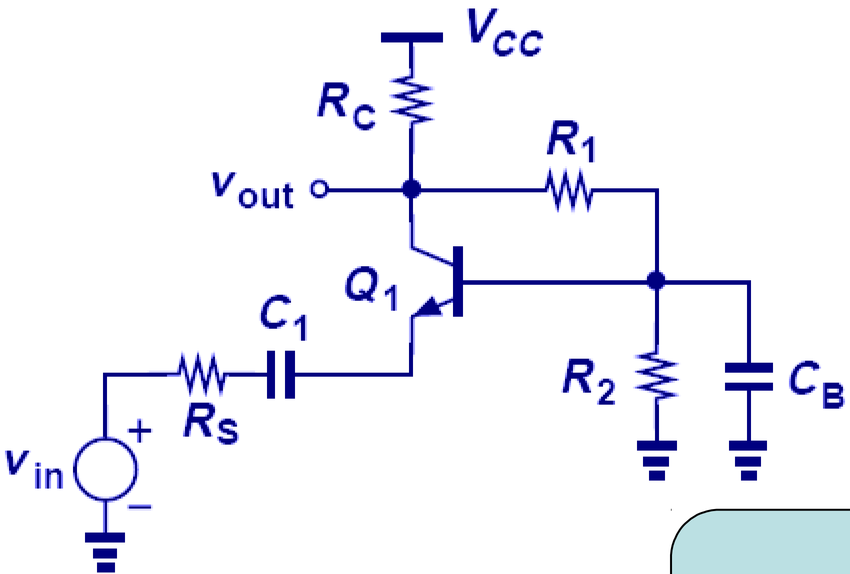
$$R_{in} = r_{\pi 1} + R_1 + r_{\pi 2}$$

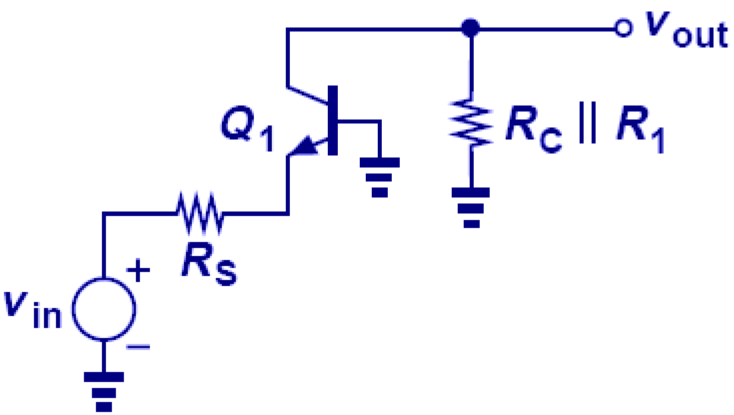
$$A_v = \frac{-R_C}{\frac{1}{g_{m1}} + \frac{R_1}{\beta + 1} + \frac{1}{g_{m2}}}$$



- **The key for solving this problem is first identifying R_{eq}, which is the impedance seen at the emitter of Q_2 in parallel with the infinite output impedance of an ideal current source. Second, use the equations for degenerated CE stage with R_E replaced by R_{eq}.**

Amplifier Example IV

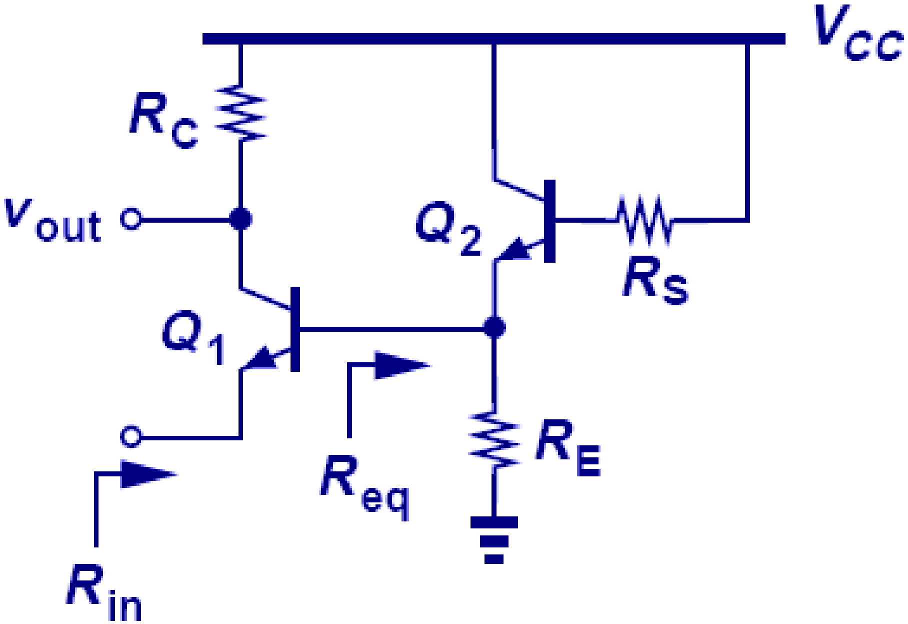


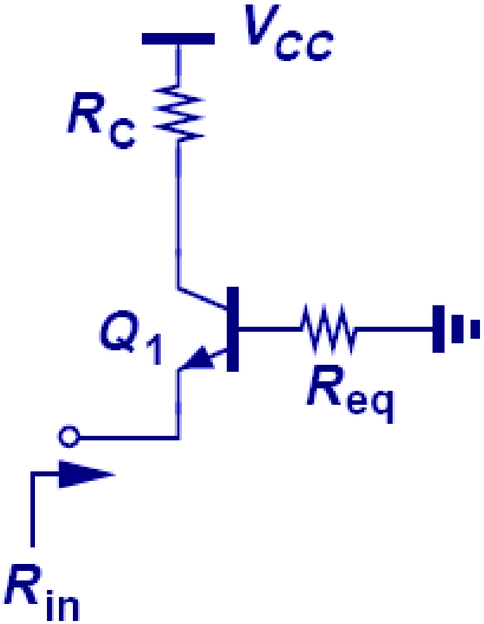


$$A_v = \frac{R_C \parallel R_1}{R_S + \frac{1}{g_m}}$$

- **The key for solving this problem is recognizing that C_B at frequency of interest shorts out R_2 and provide a ground for R_1.**
- **R_1 appears in parallel with R_C and the circuit simplifies to a simple CB stage.**

Amplifier Example V

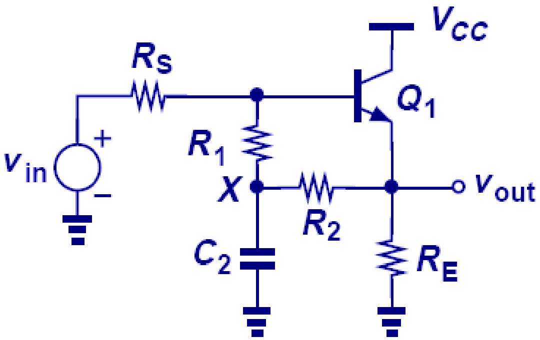




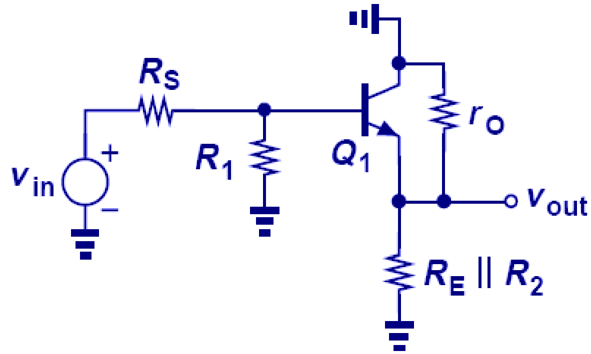
$$R_{in} = \frac{1}{\beta+1}\left[\left(\frac{R_B}{\beta+1}+\frac{1}{g_{m2}}\right)\| R_E\right]+\frac{1}{g_{m1}}$$

- The key for solving this problem is recognizing the equivalent base resistance of Q_1 is the parallel connection of R_E and the impedance seen at the emitter of Q_2.

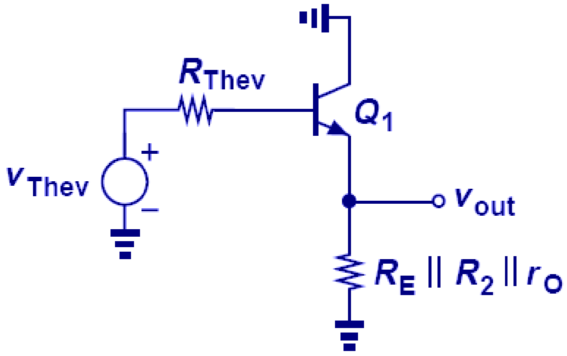
Amplifier Example VI



(a)



(b)



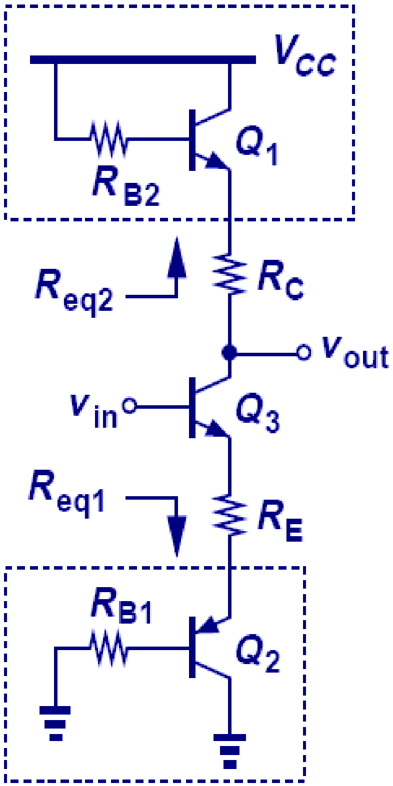
(c)

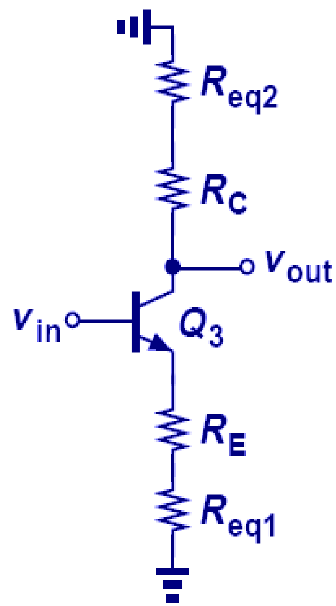
$$\frac{v_{out}}{v_{in}} = \frac{R_E \parallel R_2 \parallel r_O}{R_E \parallel R_2 \parallel r_O + \frac{1}{g_m} + \frac{R_S \parallel R_1}{\beta + 1}} \cdot \frac{R_1}{R_1 + R_S}$$

$$R_{out} = \left(\frac{R_S \parallel R_1}{\beta + 1} + \frac{1}{g_m} \right) \parallel R_E \parallel R_2 \parallel r_O$$

- **The key in solving this problem is recognizing a DC supply is actually an AC ground and using Thevenin transformation to simplify the circuit into an emitter follower.**

Amplifier Example VII





$$R_{in} = r_{\pi 1} + (\beta + 1)\left(R_E + \frac{R_{B1}}{\beta + 1} + \frac{1}{g_{m2}} \right)$$

$$R_{out} = R_C + \frac{R_{B2}}{\beta + 1} + \frac{1}{g_{m3}}$$

$$A_v = -\frac{R_C + \frac{R_{B2}}{\beta + 1} + \frac{1}{g_{m3}}}{\frac{R_{B1}}{\beta + 1} + \frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

- Impedances seen at the emitter of Q_1 and Q_2 can be lumped with R_C and R_E, respectively, to form the equivalent emitter and collector impedances.

Chapter 6 Physics of MOS Transistors

- 6.1 Structure of MOSFET
- 6.2 Operation of MOSFET
- 6.3 MOS Device Models
- 6.4 PMOS Transistor
- 6.5 CMOS Technology
- 6.6 Comparison of Bipolar and CMOS Devices

Chapter Outline

Operation of MOSFETs

- MOS Structure
- Operation in Triode Region
- Operation in Saturation
- I/V Characteristics

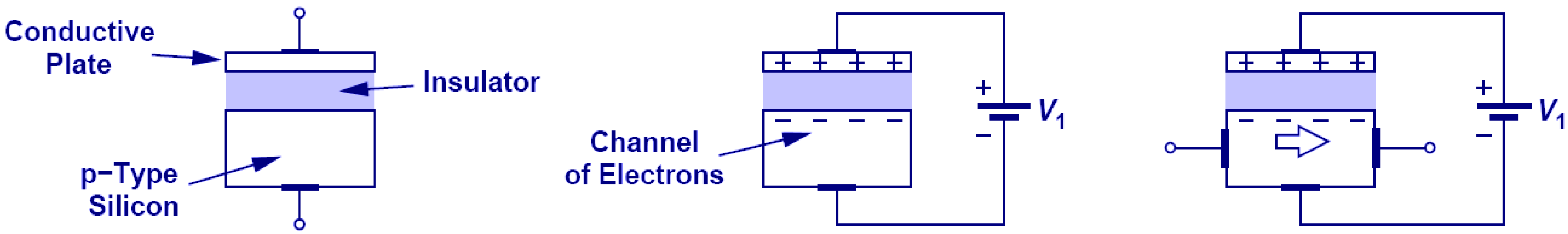
MOS Device Models

- Large−Signal Model
- Small−Signal Model

PMOS Devices

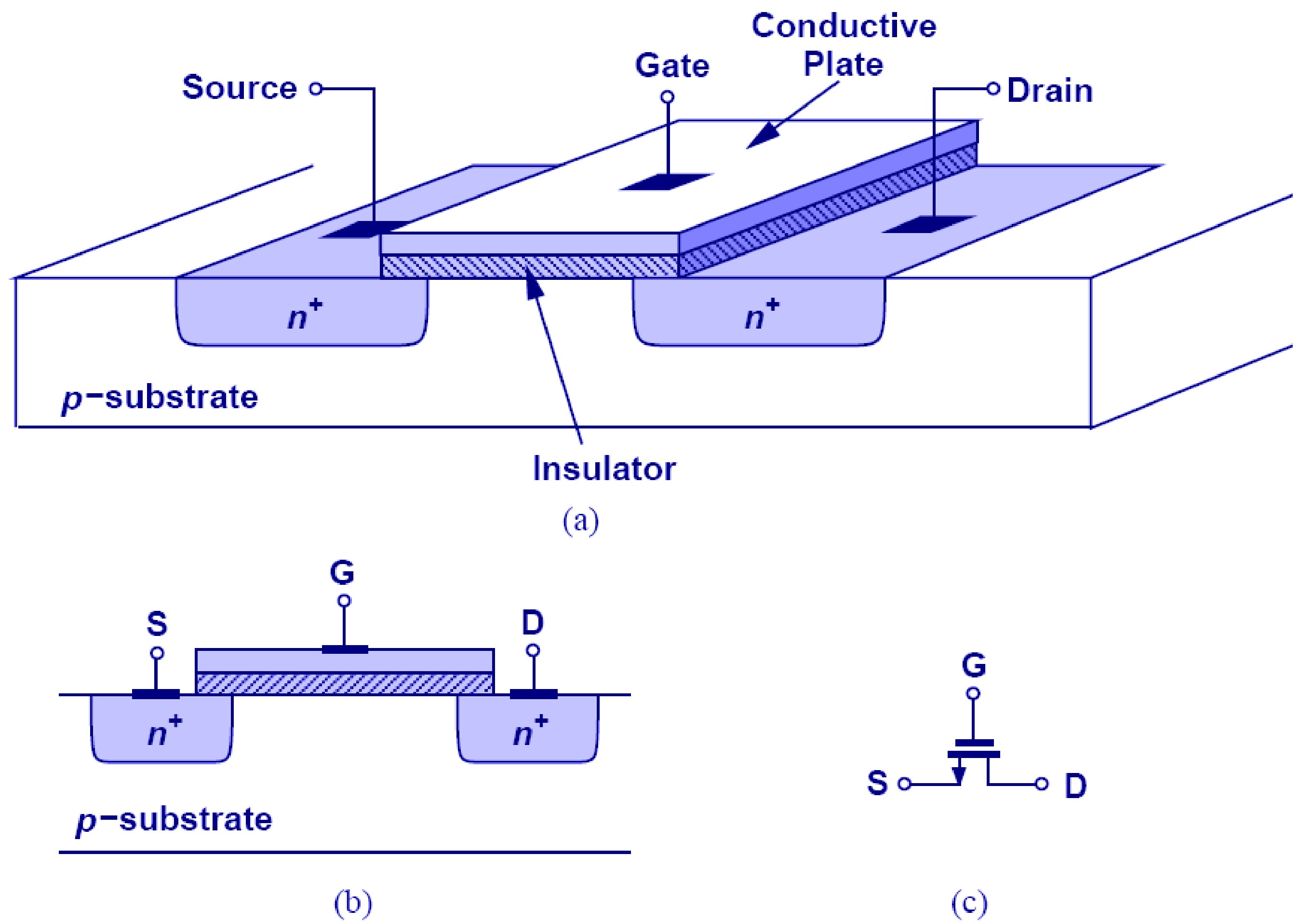
- Structure
- Models

Metal-Oxide-Semiconductor (MOS) Capacitor



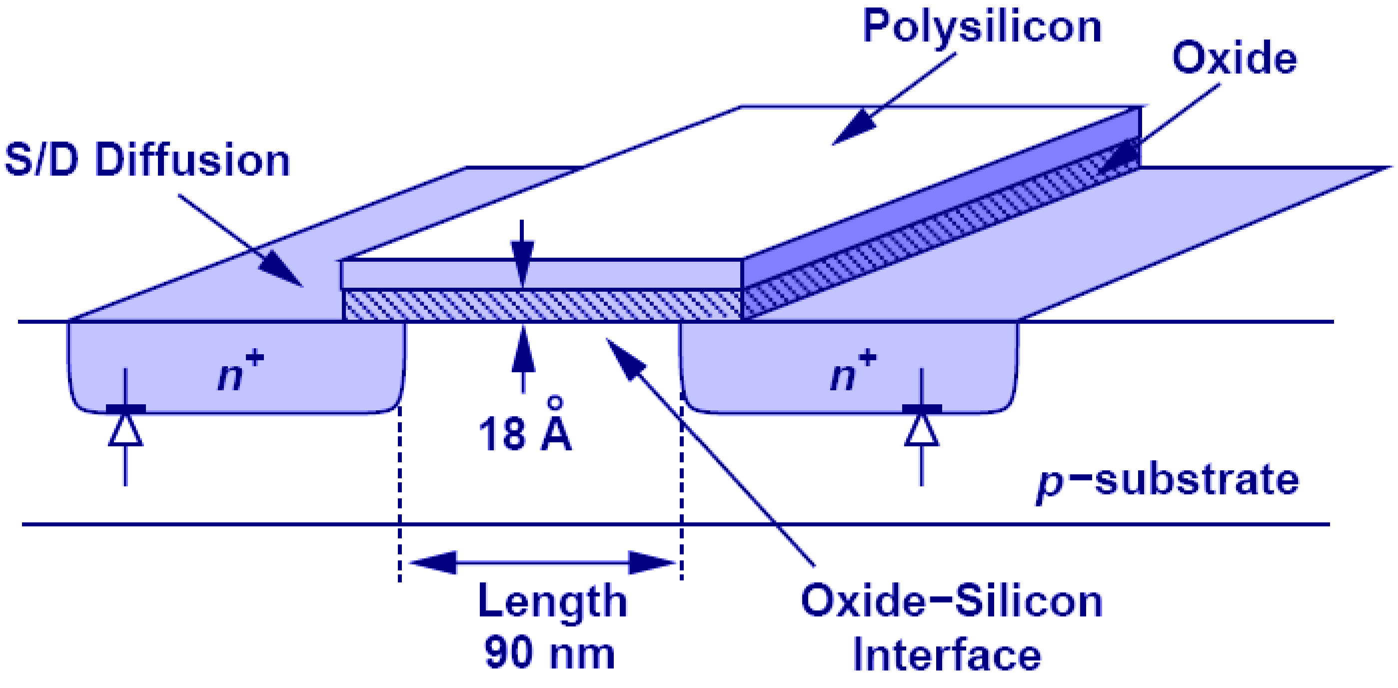
- **The MOS structure can be thought of as a parallel-plate capacitor, with the top plate being the positive plate, oxide being the dielectric, and Si substrate being the negative plate. (We are assuming P-substrate.)**

Structure and Symbol of MOSFET



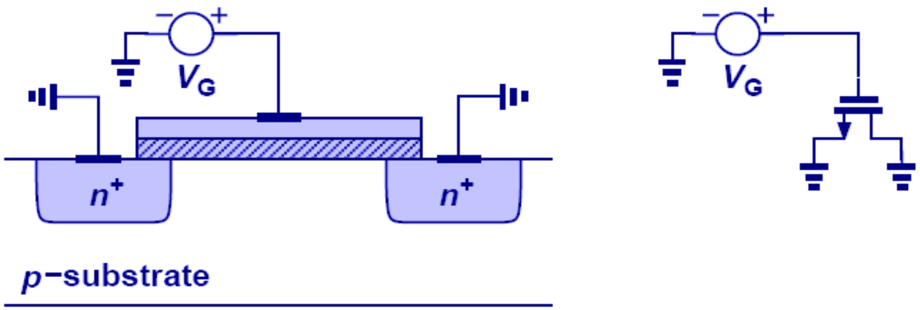
- **This device is symmetric, so either of the n+ regions can be source or drain.**

State of the Art MOSFET Structure

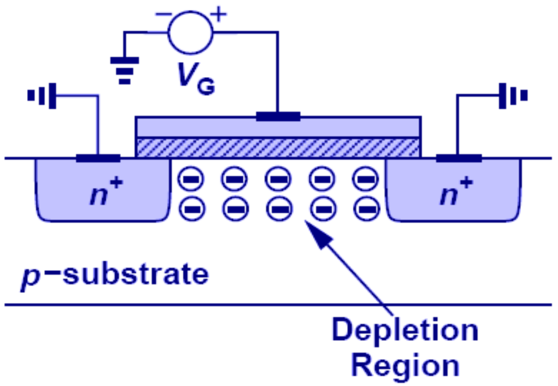


- The gate is formed by polysilicon, and the insulator by Silicon dioxide.

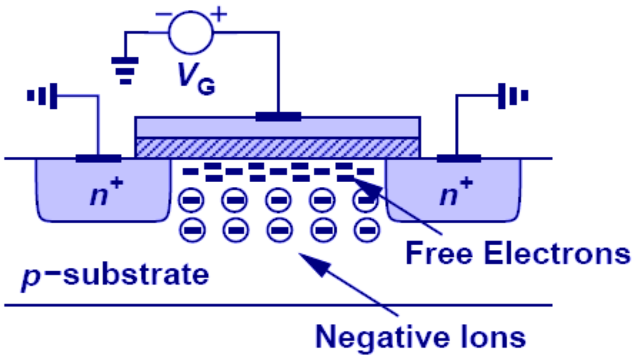
Formation of Channel



(a)



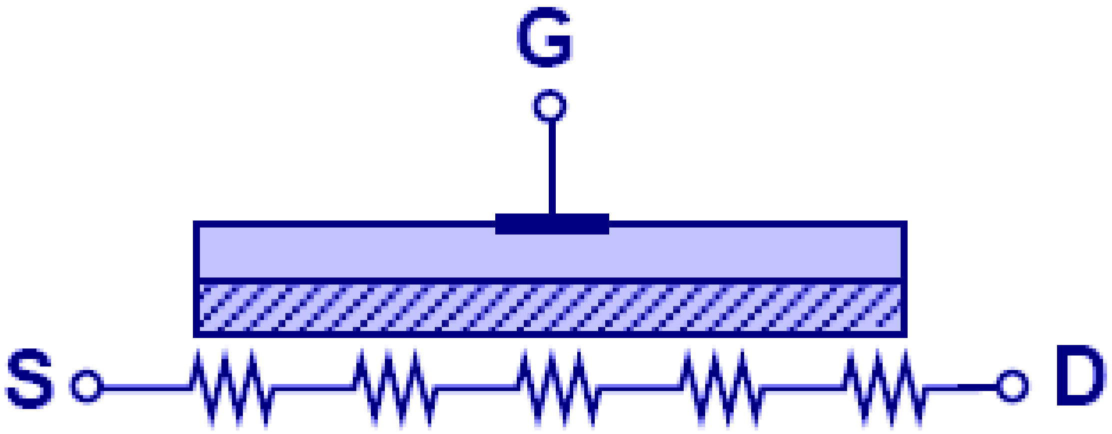
(b)



(c)

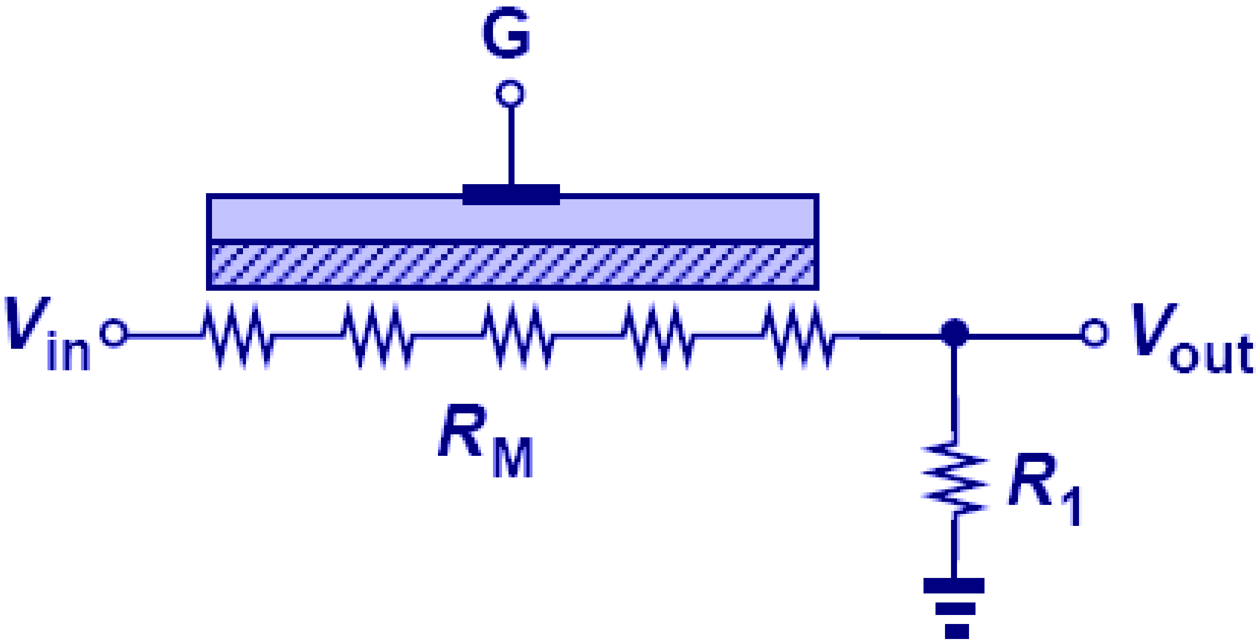
- **First, the holes are repelled by the positive gate voltage, leaving behind negative ions and forming a depletion region. Next, electrons are attracted to the interface, creating a channel ("inversion layer").**

Voltage-Dependent Resistor



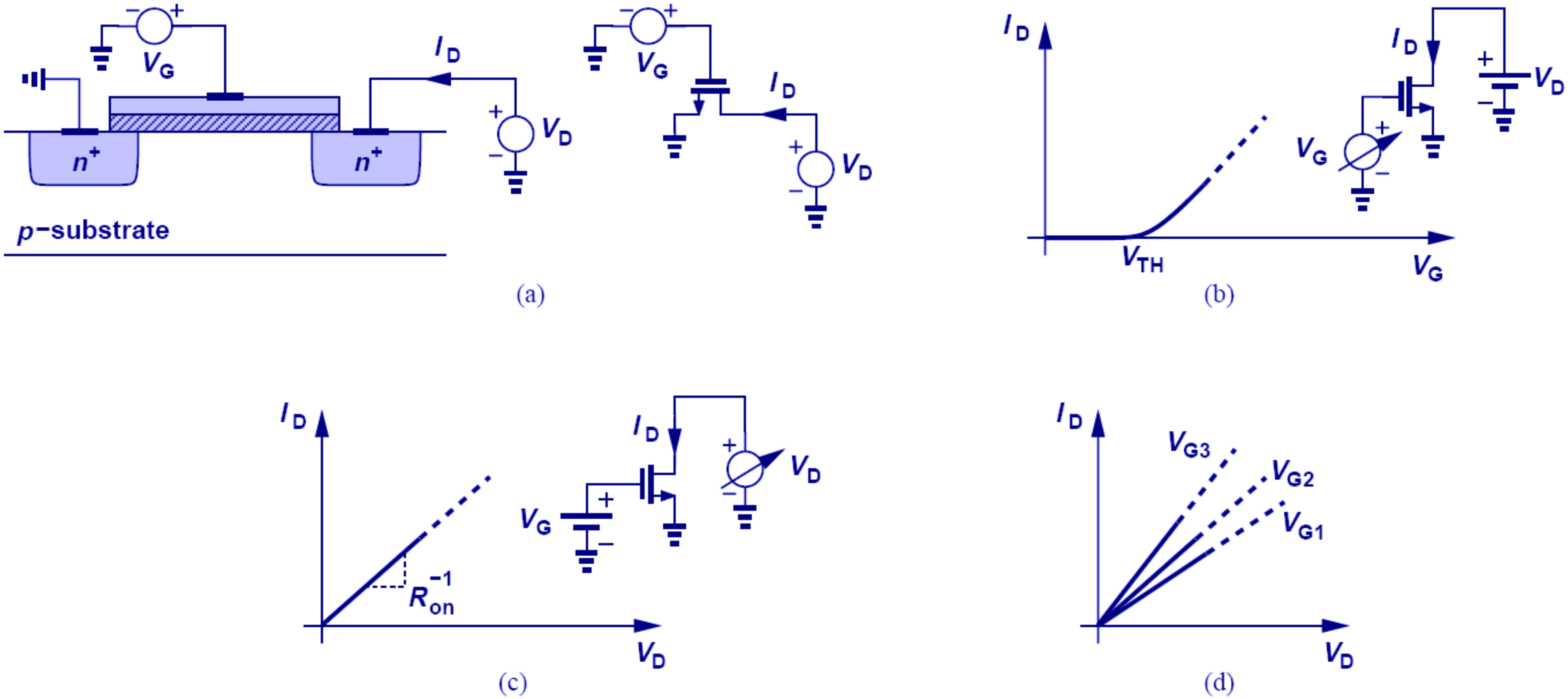
- The inversion channel of a MOSFET can be seen as a resistor.
- Since the charge density inside the channel depends on the gate voltage, this resistance is also voltage-dependent.

Voltage-Controlled Attenuator



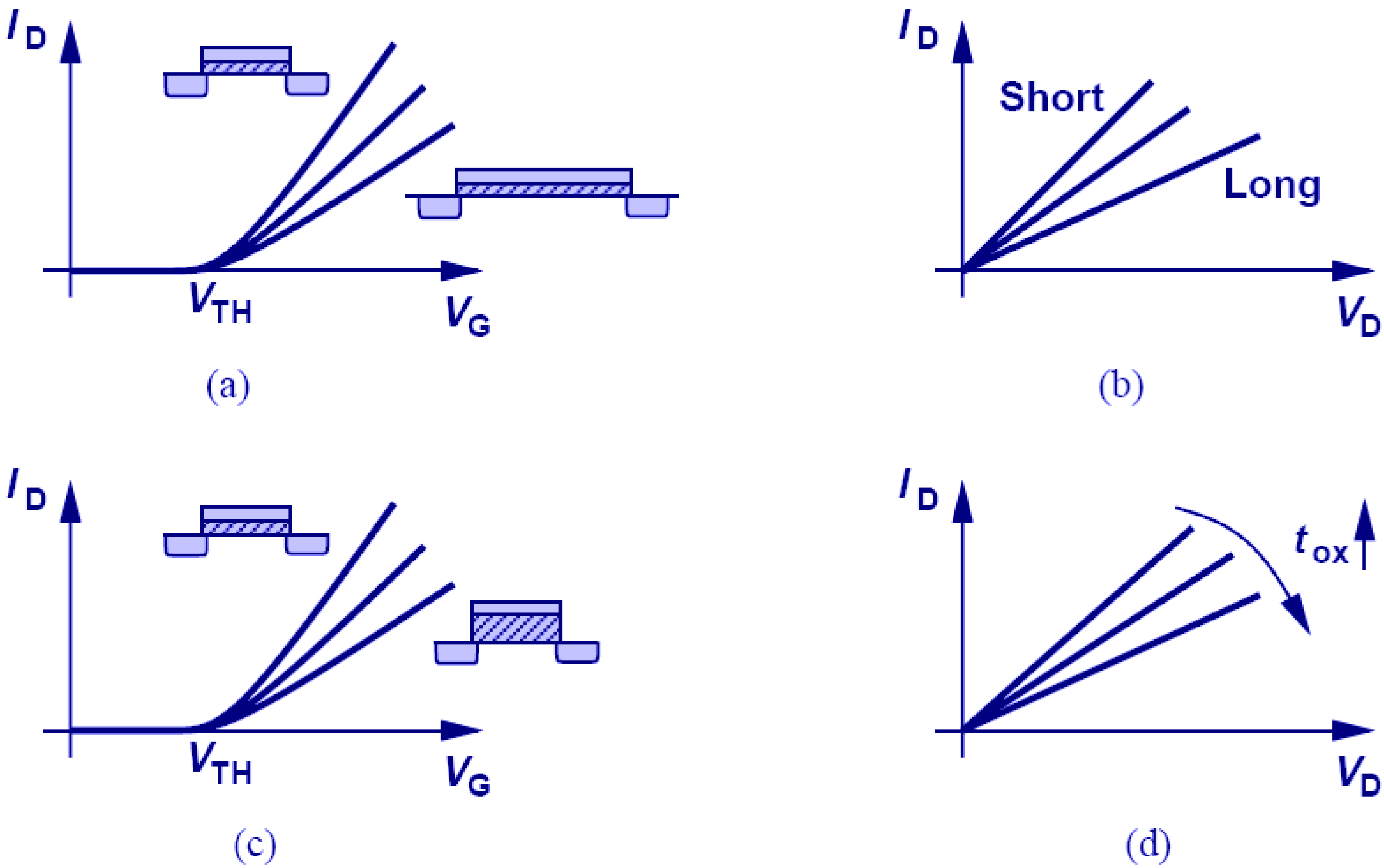
- As the gate voltage decreases, the output drops because the channel resistance increases.
- This type of gain control finds application in cell phones to avoid saturation near base stations.

MOSFET Characteristics



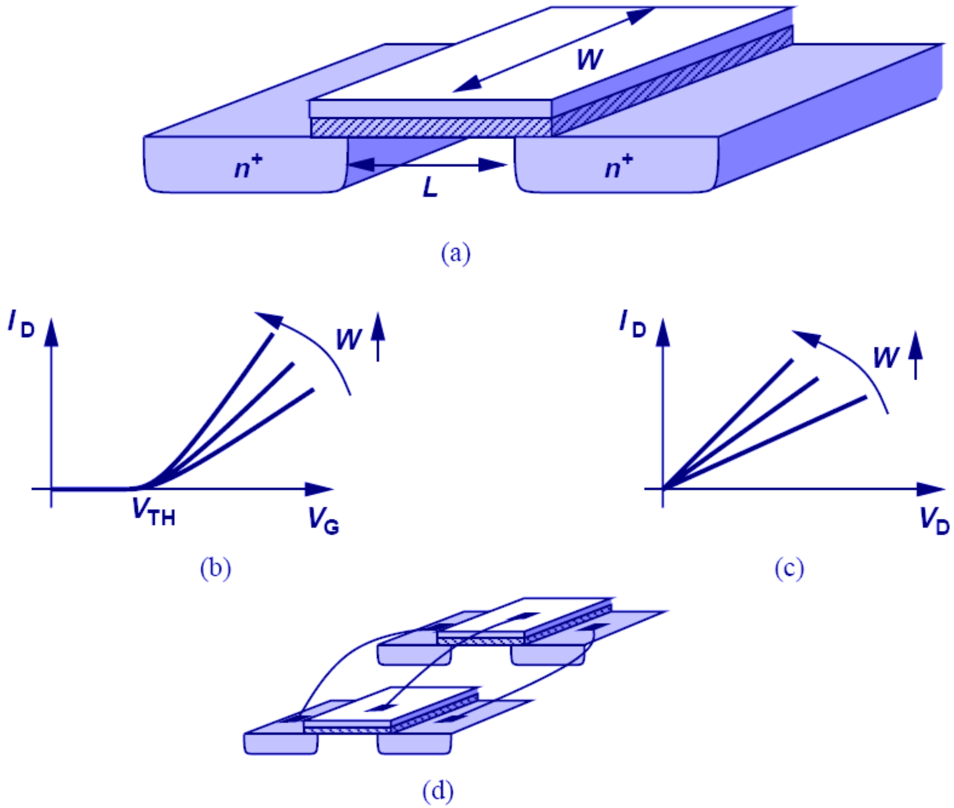
- **The MOS characteristics are measured by varying V_G while keeping V_D constant, and varying V_D while keeping V_G constant.**
- **(d) shows the voltage dependence of channel resistance.**

L and t_{ox} Dependence



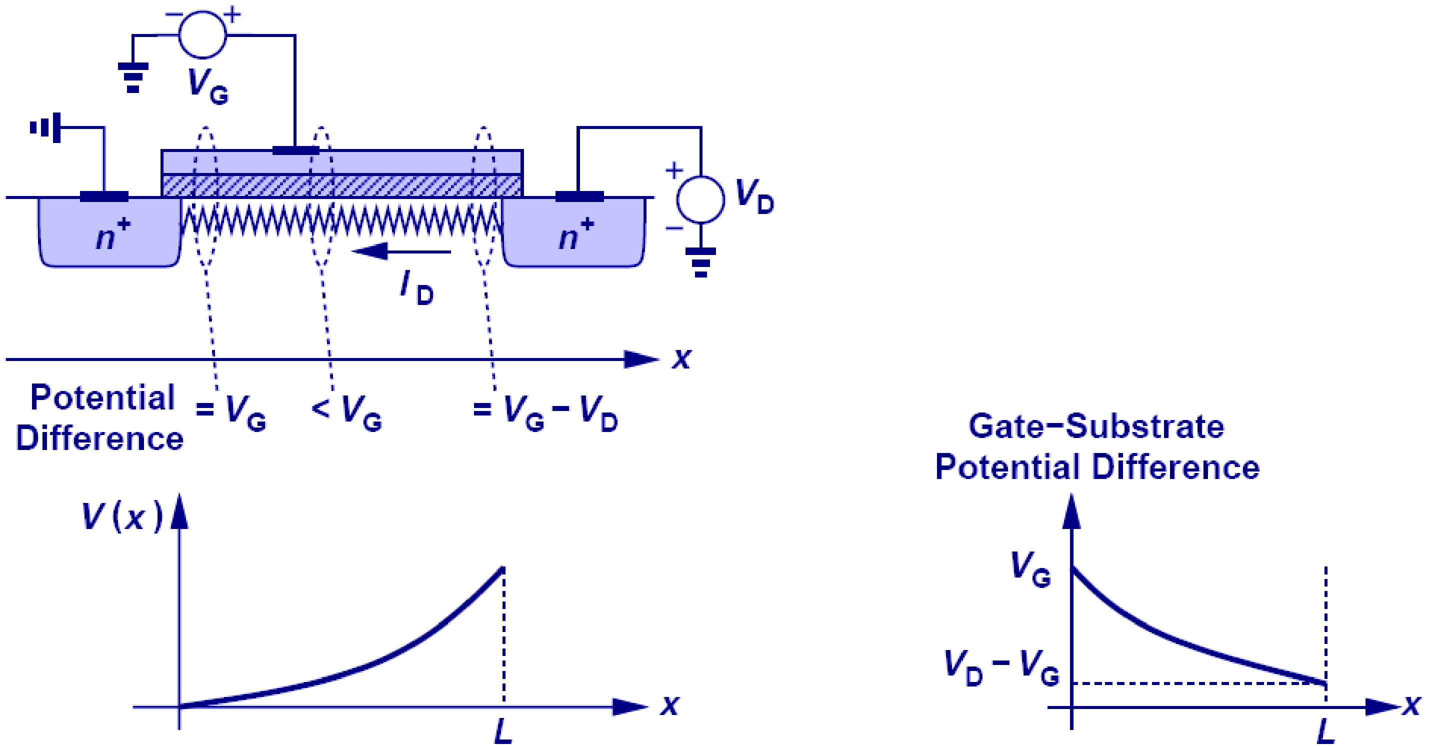
- **Small gate length and oxide thickness yield low channel resistance, which will increase the drain current.**

Effect of W



- As the gate width increases, the current increases due to a decrease in resistance. However, gate capacitance also increases thus, limiting the speed of the circuit.
- An increase in W can be seen as two devices in parallel.

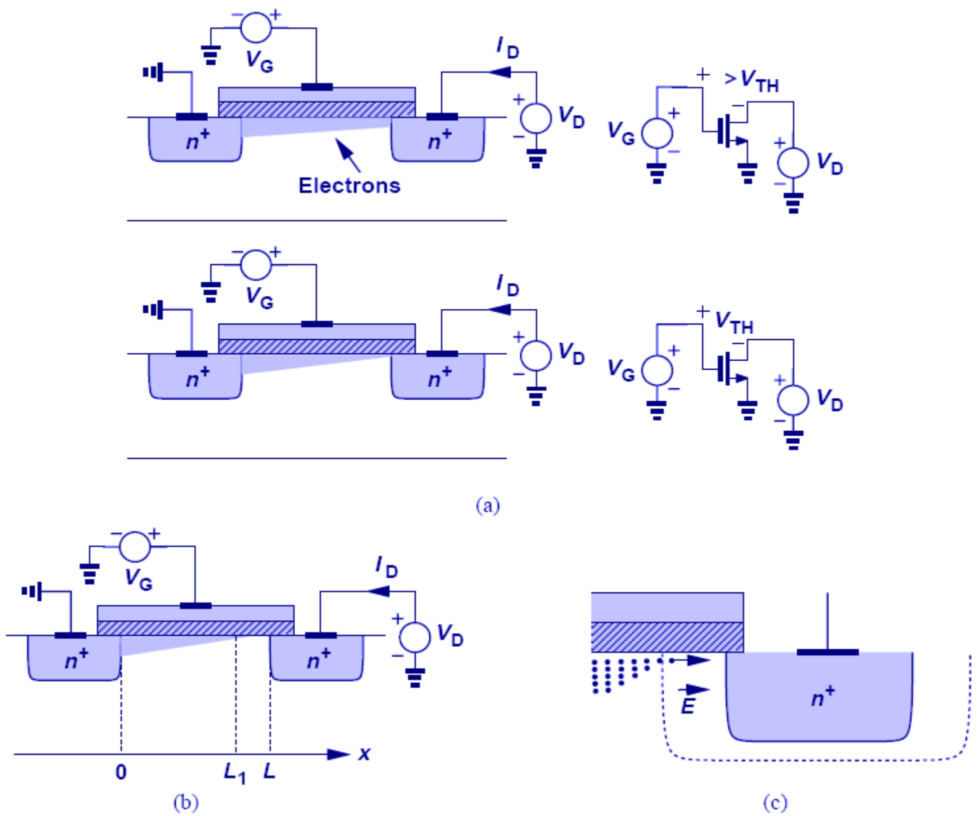
Channel Potential Variation



(a) (b)

- **Since there's a channel resistance between drain and source, and if drain is biased higher than the source, channel potential increases from source to drain, and the potential between gate and channel will decrease from source to drain.**

Channel Pinch-Off



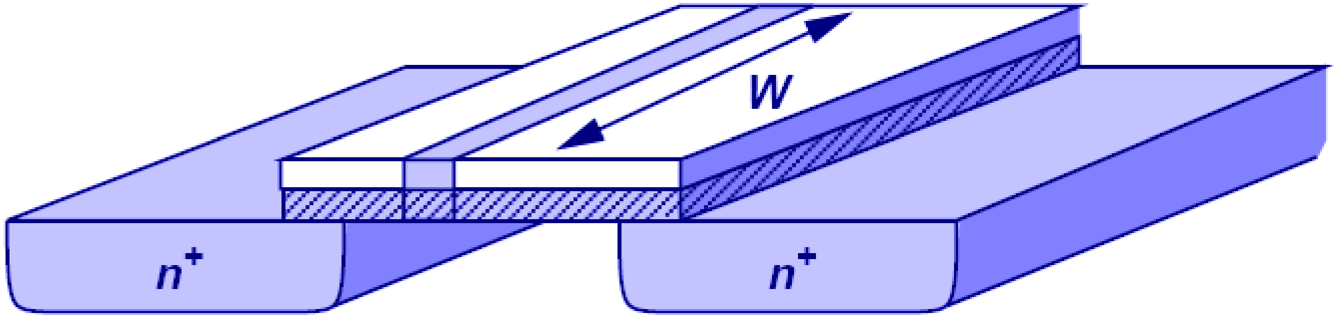
(a)

(b)

(c)

- As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain.
- When $V_D - V_G = V_{th}$, the channel at drain totally pinches off, and when $V_D - V_G > V_{th}$, the channel length starts to decrease.

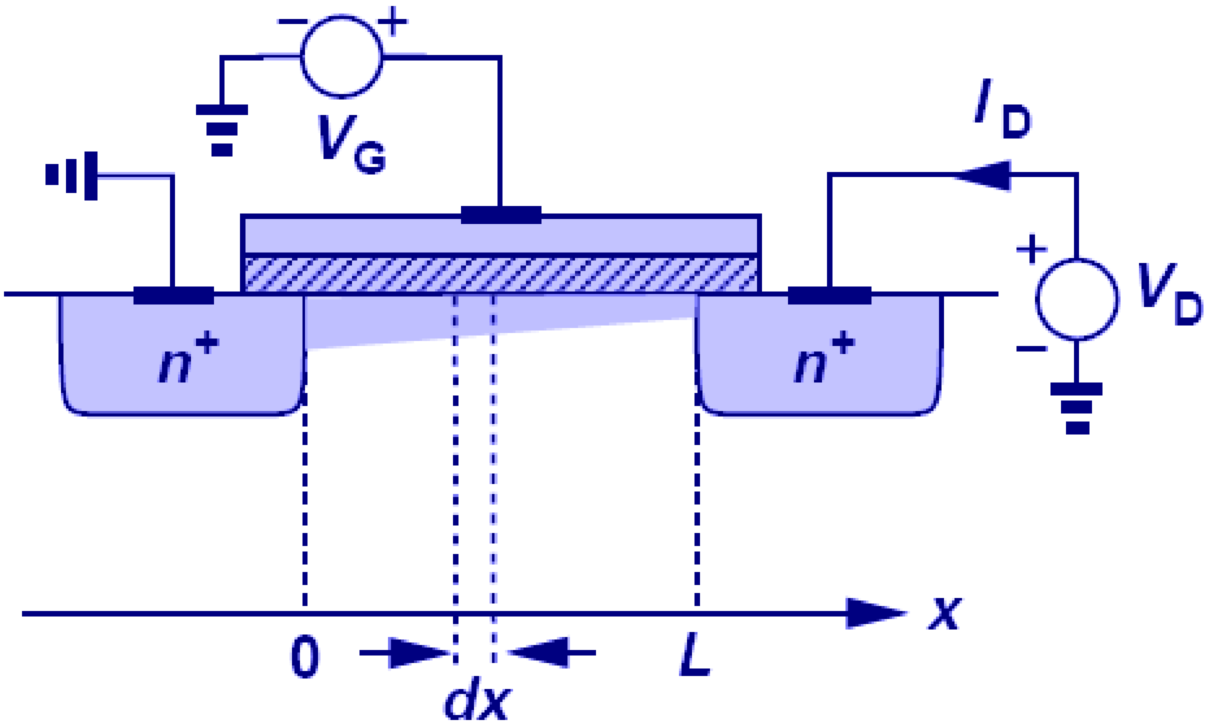
Channel Charge Density



$$Q = WC_{ox}(V_{GS} - V_{TH})$$

- **The channel charge density is equal to the gate capacitance times the gate voltage in excess of the threshold voltage.**

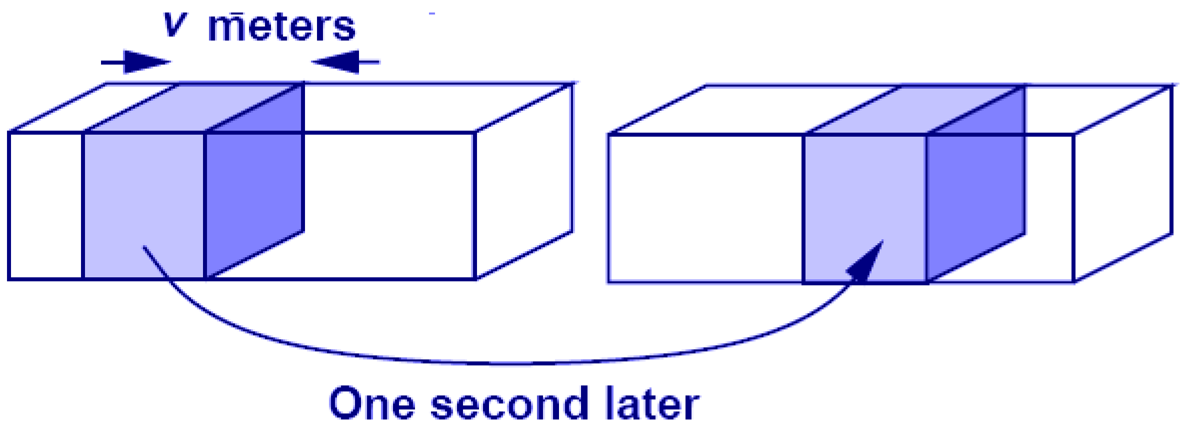
Charge Density at a Point



$$Q(x) = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]$$

- **Let x be a point along the channel from source to drain, and V(x) its potential; the expression above gives the charge density (per unit length).**

Charge Density and Current



$$I = Q \cdot v$$

- The current that flows from source to drain (electrons) is related to the charge density in the channel by the charge velocity.

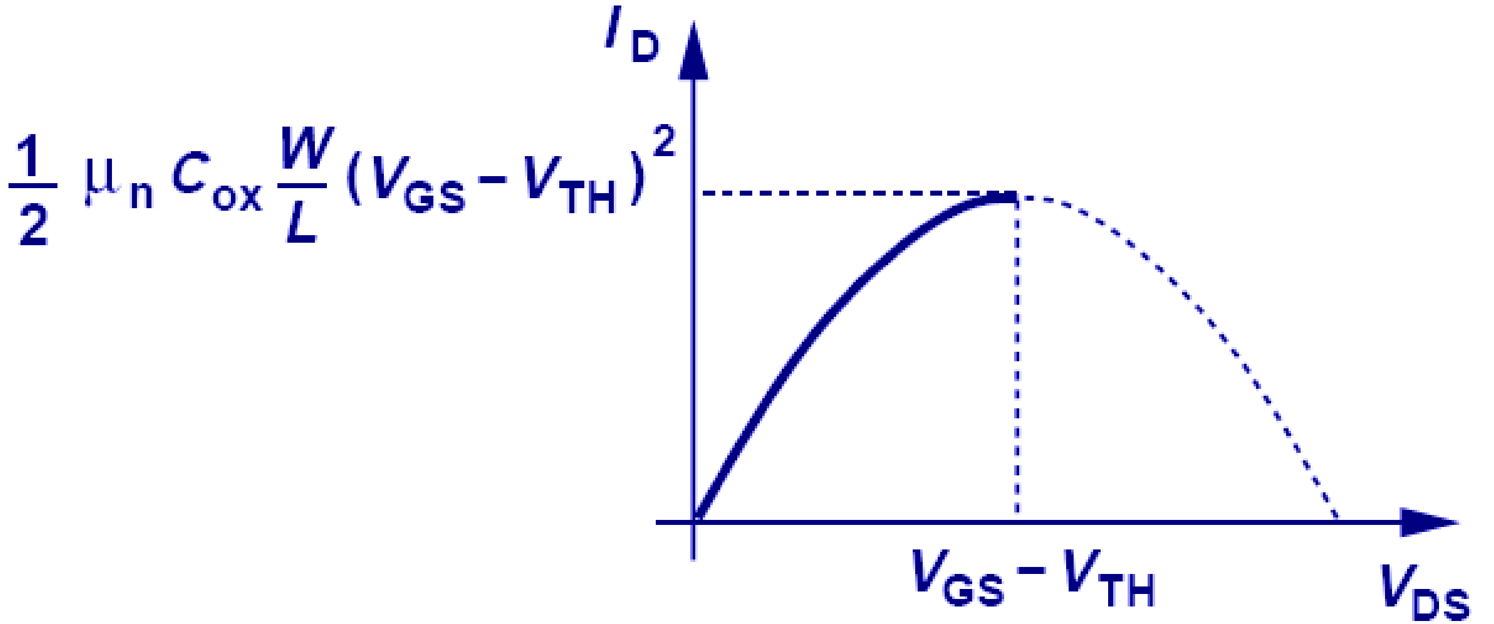
Drain Current

$$v = +\mu_n \frac{dV}{dx}$$

$$I_D = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]\mu_n \frac{dV(x)}{dx}$$

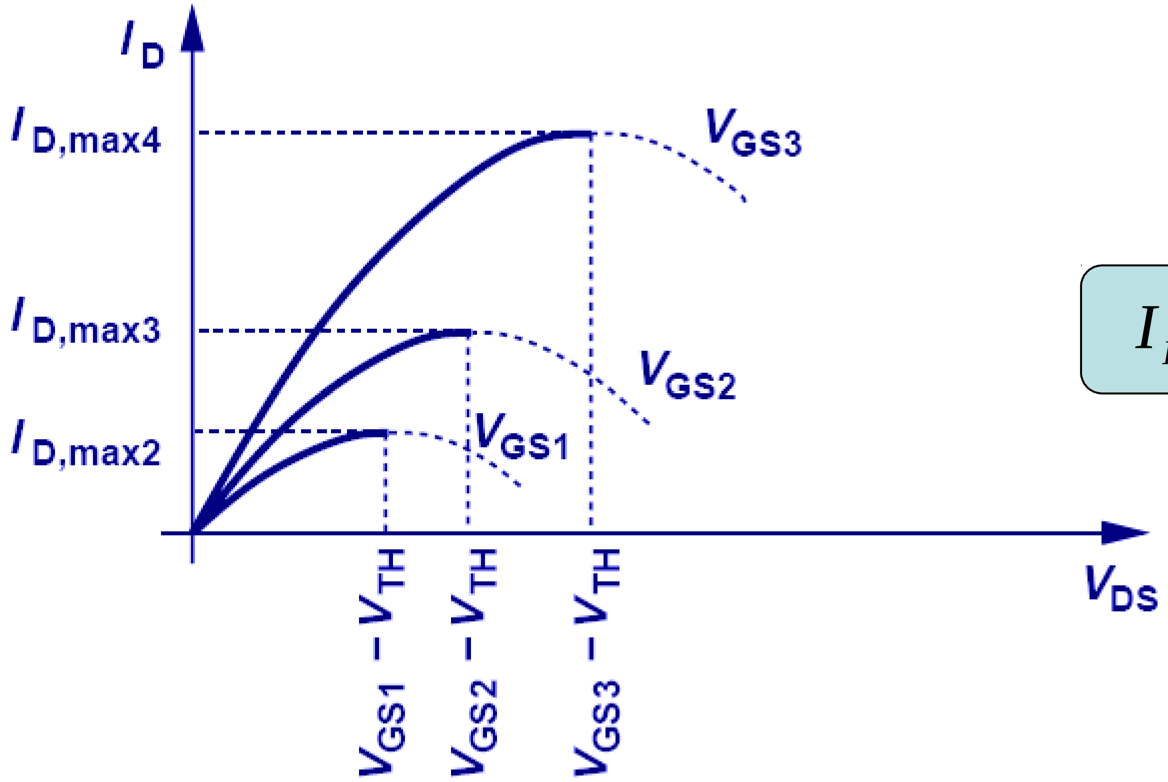
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]$$

Parabolic I_D-V_{DS} Relationship



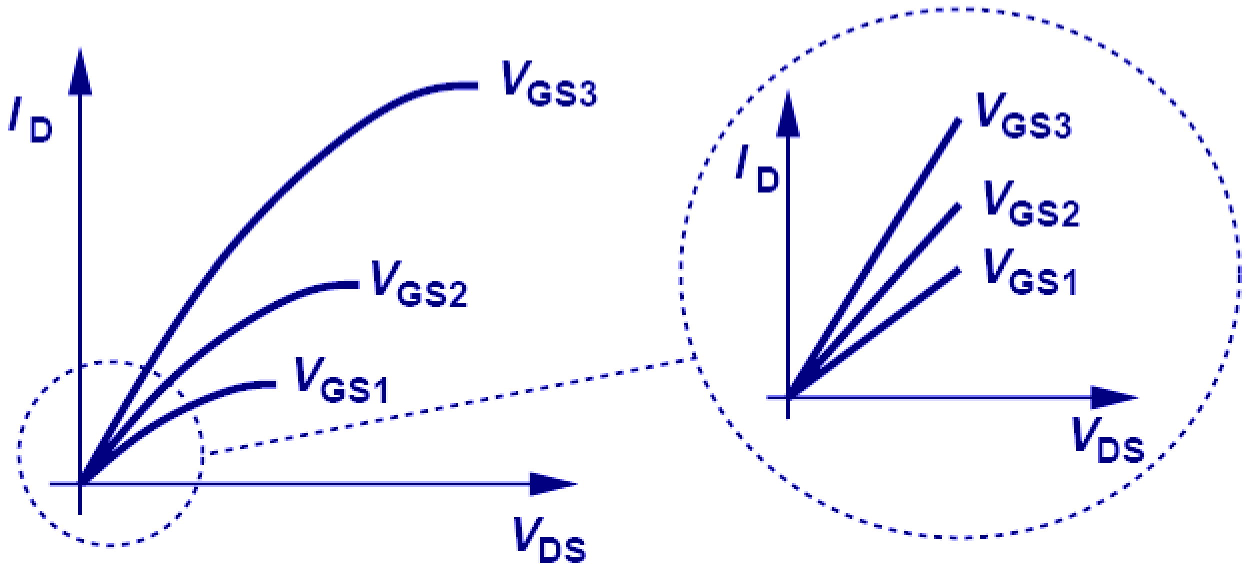
- By keeping V_G constant and varying V_{DS}, we obtain a parabolic relationship.
- The maximum current occurs when V_{DS} equals to V_{GS}- V_{TH}.

I_D-V_{DS} for Different Values of V_{GS}



$$I_{D,\max} \propto (V_{GS} - V_{TH})^2$$

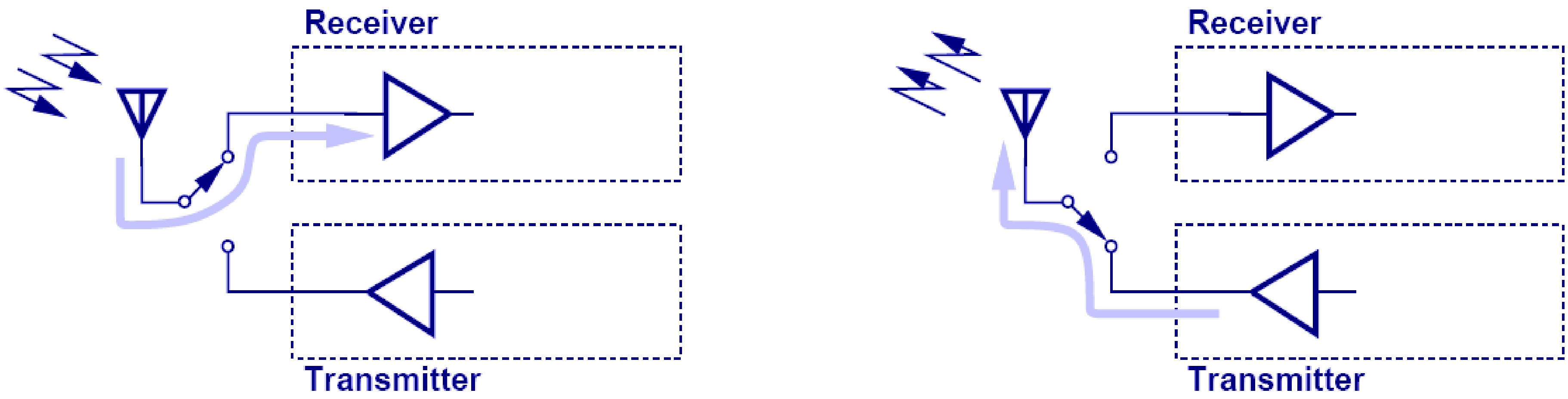
Linear Resistance



$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

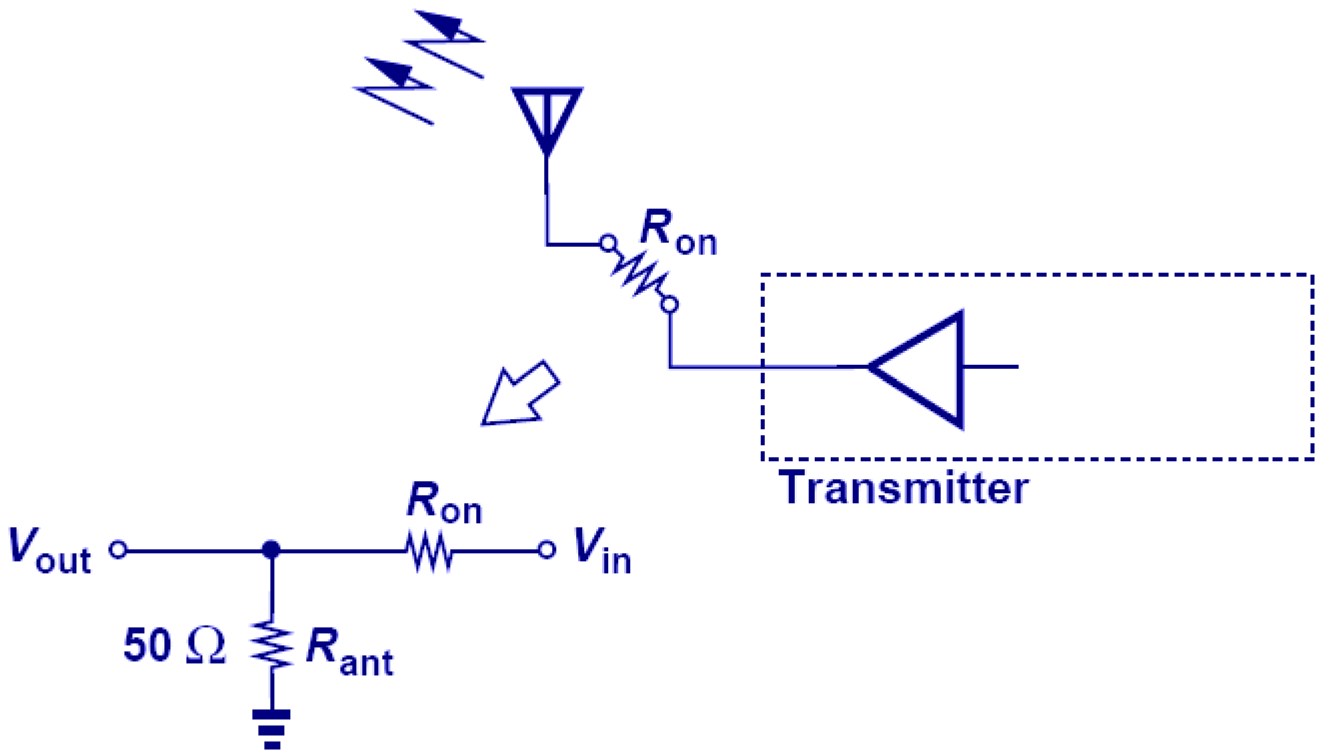
- **At small V_{DS}, the transistor can be viewed as a resistor, with the resistance depending on the gate voltage.**
- **It finds application as an electronic switch.**

Application of Electronic Switches



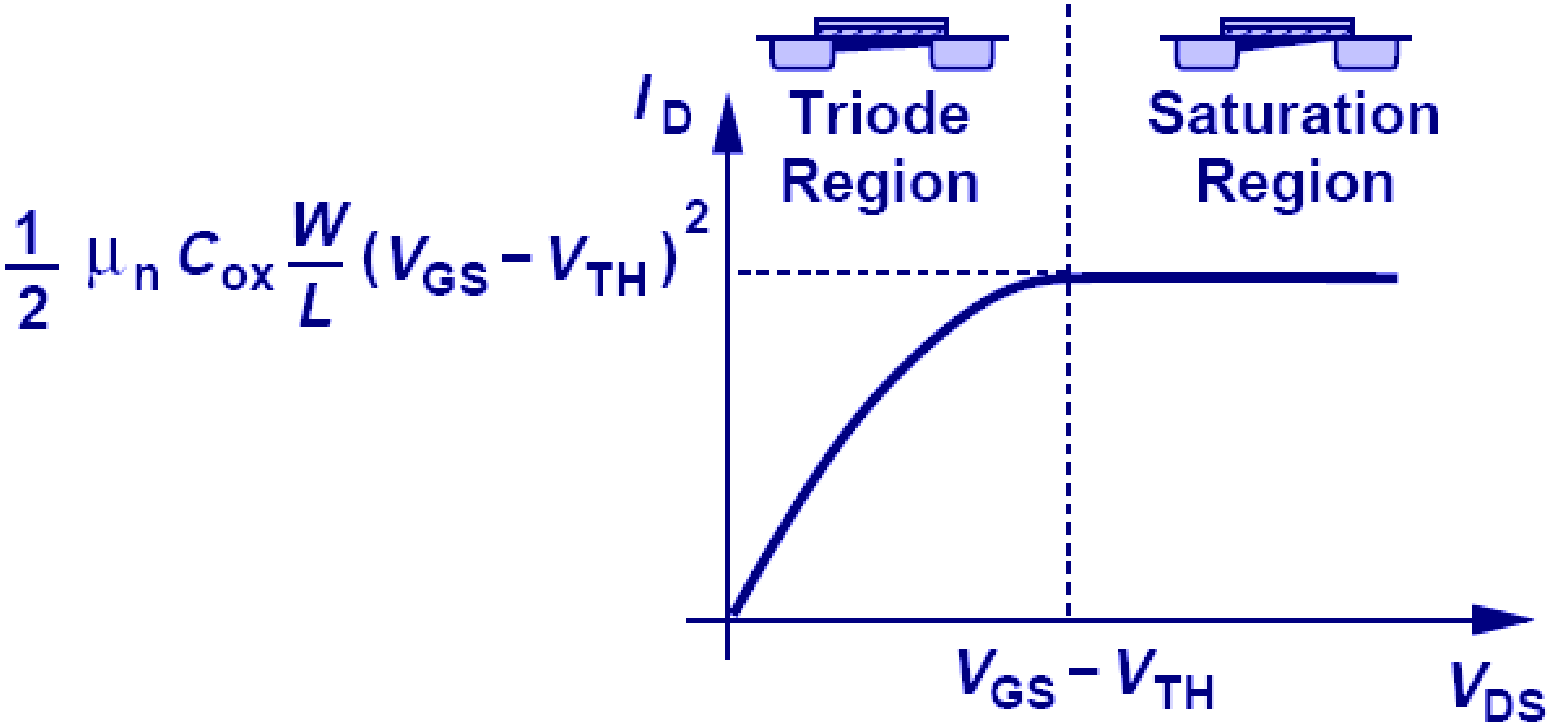
➢ **In a cordless telephone system in which a single antenna is used for both transmission and reception, a switch is used to connect either the receiver or transmitter to the antenna.**

Effects of On-Resistance

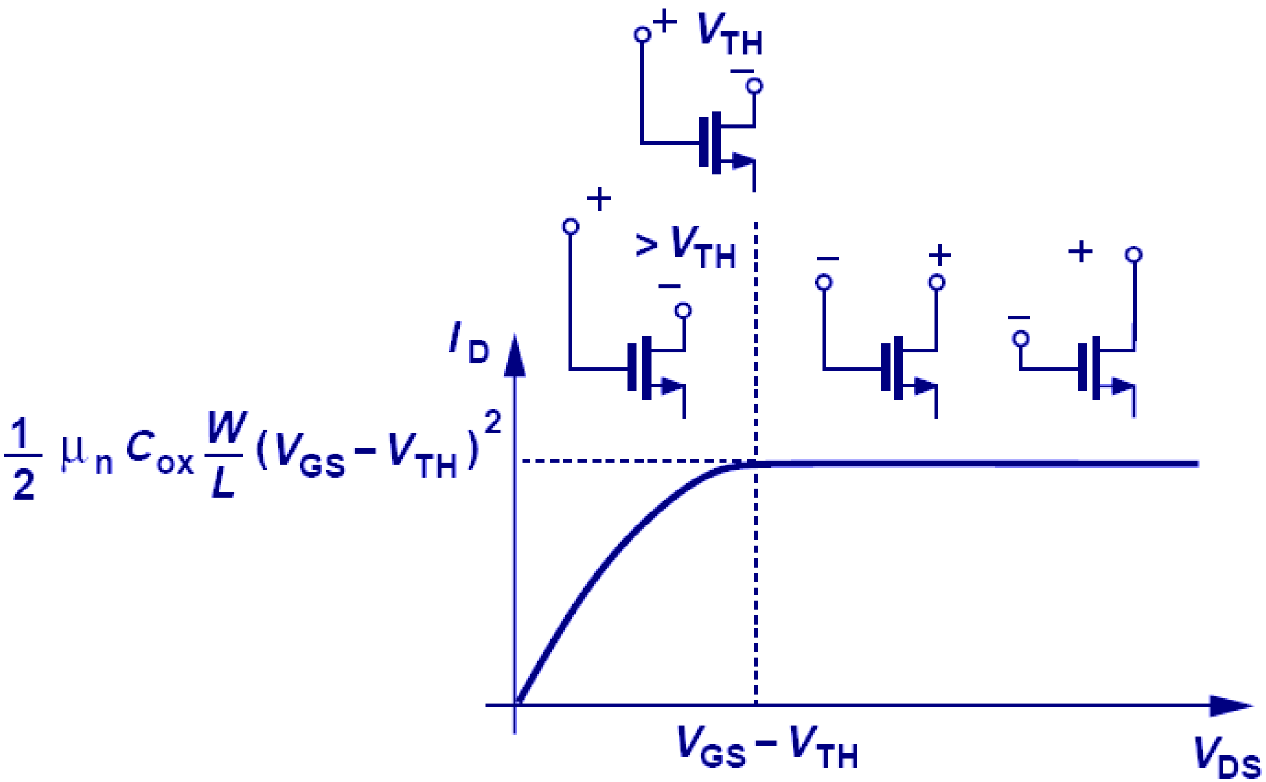


- **To minimize signal attenuation, R_{on} of the switch has to be as small as possible. This means larger W/L aspect ratio and greater V_{GS}.**

Different Regions of Operation

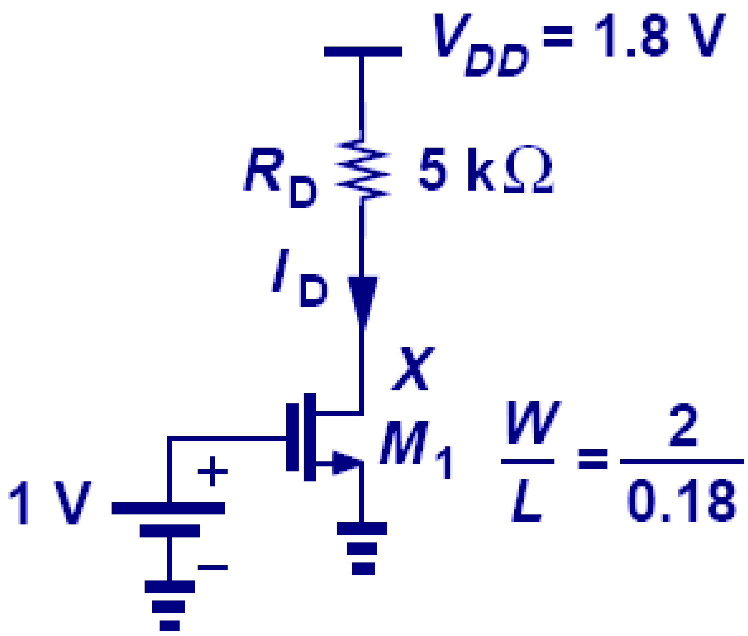


How to Determine 'Region of Operation'



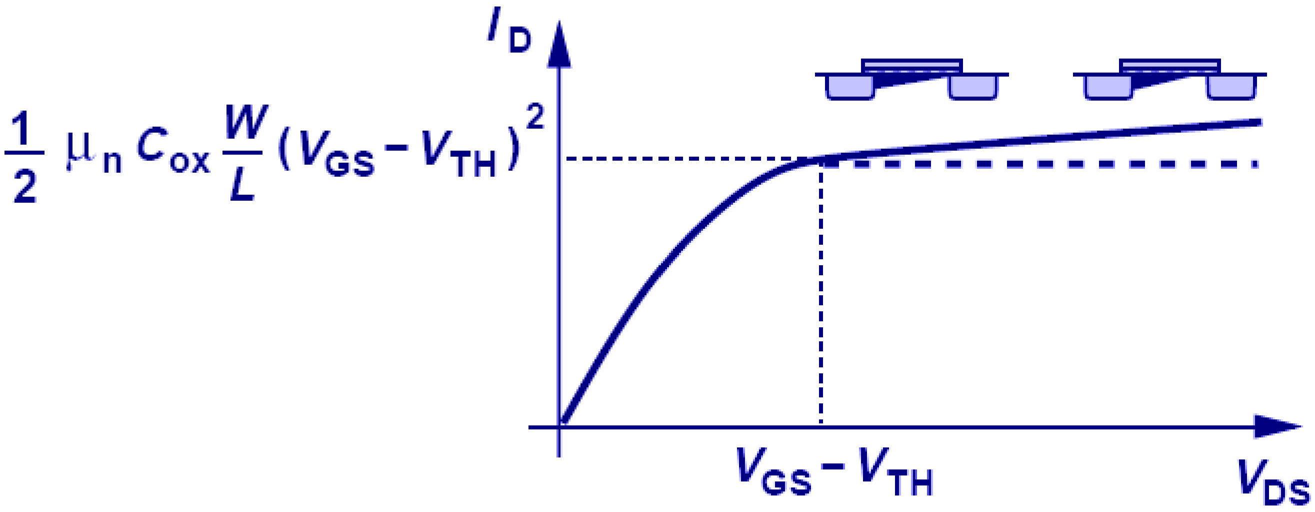
- When the potential difference between gate and drain is greater than V_{TH}, the MOSFET is in triode region.
- When the potential difference between gate and drain becomes equal to or less than V_{TH}, the MOSFET enters saturation region.

Triode or Saturation?



- When the region of operation is not known, a region is assumed (with an intelligent guess). Then, the final answer is checked against the assumption.

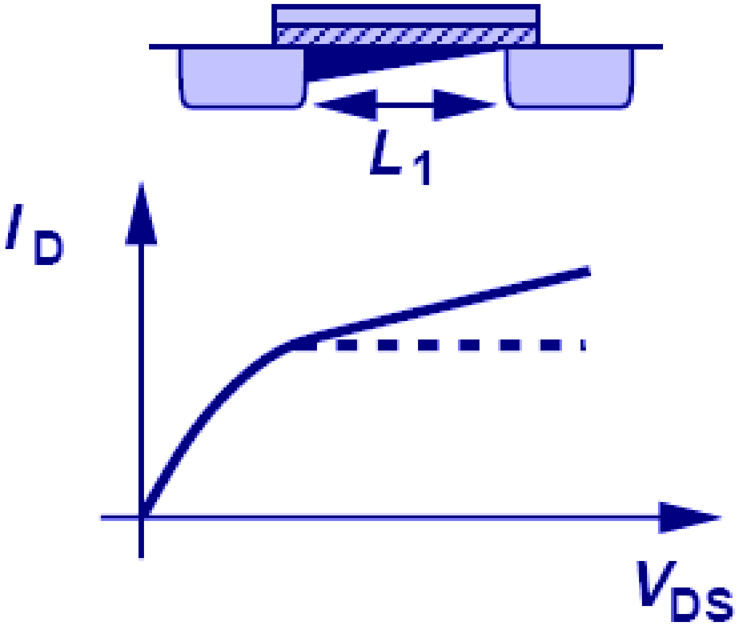
Channel-Length Modulation

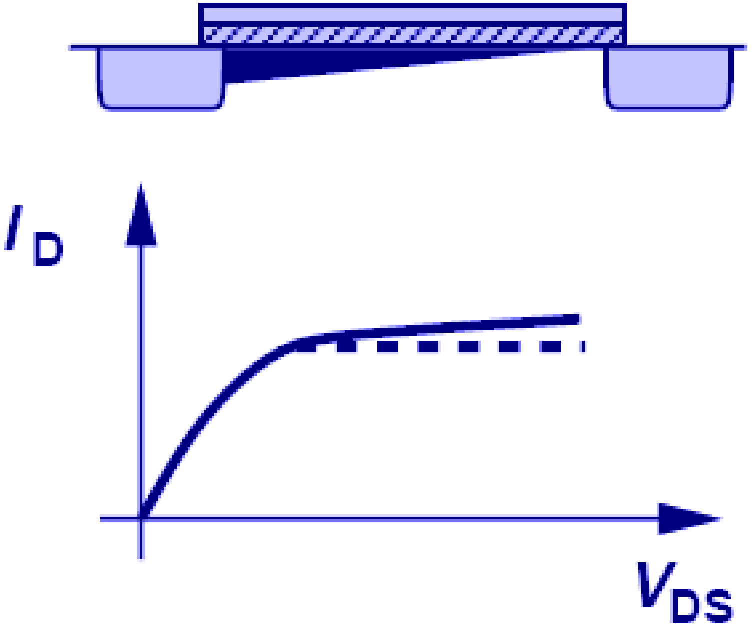


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1+\lambda V_{DS})$$

- **The original observation that the current is constant in the saturation region is not quite correct. The end point of the channel actually moves toward the source as V_D increases, increasing I_D. Therefore, the current in the saturation region is a weak function of the drain voltage.**

λ and L





- **Unlike the Early voltage in BJT, the channel- length modulation factor can be controlled by the circuit designer.**
- **For long L, the channel-length modulation effect is less than that of short L.**

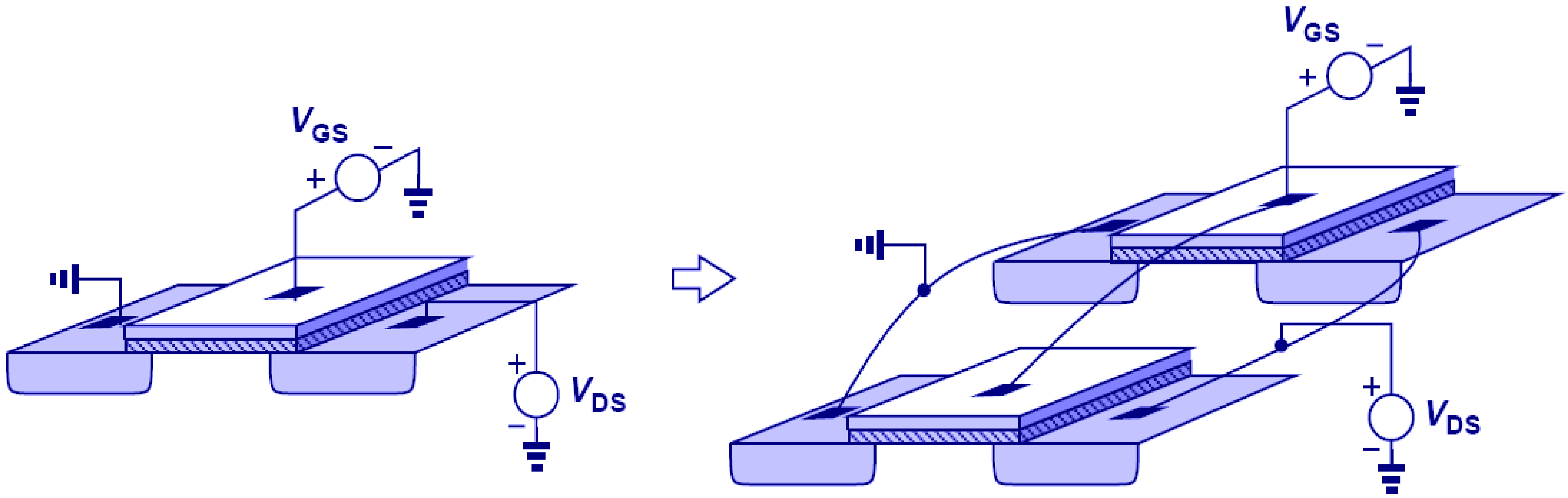
Transconductance

$\frac{W}{L}$ Constant, $V_{GS}-V_{TH}$ Variable	$\frac{W}{L}$ Variable, $V_{GS}-V_{TH}$ Constant	$\frac{W}{L}$ Variable, $V_{GS}-V_{TH}$ Constant
$g_m \propto \sqrt{I_D}$ $g_m \propto V_{GS}-V_{TH}$	$g_m \propto I_D$ $g_m \propto \frac{W}{L}$	$g_m \propto \sqrt{\frac{W}{L}}$ $g_m \propto \frac{1}{V_{GS}-V_{TH}}$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \qquad g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \qquad g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

- **Transconductance is a measure of how strong the drain current changes when the gate voltage changes.**
- **It has three different expressions.**

Doubling of g_m Due to Doubling W/L



- If W/L is doubled, effectively two equivalent transistors are added in parallel, thus doubling the current (if V_{GS}-V_{TH} is constant) and hence g_m.

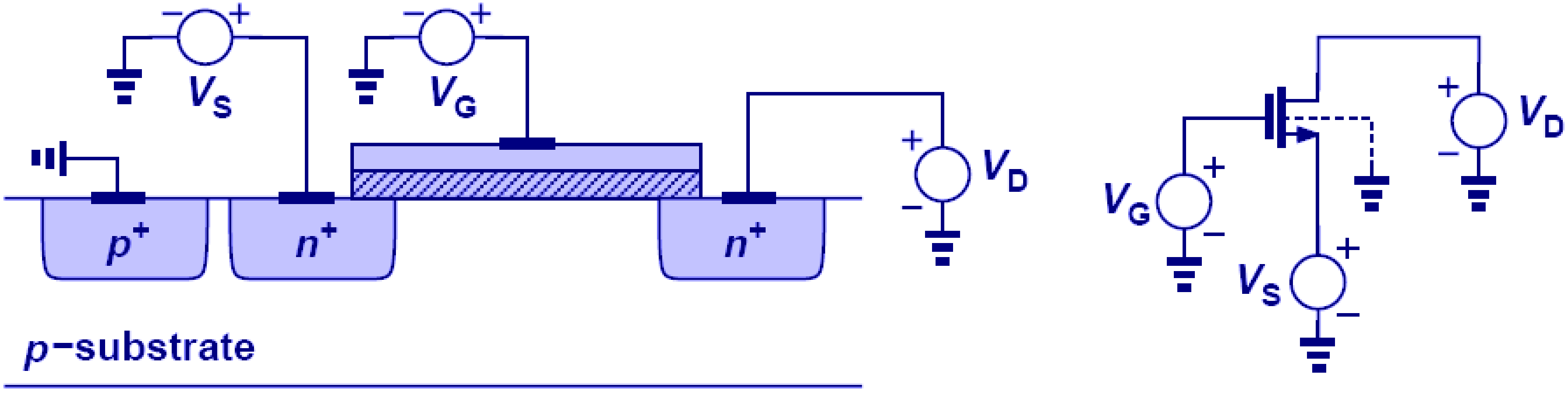
Velocity Saturation

$$I_D = v_{sat} \cdot Q = v_{sat} \cdot WC_{ox}\left(V_{GS} - V_{TH}\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = v_{sat} WC_{ox}$$

- **Since the channel is very short, it does not take a very large drain voltage to velocity saturate the charge particles.**
- **In velocity saturation, the drain current becomes a linear function of gate voltage, and gm becomes a function of W.**

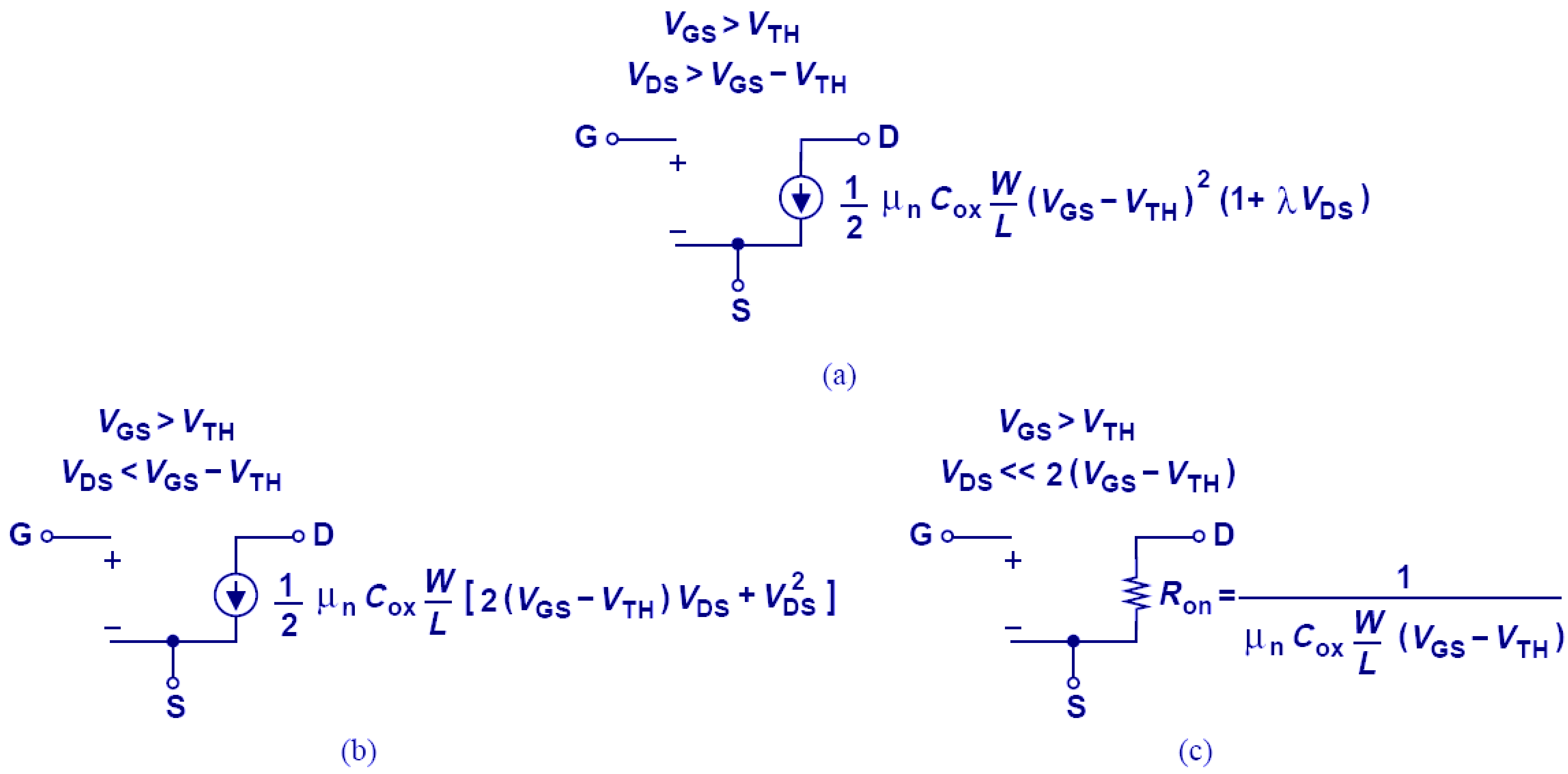
Body Effect



$$V_{TH} = V_{TH0} + \rho\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

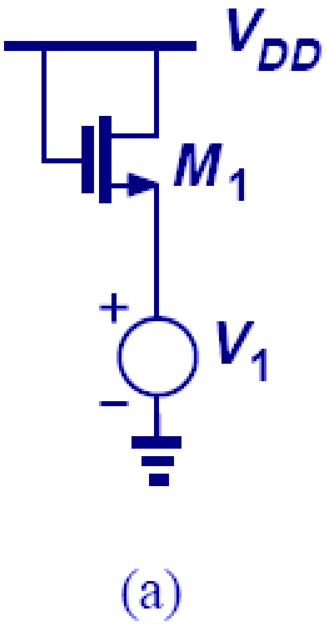
- As the source potential departs from the bulk potential, the threshold voltage changes.

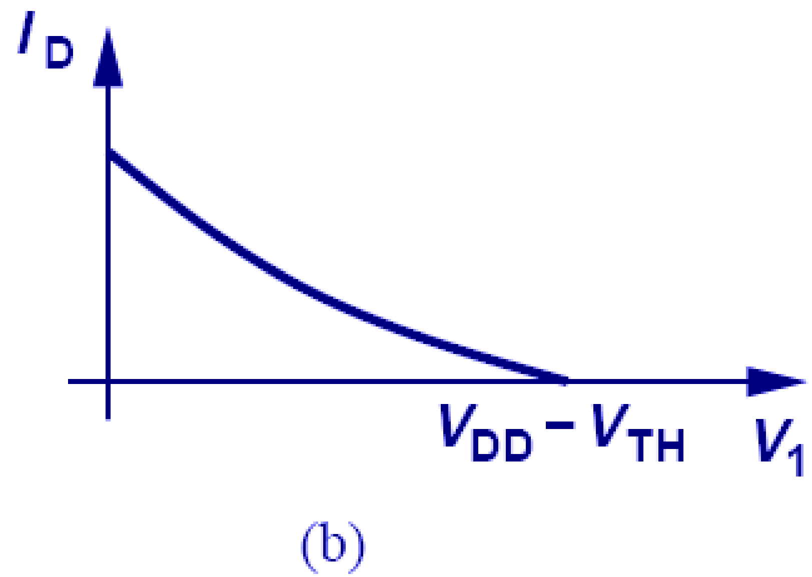
Large-Signal Models



- **Based on the value of V_{DS}, MOSFET can be represented with different large-signal models.**

Example: Behavior of I_D with V_1 as a Function

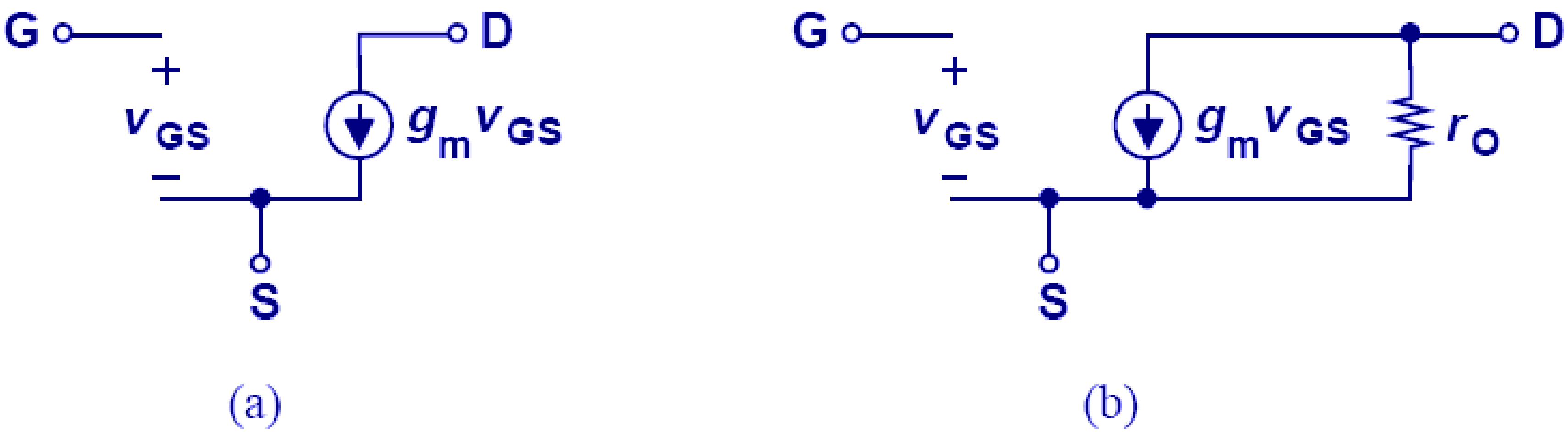




$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_1 - V_{TH})^2$$

- **Since V_1 is connected at the source, as it increases, the current drops.**

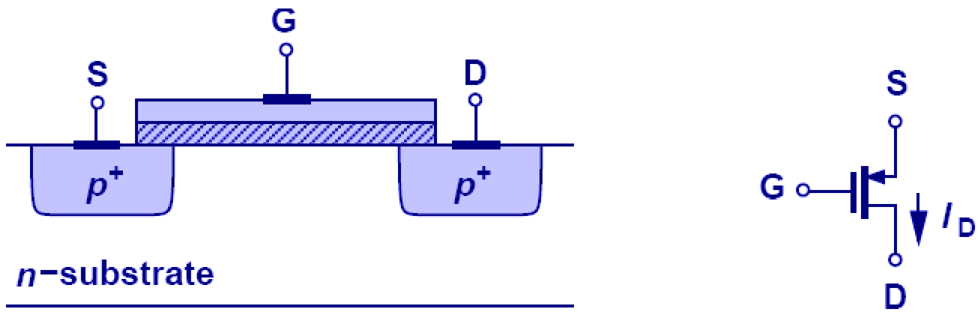
Small-Signal Model



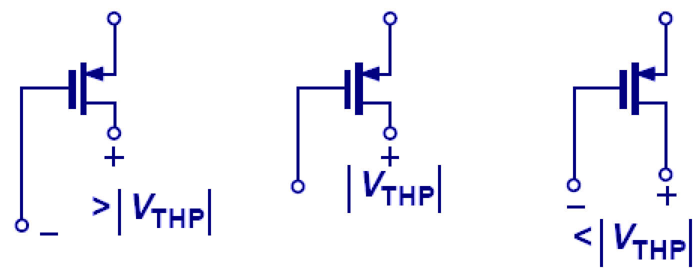
$$r_o \approx \frac{1}{\lambda I_D}$$

- **When the bias point is not perturbed significantly, small-signal model can be used to facilitate calculations.**
- **To represent channel-length modulation, an output resistance is inserted into the model.**

PMOS Transistor



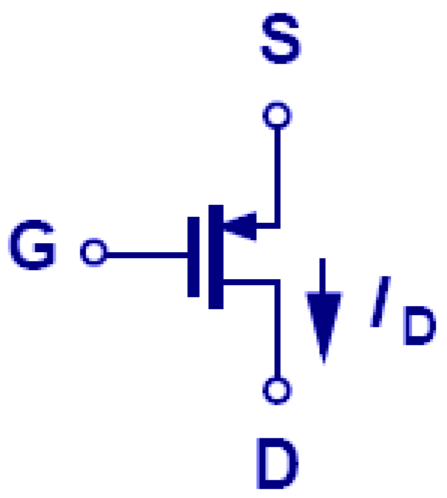
(a) (b)



(c)

- Just like the PNP transistor in bipolar technology, it is possible to create a MOS device where holes are the dominant carriers. It is called the PMOS transistor.
- It behaves like an NMOS device with all the polarities reversed.

PMOS Equations



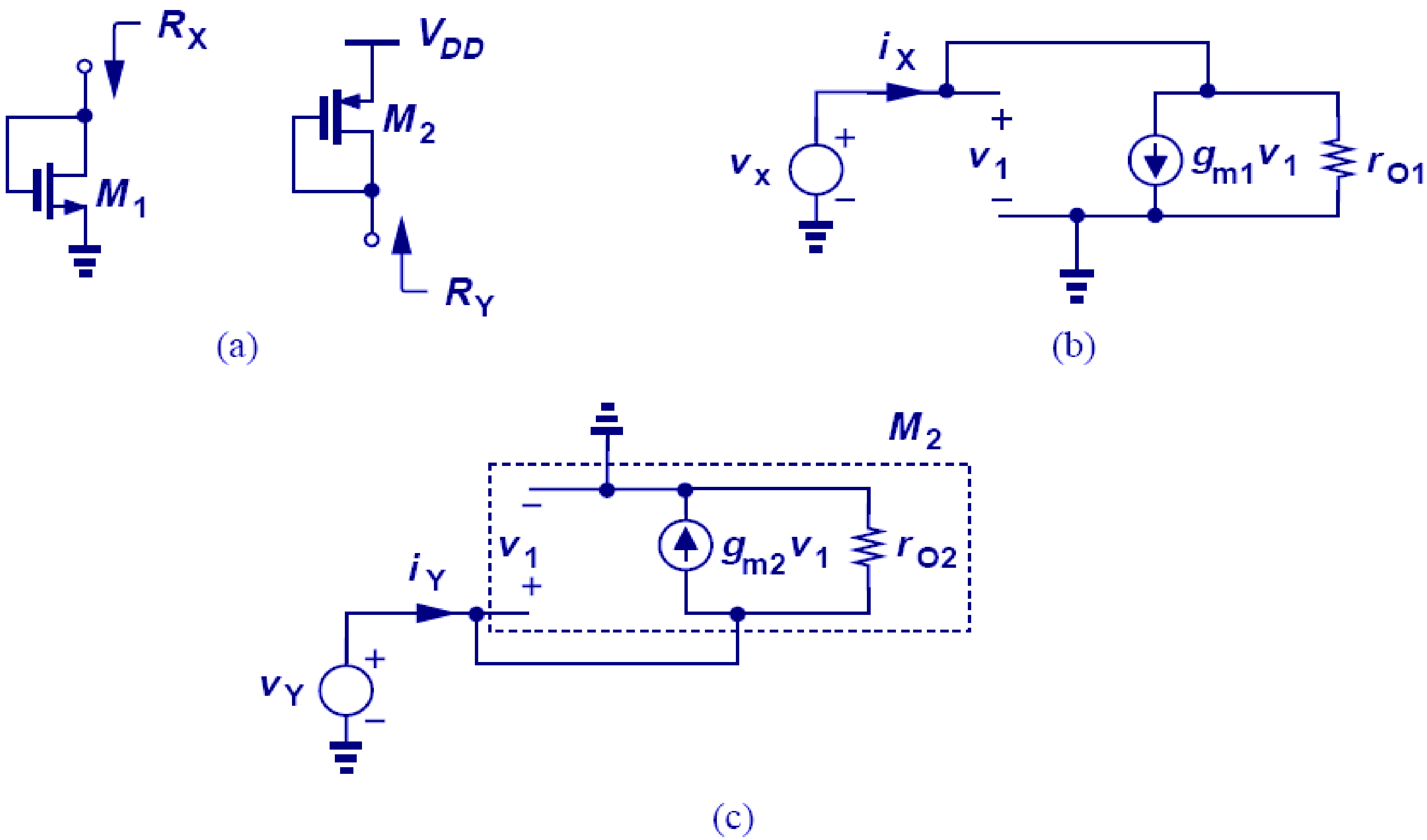
$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left(1 - \lambda V_{DS}\right)$$

$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2\left(V_{GS} - V_{TH}\right)V_{DS} - V_{DS}^2\right]$$

$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(|V_{GS}| - |V_{TH}|\right)^2\left(1 + \lambda|V_{DS}|\right)$$

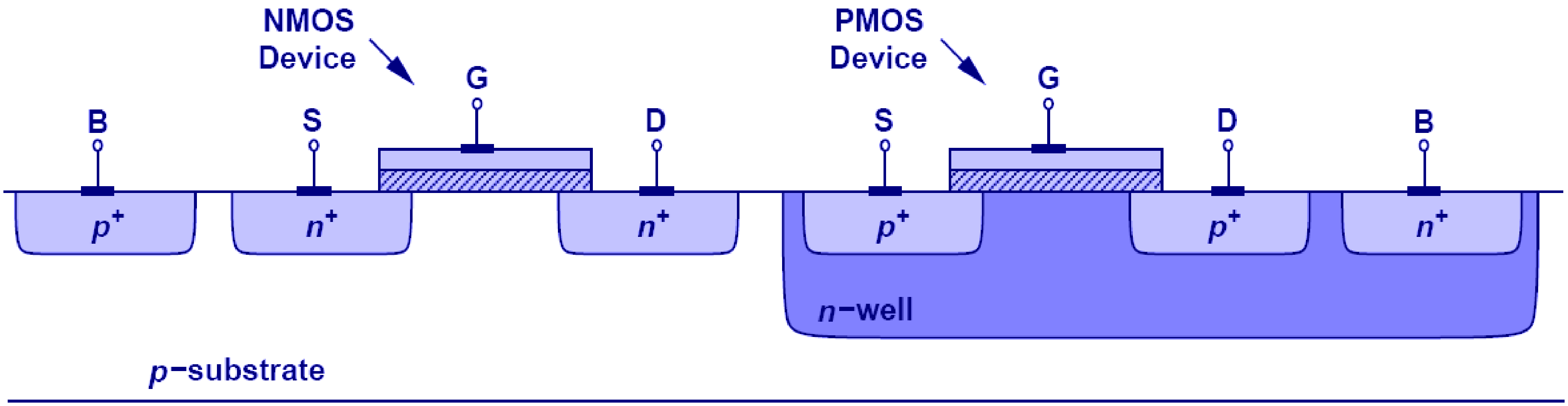
$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2\left(|V_{GS}| - |V_{TH}|\right)|V_{DS}| - V_{DS}^2\right]$$

Small-Signal Model of PMOS Device



- The small-signal model of PMOS device is identical to that of NMOS transistor; therefore, R_X equals R_Y and hence $(1/g_m)||r_o$.

CMOS Technology



- It possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.
- It is known as CMOS, or "Complementary MOS".

Comparison of Bipolar and MOS Transistors

Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel−Length Modulation
Diffusion Current	Drift Current
−	Voltage−Dependent Resistor

- **Bipolar devices have a higher g_m than MOSFETs for a given bias current due to its exponential IV characteristics.**

Chapter 7 CMOS Amplifiers

- 7.1 General Considerations
- 7.2 Common-Source Stage
- 7.3 Common-Gate Stage
- 7.4 Source Follower
- 7.5 Summary and Additional Examples

Chapter Outline

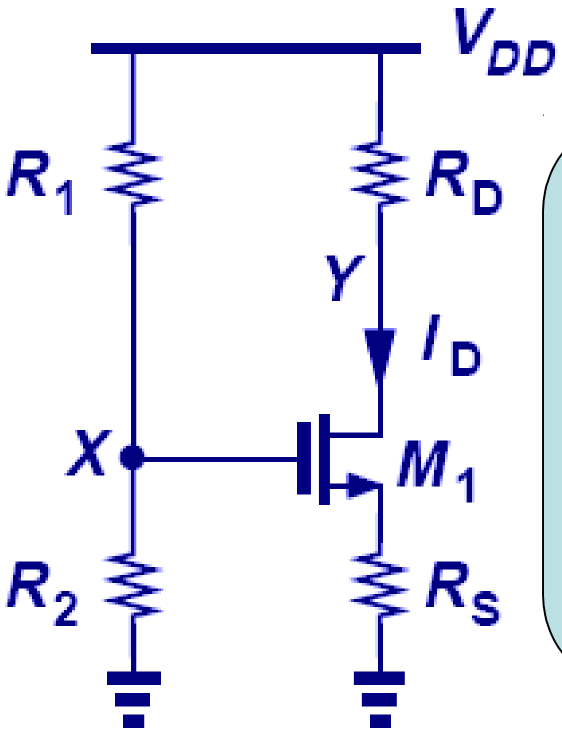
General Concepts

- Biasing of MOS Stages
- Realization of Current Sources

MOS Amplifiers

- Common−Source Stage
- Common−Gate Stage
- Source Follower

MOS Biasing

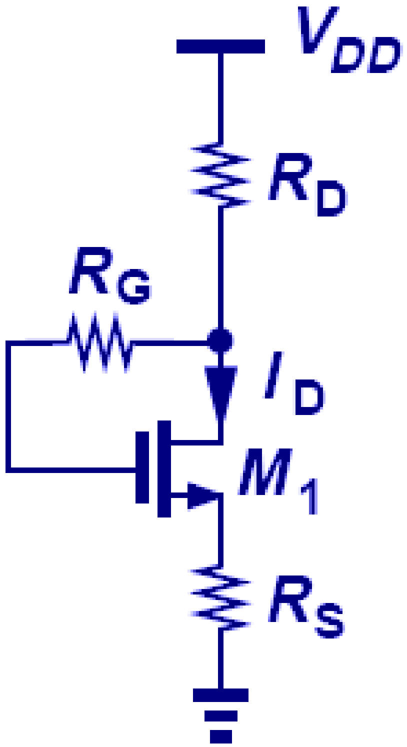


$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1\left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH}\right)}$$

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}$$

- **Voltage at X is determined by V_{DD}, R_1, and R_2.**
- **V_{GS} can be found using the equation above, and I_D can be found by using the NMOS current equation.**

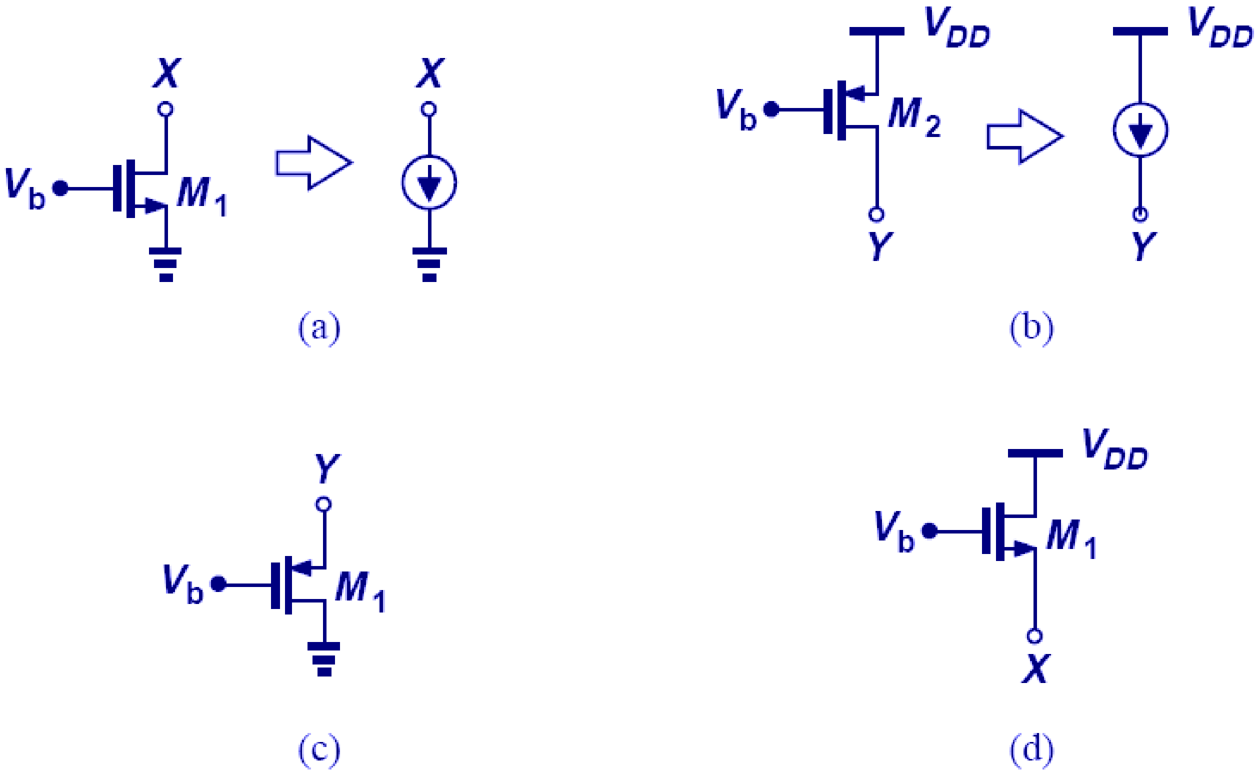
Self-Biased MOS Stage



$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

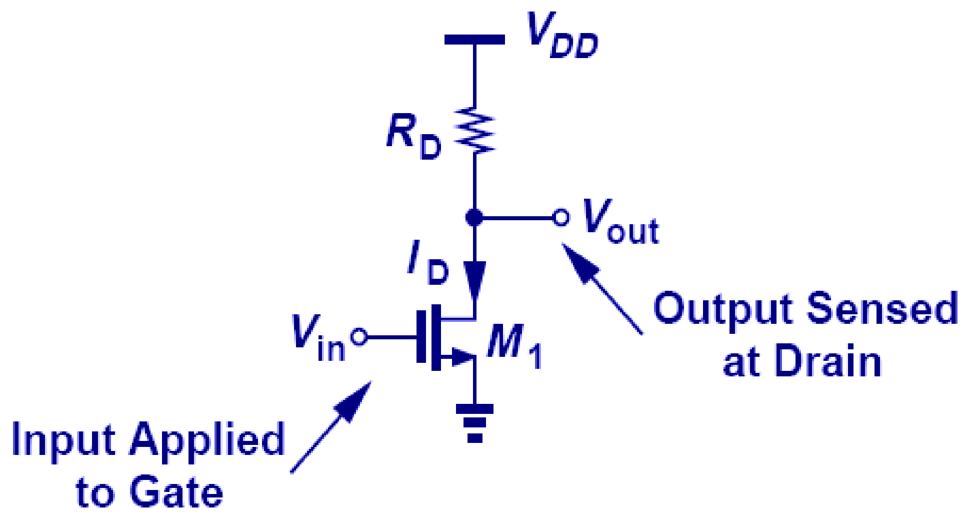
- The circuit above is analyzed by noting M1 is in saturation and no potential drop appears across R_G.

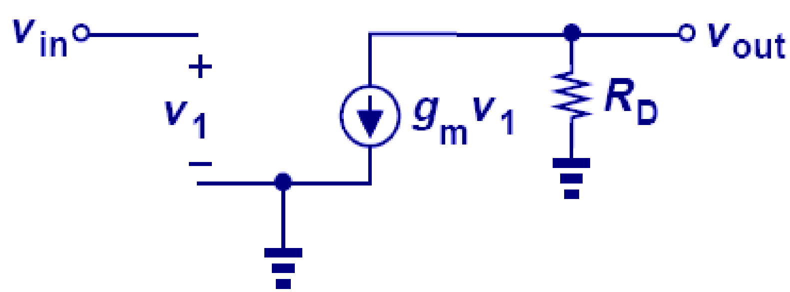
Current Sources



- **When in saturation region, a MOSFET behaves as a current source.**
- **NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from V_{DD} to a point (sources current).**

Common-Source Stage



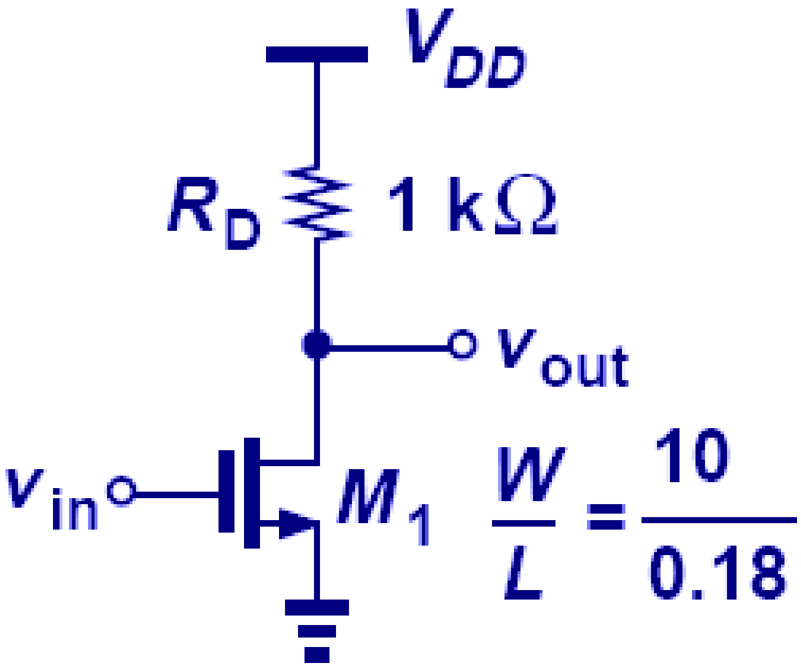


$$\lambda = 0$$

$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} R_D$$

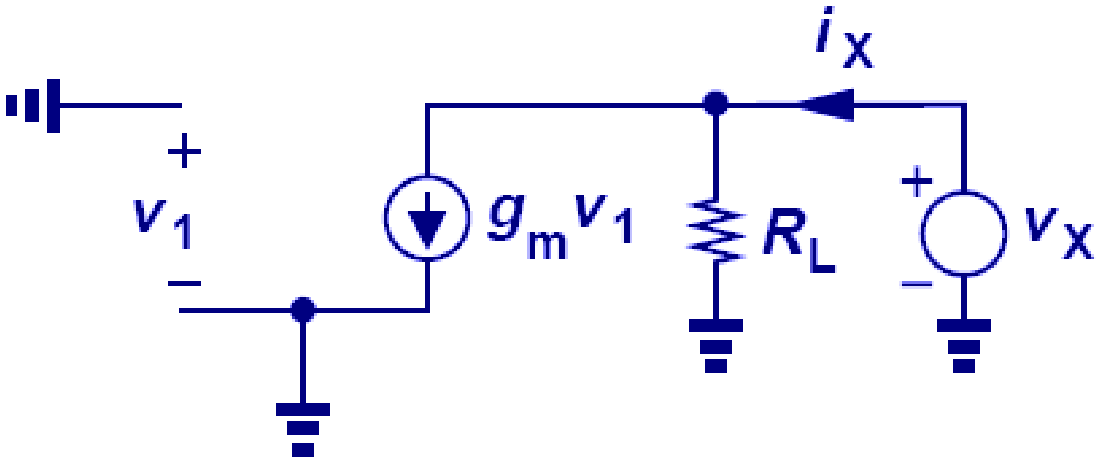
Operation in Saturation



$$R_D I_D < V_{DD} - (V_{GS} - V_{TH})$$

- In order to maintain operation in saturation, V_{out} cannot fall below V_{in} by more than one threshold voltage.
- The condition above ensures operation in saturation.

CS Stage with λ=0

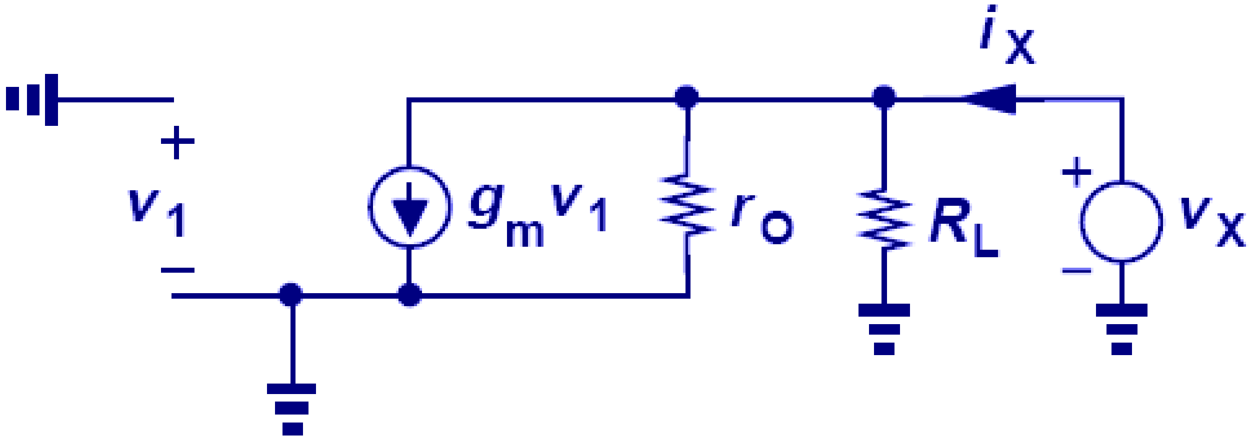


$$A_v = -g_m R_L$$

$$R_{in} = \infty$$

$$R_{out} = R_L$$

CS Stage with $\lambda \neq 0$



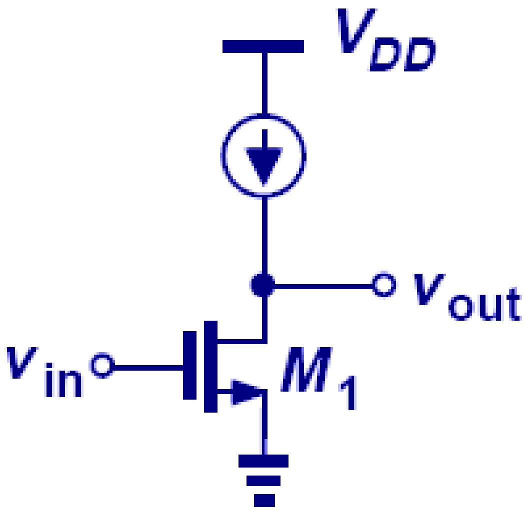
$$A_v = -g_m (R_L \| r_O)$$

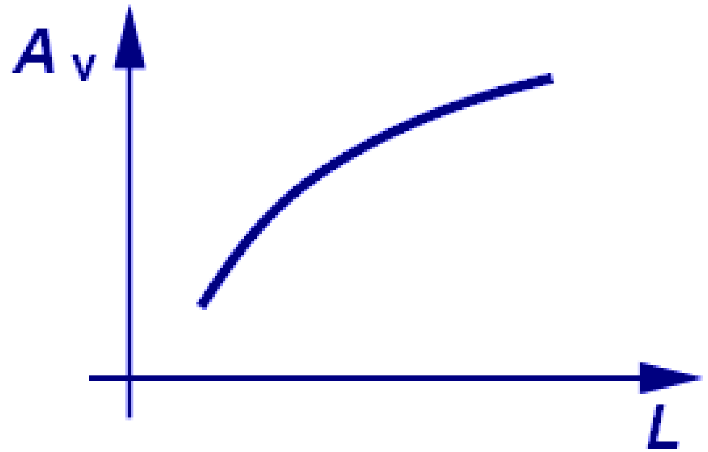
$$R_{in} = \infty$$

$$R_{out} = R_L \| r_O$$

- **However, Early effect and channel length modulation affect CE and CS stages in a similar manner.**

CS Gain Variation with Channel Length

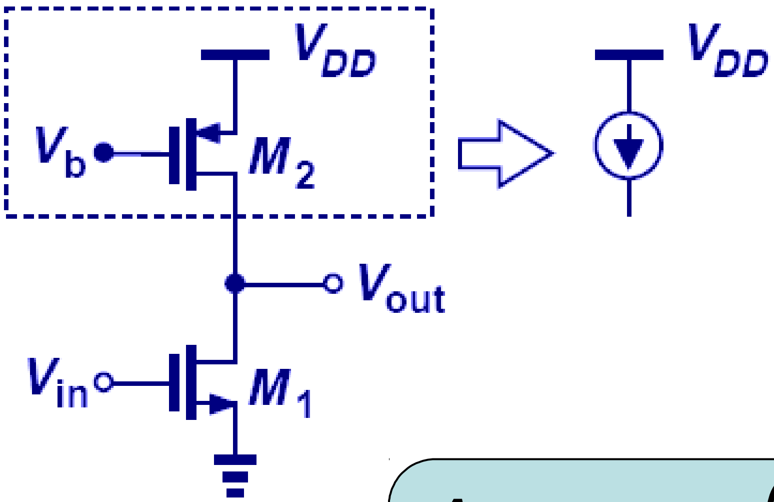


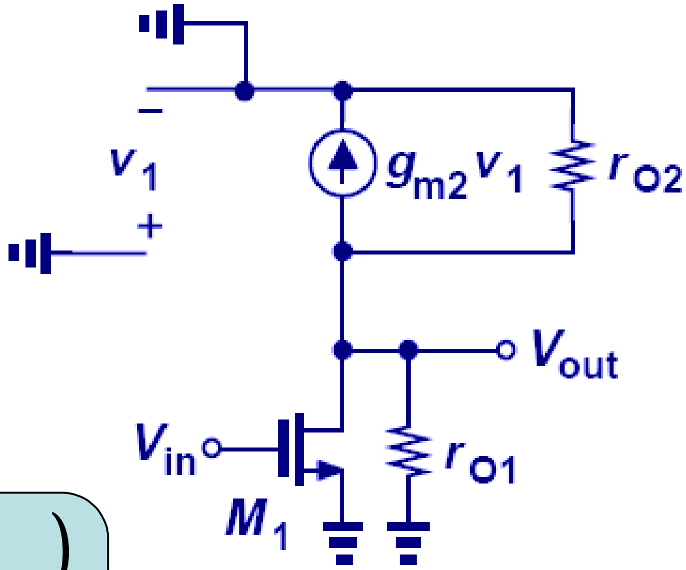


$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}}}{\lambda\sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

- Since λ is inversely proportional to L, the voltage gain actually becomes proportional to the square root of L.

CS Stage with Current-Source Load



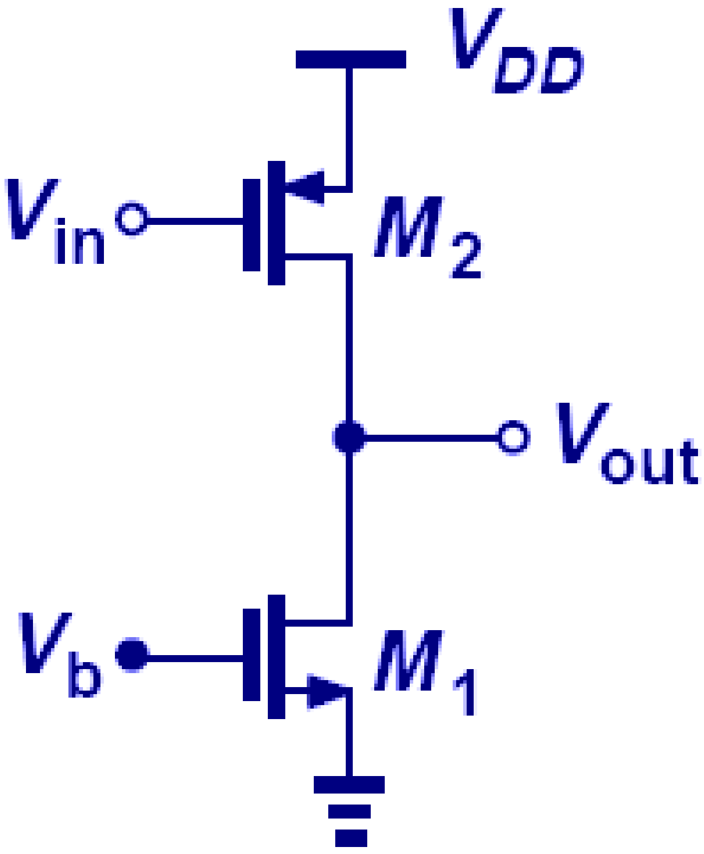


$$A_v = -g_{m1}(r_{O1} \| r_{O2})$$

$$R_{out} = r_{O1} \| r_{O2}$$

- To alleviate the headroom problem, an active current-source load is used.
- This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

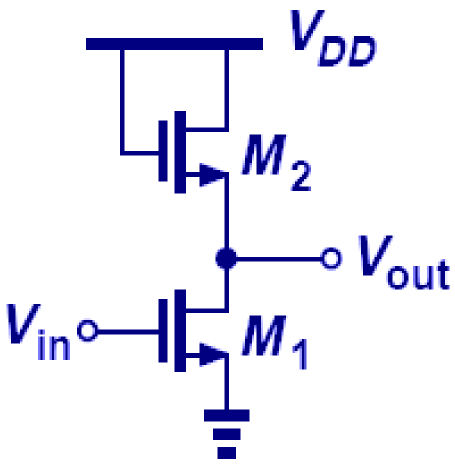
PMOS CS Stage with NMOS as Load

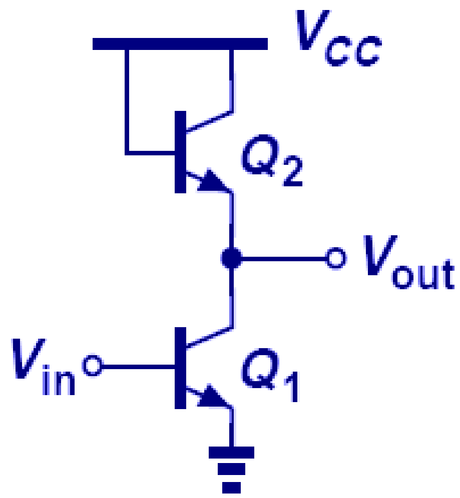


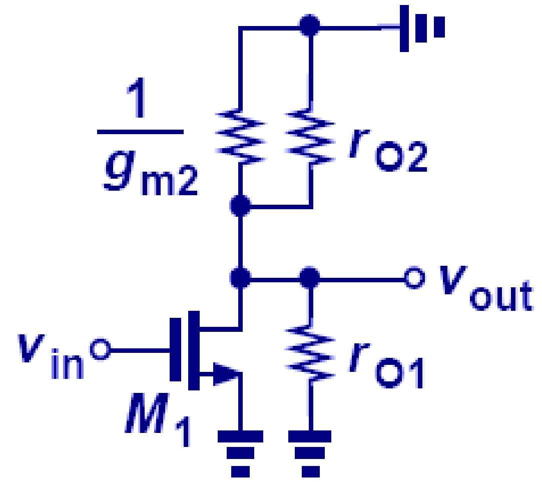
$$A_v = -g_{m2}(r_{O1} \| r_{O2})$$

- **Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.**

CS Stage with Diode-Connected Load





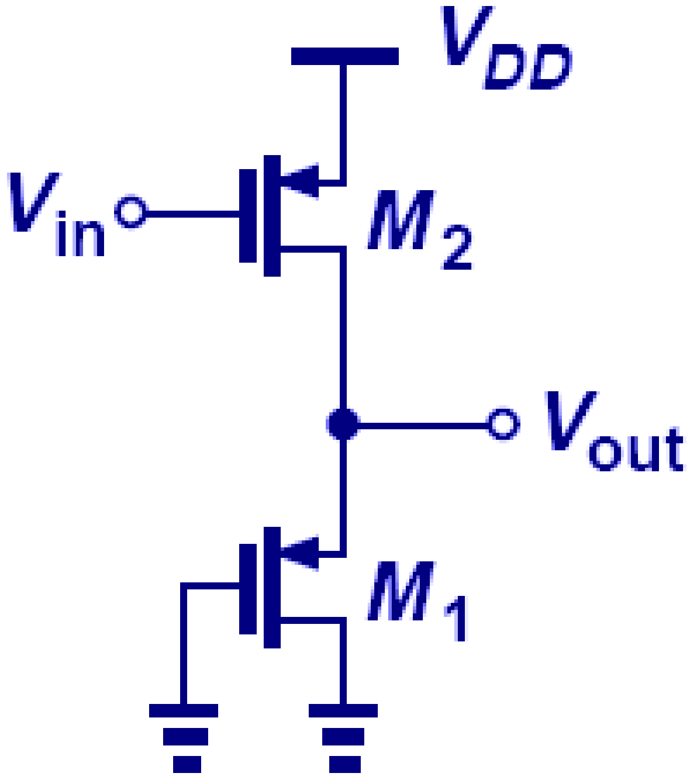


$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \| r_{O2} \| r_{O1}\right)$$

- **Lower gain, but less dependent on process parameters.**

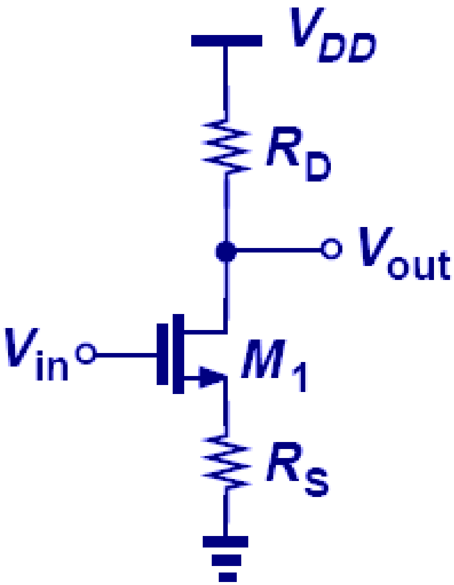
CS Stage with Diode-Connected PMOS Device

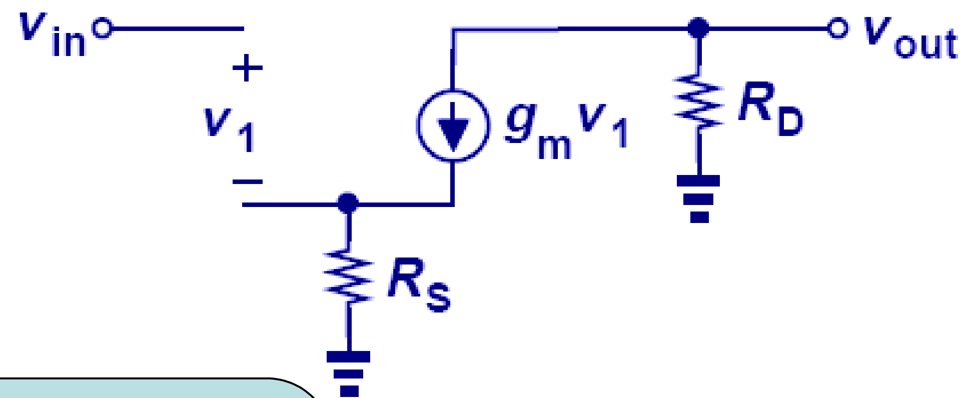


$$A_v = -g_{m2}\left(\frac{1}{g_{m1}} \| r_{o1} \| r_{o2}\right)$$

- **Note that PMOS circuit symbol is usually drawn with the source on top of the drain.**

CS Stage with Degeneration



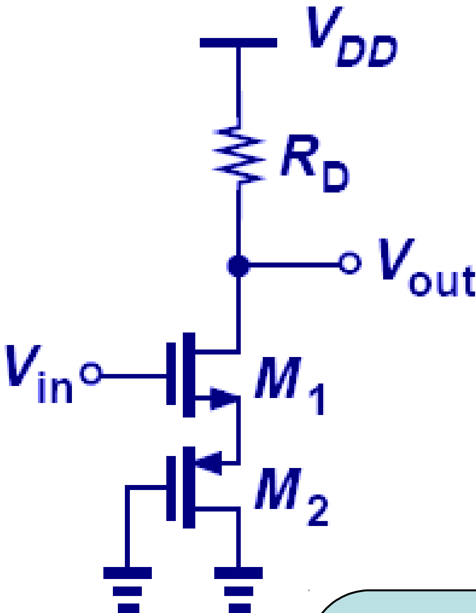


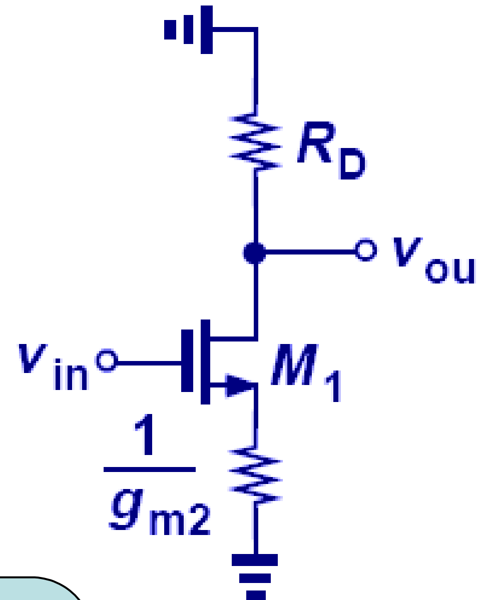
$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

$$\lambda = 0$$

- **Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.**

Example of CS Stage with Degeneration

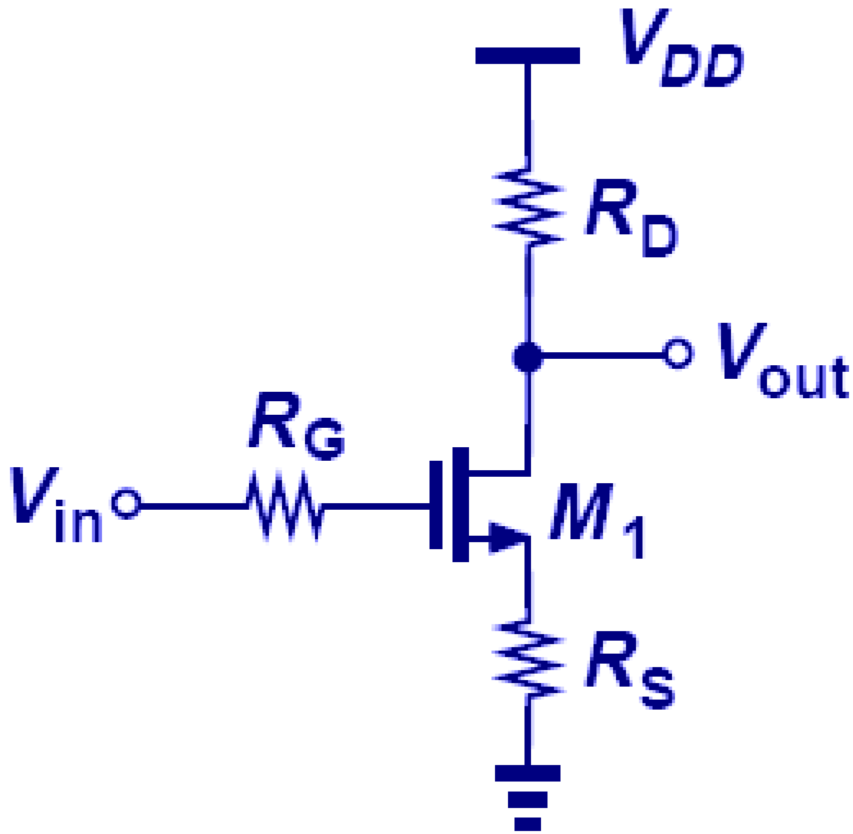




$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- **A diode-connected device degenerates a CS stage.**

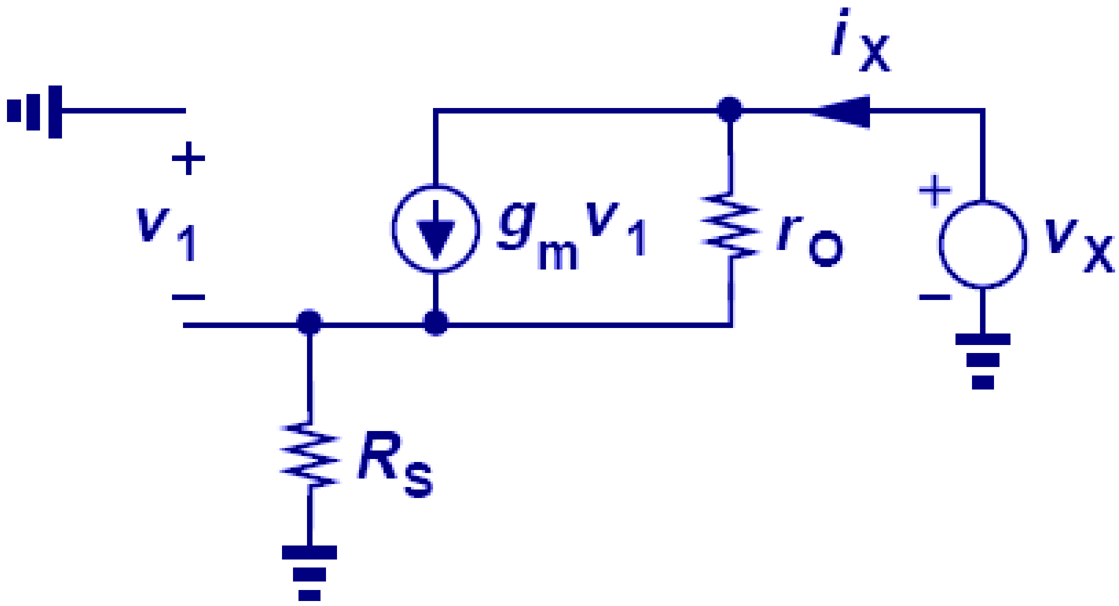
CS Stage with Gate Resistance



$$V_{R_G} = 0$$

- Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.

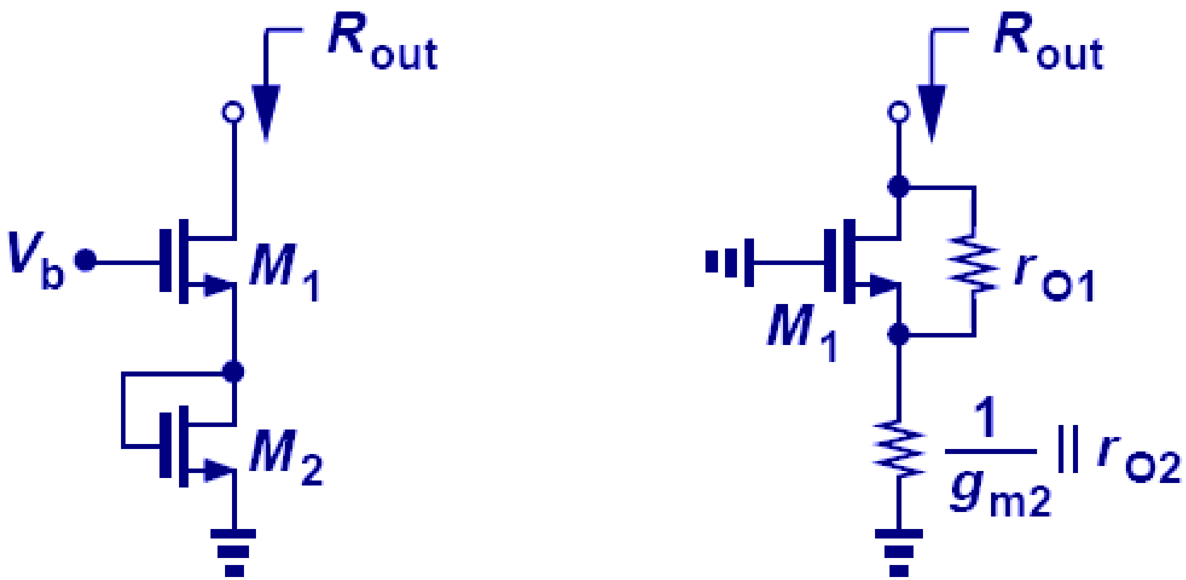
Output Impedance of CS Stage with Degeneration



$$r_{out} \approx g_m r_O R_S + r_O$$

- **Similar to the bipolar counterpart, degeneration boosts output impedance.**

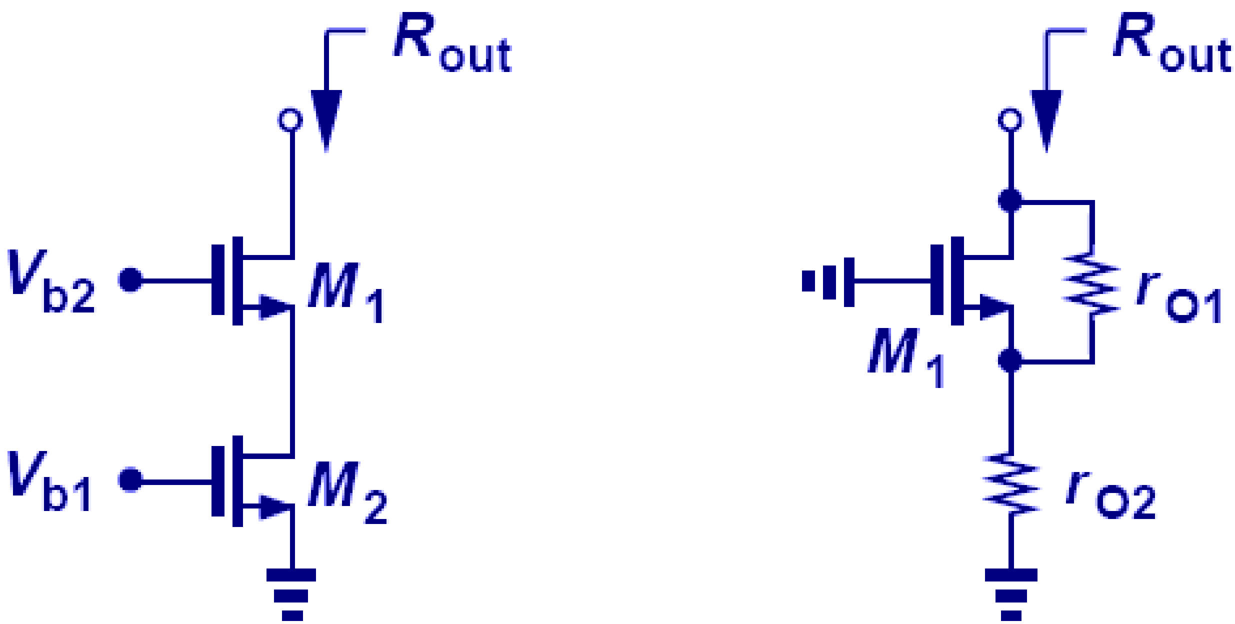
Output Impedance Example (I)



$$R_{out} = r_{O1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right) + \frac{1}{g_{m2}}$$

- **When $1/g_m$ is parallel with r_{O2}, we often just consider $1/g_m$.**

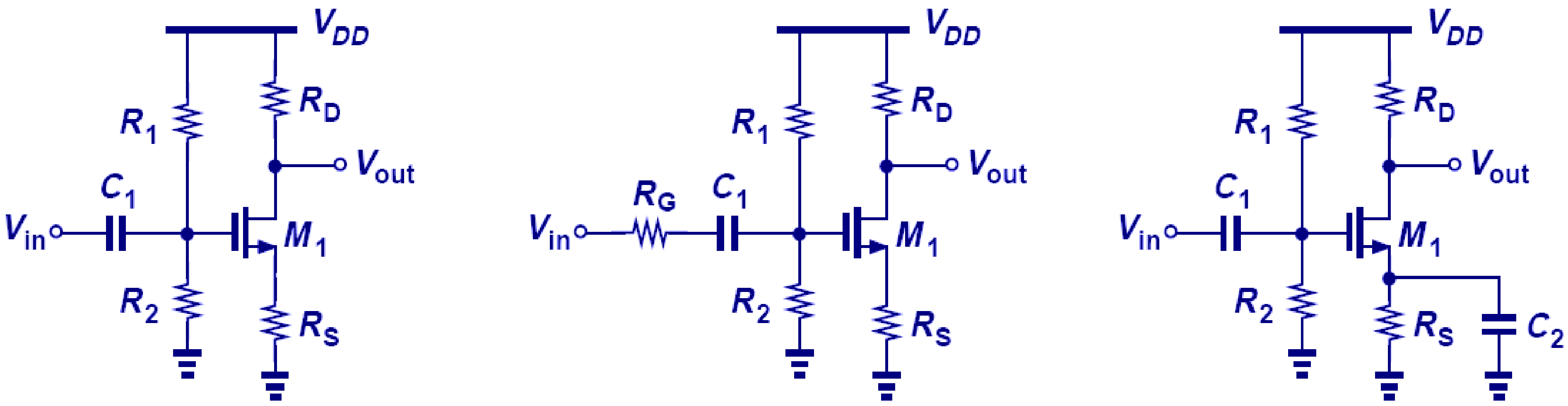
Output Impedance Example (II)



$$R_{out} \approx g_{m1} r_{O1} r_{O2} + r_{O1}$$

- **In this example, the impedance that degenerates the CS stage is r_O, instead of $1/g_m$ in the previous example.**

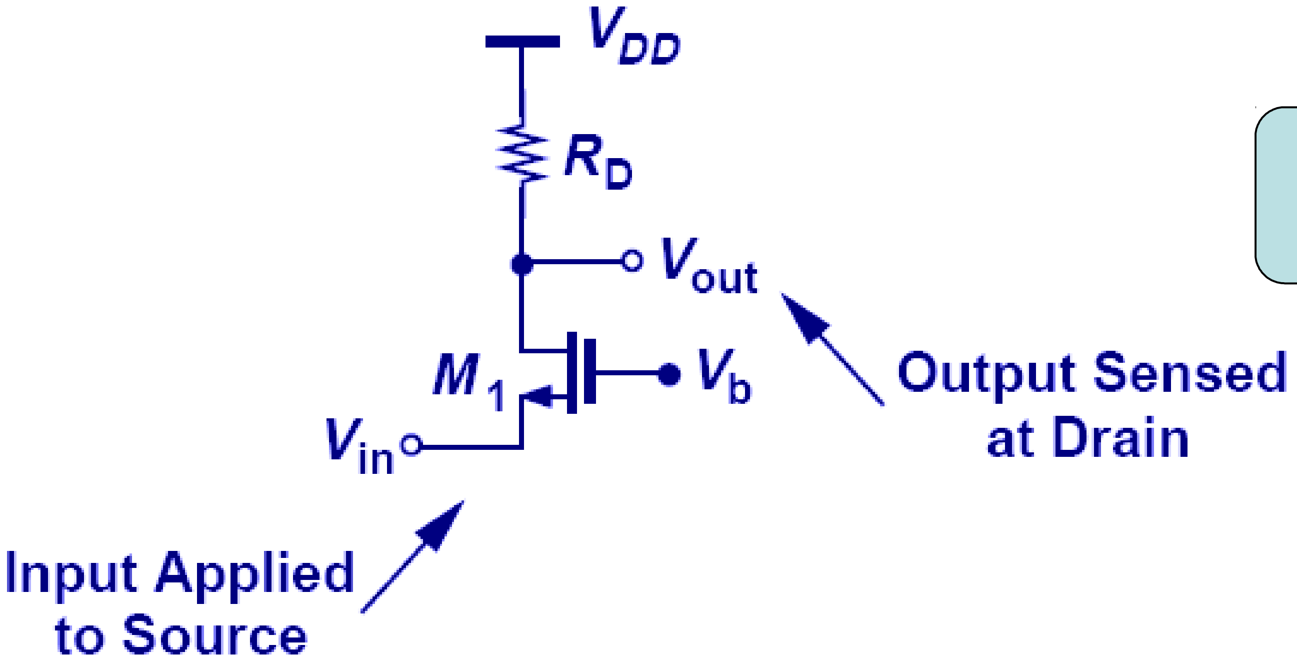
CS Core with Biasing



$$A_v = \frac{R_1 \| R_2}{R_G + R_1 \| R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, \quad A_v = -\frac{R_1 \| R_2}{R_G + R_1 \| R_2} g_m R_D$$

- **Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.**

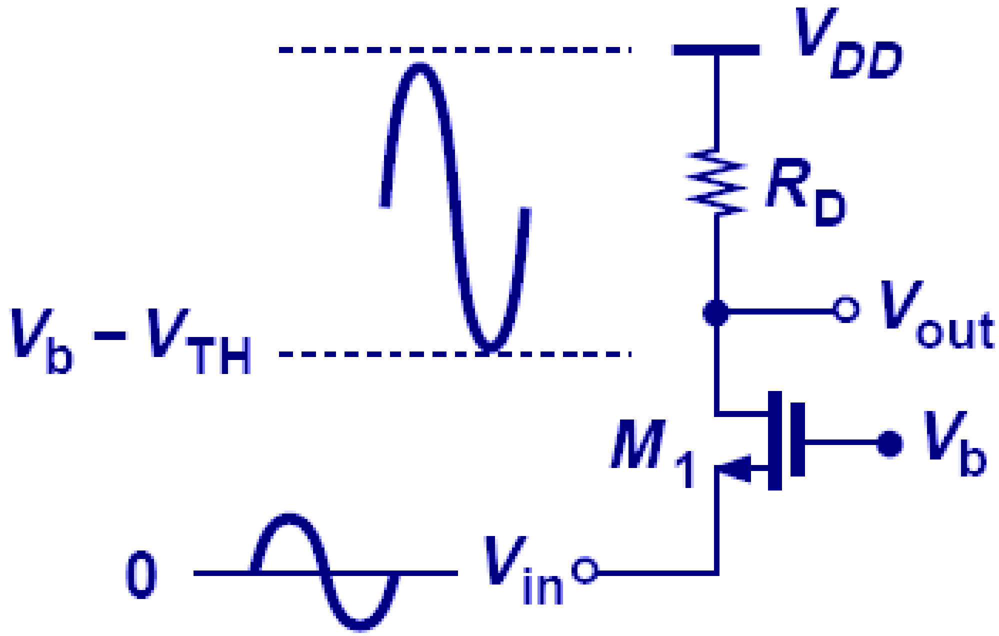
Common-Gate Stage



$$A_v = g_m R_D$$

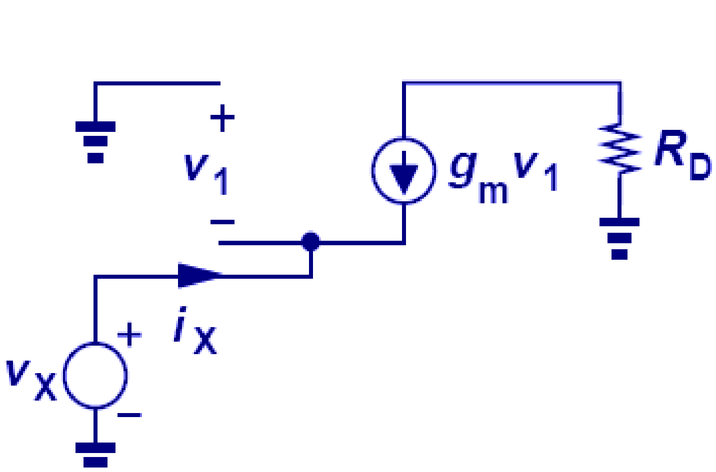
- **Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.**

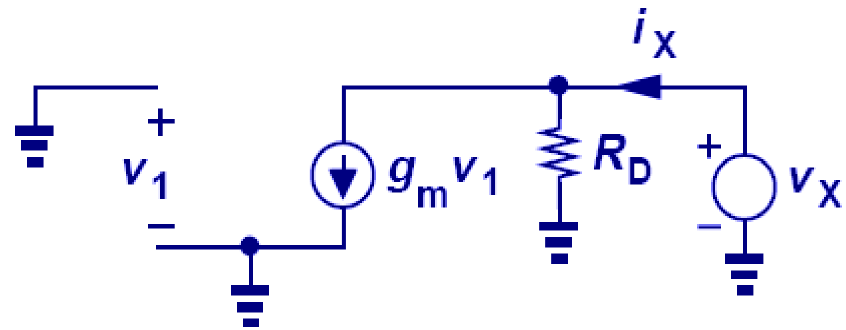
Signal Levels in CG Stage



- **In order to maintain M_1 in saturation, the signal swing at V_{out} cannot fall below V_b-V_{TH}.**

I/O Impedances of CG Stage





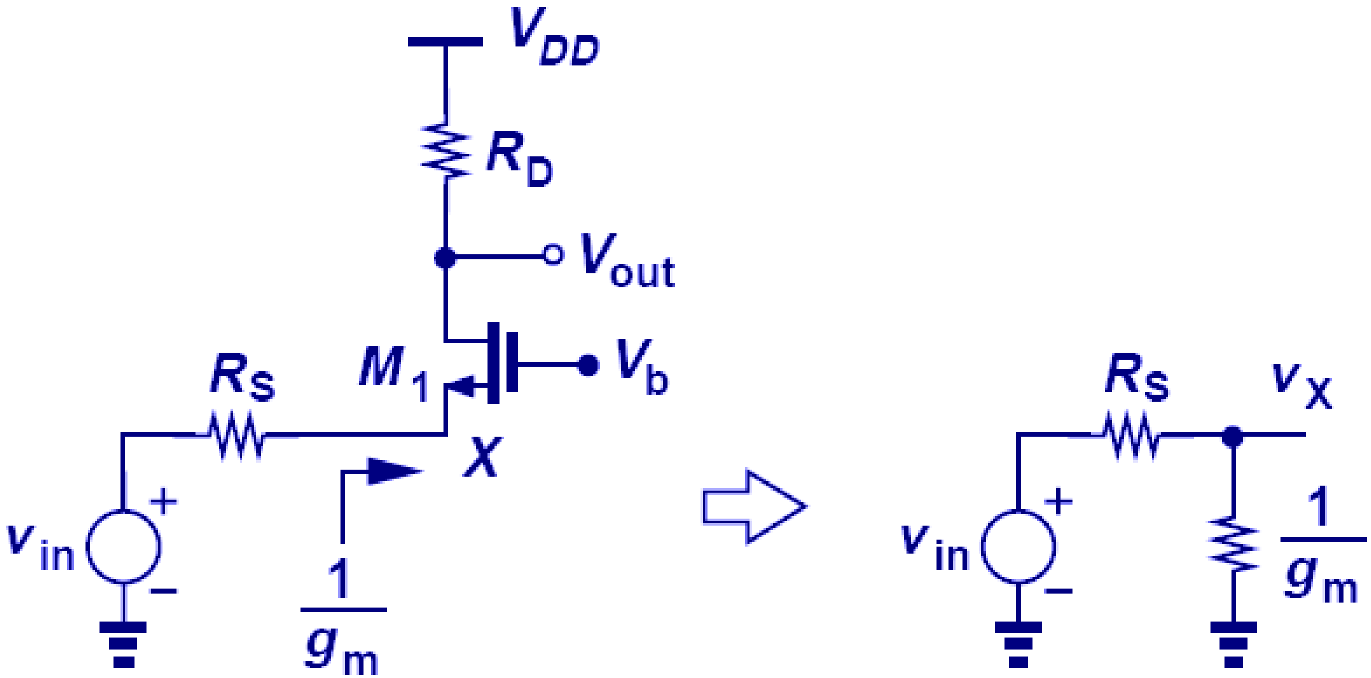
$$R_{in} = \frac{1}{g_m}$$

$$\lambda = 0$$

$$R_{out} = R_D$$

- **The input and output impedances of CG stage are similar to those of CB stage.**

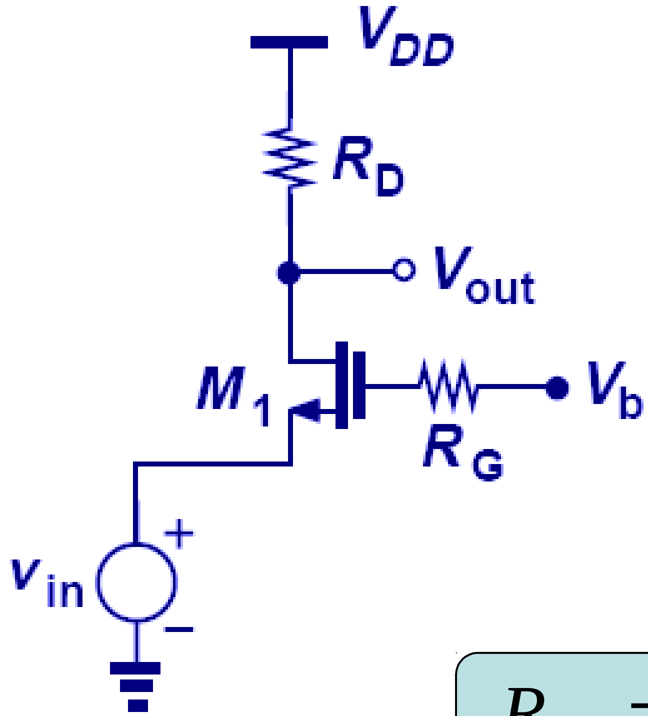
CG Stage with Source Resistance

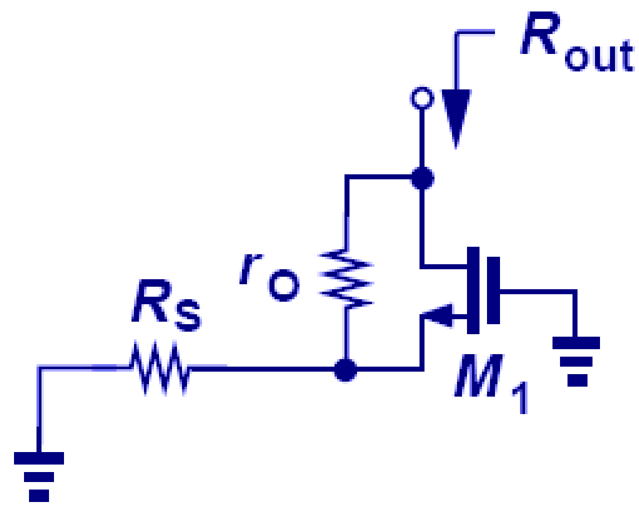


$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$

- **When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.**

Generalized CG Behavior

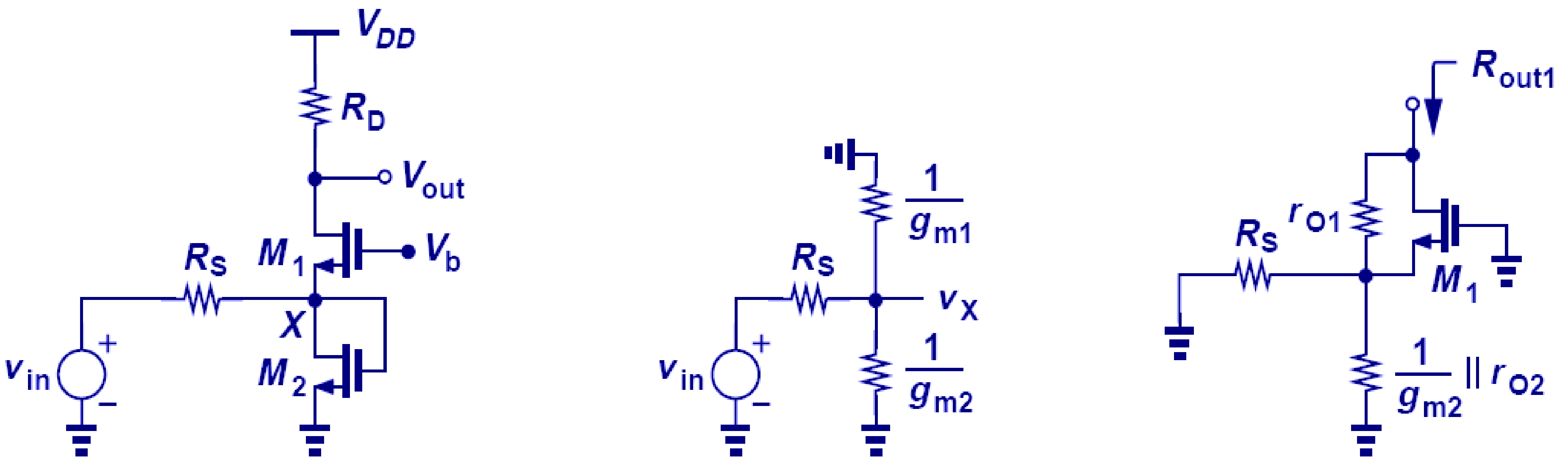




$$R_{out} = (1 + g_m r_O) R_S + r_O$$

- **When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).**
- **The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.**

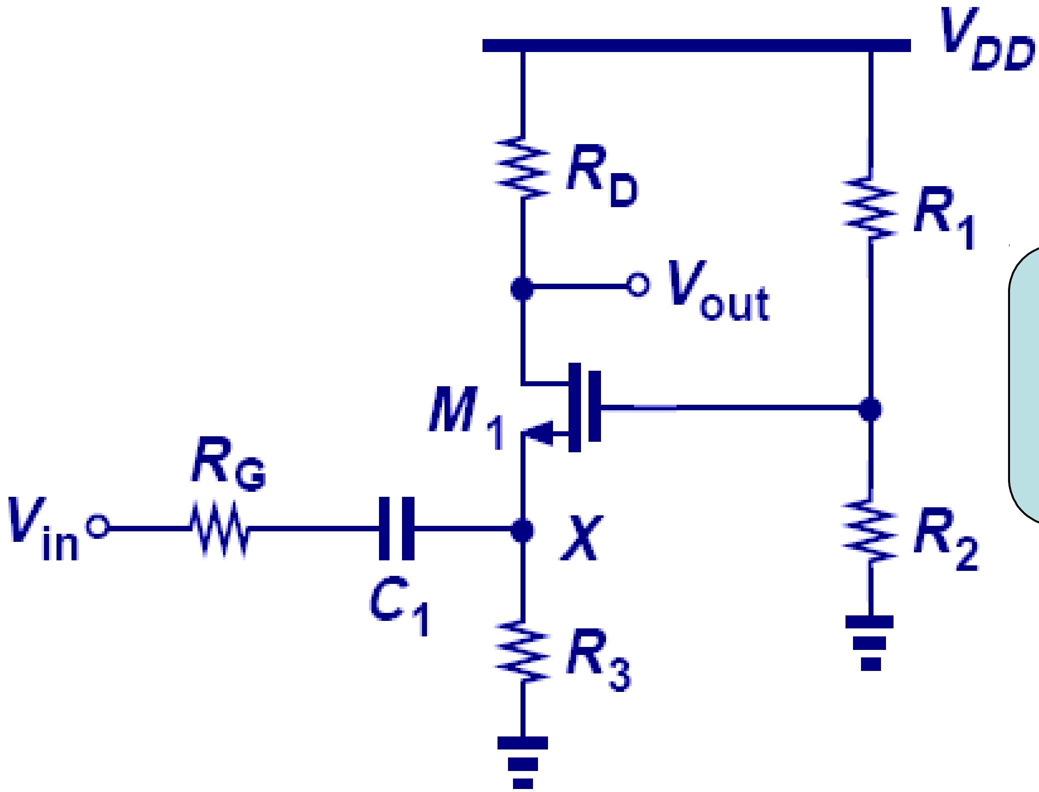
Example of CG Stage



$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}R_D}{1+(g_{m1}+g_{m2})R_S} \qquad R_{out} \approx \left[g_{m1}r_{O1}\left(\frac{1}{g_{m2}} \| R_S\right) + r_{O1}\right] \| R_D$$

- **Diode-connected M_2 acts as a resistor to provide the bias current.**

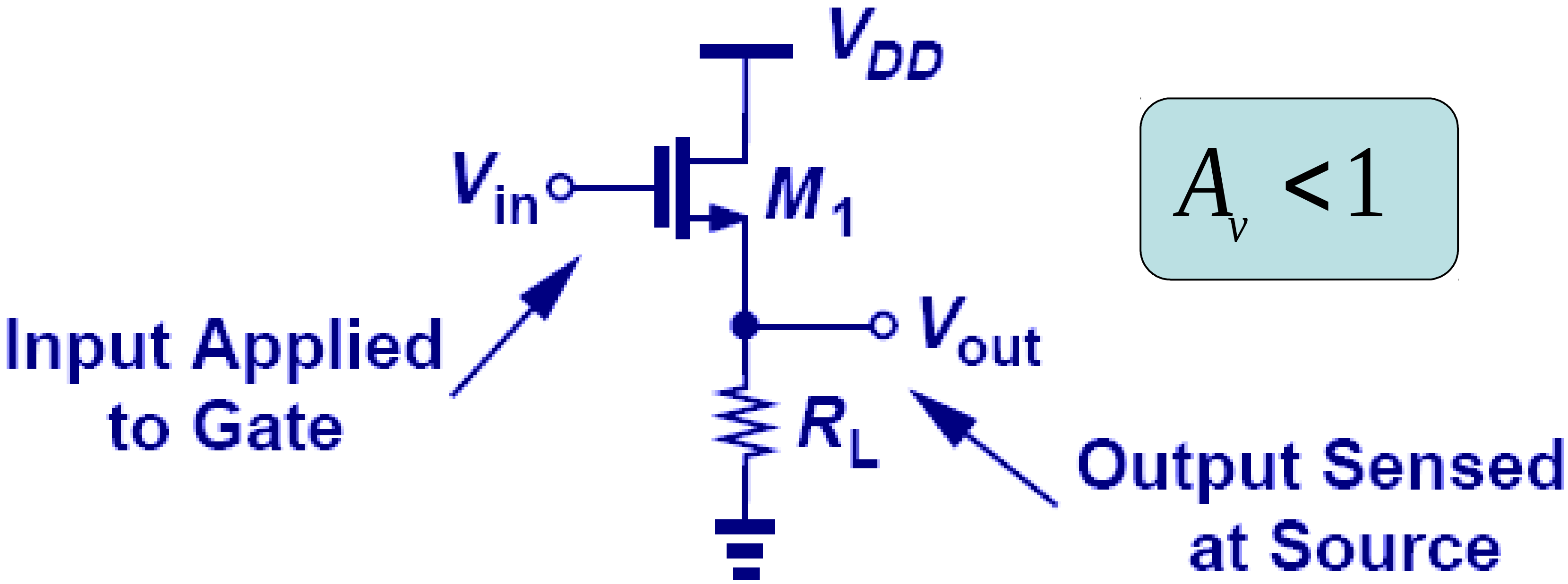
CG Stage with Biasing



$$\frac{v_{out}}{v_{in}} = \frac{R_3 \| (1/g_m)}{R_3 \| (1/g_m) + R_S} \cdot g_m R_D$$

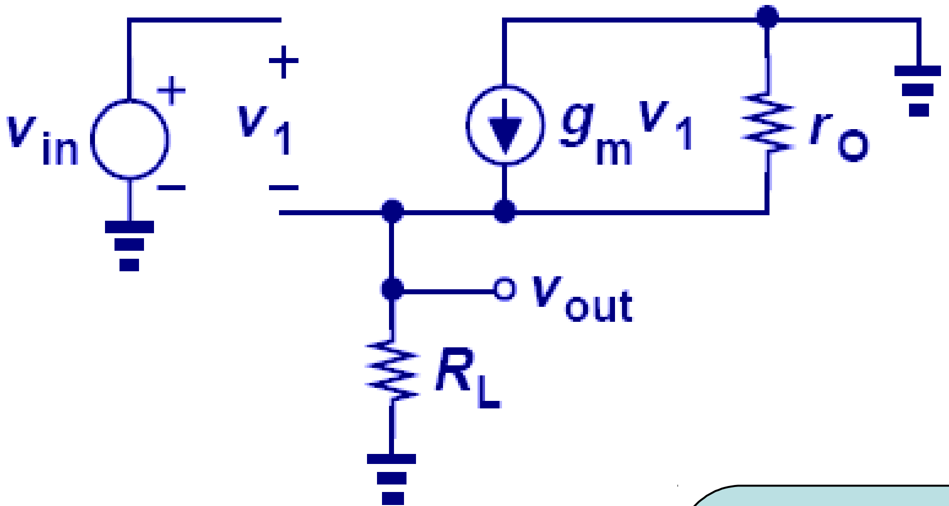
- R_1 and R_2 provide gate bias voltage, and R_3 provides a path for DC bias current of M_1 to flow to ground.

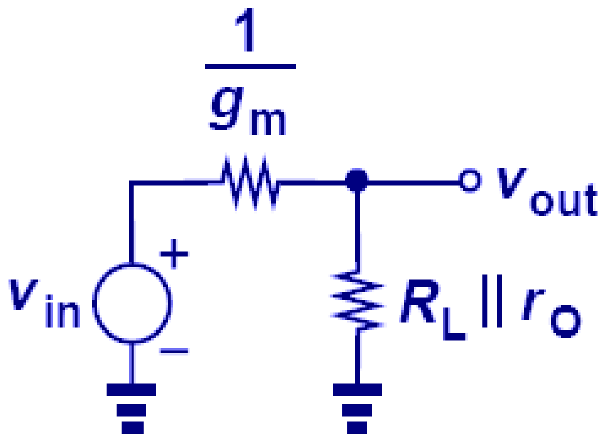
Source Follower Stage



$$A_v < 1$$

Source Follower Core

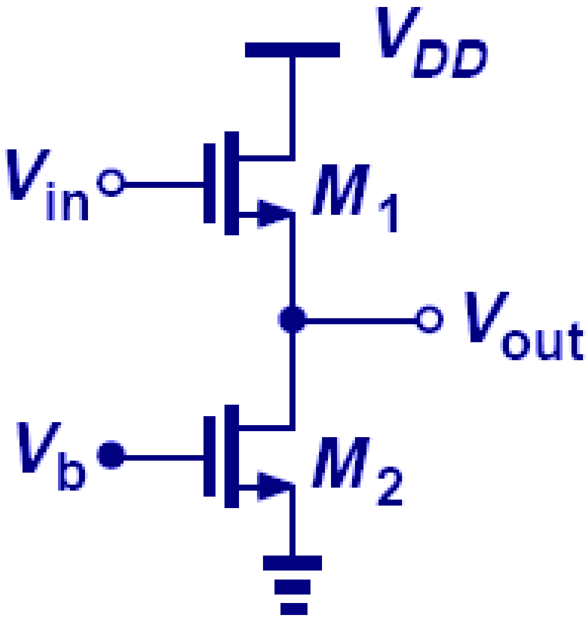


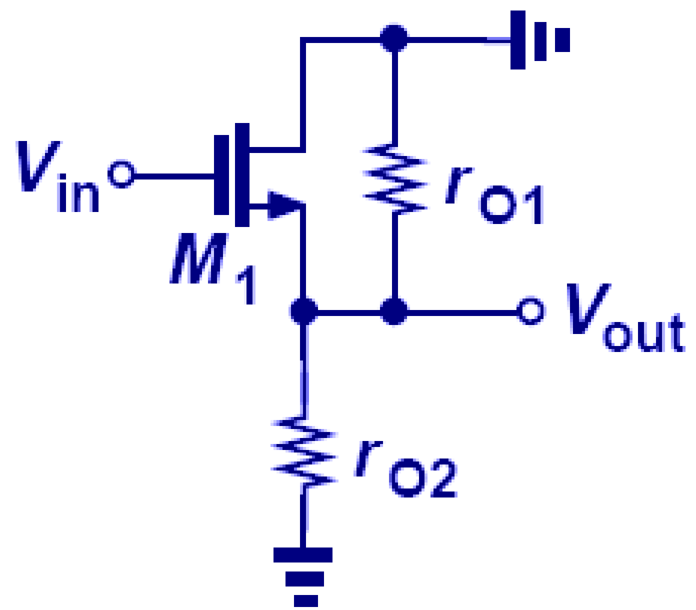


$$\frac{v_{out}}{v_{in}} = \frac{r_O \| R_L}{\frac{1}{g_m} + r_O \| R_L}$$

- **Similar to the emitter follower, the source follower can be analyzed as a resistor divider.**

Source Follower Example

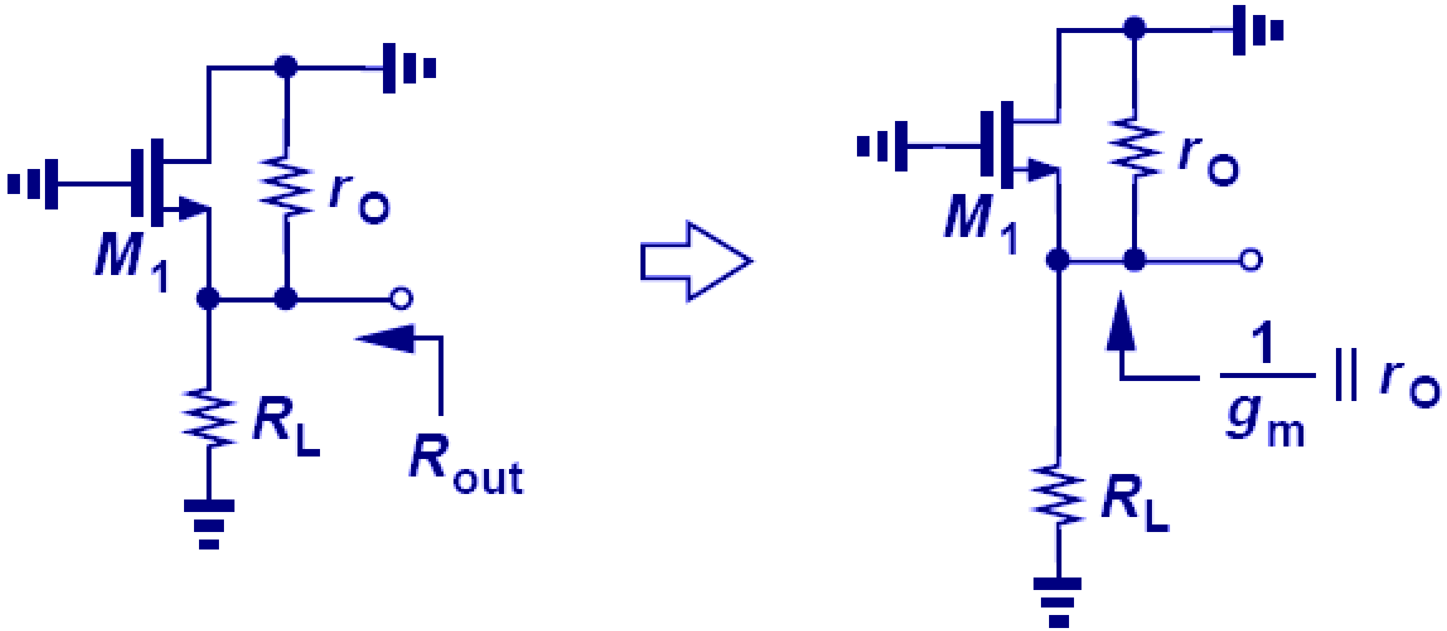




$$A_v = \frac{r_{O1} \| r_{O2}}{\frac{1}{g_{m1}} + r_{O1} \| r_{O2}}$$

- **In this example, M_2 acts as a current source.**

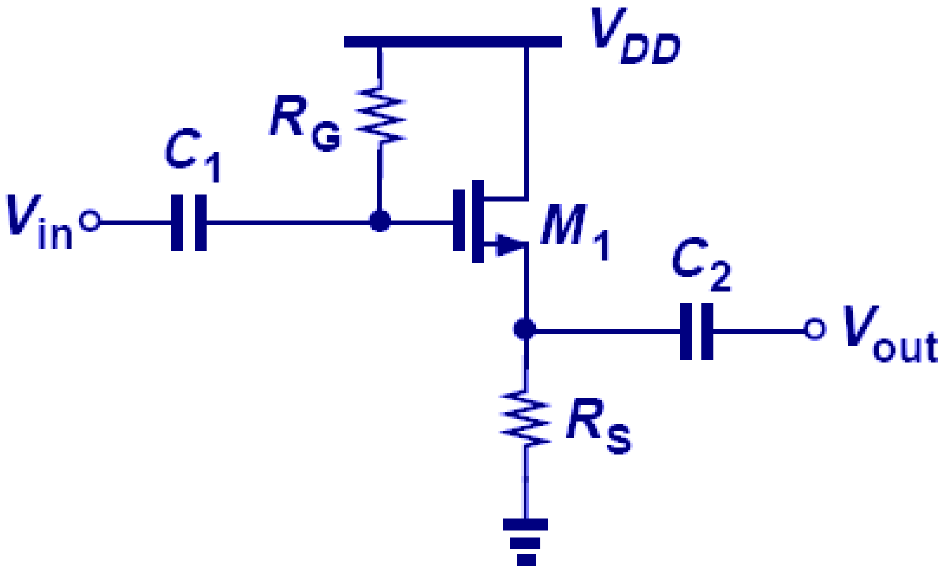
Output Resistance of Source Follower



$$R_{out} = \frac{1}{g_m} \parallel r_O \parallel R_L \approx \frac{1}{g_m} \parallel R_L$$

- **The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.**

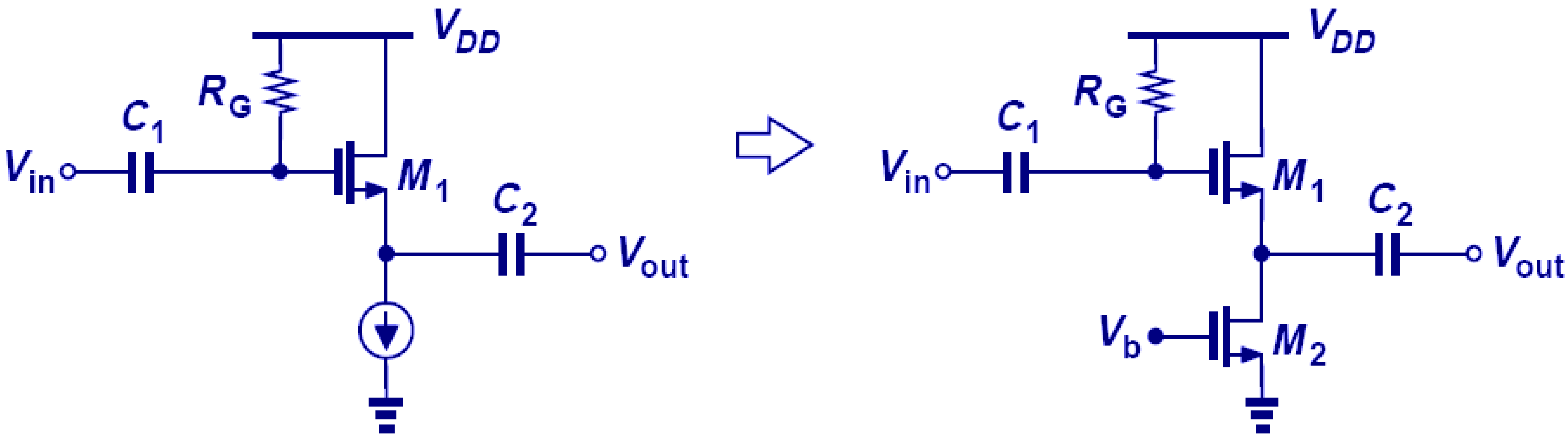
Source Follower with Biasing



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - I_D R_S - V_{TH})^2$$

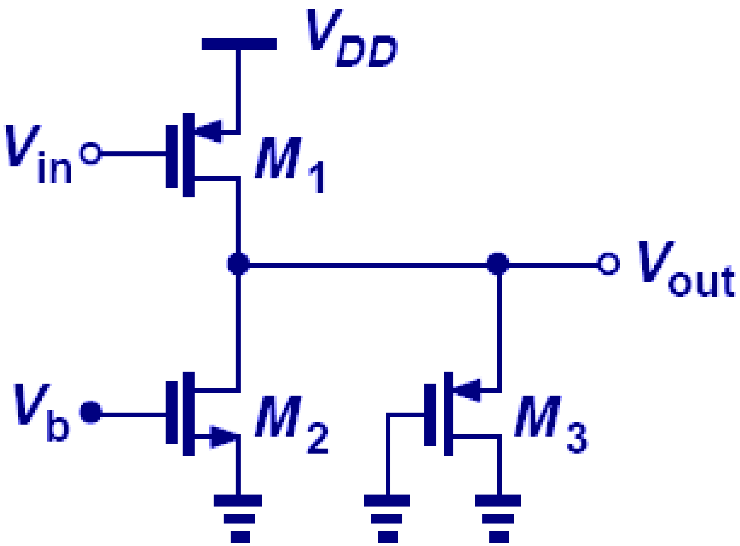
- R_G sets the gate voltage to V_{DD}, whereas R_S sets the drain current.
- The quadratic equation above can be solved for I_D.

Supply-Independent Biasing

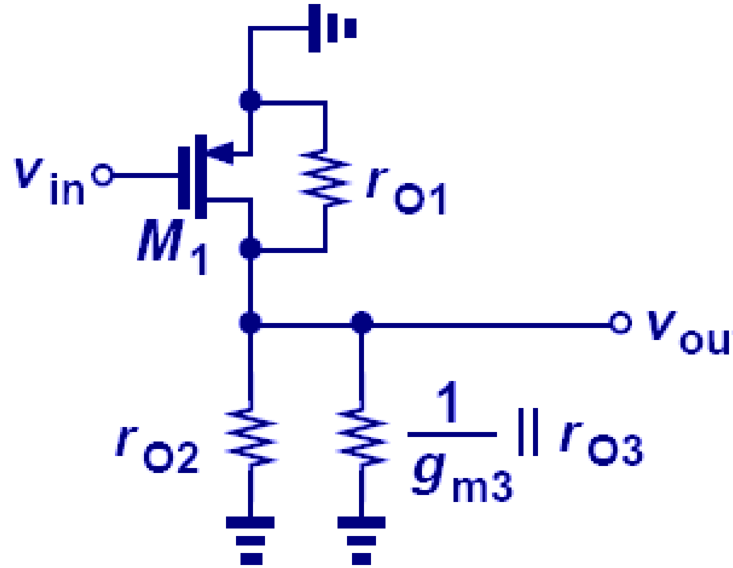


- **If R_s is replaced by a current source, drain current I_D becomes independent of supply voltage.**

Example of a CS Stage (I)



(a)



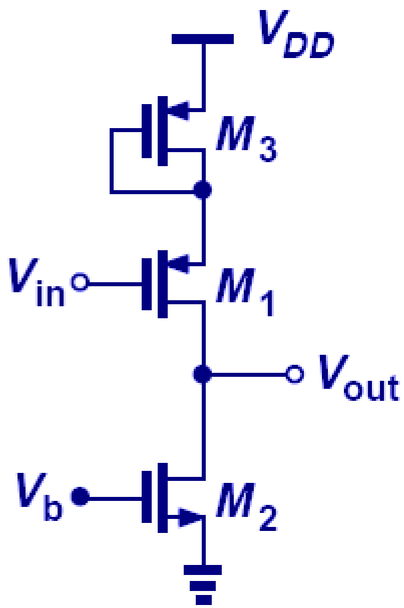
(b)

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}\right)$$

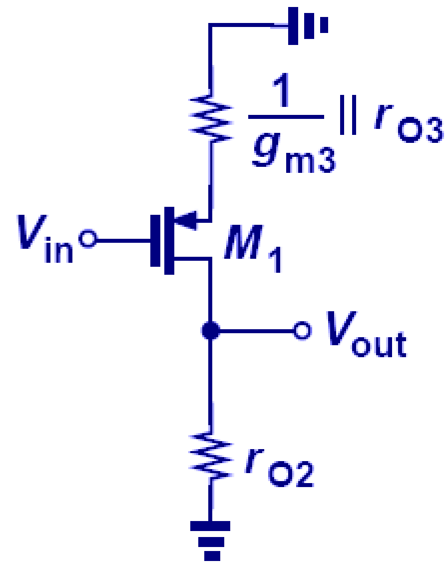
$$R_{out} = \frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}$$

- **M_1 acts as the input device and M_2, M_3 as the load.**

Example of a CS Stage (II)



(a)

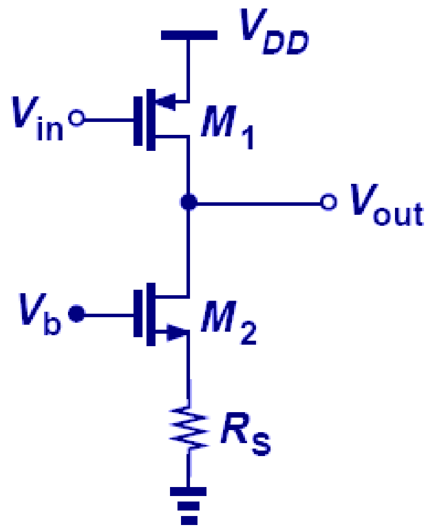


(b)

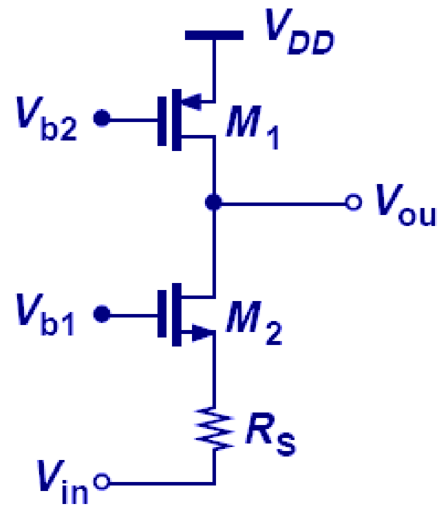
$$A_v = -\frac{r_{O2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} \| r_{O3}}$$

- **M_1 acts as the input device, M_3 as the source resistance, and M_2 as the load.**

Examples of CS and CG Stages



(a)



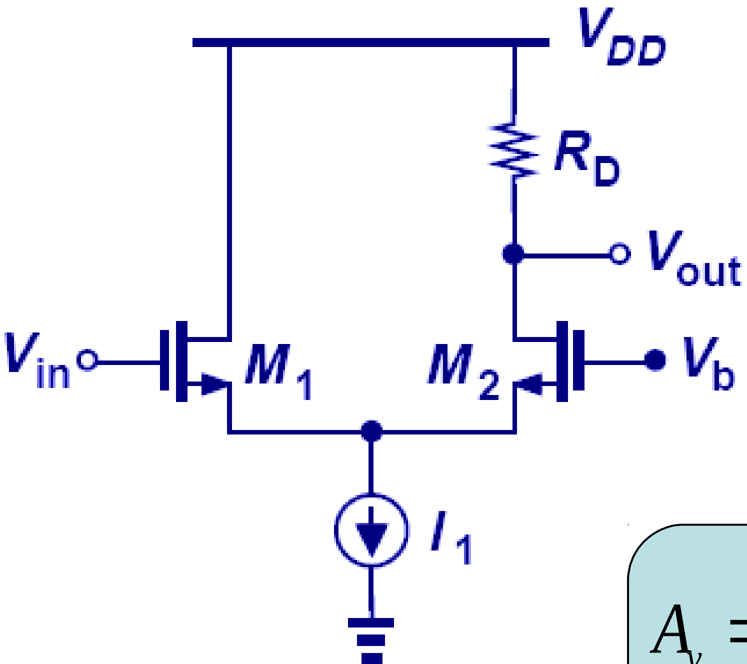
(b)

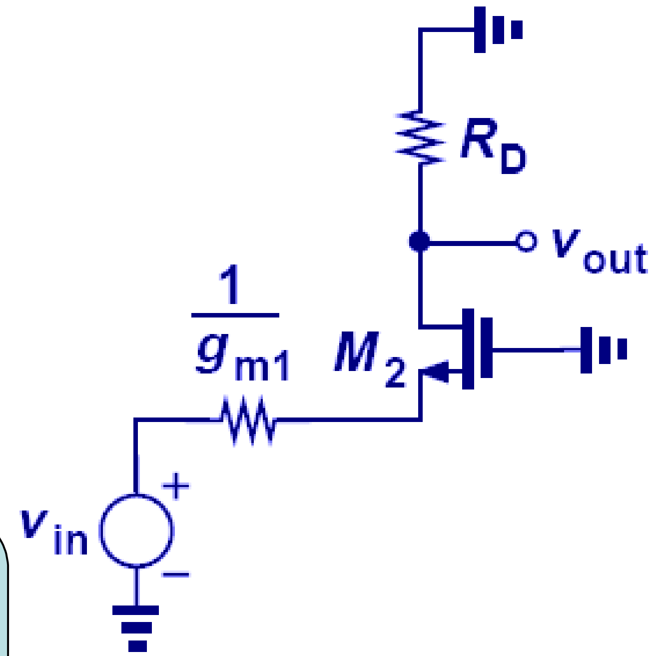
$$A_{v\_CS} = -g_{m2}\left[(1+g_{m1}r_{O1})R_S + r_{O1}\right] \| r_{O1}$$

$$A_{v\_CG} = \frac{r_{O2}}{\frac{1}{g_m} + R_S}$$

- **With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.**

Example of a Composite Stage (I)

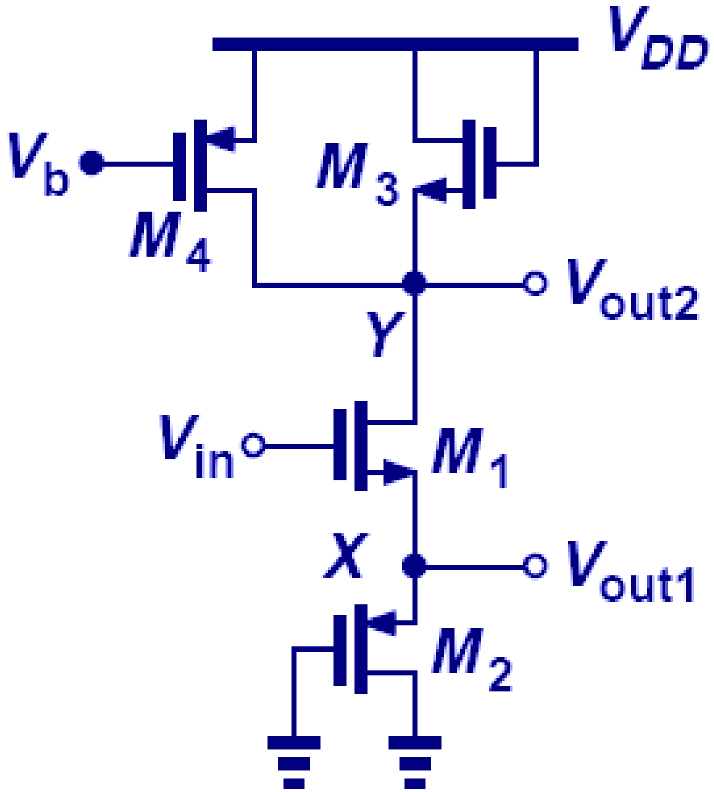




$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.

Example of a Composite Stage (II)



$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}} \| r_{O3} \| r_{O4}}{\frac{1}{g_{m2}} \| r_{O2} + \frac{1}{g_{m1}}}$$

- This example shows that by probing different places in a circuit, different types of output can be obtained.
- V_{out1} is a result of M_1 acting as a source follower whereas V_{out2} is a result of M_1 acting as a CS stage with degeneration.

Chapter 8 Operational Amplifier as A Black Box

- 8.1 General Considerations
- 8.2 Op-Amp-Based Circuits
- 8.3 Nonlinear Functions
- 8.4 Op-Amp Nonidealities
- 8.5 Design Examples

Chapter Outline

General Concepts

- Op Amp Properties

Linear Op Amp Circuits

- Noninverting Amplfier
- Inverting Amplifier
- Inetgrator and Differentiator
- Voltage Added

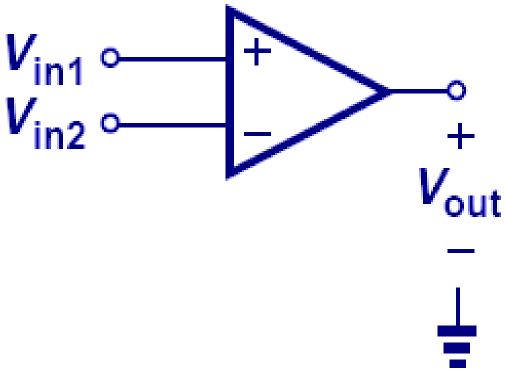
Nonlinear Op Amp Circuits

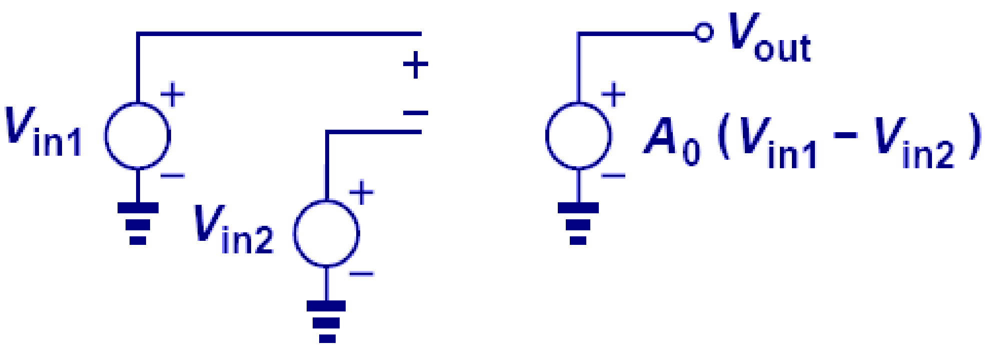
- Precision Rectifier
- Logarithmic Amplifier
- Square Root Circuit

Op Amp Nonidealities

- DC Offsets
- Input Bias Currents
- Speed Limitations
- Finite Input and Output Impedances

Basic Op Amp

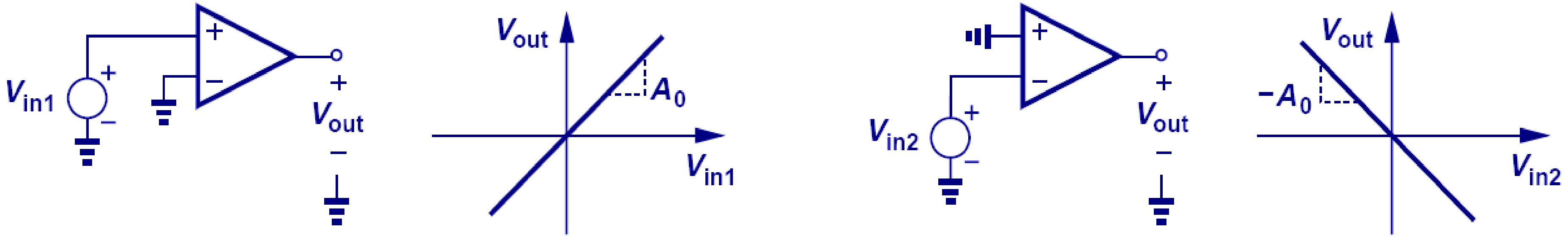




$$V_{out} = A_0 (V_{in1} - V_{in2})$$

- Op amp is a circuit that has two inputs and one output.
- It amplifies the difference between the two inputs.

Inverting and Non-inverting Op Amp

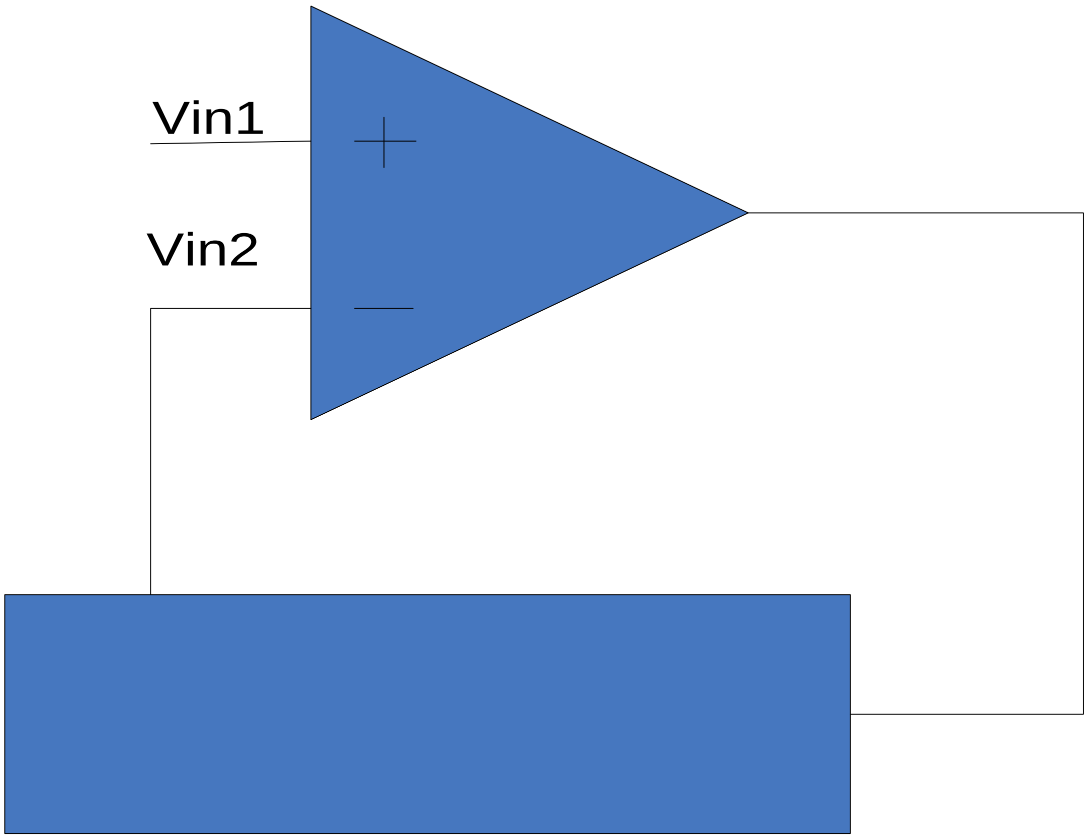


- If the negative input is grounded, the gain is positive.
- If the positive input is grounded, the gain is negative.

Ideal Op Amp

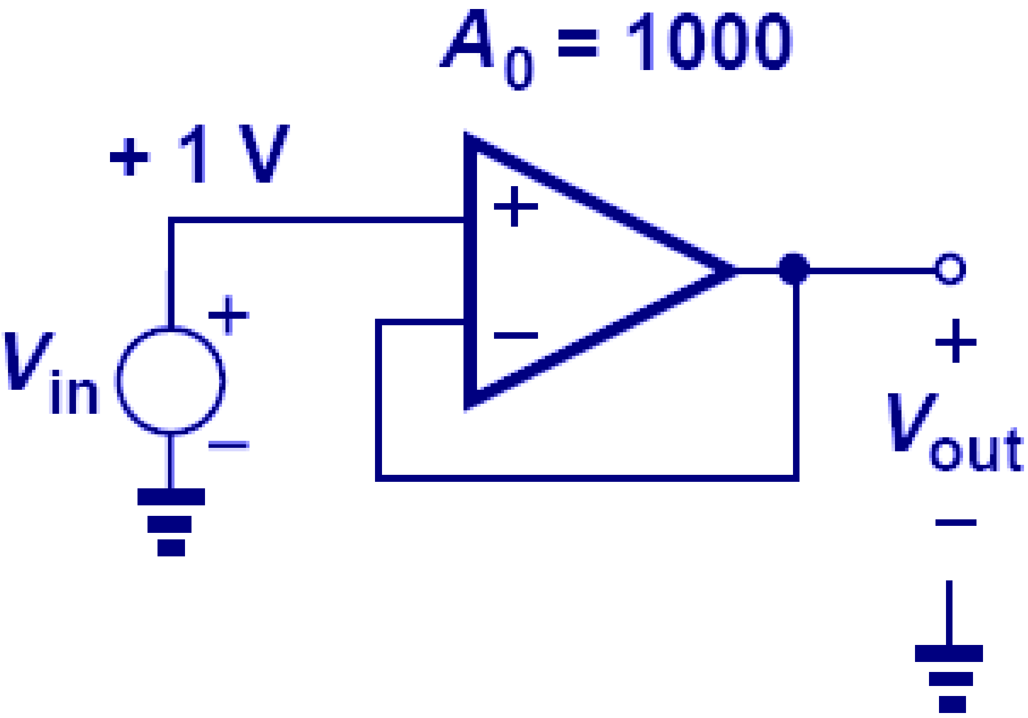
- **Infinite gain**
- **Infinite input impedance**
- **Zero output impedance**
- **Infinite speed**

Virtual Short



- **Due to infinite gain of op amp, the circuit forces V_{in2} to be close to V_{in1}, thus creating a virtual short.**

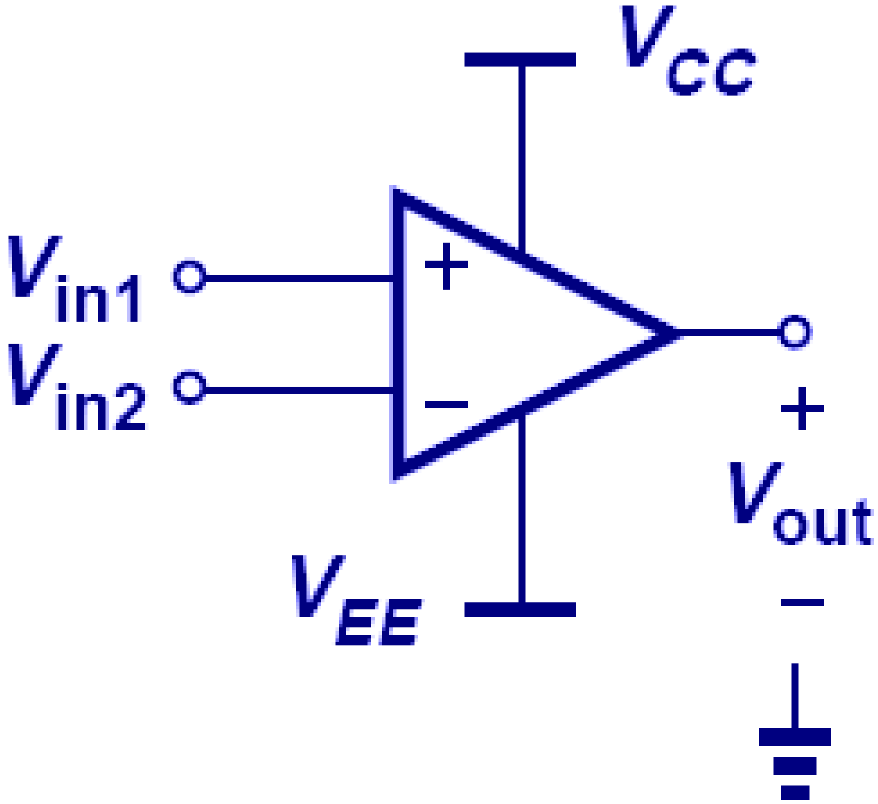
Unity Gain Amplifier



$$V_{out} = A_0 (V_{in} - V_{out})$$

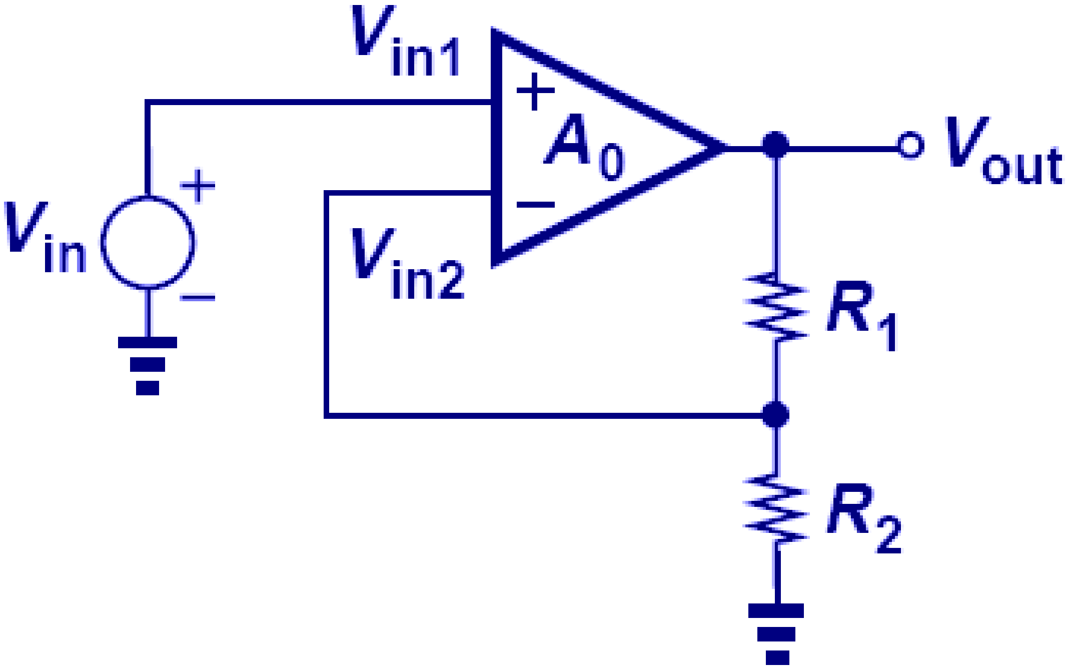
$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + A_0}$$

Op Amp with Supply Rails



- To explicitly show the supply voltages, V_{CC} and V_{EE} are shown.
- In some cases, V_{EE} is zero.

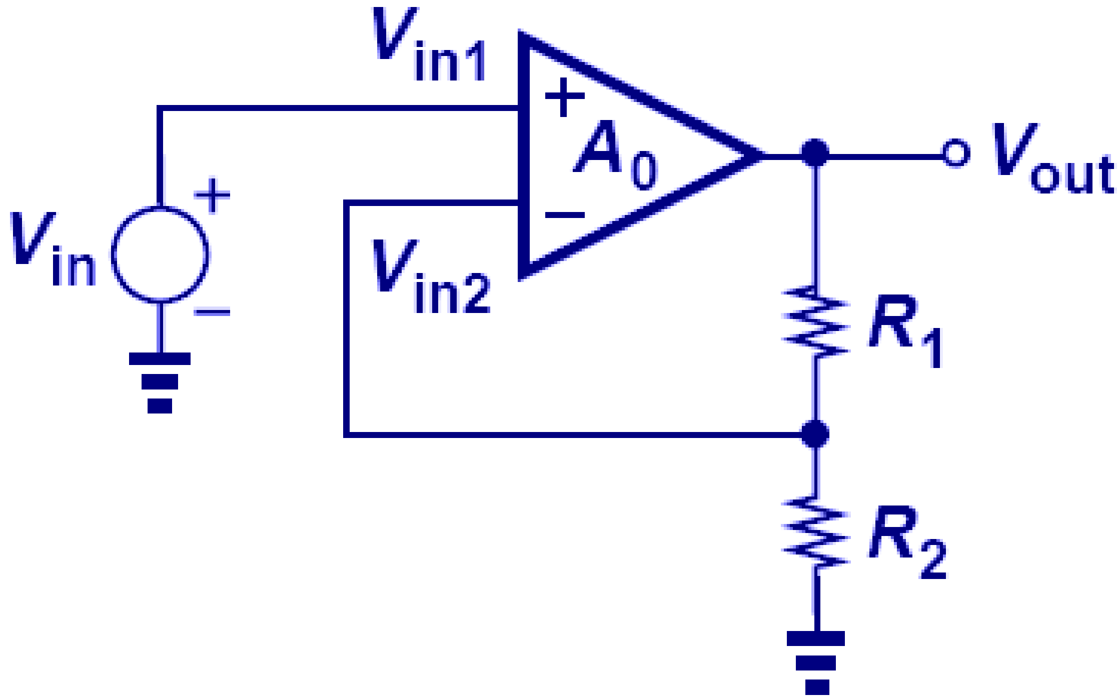
Noninverting Amplifier (Infinite A_0)



$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_1}{R_2}$$

- A noninverting amplifier returns a fraction of output signal thru a resistor divider to the negative input.
- With a high A_o, V_{out}/V_{in} depends only on ratio of resistors, which is very precise.

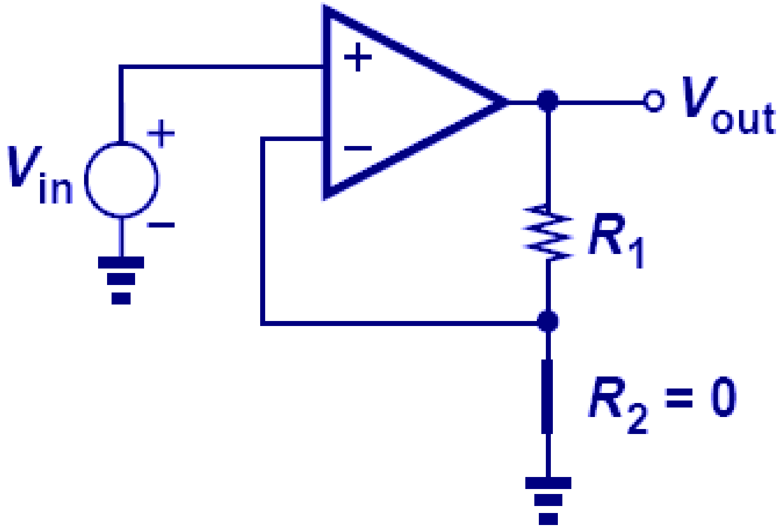
Noninverting Amplifier (Finite A_0)

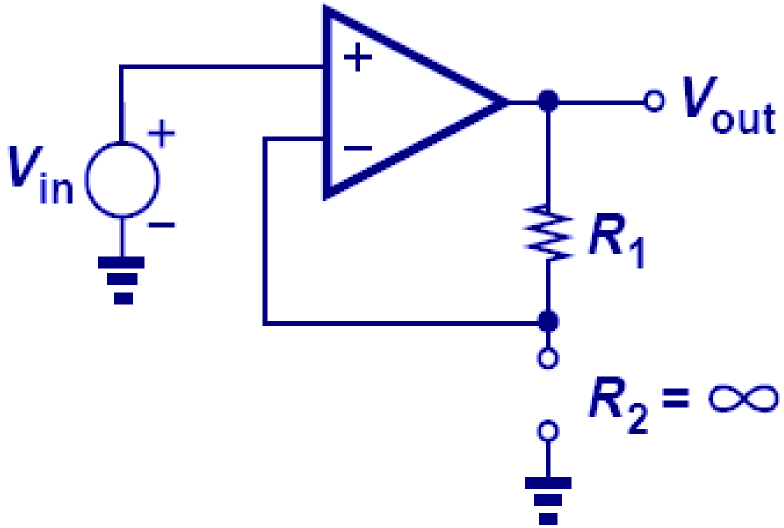


$$\frac{V_{out}}{V_{in}} \approx \left(1+\frac{R_1}{R_2}\right)\left[1-\left(1+\frac{R_1}{R_2}\right)\frac{1}{A_0}\right]$$

- **The error term indicates the larger the closed-loop gain, the less accurate the circuit becomes.**

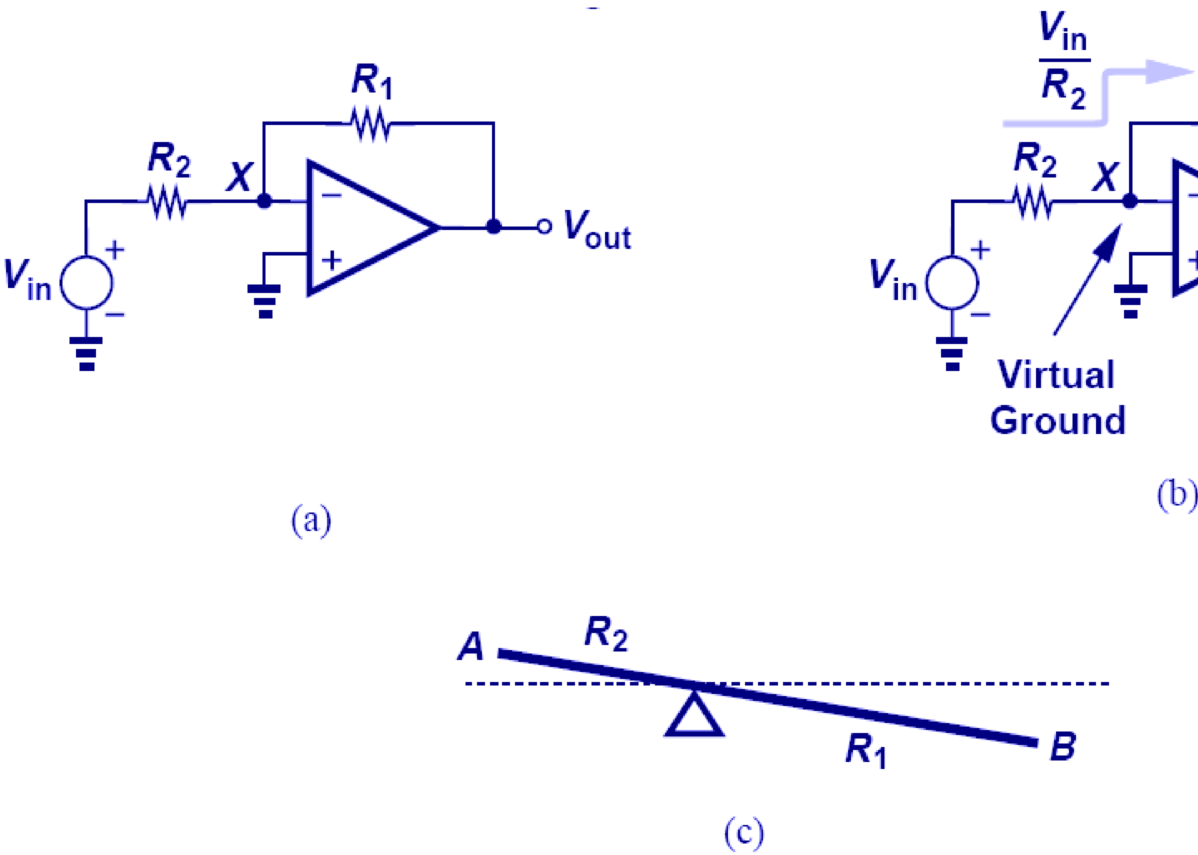
Extreme Cases of R_2 (Infinite A_0)





- If R_2 is zero, the loop is open and V_{out}/V_{in} is equal to the intrinsic gain of the op amp.
- If R_2 is infinite, the circuit becomes a unity-gain amplifier and V_{out}/V_{in} becomes equal to one.

Inverting Amplifier

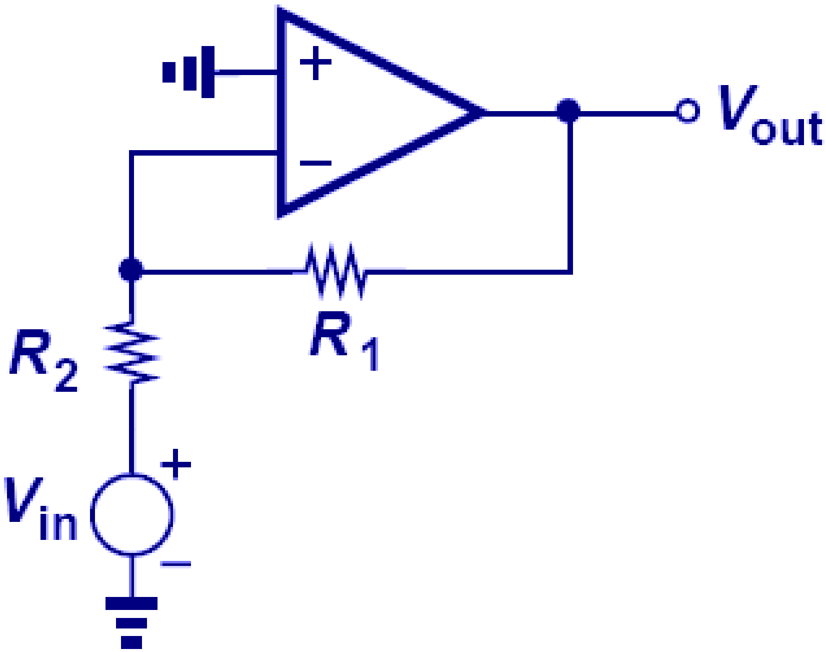


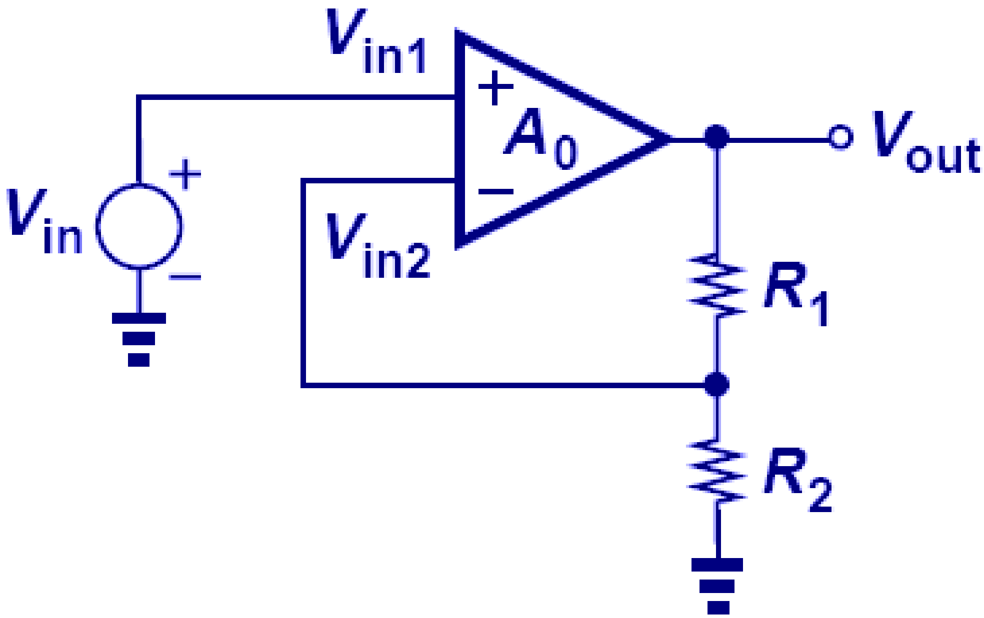
$$\frac{0 - V_{out}}{R_1} = \frac{V_{in}}{R_2}$$

$$\frac{V_{out}}{V_{in}} = \frac{-R_1}{R_2}$$

- Infinite A_0 forces the negative input to be a virtual ground.

Another View of Inverting Amplifier

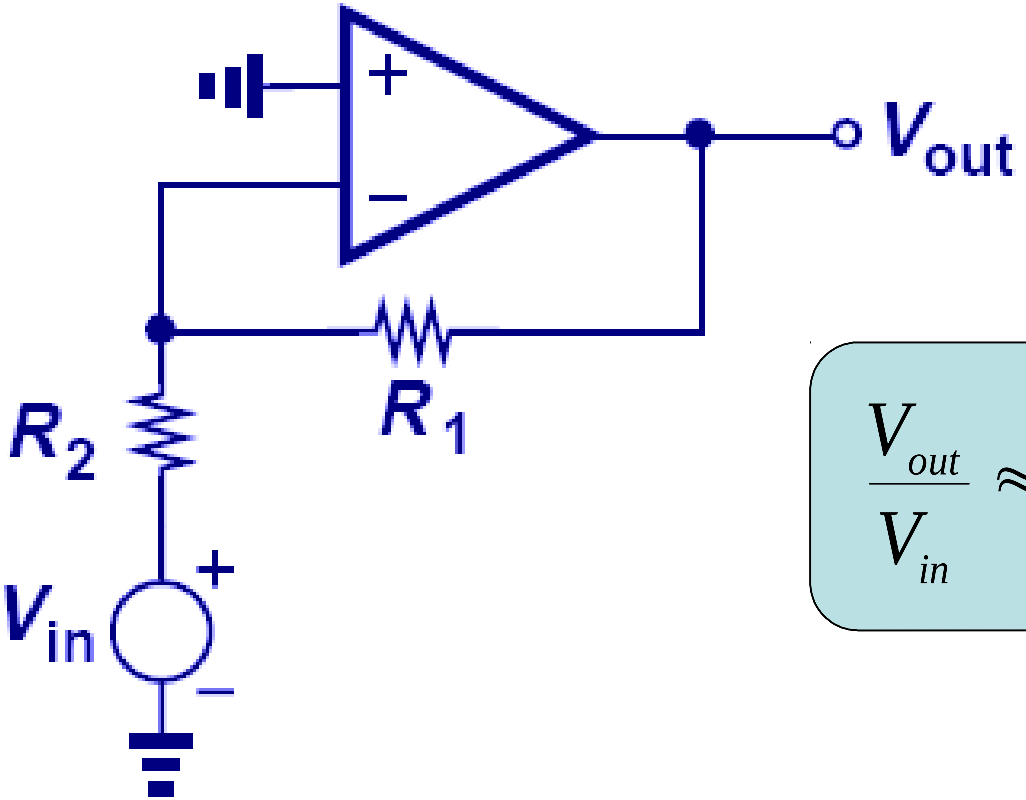




Inverting

Noninverting

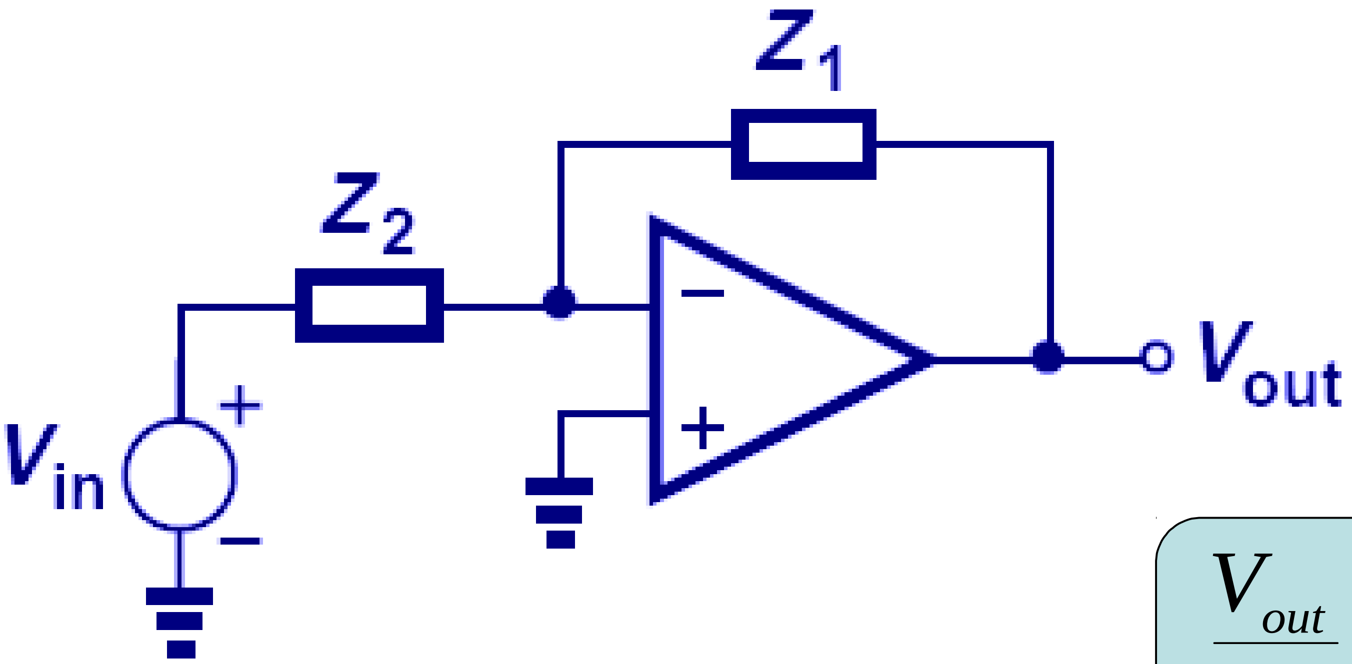
Gain Error Due to Finite A_0



$$\frac{V_{out}}{V_{in}} \approx -\frac{R_1}{R_2}\left[1-\frac{1}{A_0}\left(1+\frac{R_1}{R_2}\right)\right]$$

- **The larger the closed loop gain, the more inaccurate the circuit is.**

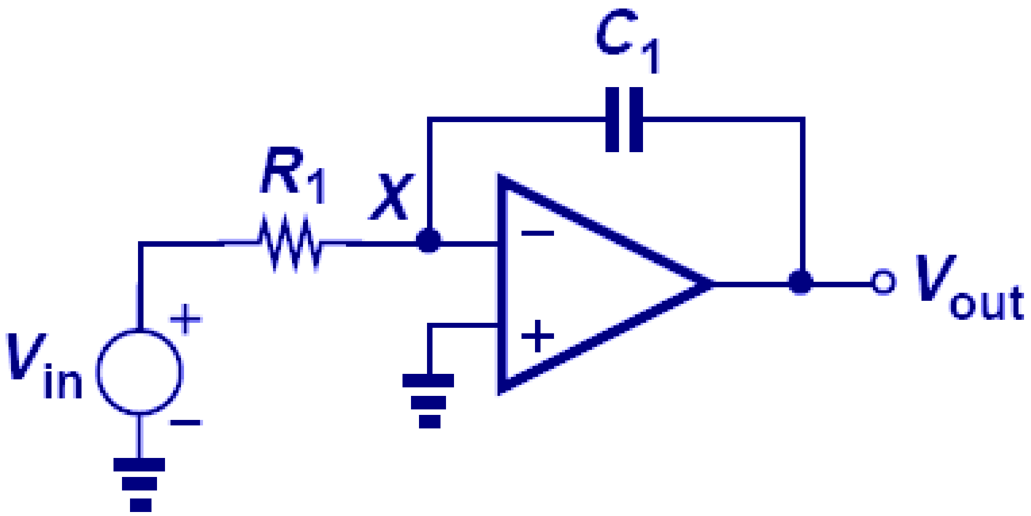
Complex Impedances Around the Op Amp

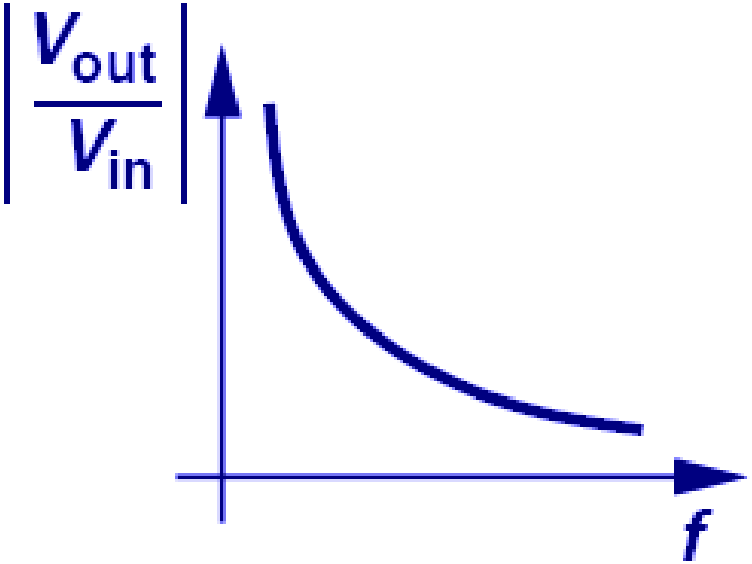


$$\frac{V_{out}}{V_{in}} \approx -\frac{Z_1}{Z_2}$$

- **The closed-loop gain is still equal to the ratio of two impedances.**

Integrator

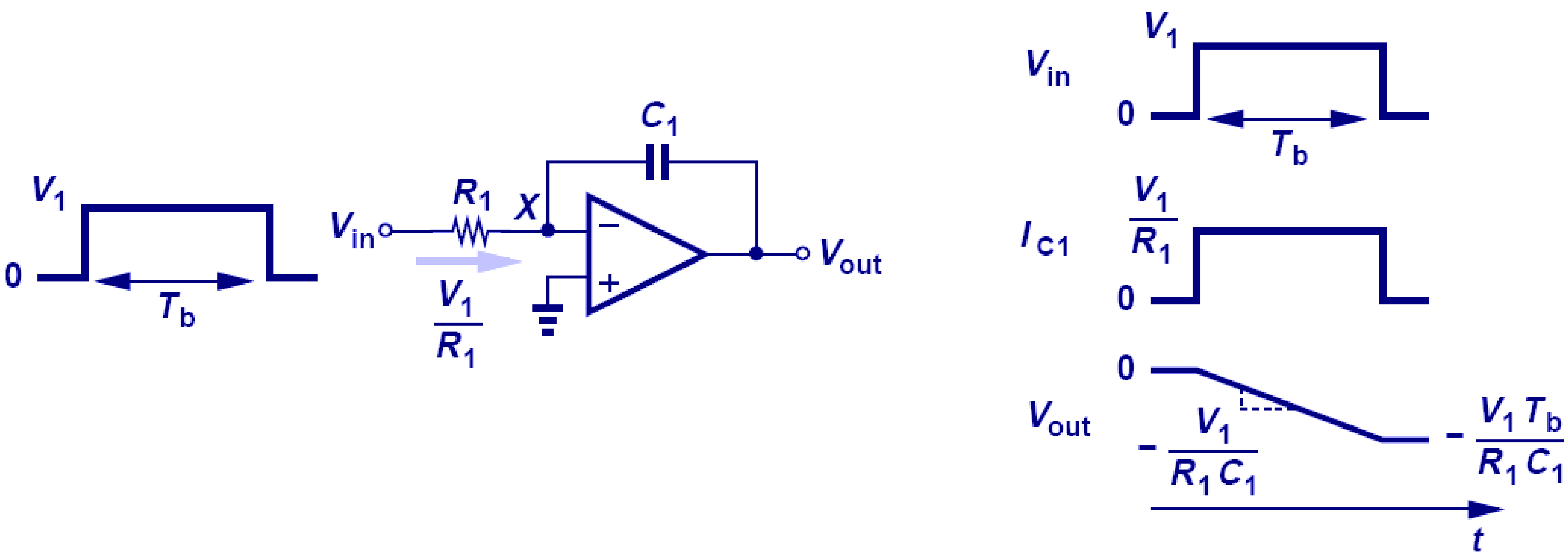




$$\frac{V_{out}}{V_{in}} = -\frac{1}{R_1 C_1 s}$$

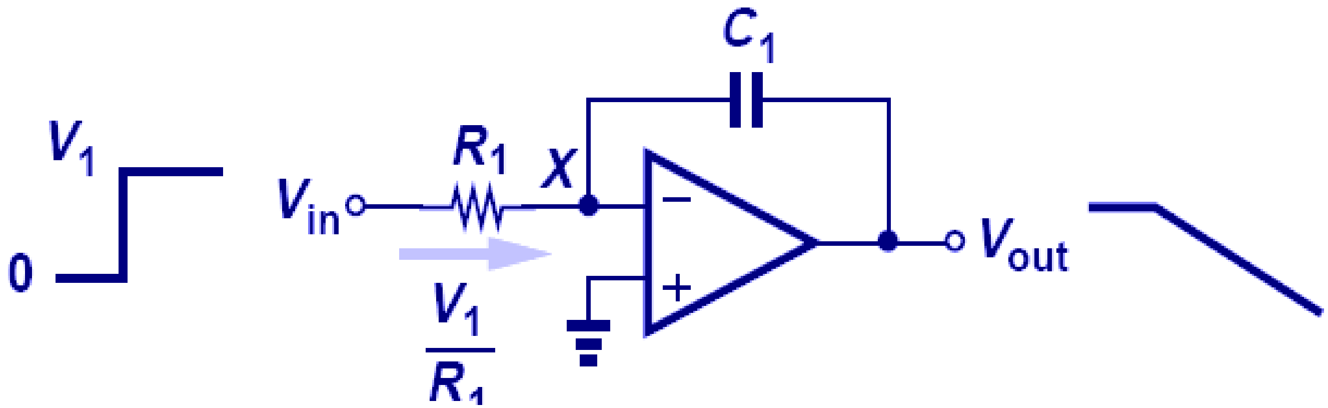
$$V_{out} = -\frac{1}{R_1 C_1}\int V_{in}\,dt$$

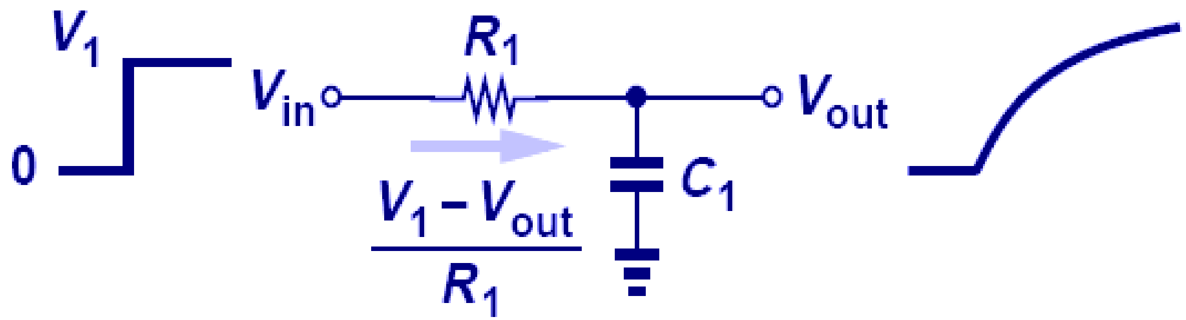
Integrator with Pulse Input



$$V_{out} = -\frac{1}{R_1C_1}\int V_{in}dt = -\frac{V_1}{R_1C_1}t \quad 0 < t < T_b$$

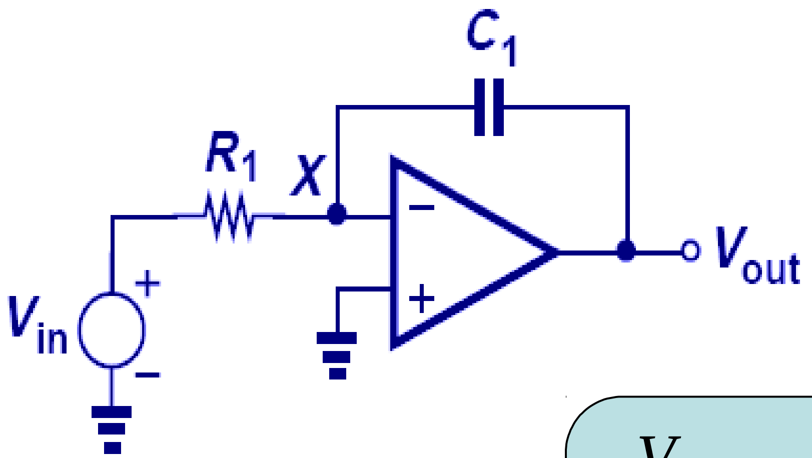
Comparison of Integrator and RC Lowpass Filter

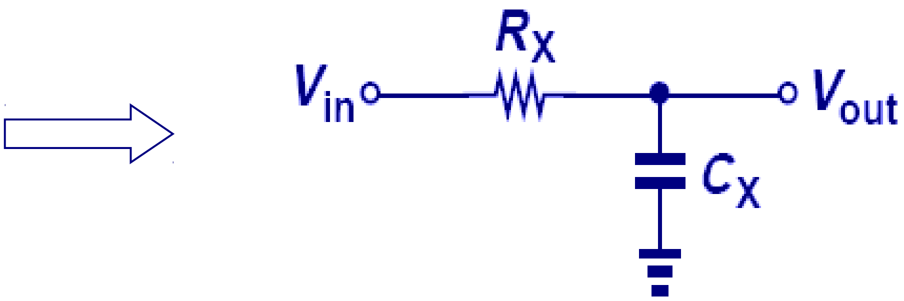




- The RC low-pass filter is actually a “passive” approximation to an integrator.
- With the RC time constant large enough, the RC filter output approaches a ramp.

Lossy Integrator

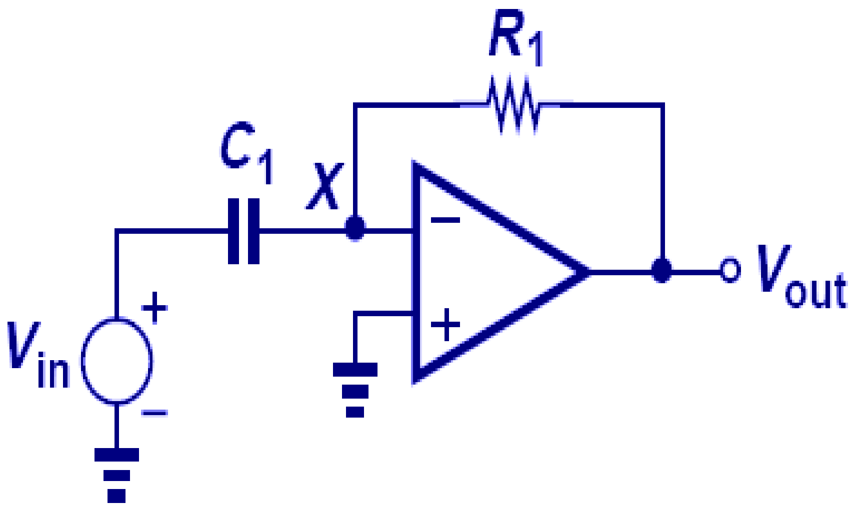


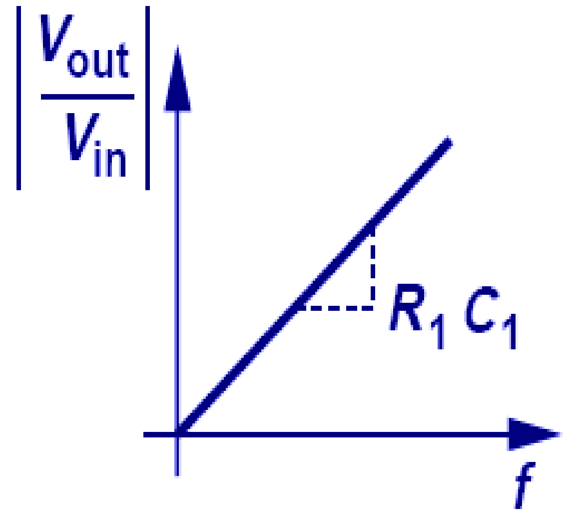


$$\frac{V_{out}}{V_{in}} = \frac{-1}{\frac{1}{A_0} + \left(1 + \frac{1}{A_0}\right) R_1 C_1 s}$$

- **When finite op amp gain is considered, the integrator becomes lossy as the pole moves from the origin to $-1/[(1+A_0)R_1C_1]$.**
- **It can be approximated as an RC circuit with C boosted by a factor of A_0+1.**

Differentiator

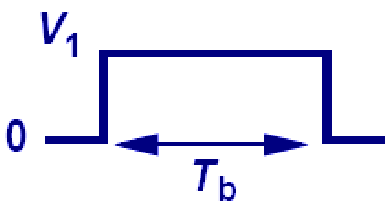


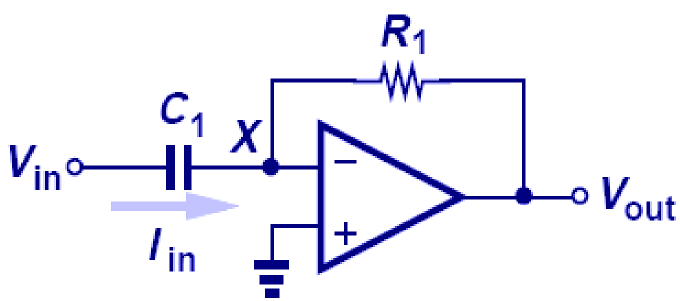


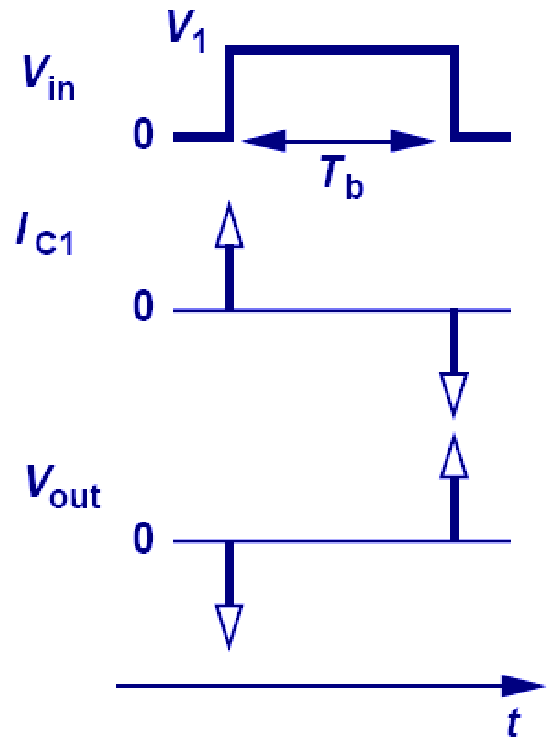
$$V_{out} = -R_1C_1\frac{dV_{in}}{dt}$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{\frac{1}{C_1s}} = -R_1C_1s$$

Differentiator with Pulse Input

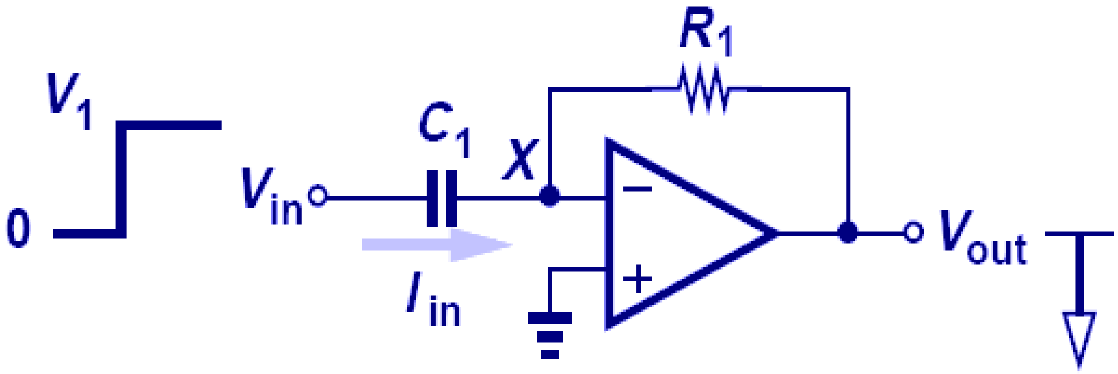


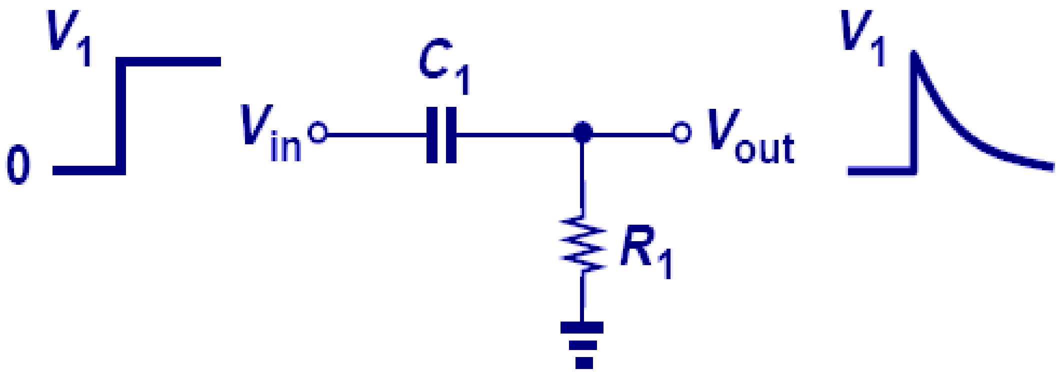




$$V_{out} = \mp R_1 C_1 V_1 \delta(t)$$

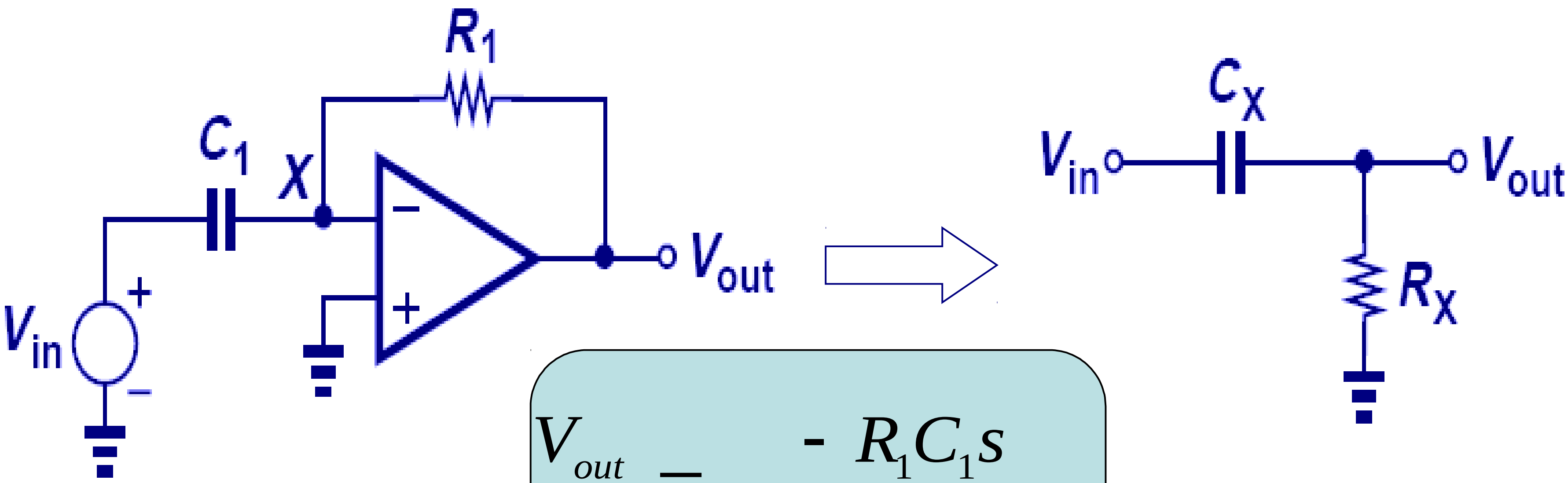
Comparison of Differentiator and High-Pass Filter





- The RC high-pass filter is actually a passive approximation to the differentiator.
- When the RC time constant is small enough, the RC filter approximates a differentiator.

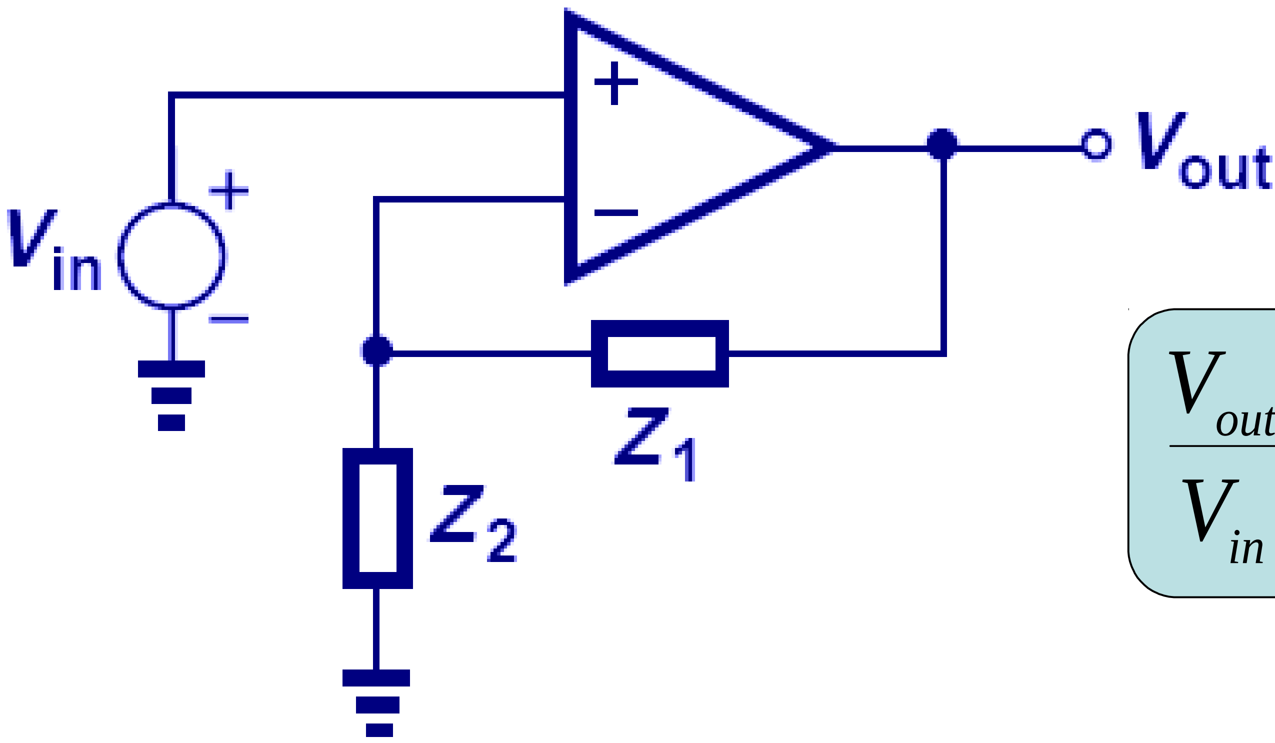
Lossy Differentiator



$$\frac{V_{out}}{V_{in}} = \frac{-R_1C_1s}{1+\frac{1}{A_0}+\frac{R_1C_1s}{A_0}}$$

- When finite op amp gain is considered, the differentiator becomes lossy as the zero moves from the origin to $-(A_0+1)/R_1C_1$.
- It can be approximated as an RC circuit with R reduced by a factor of (A_0+1).

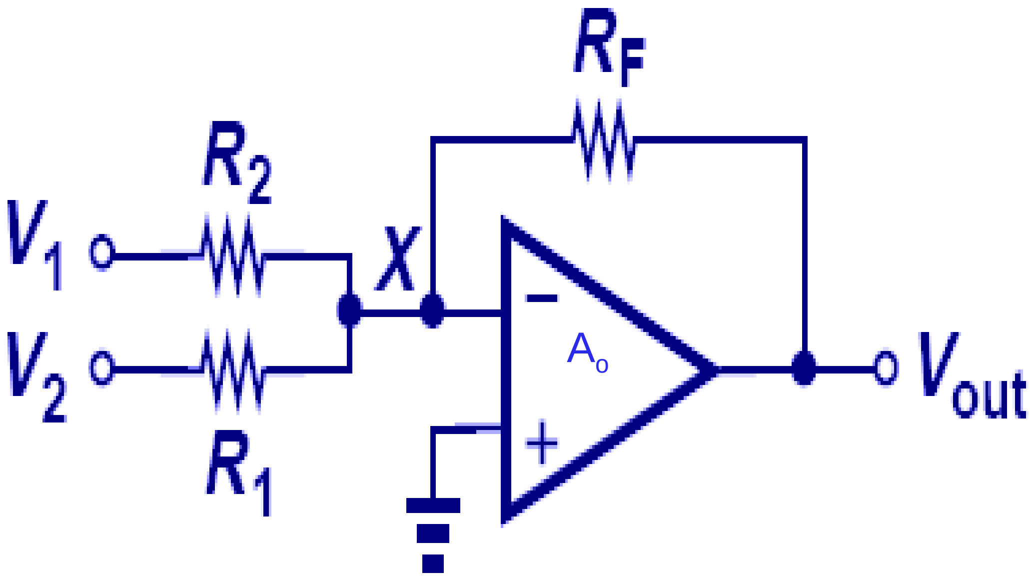
Op Amp with General Impedances



$$\frac{V_{out}}{V_{in}} = 1 + \frac{Z_1}{Z_2}$$

- **This circuit cannot operate as ideal integrator or differentiator.**

Voltage Adder



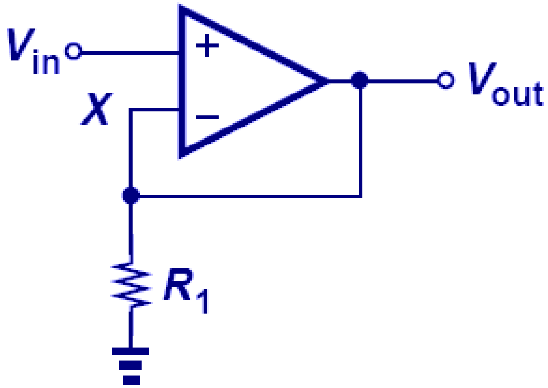
$$V_{out} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

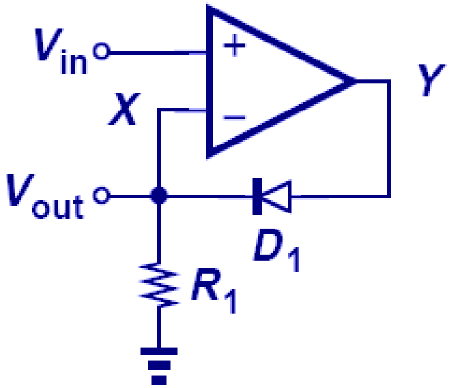
$$V_{out} = \frac{-R_F}{R}(V_1 + V_2)$$

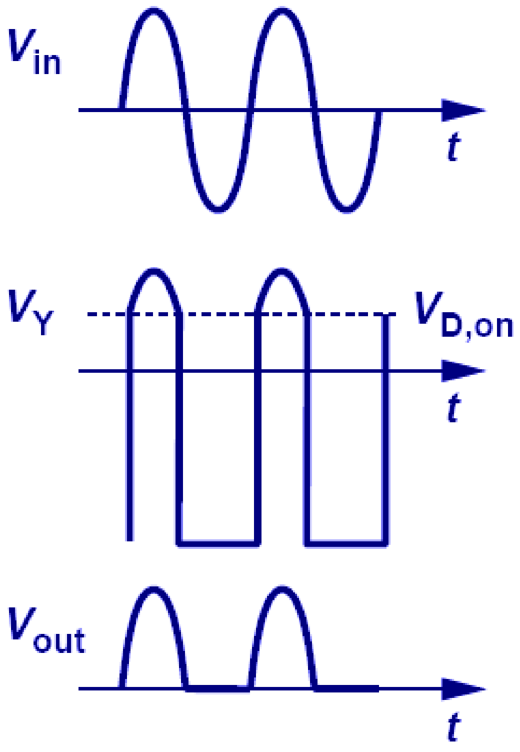
$If\ R_1 = R_2 = R$

- **If A_o is infinite, X is pinned at ground, currents proportional to V_1 and V_2 will flow to X and then across R_F to produce an output proportional to the sum of two voltages.**

Precision Rectifier

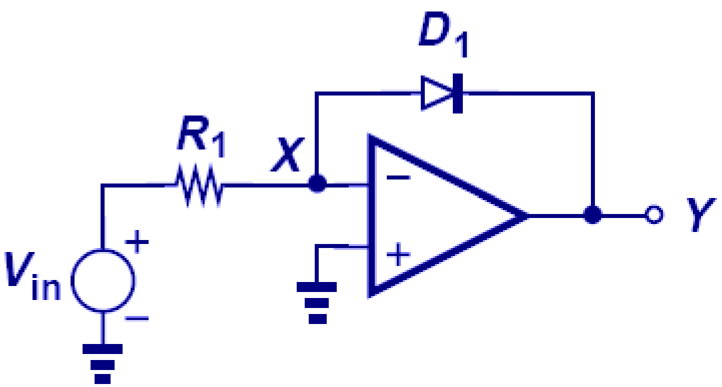


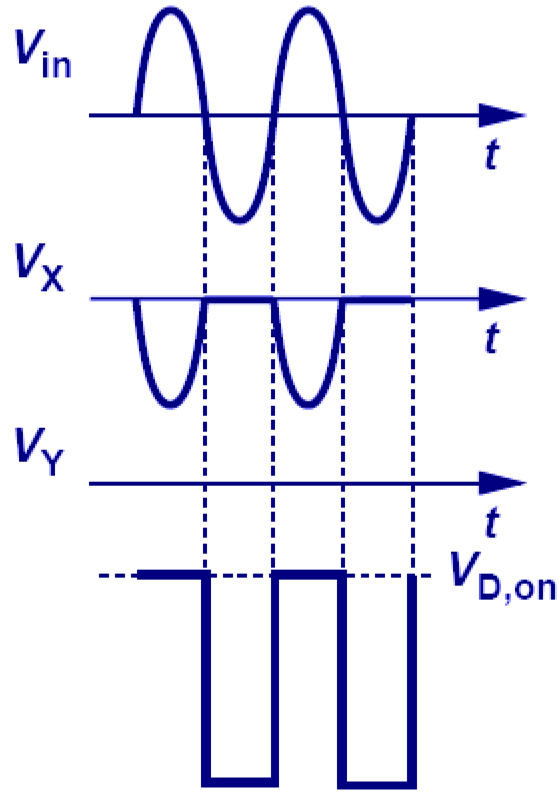




- When V_{in} is positive, the circuit in b) behaves like that in a), so the output follows input.
- When V_{in} is negative, the diode opens, and the output drops to zero. Thus performing rectification.

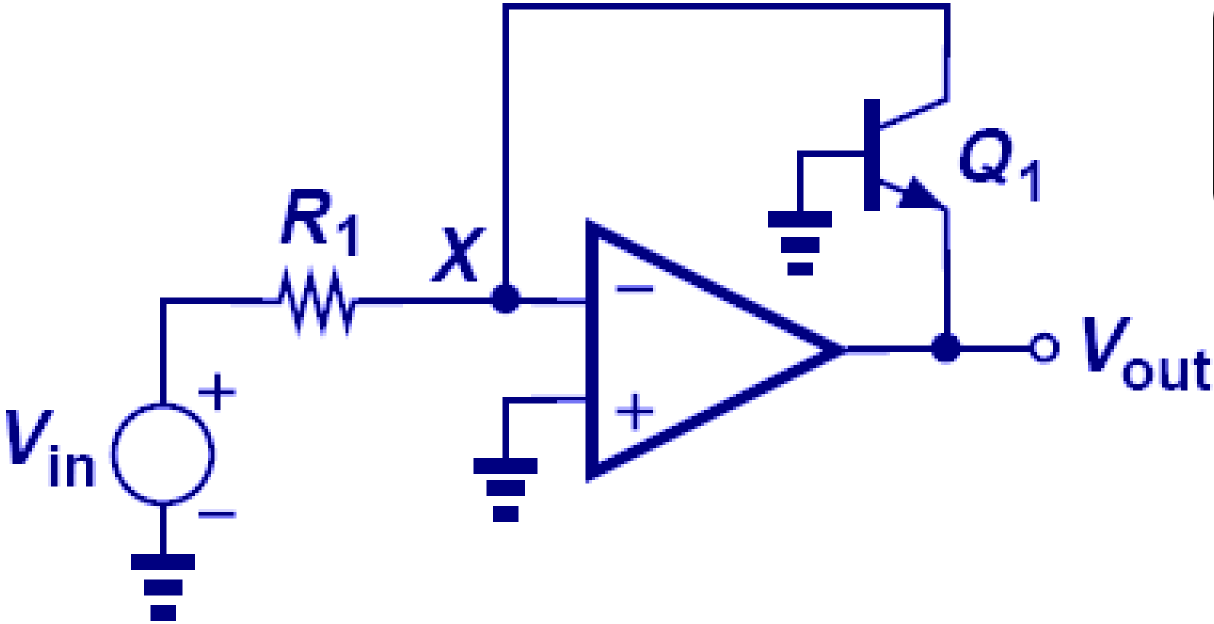
Inverting Precision Rectifier





- When V_{in} is positive, the diode is on, V_y is pinned around $V_{D,on}$, and V_x at virtual ground.
- When V_{in} is negative, the diode is off, V_y goes extremely negative, and V_x becomes equal to V_{in}.

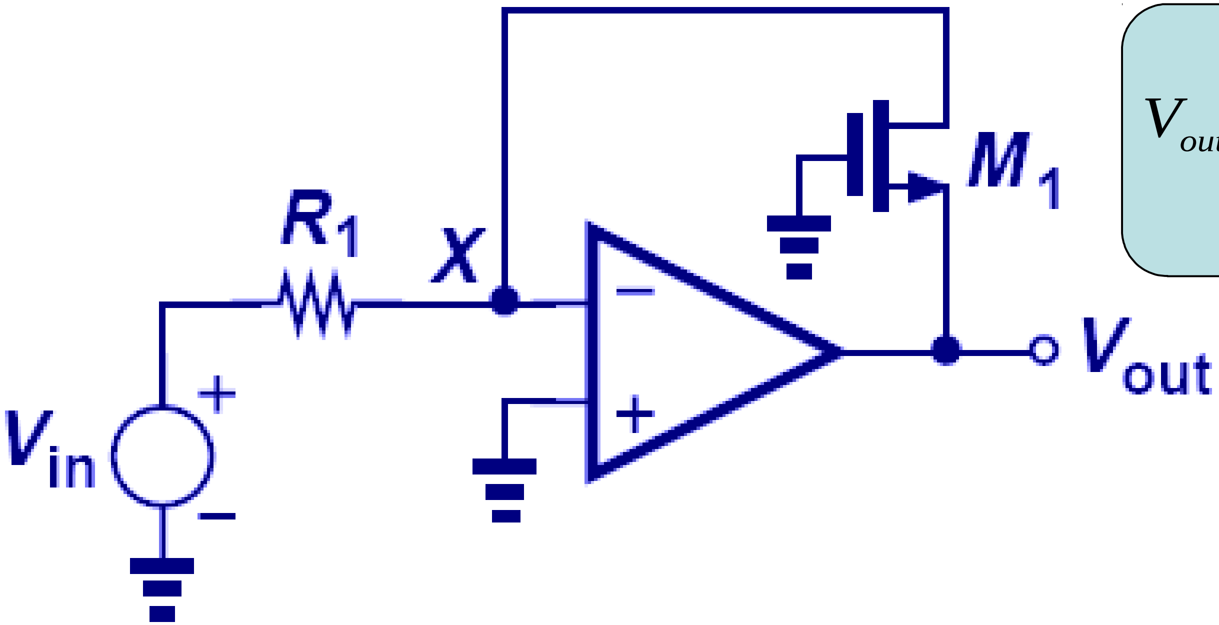
Logarithmic Amplifier



$$V_{out} = -V_T \ln \frac{V_{in}}{R_1 I_S}$$

- By inserting a bipolar transistor in the loop, an amplifier with logarithmic characteristic can be constructed.
- This is because the current to voltage conversion of a bipolar transistor is a natural logarithm.

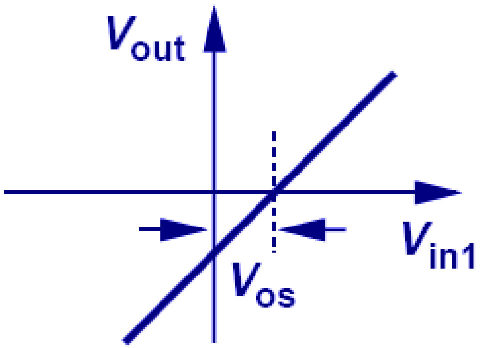
Square-Root Amplifier

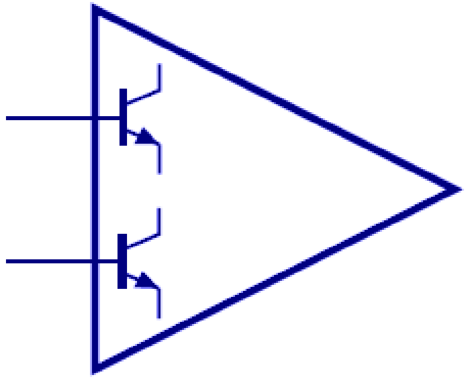


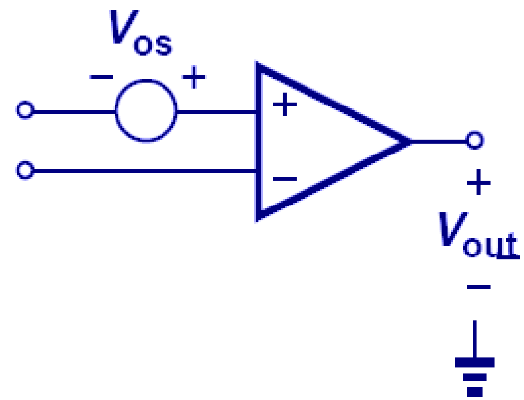
$$V_{out} = -\sqrt{\frac{2V_{in}}{\mu_n C_{ox} \frac{W}{L} R_1}} - V_{TH}$$

- **By replacing the bipolar transistor with a MOSFET, an amplifier with a square-root characteristic can be built.**
- **This is because the current to voltage conversion of a MOSFET is square-root.**

Op Amp Nonidealities: DC Offsets

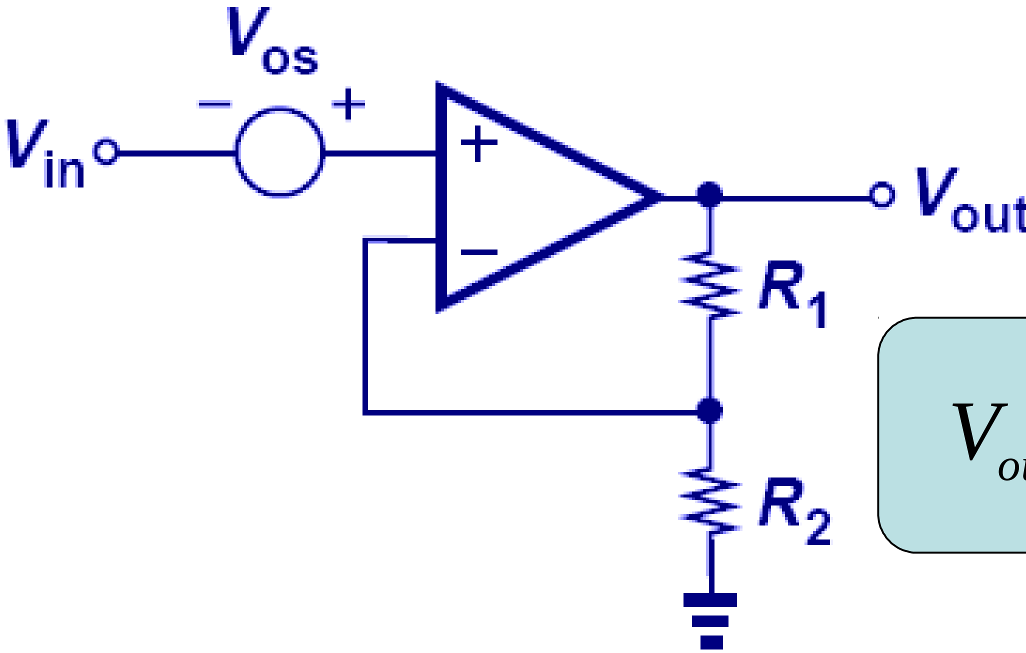






- **Offsets in an op amp that arise from input stage mismatch cause the input-output characteristic to shift in either the positive or negative direction (the plot displays positive direction).**

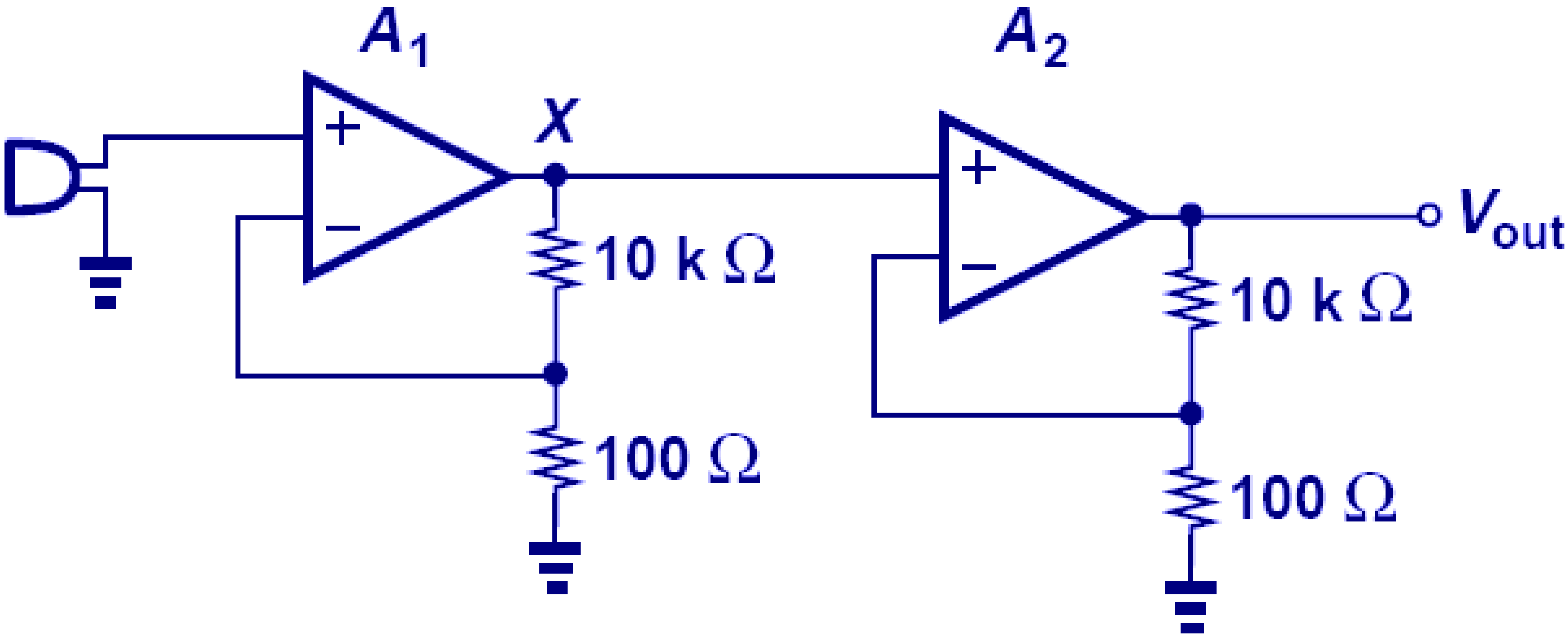
Effects of DC Offsets



$$V_{out} = \left(1 + \frac{R_1}{R_2}\right)(V_{in} + V_{os})$$

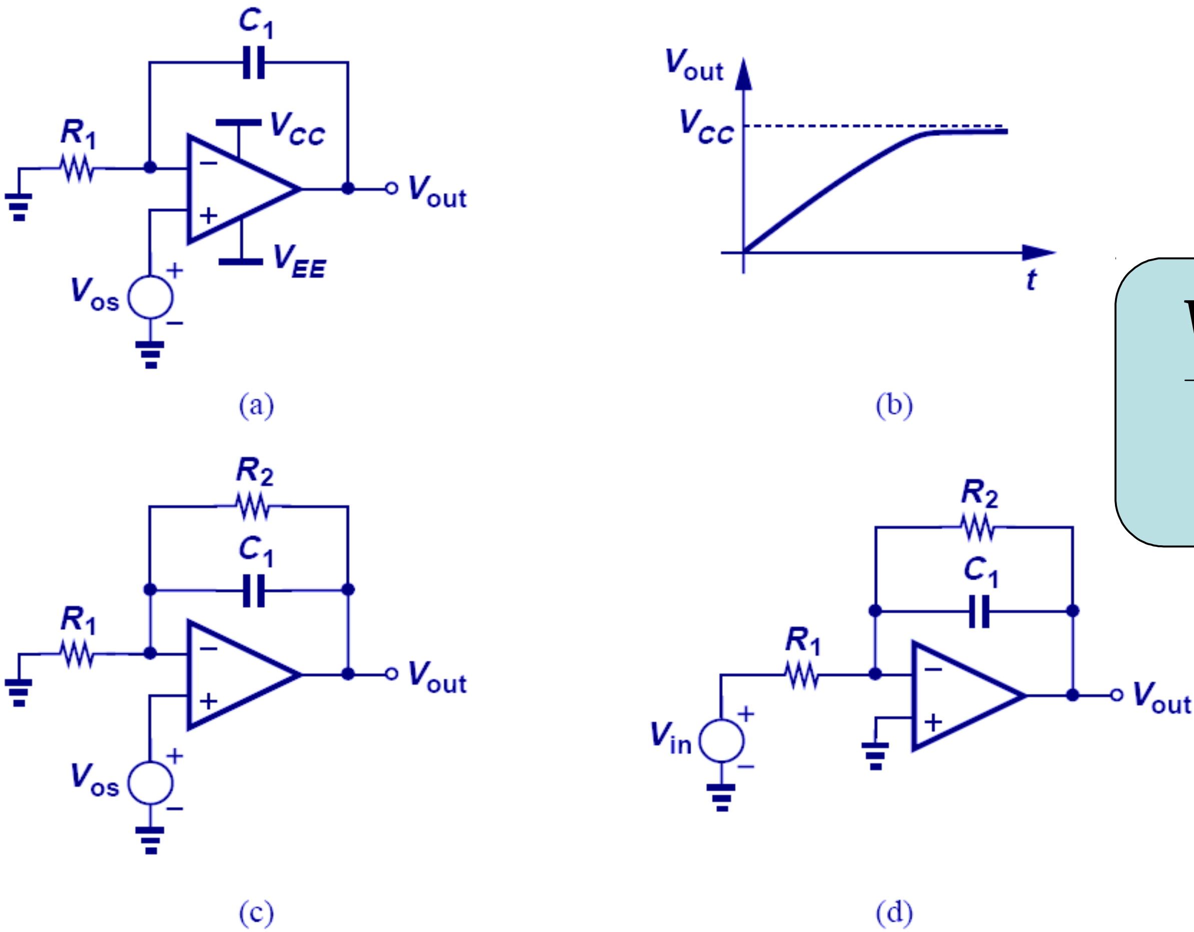
- **As it can be seen, the op amp amplifies the input as well as the offset, thus creating errors.**

Saturation Due to DC Offsets



- **Since the offset will be amplified just like the input signal, output of the first stage may drive the second stage into saturation.**

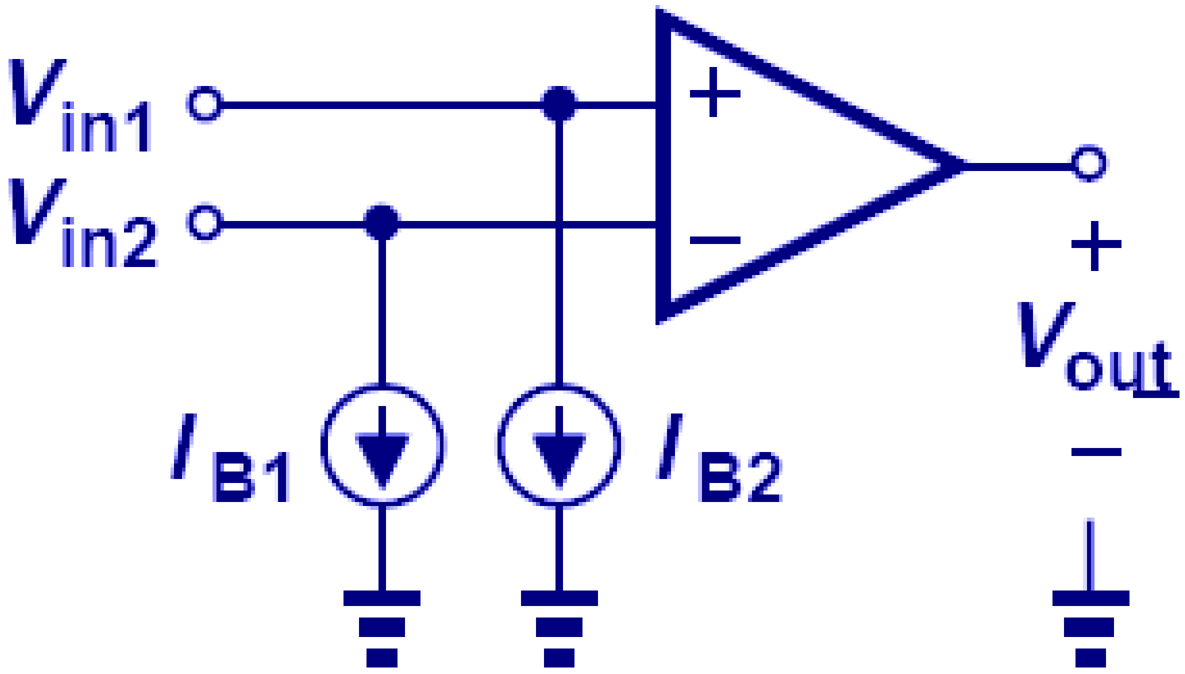
Offset in Integrator



$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}\frac{1}{R_2C_1s+1}$$

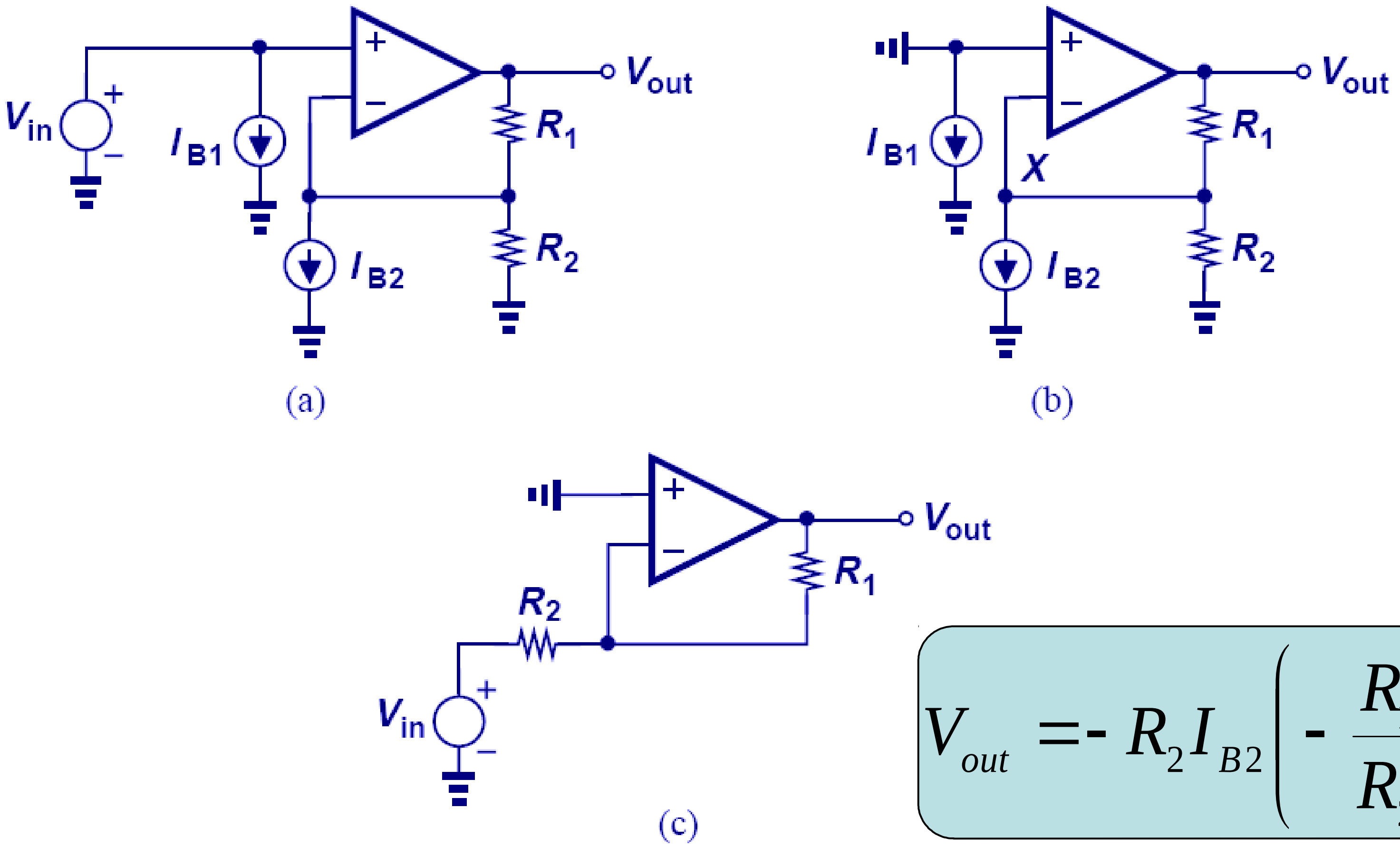
- A resistor can be placed in parallel with the capacitor to "absorb" the offset. However, this means the closed-loop transfer function no longer has a pole at origin.

Input Bias Current



- **The effect of bipolar base currents can be modeled as current sources tied from the input to ground.**

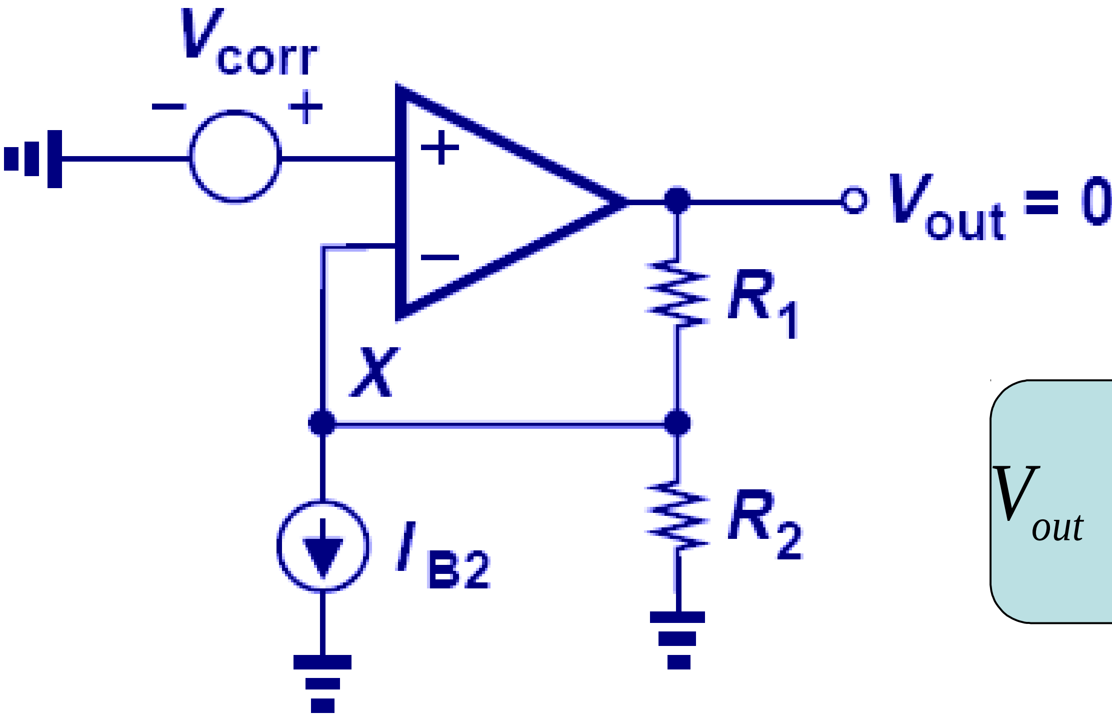
Effects of Input Bias Current on Noninverting Amplifier



$$V_{out} = -R_2 I_{B2}\left(-\frac{R_1}{R_2}\right) = R_1 I_{B2}$$

- **It turns out that I_{B1} has no effect on the output and I_{B2} affects the output by producing a voltage drop across R_1.**

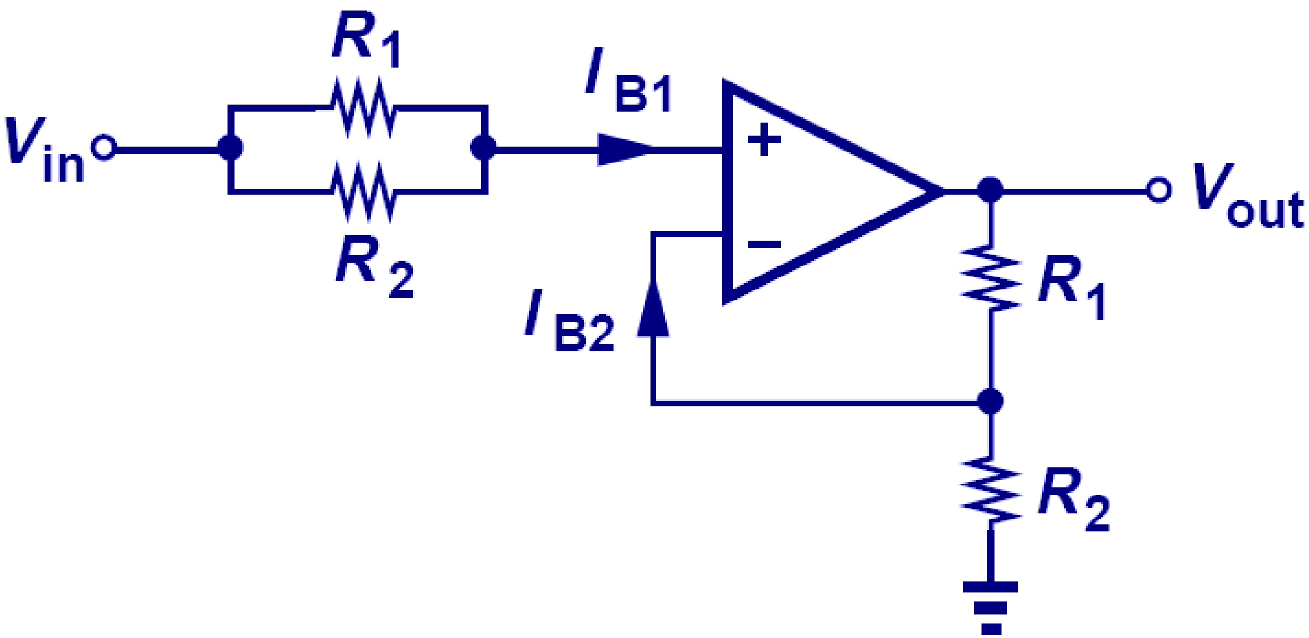
Input Bias Current Cancellation



$$V_{out} = V_{corr}\left(1 + \frac{R_1}{R_2}\right) + I_{B2}R_1$$

- We can cancel the effect of input bias current by inserting a correction voltage in series with the positive terminal.
- In order to produce a zero output, $V_{corr} = -I_{B2}(R_1 || R_2)$.

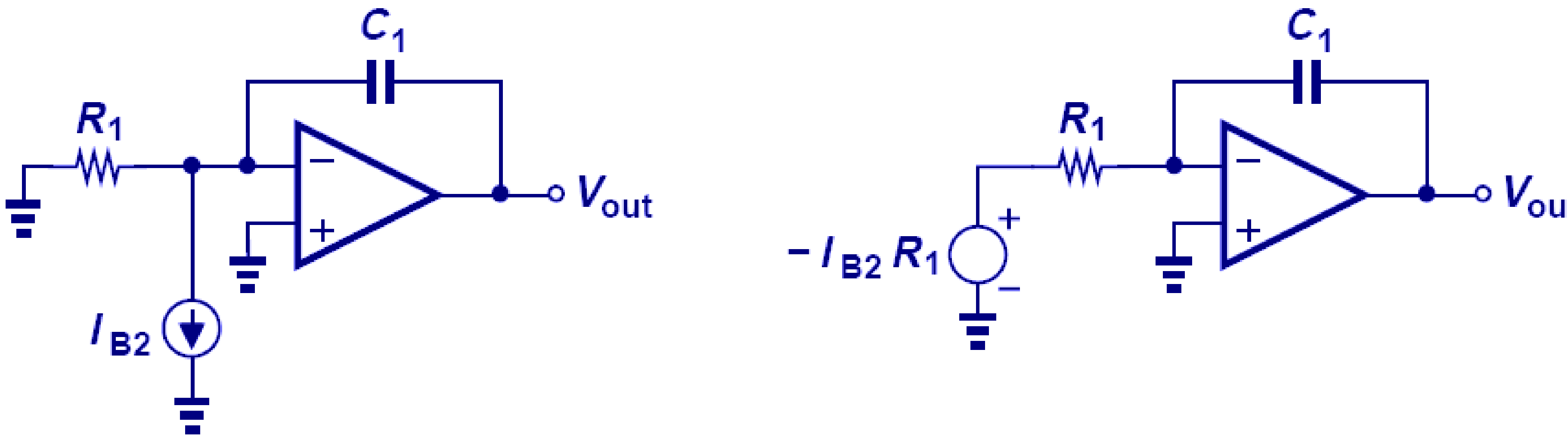
Correction for β Variation



$$I_{B1} = I_{B2}$$

- **Since the correction voltage is dependent upon β, and β varies with process, we insert a parallel resistor combination in series with the positive input. As long as $I_{B1} = I_{B2}$, the correction voltage can track the β variation.**

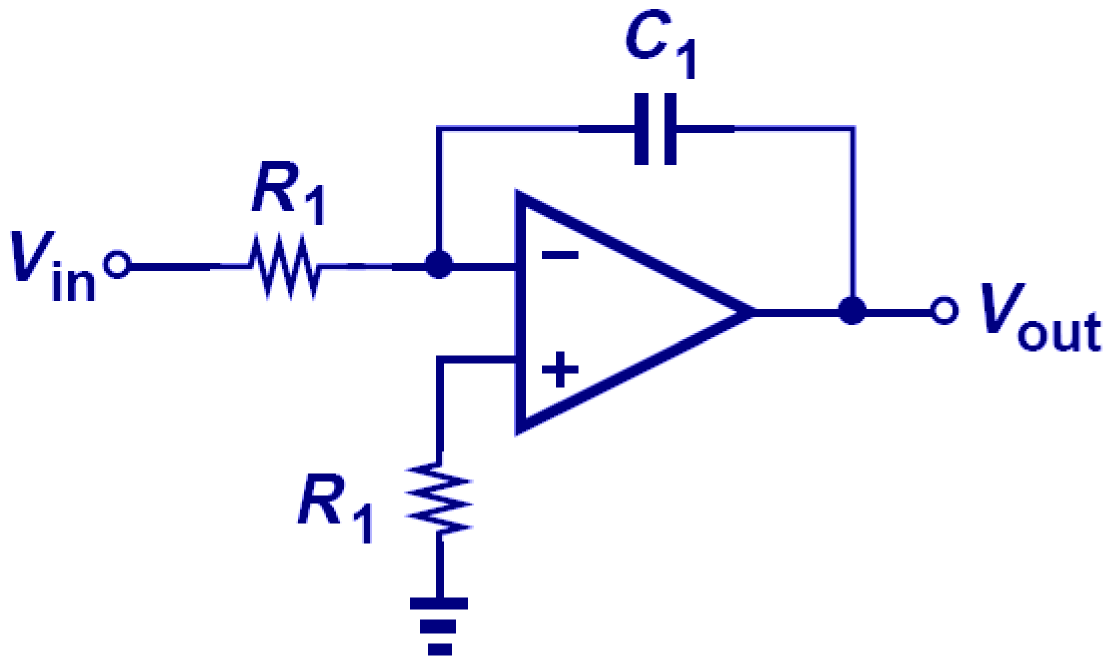
Effects of Input Bias Currents on Integrator



$$V_{out} = -\frac{1}{R_1 C_1}\int(-I_{B2}R_1)dt$$

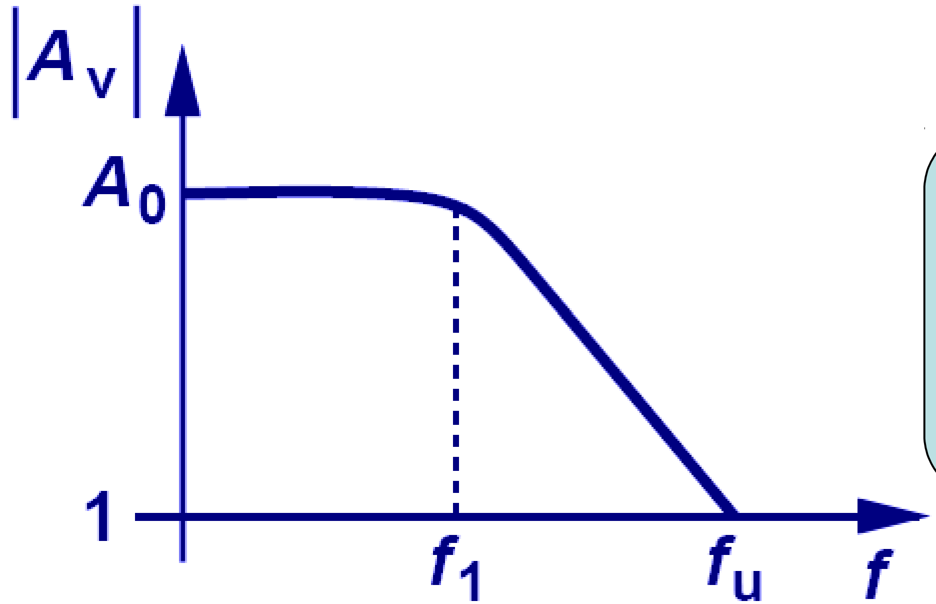
- **Input bias current will be integrated by the integrator and eventually saturate the amplifier.**

Integrator's Input Bias Current Cancellation



- By placing a resistor in series with the positive input, integrator input bias current can be cancelled.
- However, the output still saturates due to other effects such as input mismatch, etc.

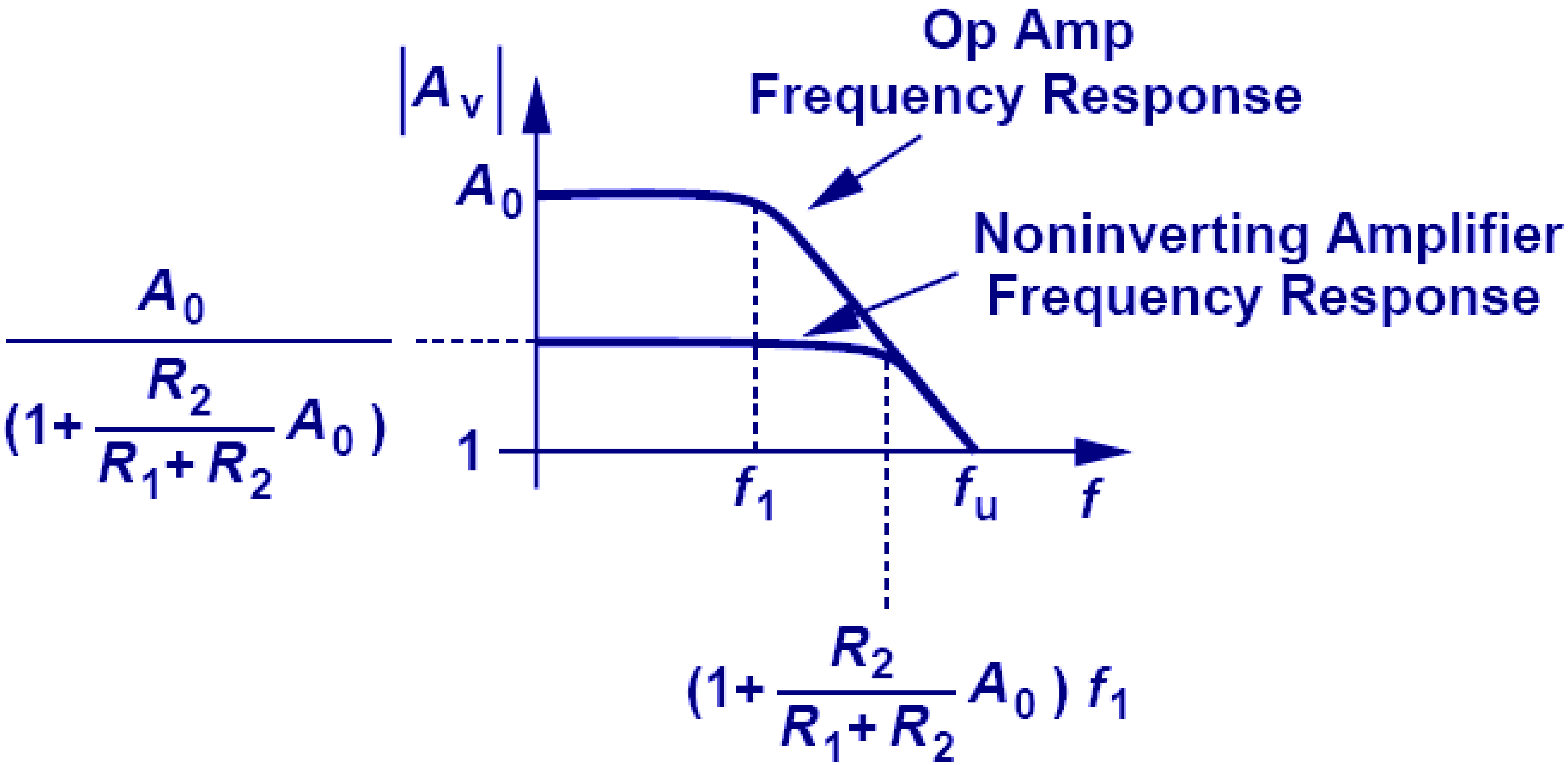
Speed Limitation



$$\frac{V_{out}}{V_{in1} - V_{in2}}(s) = \frac{A_0}{1 + \frac{s}{\omega_1}}$$

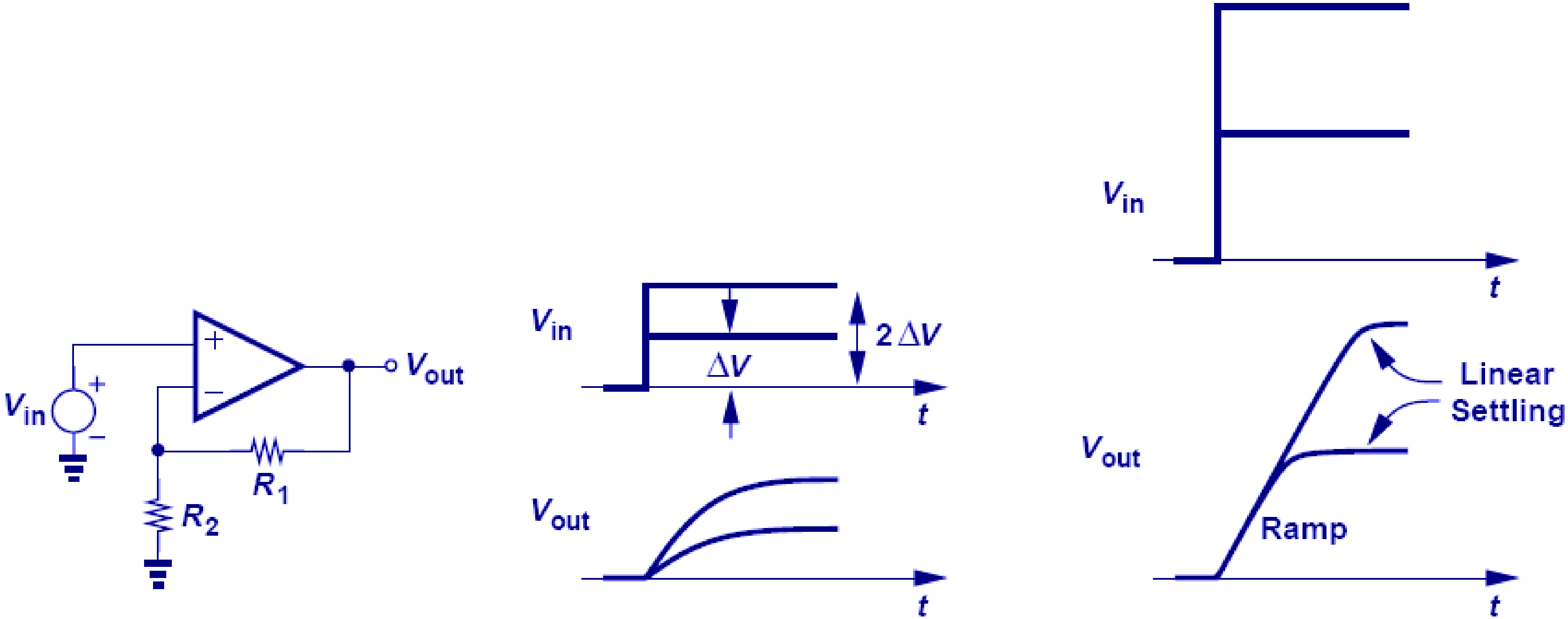
- **Due to internal capacitances, the gain of op amps begins to roll off.**

Bandwidth and Gain Tradeoff



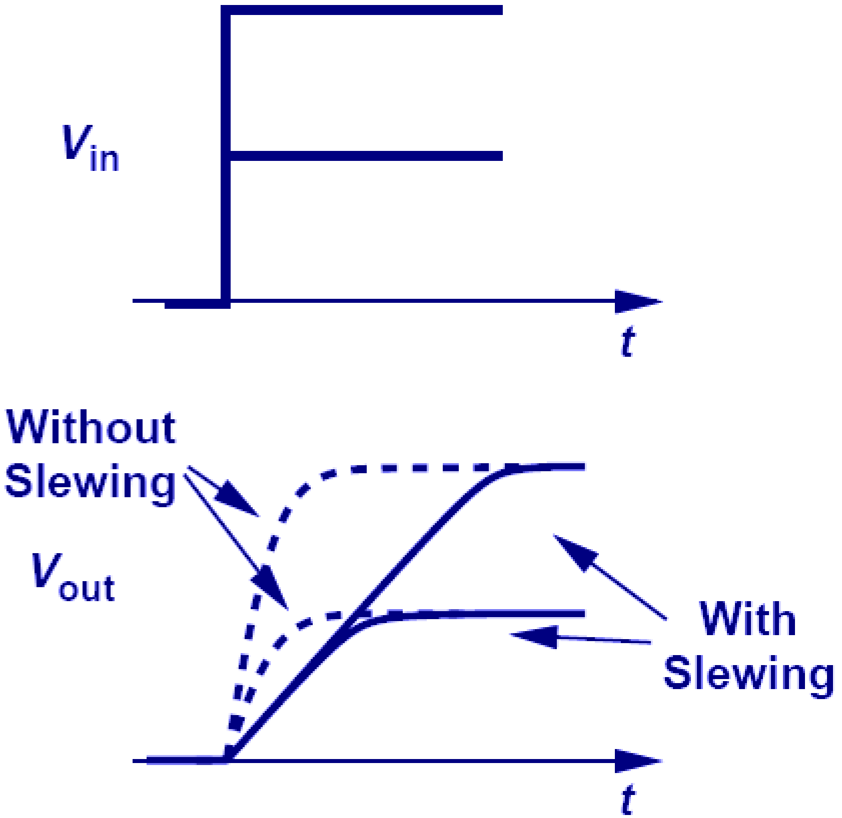
- Having a loop around the op amp (inverting, noninverting, etc) helps to increase its bandwidth. However, it also decreases the low frequency gain.

Slew Rate of Op Amp



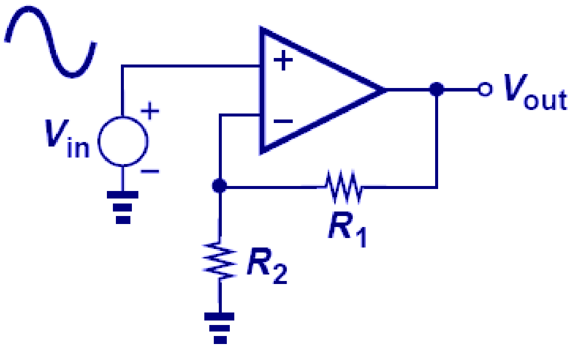
- In the linear region, when the input doubles, the output and the output slope also double. However, when the input is large, the op amp slews so the output slope is fixed by a constant current source charging a capacitor.
- This further limits the speed of the op amp.

Comparison of Settling with and without Slew Rate

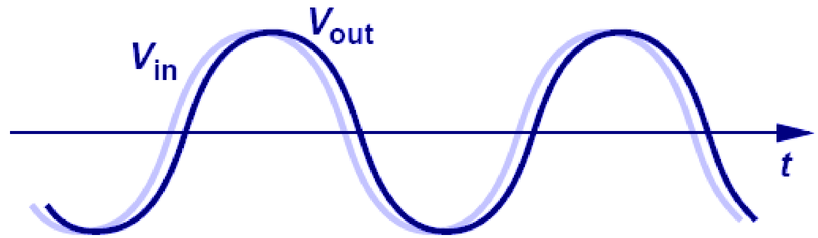


- **As it can be seen, the settling speed is faster without slew rate (as determined by the closed-loop time constant).**

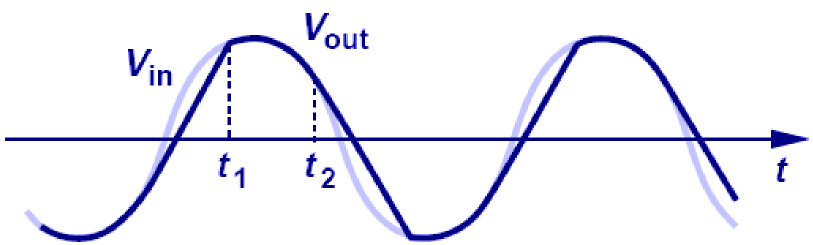
Slew Rate Limit on Sinusoidal Signals



(a)



(b)

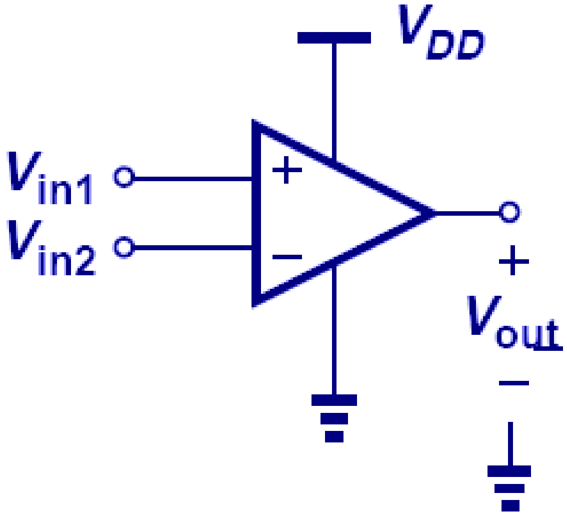


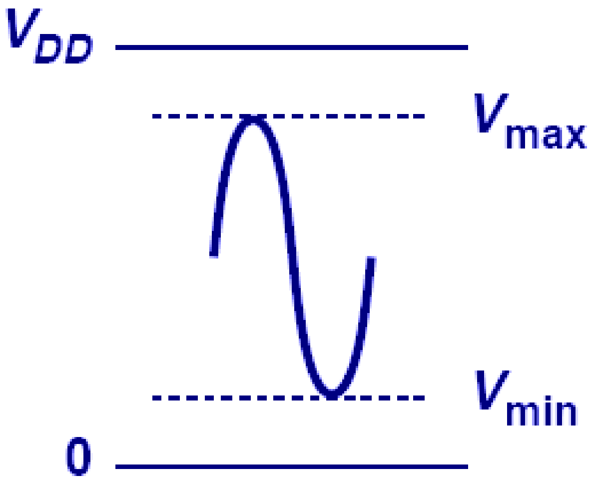
(c)

$$\frac{dV_{out}}{dt} = V_0 \left(1 + \frac{R_1}{R_2}\right) \omega \cos \omega t$$

- **As long as the output slope is less than the slew rate, the op amp can avoid slewing.**
- **However, as operating frequency and/or amplitude is increased, the slew rate becomes insufficient and the output becomes distorted.**

Maximum Op Amp Swing

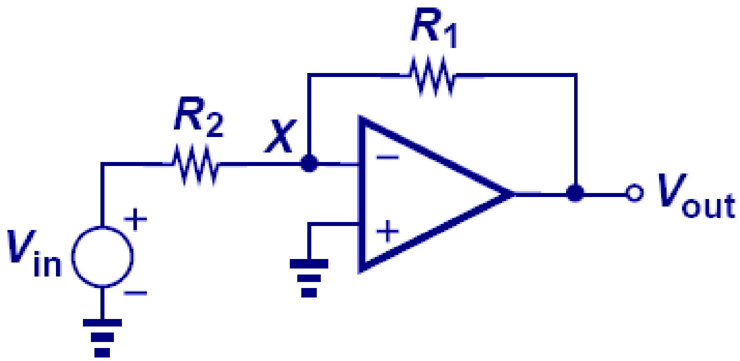


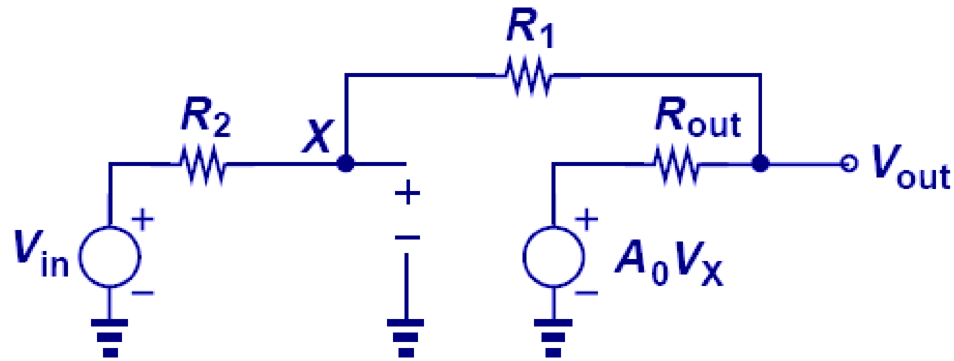


$$V_{out} = \frac{V_{max} - V_{min}}{2} \sin \omega t + \frac{V_{max} + V_{min}}{2} \qquad \omega_{FP} = \frac{SR}{\frac{V_{max} - V_{min}}{2}}$$

- **To determine the maximum frequency before op amp slews, first determine the maximum swing the op amp can have and divide the slew rate by it.**

Nonzero Output Resistance





$$\frac{v_{out}}{v_{in}} = -\frac{R_1}{R_2}\frac{A_0 - \dfrac{R_{out}}{R_1}}{1 + \dfrac{R_{out}}{R_2} + A_0 + \dfrac{R_1}{R_2}}$$

- **In practical op amps, the output resistance is not zero.**
- **It can be seen from the closed loop gain that the nonzero output resistance increases the gain error.**

Design Examples

- **Many design problems are presented at the end of the chapter to study the effects of finite loop gain, restrictions on peak to peak swing to avoid slewing, and how to design for a certain gain error.**