Assignment 2.1

Problem statement:

Generate a timer interrupt using spike simulator. The timer interrupt should be handled using vector based interrupt.

Register information:

CSR Registers to write

1. Mstatus
2. Mie
3. Mtvec

CSR Registers to read

1. mip

Base registers to use

1. Stack pointer (SP)
2. Temporary registers

Timer registers, memory map

1. Mtime - 0x200bff8
2. Mtimecmp - 0x2004000

Steps to do:

1. Initialize temporary registers to zero.
2. Clear the MTIP bit.
3. Set the Stack pointer register to a valid address.
4. Set the mtvec to point to vtrap_entry.
    a. vtrap_entry is the entry point for H/W, when interrupt happens.
    b. Timer interrupt will come at mtvec base + 28
    c. At mtvec base + 28. Timer interrupt handler code should be called.
5. Now set the lsb of mtvec to 1. This will enable vectored based interrupt.
6. Let *delta* be the time period after which timer interrupt should happen.
7. Now, write code for *mtimecmp=mtime+delta.*
    a. *mtime* and *mtimecmp* are memory mapped registers.
    b. They are 64 bits.
    c. Store the value *mtime+delta* to *mtimecmp* register.
    d. Now, *mtimecmp* has a value greater than *mtime*.
    e. When *mtime* becomes greater than *mtimecmp*. Timer interrupt will happen.
8. Set the MIE bit in mstatus register. This will enable interrupts.

9. Set the MTIE bit in mie register. This will enable machine timer interrupts.
    a. By doing abv two steps, we are ensuring the hardware reports the interrupt to the OS.
    b. When timer interrupt happens. H/W will jump to mtvec base+ 4*7.
10. Wait in an infinite loop for interrupt to happen.

Write a machine timer interrupt handler code.

1. Any specific action for timer interrupt has to be coded here.
2. The MTIP bit has to be cleared. This is mandatory.

Clearing the MTIP bit

Store -1 value to the mtimecmp register. This will clear the MTIP bit.

mtime register
Mtime register is a counter. It starts running from the time the processor is powered on.

mtimecmp register
This register is used to compare with mtime. When mtime > mtimecmp, a timer interrupt happens.